

Features

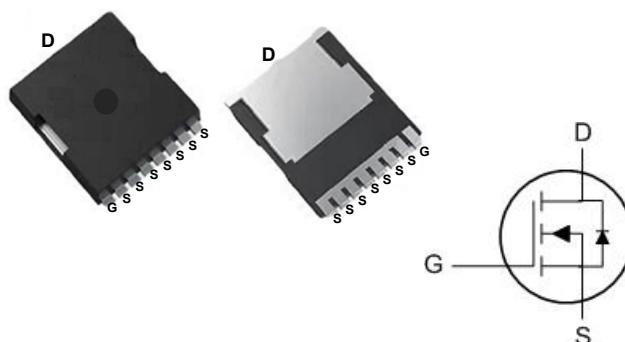
- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

Product Summary


BVDSS	RDSON	ID
40V	0.9mΩ	300A

TOLL Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	300	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	175	A
I_{DM}	Pulsed Drain Current ²	960	A
EAS	Single Pulse Avalanche Energy ³	809	mJ
I_{AS}	Avalanche Current	---	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	180	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	35	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	40	---	---	V
$\Delta BV_{DSS} / \Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	---	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=1A$	---	0.9	1.1	$\text{m}\Omega$
		$V_{GS}=4.5V$, $I_D=1A$	---	---	---	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	2	3	4	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=40V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=40V$, $V_{GS}=0V$, $T_J=150^\circ\text{C}$	---	100	---	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=20V$, $I_D=35A$	---	---	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	3	---	Ω
Q_g	Total Gate Charge	$V_{DS}=20V$, $V_{GS}=10V$, $I_D=20A$	---	112	---	nC
Q_{gs}	Gate-Source Charge		---	41	---	
Q_{gd}	Gate-Drain Charge		---	19	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V$, $V_{DS}=20V$, $R_G=1.6\Omega$	---	32	---	ns
T_r	Rise Time		---	65	---	
$T_{d(off)}$	Turn-Off Delay Time		---	72	---	
T_f	Fall Time		---	40	---	
C_{iss}	Input Capacitance	$V_{DS}=20V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	8780	---	pF
C_{oss}	Output Capacitance		---	3429	---	
C_{rss}	Reverse Transfer Capacitance		---	108	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	300	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=25A$, $T_J=25^\circ\text{C}$	0.7	0.9	1.1	V
t_{rr}	Reverse Recovery Time	$I_F=40A$, $di/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	68	---	nS
Q_{rr}	Reverse Recovery Charge		---	120	---	nC

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The EAS data shows Max. rating . The test condition is $T_J=25^\circ\text{C}$, $V_{DD}=32V$, $V_{GS}=10V$, $L=0.5\text{mH}$

4.The power dissipation is limited by 150°C junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics

Fig 1: Output Characteristics

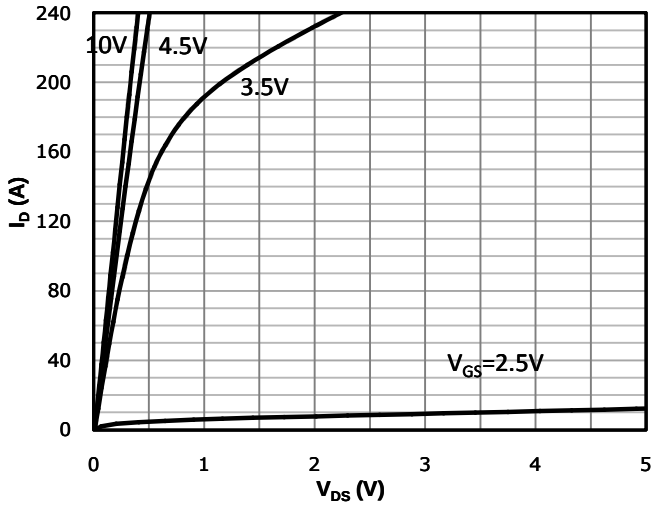


Fig 2: Transfer Characteristics

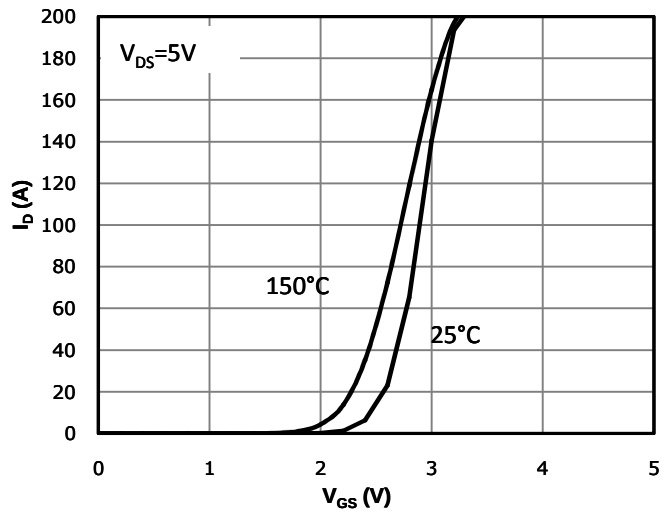


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

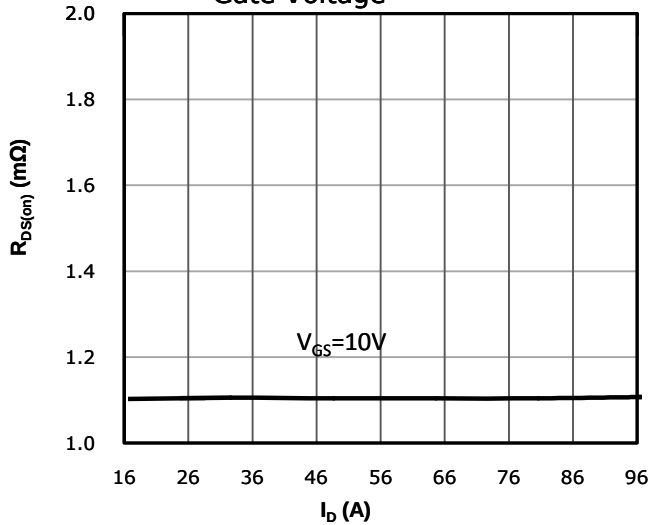


Fig 4: $R_{DS(on)}$ vs Gate Voltage

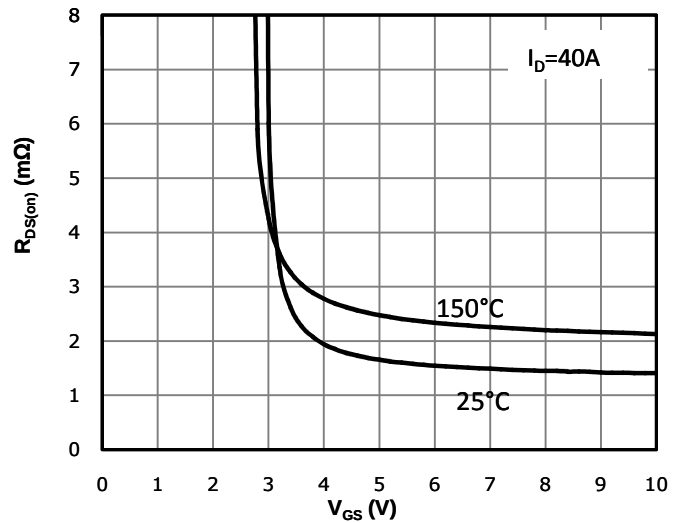


Fig 5: $R_{DS(on)}$ vs. Temperature

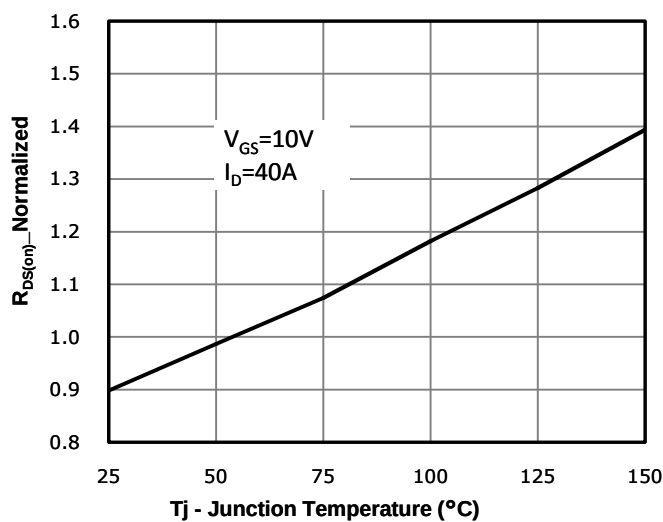


Fig 6: Capacitance Characteristics

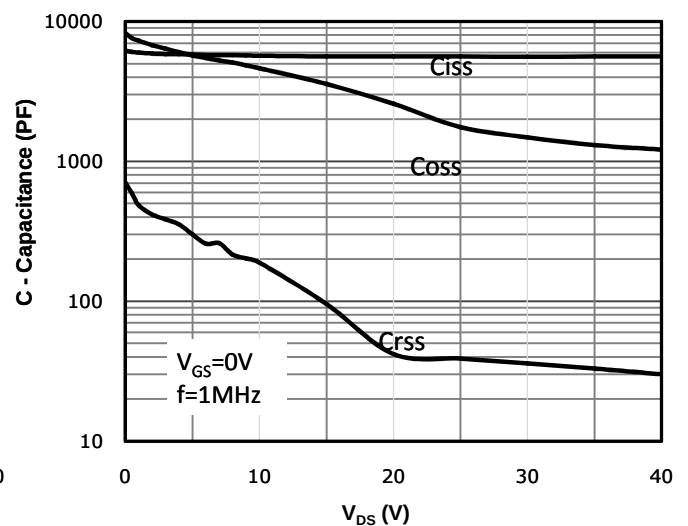


Fig 7: Gate Charge Characteristics

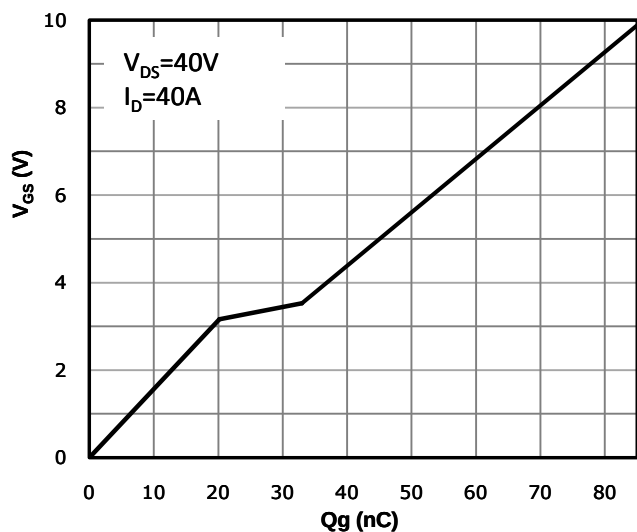


Fig 8: Body-diode Forward Characteristics

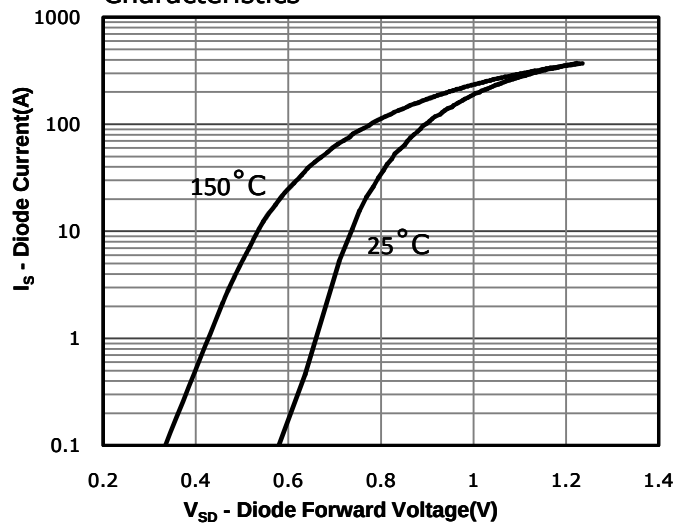


Fig 9: Power Dissipation

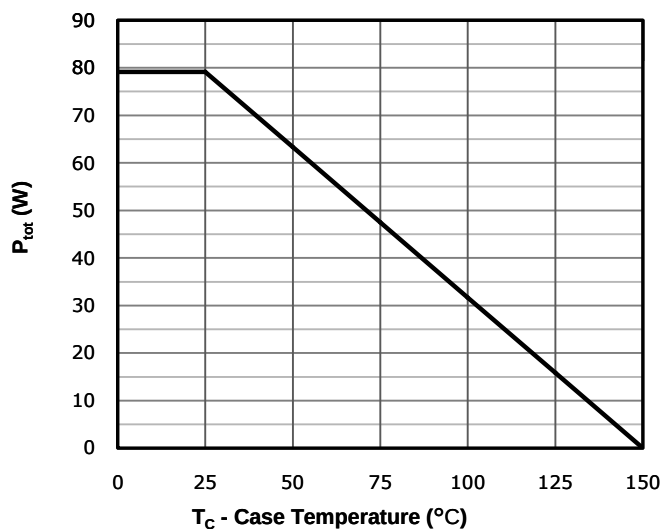


Fig 10: Drain Current Derating

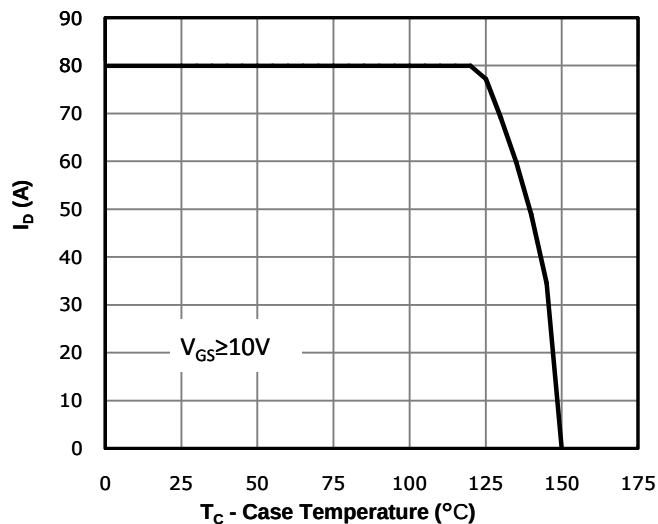


Fig 11: Safe Operating Area

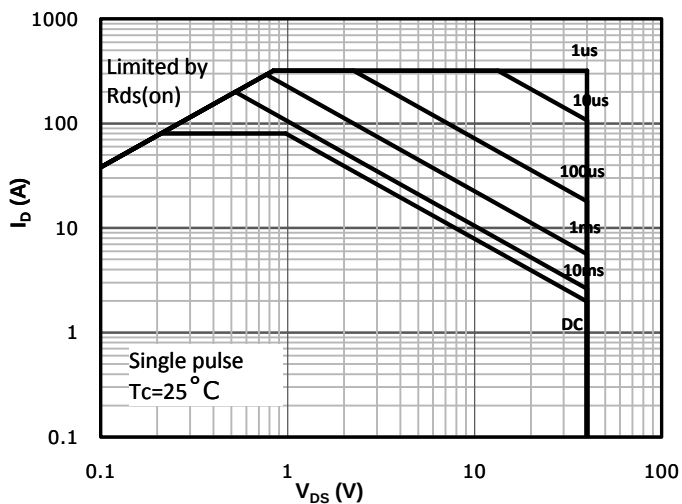
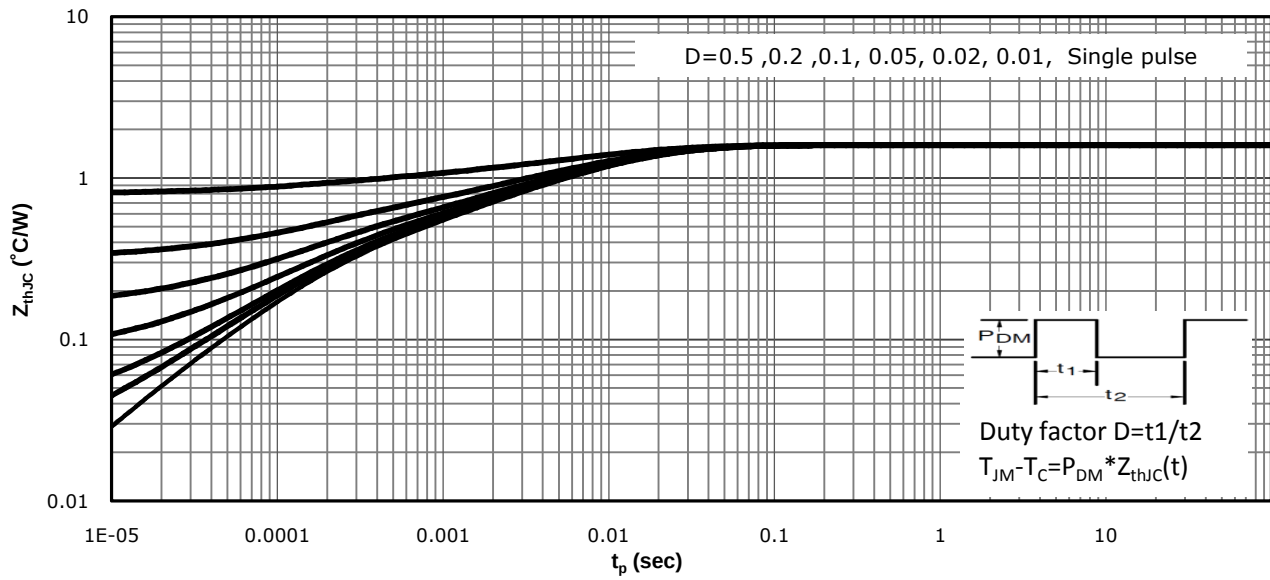


Fig 12: Max. Transient Thermal Impedance



■ Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

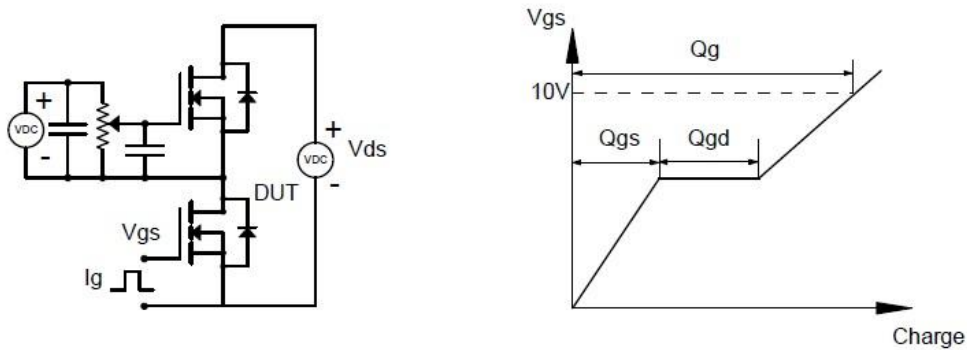


Figure B: Resistive Switching Test Circuit & Waveforms

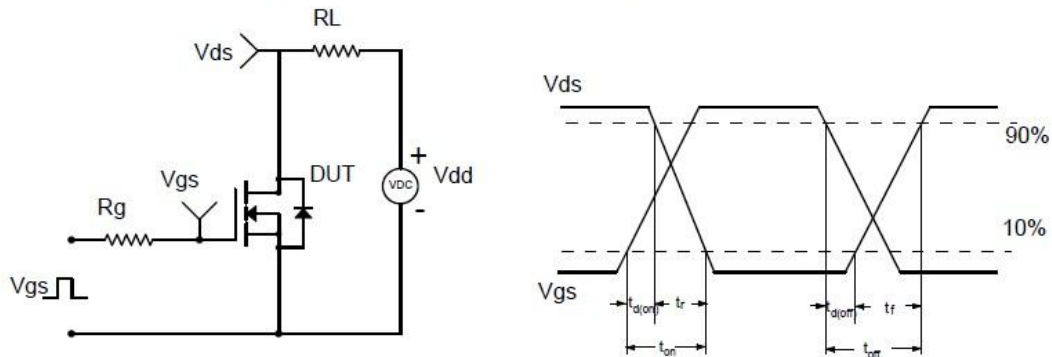


Figure C: Unclamped Inductive Switching (UIS) Test

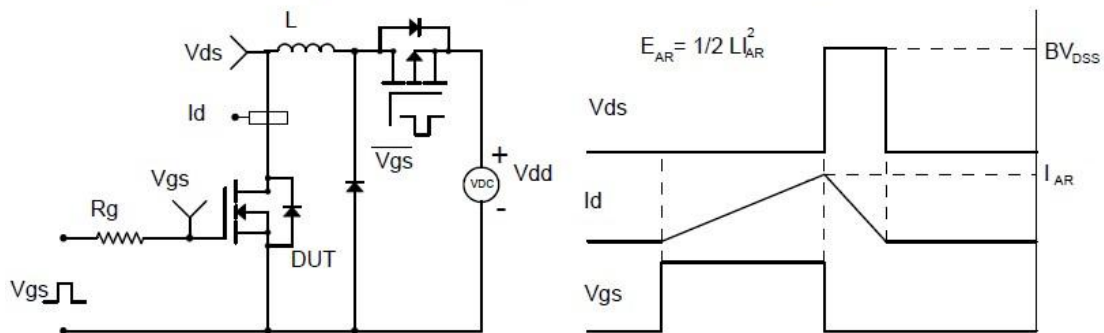
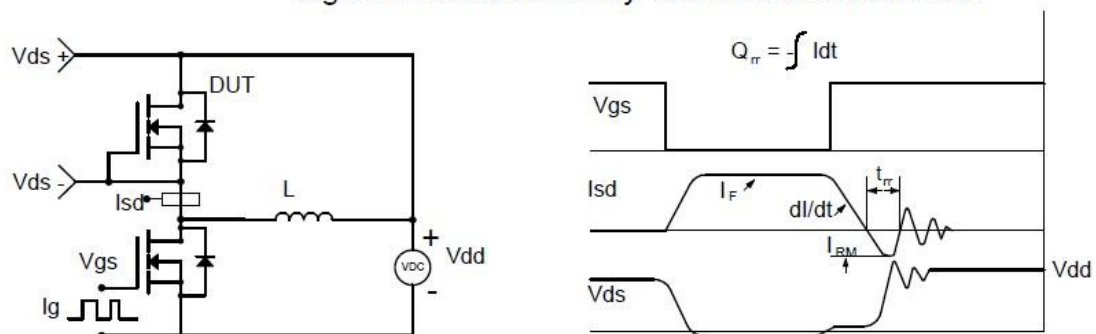
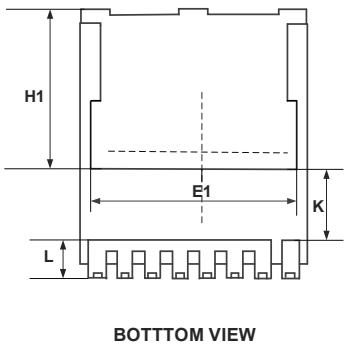
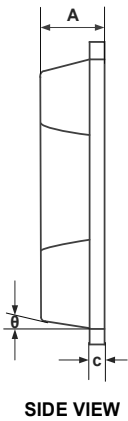
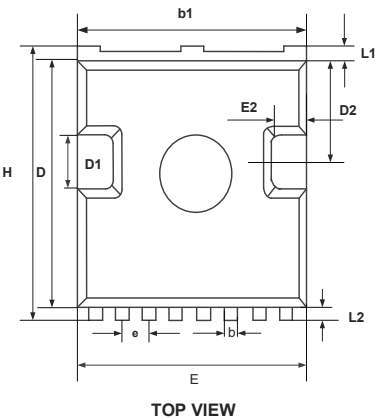


Figure D: Diode Recovery Test Circuit & Waveforms



Mechanical Dimensions for TOLL-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	