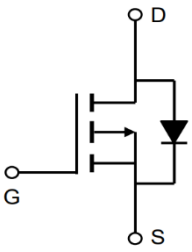
AP3401MI-L

-30V P-Channel Enhancement Mode MOSFET

Description

The AP3401MI-L uses advanced Trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

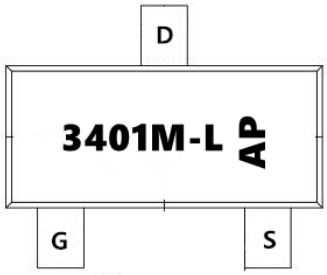


General Features

V_{DS} = -30V I_D =-4.2A

$R_{DS(ON)}$ < 55mΩ @ V_{GS}=10V **(Type：45mΩ)**

$R_{DS(ON)}$ < 68mΩ @ V_{GS}=4.5V **(Type：53mΩ)**



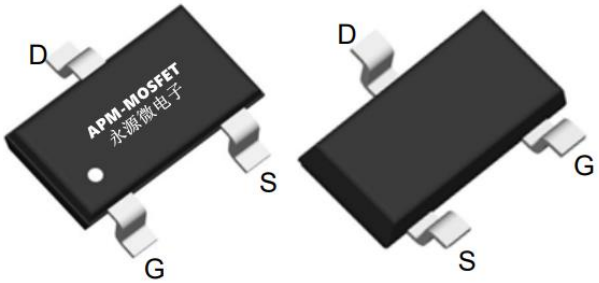
Top View **Bottom View**

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP3401MI-L	SOT23-3L	3401M-L AP	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage	-30	V
VGSS	Gate-Source Voltage	±12	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-4.2	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1]	-2.7	A
IDM	Pulsed Drain Current note1	-16.8	A
P_D	Power Dissipation T_A= 25℃	1.5	W
R_{θ}JA	Thermal Resistance Junction-Ambient [1]	125	℃/W
R_{θ}JC	Thermal Resistance Junction-Case[1]	124	℃/W
TJ, TSTG	Operating and Storage Temperature Range	-55 to +150	℃

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= -250μA	-30	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}= -30V, V_{GS}=0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}= ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= -250μA	-0.5	-0.9	-1.5	V
RDS(on)	Static Drain-Source on-Resistance note2	V_{GS}= -10V, I_D= -4A	-	45	55	mΩ
		V_{GS}= -4.5V, I_D= -3A	-	53	68	
		V_{GS}= -2.5V, I_D= -1A	-	72	96	V
Ciss	Input Capacitance	V_{DS}= -15V, V_{GS}=0V, f=1.0MHz	-	1500	-	pF
Coss	Output Capacitance		-	80	-	pF
Crss	Reverse Transfer Capacitance		-	2	-	pF
Q_g	Total Gate Charge	V_{DS}= -15V, I_D= -4.2A, V_{GS}= -10V	-	8.5	-	nC
Qgs	Gate-Source Charge		-	1.8	-	nC
Qgd	Gate-Drain("Miller") Charge		-	2.7	-	nC
td(on)	Turn-on Delay Time	V_{DD}= -15V, I_D= -1A, V_{GS}= -10V, R_{GEN}=2.5Ω	-	7	-	ns
tr	Turn-on Rise Time		-	3	-	ns
td(off)	Turn-off Delay Time		-	20	-	ns
t_f	Turn-off Fall Time		-	12	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4.2	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16.8	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S= -4.2A	-	-0.8	-1.2	V

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

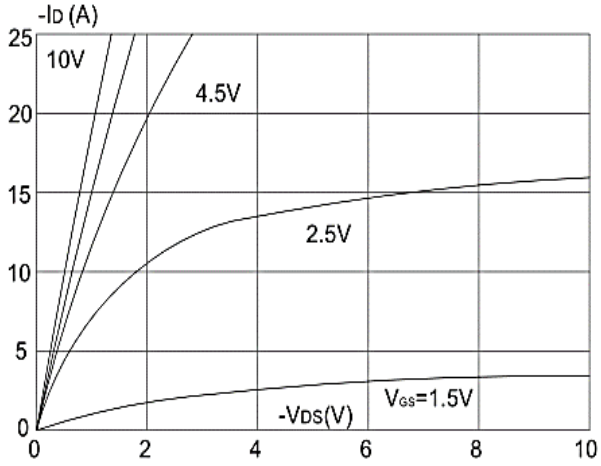


Figure1: Output Characteristics

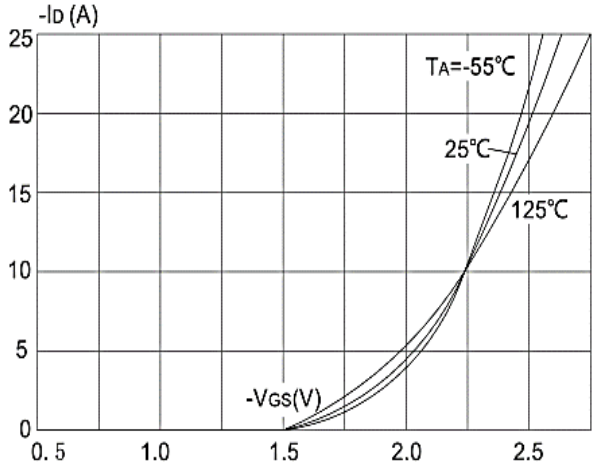


Figure 2: Typical Transfer Characteristics

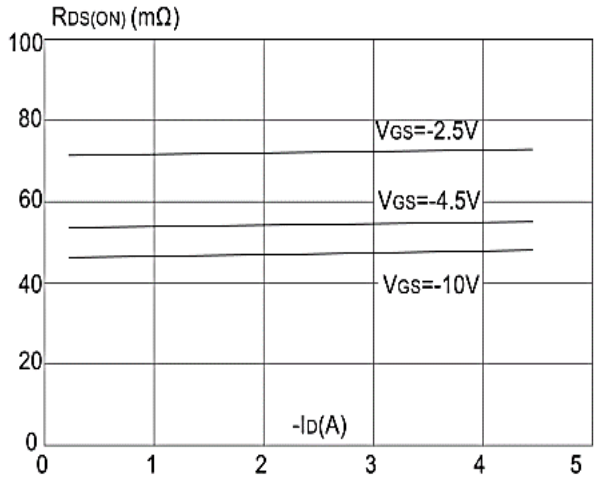


Figure 3:On-resistance vs. Drain Current

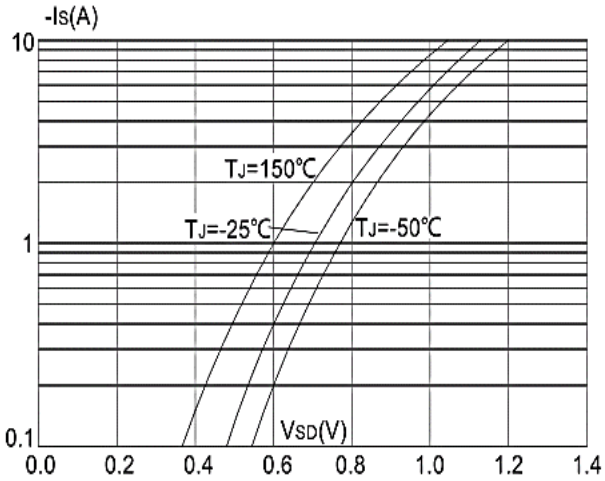


Figure 4: Body Diode Characteristics

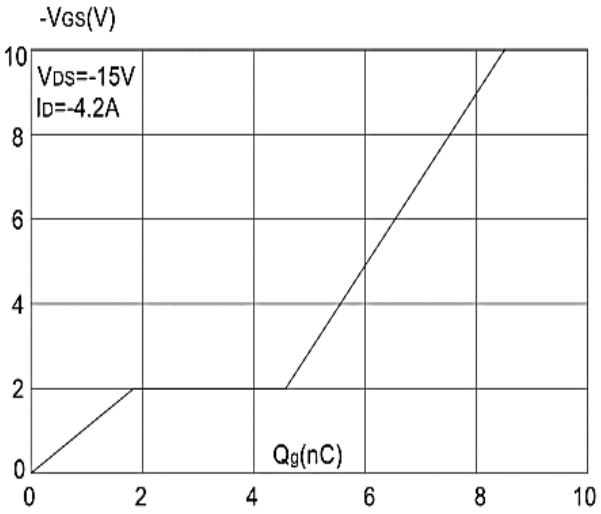


Figure 5: Gate Charge Characteristics

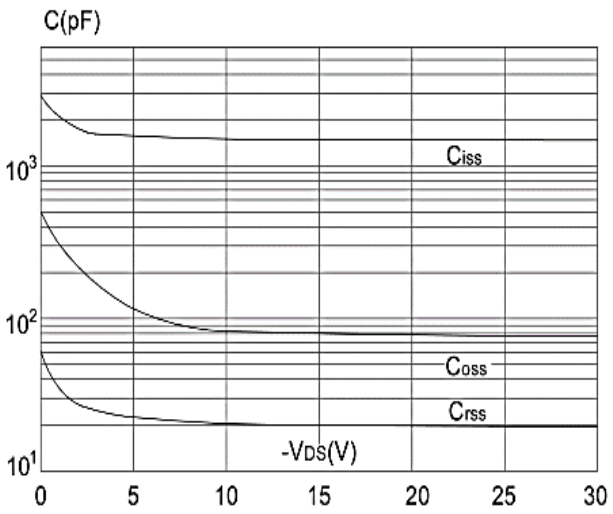


Figure 6: Capacitance Characteristics

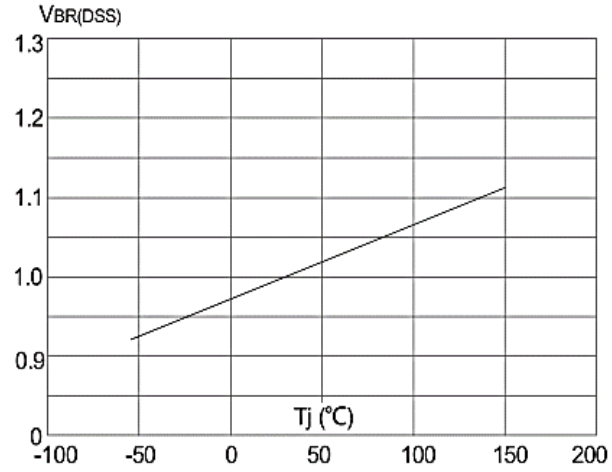


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

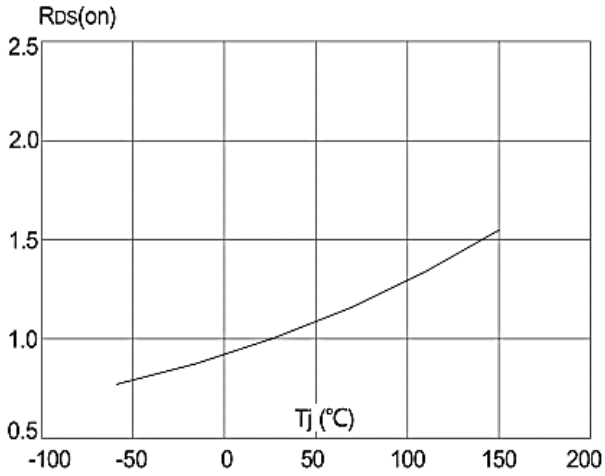


Figure 8: Normalized on Resistance vs. Junction Temperature

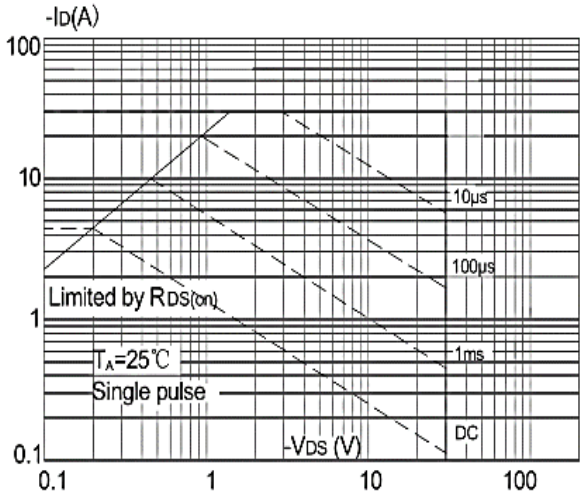


Figure 9: Maximum Safe Operating Area

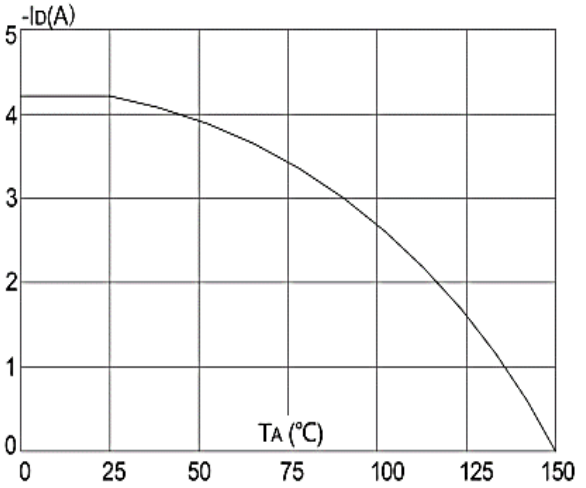


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

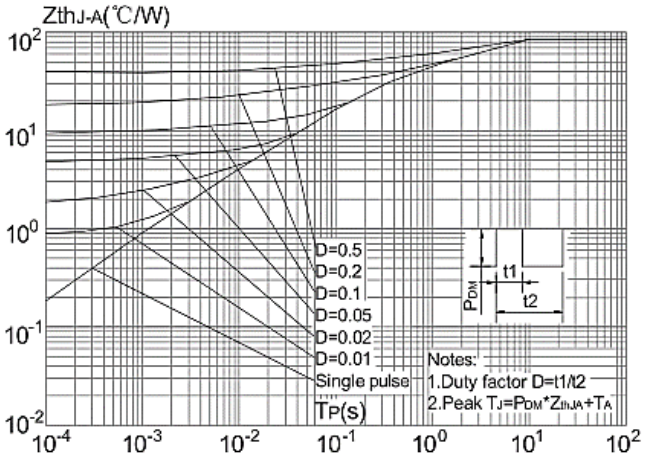
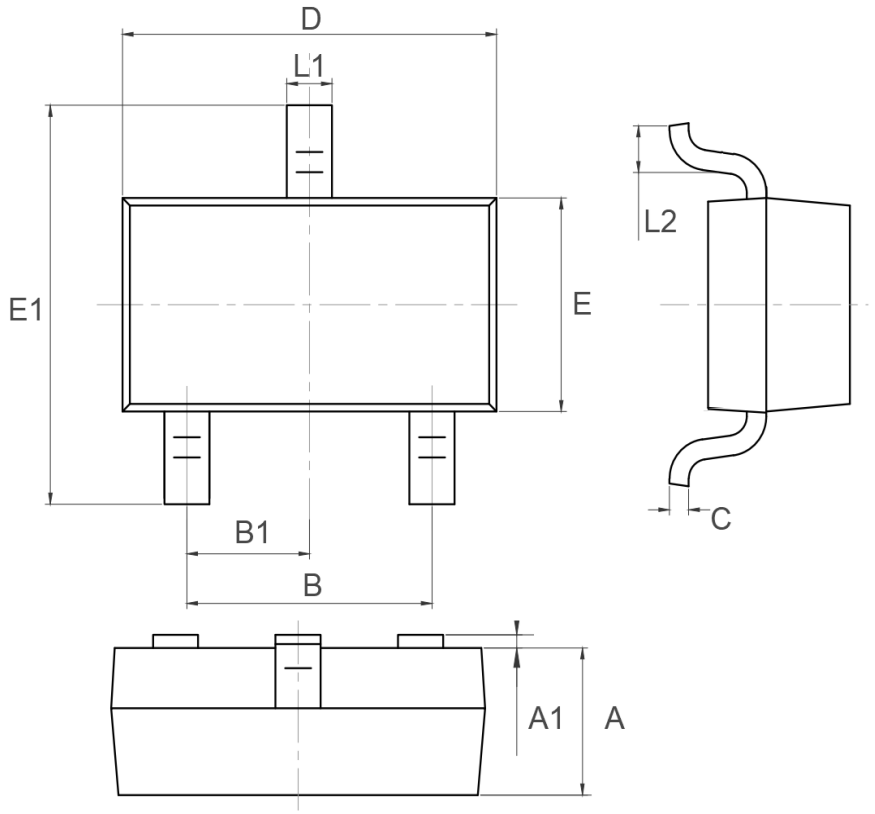


Figure.11: Maximum Effective TransientThermal Impedance, Junction-to-Ambient

Package Mechanical Data-SOT23-3L



Symbol	Dimensions In Millimeters		
	min.	Typ.	max.
A	1.00	1.10	1.20
A1	0.00	0.05	0.10
B	1.80	1.90	2.00
B1	0.95TYP		
C	0.10	0.15	0.20
D	2.82	2.92	3.02
E	1.50	1.60	1.70
E1	2.65	2.80	2.95
L1	0.30	0.40	0.50
L2	0.30	0.45	0.60

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-30V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2022/8/31	Initial release

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