1Gb DDR2 SDRAM Specification

Specifications

- Density: 1G bits
- Organization
  - 8 banks x 16M words x 8 bits
  - 8 banks x 8M words x 16 bits
- Package
  - 60-ball FBGA (x8)
  - 84-ball FBGA (x16)
  - Lead-free(RoHS compliant)
- Power supply
  - V_{DD},V_{DDQ}=1.7 to 1.9V
- Data Rate: 1066Mbps/800Mbps
- 1KB page size (x8)
  - Row address: AX0 to AX13
  - Column address: AY0 to AY9
- 2KB page size (x16)
  - Row address: AX0 to AX12
  - Column address: AY0 to AY9
- Eight internal banks for concurrent operation
- Interface: SSTL_18
  - Burst lengths (BL): 4 , 8
- Burst type (BT):
  - Sequential
  - Interleave
- CAS latency (CL): 3, 4, 5, 6, 7
- Precharge: Auto precharge option for each burst access
- Driver strength: Normal/Weak
- Low self-refresh current (IDD6) parts are available
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/64ms
  - Average auto-refresh period
    7.8us at TC ≤ +85℃
    3.9us at TC > +85℃
- Automotive grade 3 compliant with AEC-Q100 grade 3
- Automotive grade 2 compliant with AEC-Q100 grade 2
- Operating case temperature range
  - TC = 0°C to +85°C (Commercial grade)
  - TC = -40°C to +95°C (Industrial range)
  - TC = -40°C to +95°C (Automotive grade 3)
  - TC = -40°C to +105°C (Automotive grade 2)

Features

- Double data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 4 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center- aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination for better signal quality
- Programmable RDQS, /RDQS output for making x8 organization compatible with x4 organization
- /DQS, (/RDQS) can be disabled for single-ended Data Strobe operation
- Off-Chip Driver (OCD) impedance adjustment is not supported

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

Table of Contents

1Gb DDR2 SDRAM Specification 1

1. Ordering Information 3

2. Package Ball Assignment 4

3. Package outline drawing 5

4. Electrical Specifications: 7

5. Block Diagram 15

6. Pin function 16

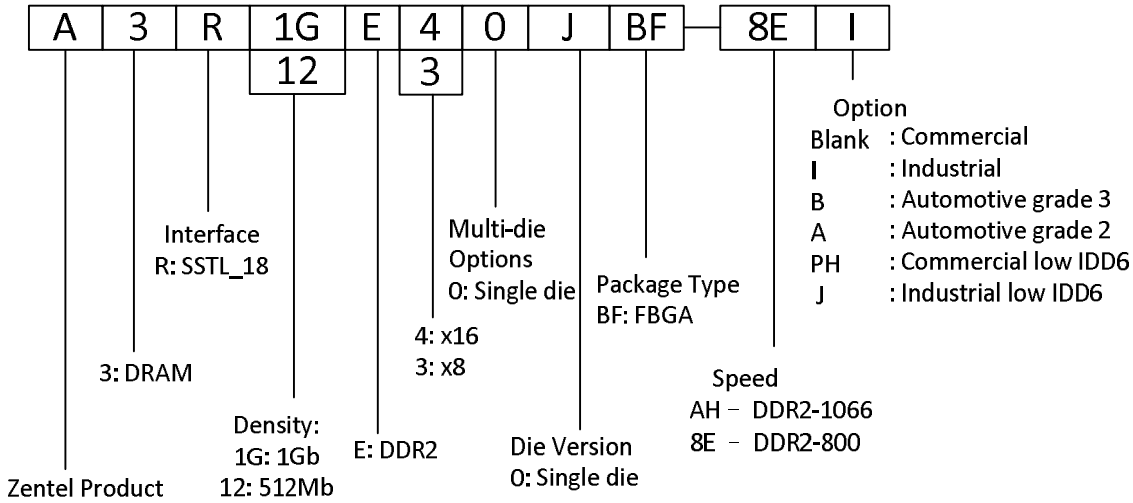
7. Command Operation 18

8. Functional Description 19

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

1. Ordering Information

Part Number	*Organization (words x bits)*	*Internal Banks*	*Speed bin (CL-tRCD-tRP)*	*Package*	*Note*
A3R1GE30JBF-8E/-8EI/-8EB/-8EA	128M × 8	8	DDR2-800 (5-5-5)	60-ball FBGA	
A3R1GE30JBF-AH/-AHI/-AHB/-AHA			DDR2-1066 (7-7-7)		
A3R1GE40JBF-8E/-8EI/-8EB/-8EA	64M × 16	8	DDR2-800 (5-5-5)	84-ball FBGA	
A3R1GE40JBF-AH/-AHI/-AHB/-AHA			DDR2-1066 (7-7-7)		
A3R1GE40JBF-8EPH	64M × 16	8	DDR2-800 (5-5-5)	84-ball FBGA	Low IDD6
A3R1GE40JBF-8EJ	64M × 16	8	DDR2-800 (5-5-5)	84-ball FBGA	
A3R1GE30JBF-8EJ	128M × 8	8	DDR2-800 (5-5-5)	60-ball FBGA	



Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

2. Package Ball Assignment

x8 : "60-Ball FBGA – 8x10.5mm, ball pitch 0.8mm, ball size 0.45mm. (package code BF)"

x16 : "84-Ball FBGA – 8x12.5mm, ball pitch 0.8mm, ball size 0.45mm. (package code BF)"

60-ball FBGA
(×8 organization)

	1	2	3	7	8	9
A	VDD	NU/ /RDQS	VSS	VSSQ	/DQS	VDDQ
B	DQ6	VSSQ	DM/RDQS	DQS	VSSQ	DQ7
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE	/WE	/RAS	/CK	ODT
G	BA2	BA0	BA1	/CAS	/CS	
H		A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	
K		A7	A9	A11	A8	VSS
L	VDD	A12	NC	NC	A13	

(Top view)

84-ball FBGA
(×16 organization)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSSQ	/UDQS	VDDQ
B	DQ14	VSSQ	UDM	UDQS	VSSQ	DQ15
C	VDDQ	DQ9	VDDQ	VDDQ	DQ8	VDDQ
D	DQ12	VSSQ	DQ11	DQ10	VSSQ	DQ13
E	VDD	NC	VSS	VSSQ	/LDQS	VDDQ
F	DQ6	VSSQ	LDM	LDQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	/WE	/RAS	/CK	ODT
L	BA2	BA0	BA1	/CAS	/CS	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	NC	NC	NC	

(Top view)

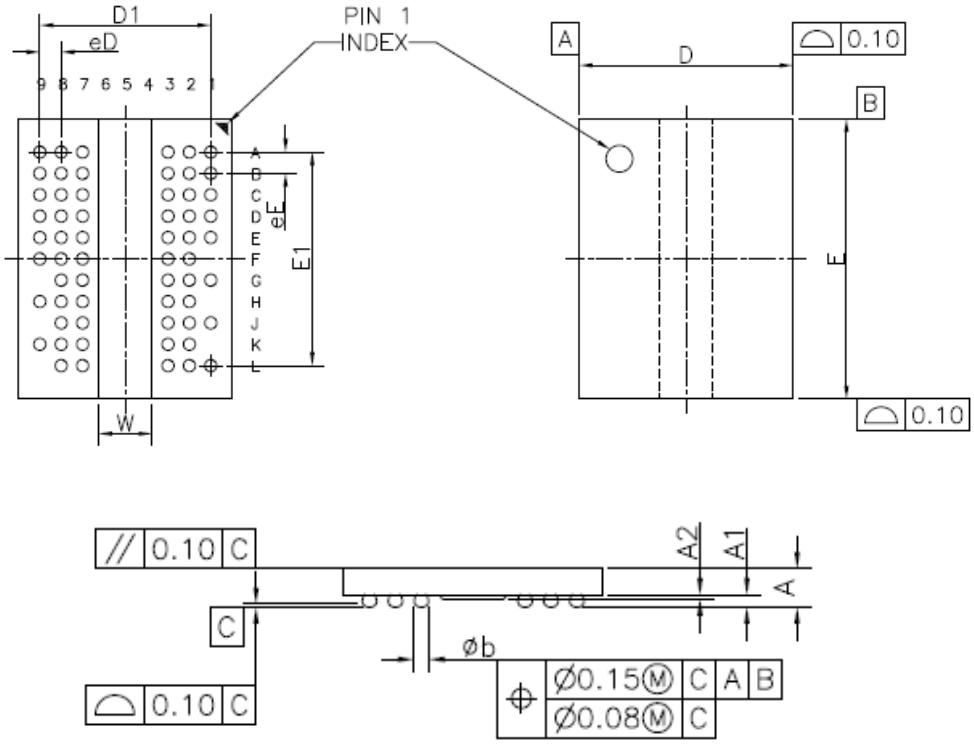
Pin name	Function	Pin name	Function
A0 to A13	Address inputs	ODT	ODT control
BA0 to BA2	Bank select	VDD	Power Supply
DQ0 to DQ15	Data input/output	VSS	Ground
DQS, /DQS	Differential data strobe	VDDQ	Power Supply for DQ circuit
UDQS, /UDQS		VSSQ	Ground for DQ circuit
LDQS, /LDQS		VREF	Input reference voltage
/CS	Chip select	VDDL	Power Supply for DLL circuit
/RAS, /CAS, /WE	Command input	VSSDL	Ground for DLL circuit
CKE	Clock enable	NC	No connection
CK, /CK	Differential clock input	NU	Not usable

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

3. Package outline drawing

x8 , 60-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu) Unit: mm



Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.30	0.35	0.40
A2	0.10	0.15	0.20
D	7.90	8.00	8.10
D1	6.40 BSC		
E	10.40	10.50	10.60
E1	8.00 BSC		
b	0.40	0.45	0.50
eD	0.80 BSC		
eE	0.80 BSC		
W	2.00 BSC		

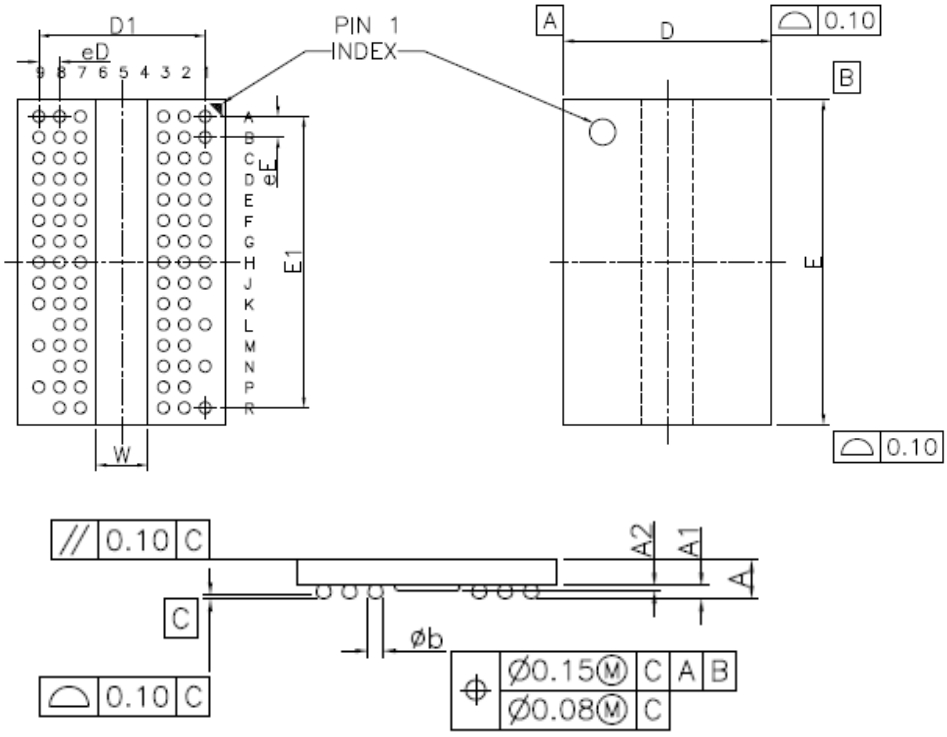
Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

x16 , 84-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm

Unit: mm



Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.30	0.35	0.40
A2	0.10	0.15	0.20
D	7.90	8.00	8.10
D1	6.40 BSC		
E	12.40	12.50	12.60
E1	11.20 BSC		
b	0.40	0.45	0.50
eD	0.80 BSC		
eE	0.80 BSC		
W	2.00 BSC		

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

4. Electrical Specifications:

All voltages are referenced to each GND level (VSS and VSSQ).

Execute power-up and Initialization sequence before proper device operation can be achieved.

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power supply voltage	VDD	-1.0 to +2.3	V	1
Power supply voltage for output	VDDQ	-0.5 to +2.3	V	1
Power supply voltage for DLL	VDDL	-0.5 to +2.3	V	1
Input voltage	VIN	-0.5 to +2.3	V	1
Output voltage	VOUT	-0.5 to +2.3	V	1
Storage temperature	Tstg	- 55 to +150	°C	1, 2
Power dissipation	PD	1.0	W	1

Notes:

1. Stresses greater than those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

4.2 Operating Temperature Condition

Product grades	Parameter	Symbol	Rating	Unit	Note
Commercial	Operating case temperature	TC	0 to +85	°C	1, 2, 3
Industrial		TC	-40 to +95	°C	1, 3
Automotive grade 3		TC	-40 to +95	°C	1, 3
Automotive grade 2		TC	-40 to 105	°C	1, 3

Notes :

1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. Supporting 0 to +85°C with full AC and DC specifications.
3. Supporting up to +85°C and being able to extend to +95°C or +105°C (Automotive grade 2 only) with doubling auto-refresh commands in frequency to a 32ms period (tREFI = 3.9µs) and higher temperature Self-Refresh entry via A7 “1” on EMRS(2).

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

4.3 Recommended DC Operating Conditions(SSTL_18)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Power Supply voltage	VDD	1.7	1.8	1.9	V	4
Power Supply voltage for output	VDDQ	1.7	1.8	1.9	V	4
Power Supply voltage for DLL	VDDL	1.7	1.8	1.9	V	4
Input reference voltage	VREF	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	1.2
Termination voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	3
DC input logic high	VIH (DC)	VREF + 0.125	-	VDDQ + 0.3	V	
DC input logic low	VIL (DC)	-0.3	-	VREF - 0.125	V	
AC input logic high	VIH (AC)	VREF + 0.200	-	-	V	
AC input logic low	VIL (AC)	-	-	VREF - 0.200	V	

Notes:

1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF are expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed ±2% VREF (DC)
3. VTT of transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together.

4.4 Overshoot / Undershoot Specification

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

4.5 DC Characteristics

Parameter	Test Condition	Symbol	Speed	IO		Unit
				X8	X16	
Operating current (ACT- PRE)	one bank; tCK = tCK (IDD), tRC = tRC (IDD), tRAS min. (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	-8E	70	70	mA
			-AH	75	75	mA

Operating current (ACT-READ-PRE)	one bank; IOUT = 0mA; BL = 4,CL = CL(IDD), AL = 0;
	tCK = tCK (IDD), tRC = tRC (IDD);
	tRAS =tRAS min. (IDD); tRCD = tRCD (IDD);
	CKE is H, /CS is H between valid commands;
	Address bus inputs are SWITCHING;
	Data pattern is same as IDD4W
		IDD1	-8E	75	75	mA

			-AH	80	80	mA
Precharge power-down standby current	all banks idle; tCK = tCK (IDD);CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	-8E	20	20	mA
			-AH	25	25	mA
Precharge quiet Standby current	all banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	-8E	30	30	mA
			-AH	35	35	mA
Idle standby current	all banks idel tCK = tCK (IDD);CKE is H, /CS is H; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITDCHING	IDD2N	-8E	35	35	mA
			-AH	40	40	mA
Active power–down Standby current (Fast PND Exit)	All banks open; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus input are Floating; MRS(12)=0	IDD3P-F	-8E	40	40	mA
			-AH	45	45	mA
Active power–down Standby current (Slow PND Exit)	All banks open;tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus input are Floating; MRS(12)=1	IDD3P-S	-8E	35	35	mA
			-AH	40	40	mA
Active standby current	all banks open; tCK = tCK (IDD); tRAS = tRAS max. (IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	-8E	70	70	mA
			-AH	75	75	mA

Operating current (Burst read operating)	all banks open, continuous burst reads, IOUT = 0mA;
	BL = 4,CL = CL(IDD), AL = 0;
	tCK = tCK (IDD);tRAS = tRAS max. (IDD), tRP = tRP (IDD);
	CKE is H, /CS is H between valid commands;
	Address bus inputs are SWITCHING;
	Data pattern is same as IDD4W
		IDD4R	-8E	135	135	mA

			-AH	165	165	mA
Operating current (Burst write operating)	all banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD),tRAS = tRAS max. (IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD4W	-8E	160	160	mA
			-AH	200	200	mA

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

Parameter	Test Condition	Symbol	Speed	IO		Unit
				X8	X16	
Auto-refresh current	tCK = tCK (IDD); Refresh command every tRFC (IDD) interval; CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	-8E	110	110	mA
			-AH	120	120	mA
Self-refresh current	Self Refresh Mode; CK and /CK at 0V; CKE ≦ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	-8E, -AH	10	10	mA
			-8EPH	-	6	mA
			-8EJ ≤ 85°C	5	5	mA
			-8EJ > 85°C	7	7	mA
Operating current (Bank interleaving)	all bank interleaving reads, IOUT = 0mA; BL = 4, CL= CL (IDD), AL = tRCD (IDD) – 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = 1 x tCK (IDD) CKE is H, CS is H between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4W;	IDD7	-8E	175	175	mA
			-AH	185	185	mA

Notes:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Input Test Condition.
3. Data bus consists of DQ, DM, DQS, /DQS, RDQS and /RDQS, IDD values must be met with all combinations of EMRS bits 10 and 11.
4. Definitions for IDD
   L is defined as VIN no greater than VIL (AC) (max.)
   H is defined as VIN no less than VIH (AC) (min.)
   STABLE is defined as inputs stable at an H or L level
   FLOATING is defined as inputs at VREF = VDDQ/2
   SWITCHING is defined as:
   Inputs changing between H and L every other clock cycle (once per two clocks) for address and control signals, and inputs changing between H and L every other data transfer (once per clock) for DQ signals not including masks or strobes.
5. Refer to AC Timing for IDD Test Conditions.
6. When TC > 85°C, IDD6 must be increased by 50% (IDD6 will increase by this amount if TC < 85°C and double refresh option is still enabled)
7. For Automotive grade 2 products, when TC > 95°C, IDD0-IDD5 and IDD7 must be increased by 10%

AC Timing for IDD Test Conditions

For purposes of IDD testing, the following parameters are to be utilized.

Parameter	DDR2-800 (5-5-5)	DDR2-1066 (7-7-7)	Unit
CL(IDD)	5	7	tCK
tRCD(IDD)	12.5	13.125	ns
tRC(IDD)	57.5	58.125	ns
tRRD(IDD)-x8	7.5	7.5	ns
tRRD(IDD)-x16	10	10	ns
tCK(IDD)	2.5	1.875	ns
tRAS(min.)(IDD)	45	45	ns
tRAS(max.)(IDD)	70000	70000	ns
tRP(IDD)	12.5	13.125	ns

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

4.6 Leakage characteristics

Parameter	Symobl	Value	Unit	Notes
Input leakage current	|ILI|	2	µA	VSS ≤ VIN ≤ VDD
Output leakage current	|ILO|	5	µA	VSSQ ≤ VOUT ≤ VDDQ

4.7 Output AC Test conditions and Output DC current drive

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

4.8 Differential input AC logic level and Differential AC output parameters

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

4.9 ODT DC Electrical Characteristics

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

4.10 Pin Capacitance (TA = 25℃, VDD, VDDQ = 1.8V ± 0.1V)

Parameter	Symbol	Pins	min	max	Unit	Notes
CLK input pin capacitance	CCK	CK, /CK	1.0	2.0	pF	1
Input pin capacitance	CIN	/CS, /RAS, /CAS, /WE, CKE, ODT, Address	1.0	1.75	pF	1
Input/output pin capacitance	CI/O	DQ, UDQS, /UDQS, LDQS, /LDQS, UDM, LDM	2.5	3.5	pf	2

Notes:
1. Matching within 0.25pF.
2. Matching within 0.50pF.

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

4.11 AC Characteristics

New unit tCK(avg) and nCK, are introduced in DDR2-1066 and DDR2-800
tCK(avg): actual tCK(avg) of the input clock under operation.
nCK: one clock cycle of the input clock, counting the actual clock edges.

Parameter	Symbol	min/max	Data Rate		Unit
			800	1066	MT/s
Max. Frequency	-	-	400	533	MHz
CAS Latency	CL	-	3, 4, 5, 6, 7		nCK
Clock Timing					
Clock cycle time @ CL=3	tCK(avg)	min	5000		ps
Clock cycle time @ CL=4	tCK(avg)	min	3750		ps
Clock cycle time @ CL=5	tCK(avg)	min	2500		ps
Clock cycle time @ CL=6	tCK(avg)	min	2500		ps
Clock cycle time @ CL=7	tCK(avg)	min	1875		ps
Max. clock cycle time for all latency	tCK(avg)	max	8000		ps
Average High pulse width	tCH(avg)	min	0.45		tCK(avg)
		max	0.55		tCK(avg)
Average Low pulse width	tCL(avg)	min	0.45		tCK(avg)
		max	0.55		tCK(avg)
CK half period	tHP	min	min(tCH(abs), tCL(abs))		ps
Core Timing Parameters					
Active to read/write command delay	tRCD	min	12.5	13.125	ns
Precharge command period	tRP	min	12.5	13.125	ns
Active to precharge command	tRAS	min	45		ns
		max	70000		ns
ACTIVATE-to-ACTIVATE command period	tRC	min	57.5	58.125	ns
CAS-to-CAS delay	tCCD	min	2		tCK(avg)
Internal READ-to-PRECHARGE command delay	tRTP	min	7.5		ns
Write recovery time	tWR	min	15		ns
Write-to-read delay	tWTR	min	7.5		ns
Active bank A to active bank B (x8)	tRRD	min	7.5		ns
Active bank A to active bank B (x16)		min	10		ns
Four active window period (x8)	tFAW	min	35		ns
Four active window period (x16)		min	45		ns
Address and control input hold time	tIH(base)	min	250	200	ps
Address and control input setup time	tIS(base)	min	175	125	ps
Read preamble	tRPRE	min	0.9		tCK(avg)
		max	1.1		tCK(avg)
READ postamble	tRPST	min	0.4		tCK(avg)
		max	0.6		tCK(avg)
DQ low-impedance time from CK, /CK	tLZ(DQ)	min	2 x tAC(min)		ps
		max	tAC(max)		ps
DQS low-impedance time from CK, /CK	tLZ(DQS)	min	tAC(min)		ps
		max	tAC(max)		ps
Data-out high-impedance time from CK,	tHZ	max	tAC(max)		ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	max	200	175	ps

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

Parameter	*Symbol*	*min/max*	*Data Rate*		*Unit*
			800	*1066*	*MT/s*
DQS output access time from CK, /CK	tDQSCK	min	+350	+325	ps
		max	-350	-325	
DQ output access time from CK, /CK	tAC	min	+400	+350	ps
		max	-400	-350	ps
DQ hold skew factor	tQHS	max	300	250	ps
DQ/DQS output hold time form DQS	tQH	min	tHP - tQHS		ps
Write command to DQS associated clock edge	WL	-	RL - 1		nCK
DQ and DM input hold time	tDH(base)	min	125	75	ps
DQ and DM input setup time	tDS(base)	min	50	0	ps
DQS latching rising transitions to associated clock edges	tDQSS	min	+0.25		tCK(avg)
		max	-0.25		
DQS input HIGH-level width	tDQSH	min	0.35		tCK(avg)
DQS input LOW-level width	tDQSL	min	0.35		tCK(avg)
DQS falling edge to CK setup time	tDSS	min	0.2		tCK(avg)
DQS falling edge hold time from CK	tDSH	min	0.2		tCK(avg)
Write preamble	tWPRE	min	0.35		tCK(avg)
Write postamble	tWPST	min	0.4		tCK(avg)
		max	0.6		tCK(avg)
Control and Address input pulse width for each input	tIPW	min	0.6		tCK(avg)
DQ and DM input pulse width for each input	tDIPW	min	0.35		tCK(avg)
Mode register set command delay	tMRD	min	2		nCK
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	min	3		nCK
Exit self refresh to a non-read command	tXSNR	min	tRFC + 10		ns
Exit self refresh to a read command	tXSRD	min	200		nCK
Exit precharge power-down to any non-read command	tXP	min	2	3	nCK
Exit active power-down to read	tXARD	min	2	3	nCK
Exit active power-down to read (slow exit low power mode)	tXARDS	min	8-AL	10-AL	nCK
Auto precharge write recovery + precharge time	tDAL	min	WR + RU(tRP/tCK(avg))		nCK
Outpt impedance test driver delay	tOIT	min	0		ns
		max	12		
MRS command to ODT update delay	tMOD	min	0		ns
		max	12		
Auto refresh to active/auto refresh command time	tRFC	min	127.5		ns
Average periodic refresh interval (TC ≦ +85℃)	tREFI	max	7.8		us
Average periodic refresh interval (TC ＞ +85℃)			3.9		us
Minimum time clocks remains ON after CKE asynchronously drops low	tDELAY	min	tIS + tCK(avg) + tIH		ns

Note:
[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

4.12 AC Input Test Conditions

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

4.13 Clock Jitter

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

4.14 Input Slew Rate Derating

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

4.15 ODT AC Electrical Characteristics

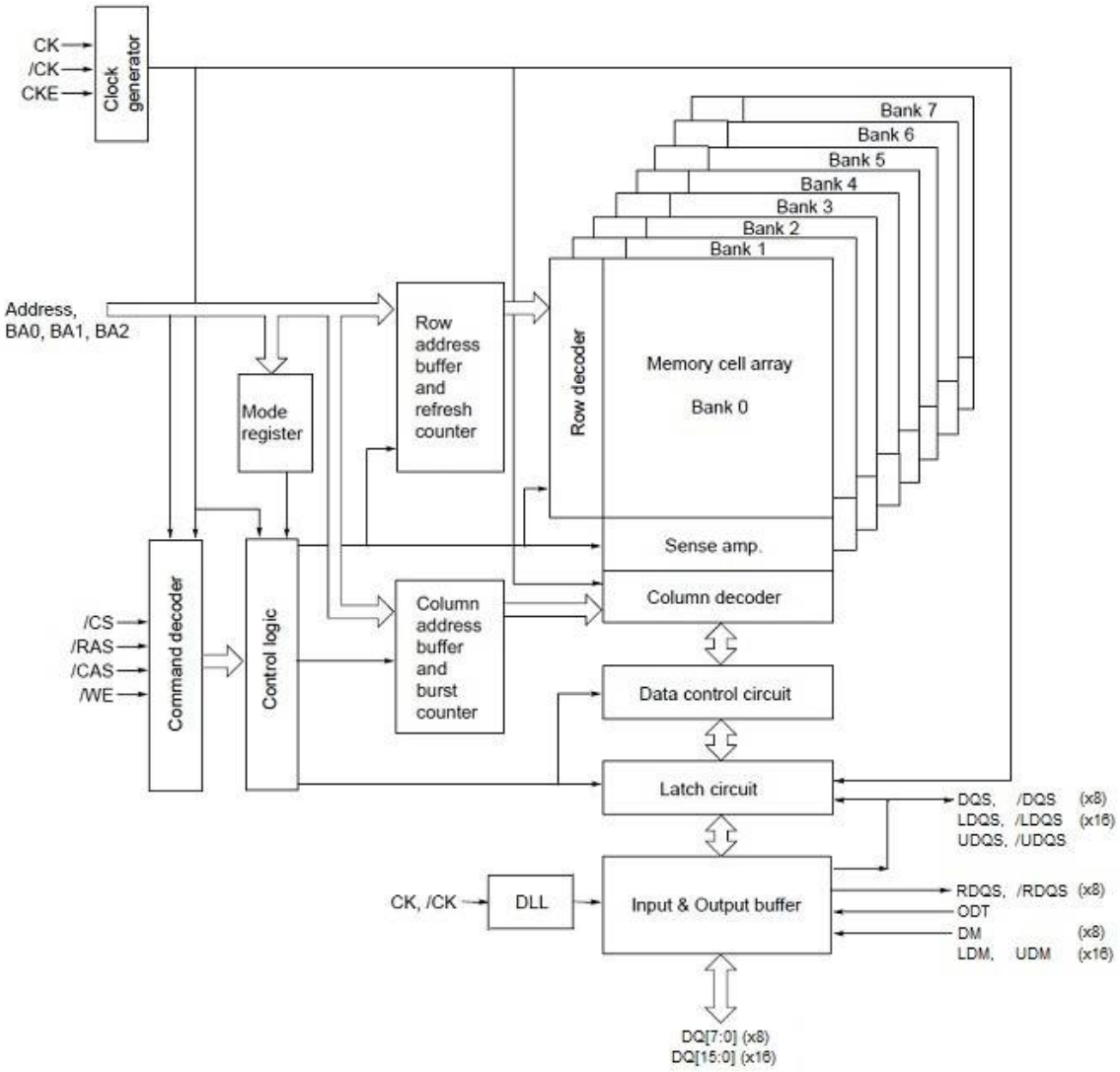
[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

4.16 AC Input Test Conditions

[Refer to section 6 in JEDEC Standard No. JESD79-2F and section 5 in JESD208]

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

5. Block Diagram



Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

6. Pin function

CK,/CK (input pins)
CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of Ck and negative edge of /CK. Output (read)data is referenced to the crossings of CK and /CK (both directions of crossing.)

/CS (input pin)
all commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

/RAS, /CAS, /WE (input pins)
/RAS, /CAS and /WE(along with /CS) define the command being entered.

A0 to A13 (input pins)
Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during mode register set commands.

Configuration	Address (A0 to A13)		Note
	Row address	Column address	
x8	AX0 to AX13	AY0 to AY9	
x16	AX0 to AX12	AY0 to AY9	

A10 (AP) (input pin)
A10 is sampled during a precharge command.

BA0, BA1, BA2 (input pins)
BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS(1), EMRS(2) cycle.

[Bank Select signal Table]

Bank	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H=VIH , L=VIL

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

CKE (input pin)
CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and Self Refresh operation (bank idle), or active power-down (row active in bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

DM, UDM and LDM (input pins)
DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
In x16 configuration, UDM controls upper byte (DQ8 to DQ15) and LDM controls lower byte (DQ0 to DQ7). In this datasheet, DM represents UDM and LDM.

DQ (input/output pins)
Bi-directional data bus.

DQS, /DQS (UDQS, /UDQS, LDQS, /LDQS (input/output pins)
Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, centered in write data. Used to capture write data. /DQS can be disable by EMRS.
In x16 configuration, UDQS, /UDQS and LDQS, /LDQS control upper byte (DQ8 to DQ15) and lower byte (DQ0 to DQ7). In this datasheet, DQS represents UDQS and LDQS, and /DQS represents /UDQS and /LDQS.

RDQS, /RDQS (output pins)
Differential Data Strobe for READ operation only. DM and RDQS functions are switch able by EMRS. These pins exist only in x8 configuration /RDQS output will be disable when /DQS is disabled by EMRS.

ODT (input pins)
ODT (On Die Termination control) is a registered high signal that enables termination resistance internal to the DDR II SDRAM. When enable, ODT is only applied to each DQ, DQS, /DQS, RDQS, /RDQS, and DM signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, UDQS, /UDQS, LDQS, /LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT. Any time the EMRS enables the ODT function; ODT may not be driven high until eight clocks after the EMRS has been enabled.

VDD, VSS, VDDQ, VSSQ (power supply)
VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

VDDL and VSSDL (power supply)
VDDL and VSSDL are power supply pins for DLL circuits.

VREF (Power supply)
SSTL_18 reference voltage: (0.50±0.01) x VDDQ

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

7. Command Operation

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the speechified initialization sequence before normal operation can continue

7.1 Command Truth Table

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA2-BA0	A13-A11	A10	A9-A0	Notes
		Previou	Currnet									
(Extended) Mode register set	(E)MRS	H	H	L	L	L	L	Register	OP CODE			1
Auto refresh	REF	H	H	L	L	L	H	X	X	X	X	1
Self refresh entry	SELF	H	L	L	L	L	H	X	X	X	X	1
Self refresh exit	SELEX	L	H	H	X	X	X	X	X	X	X	1, 6
				L	H	H	H					
Single bank precharge	PRE	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge all banks	PALL	H	H	L	L	H	L	X	X	H	X	1
Bank activate	ACT	H	H	L	L	H	H	BA	Row Address			1, 2, 7
Write	WRIT	H	H	L	H	L	L	BA	CA	L	CA	1, 2, 3
Write with auto precharge	WRITA	H	H	L	H	L	L	BA	CA	H	CA	1, 2, 3
Read	READ	H	H	L	H	L	H	BA	CA	L	CA	1, 2, 3
Read with auto precharge	READA	H	H	L	H	L	H	BA	CA	H	CA	1, 2, 3
No operation	NOP	H	X	L	H	H	H	X	X	X	X	1
Device deselect	DESL	H	X	H	X	X	X	X	X	X	X	1
Power down mode entry	PDEN	H	L	H	X	X	X	X	X	X	X	1, 4
				L	H	H	H					
Power down mode exit	PDEX	L	H	H	X	X	X	X	X	X	X	1, 4
				L	H	H	H					

Notes:

1. All DDR2 commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock
2. Bank select (BA0, BA1 and BA2), determine which bank is to be operated upon
3. Burst reads or writes should not be terminated other than specified as “Reads interrupted by a Read” in burst read command[READ] or “Writes interrupted by a Write” in burst write command [WRIT]
4. The power down mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements of the device. Onc clock delay is required for mode entry and exit
5. The state of ODT does not affect the states described in this table. The ODT function is no available during self-refresh
6. Self-refresh exit is asynchronous
7. 8-bank device sequential bank activation restriction: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

7.2 CKE Truth Table

[Refer to section 4 in JEDEC Standard No. JESD79-2F and section 3 in JESD208]

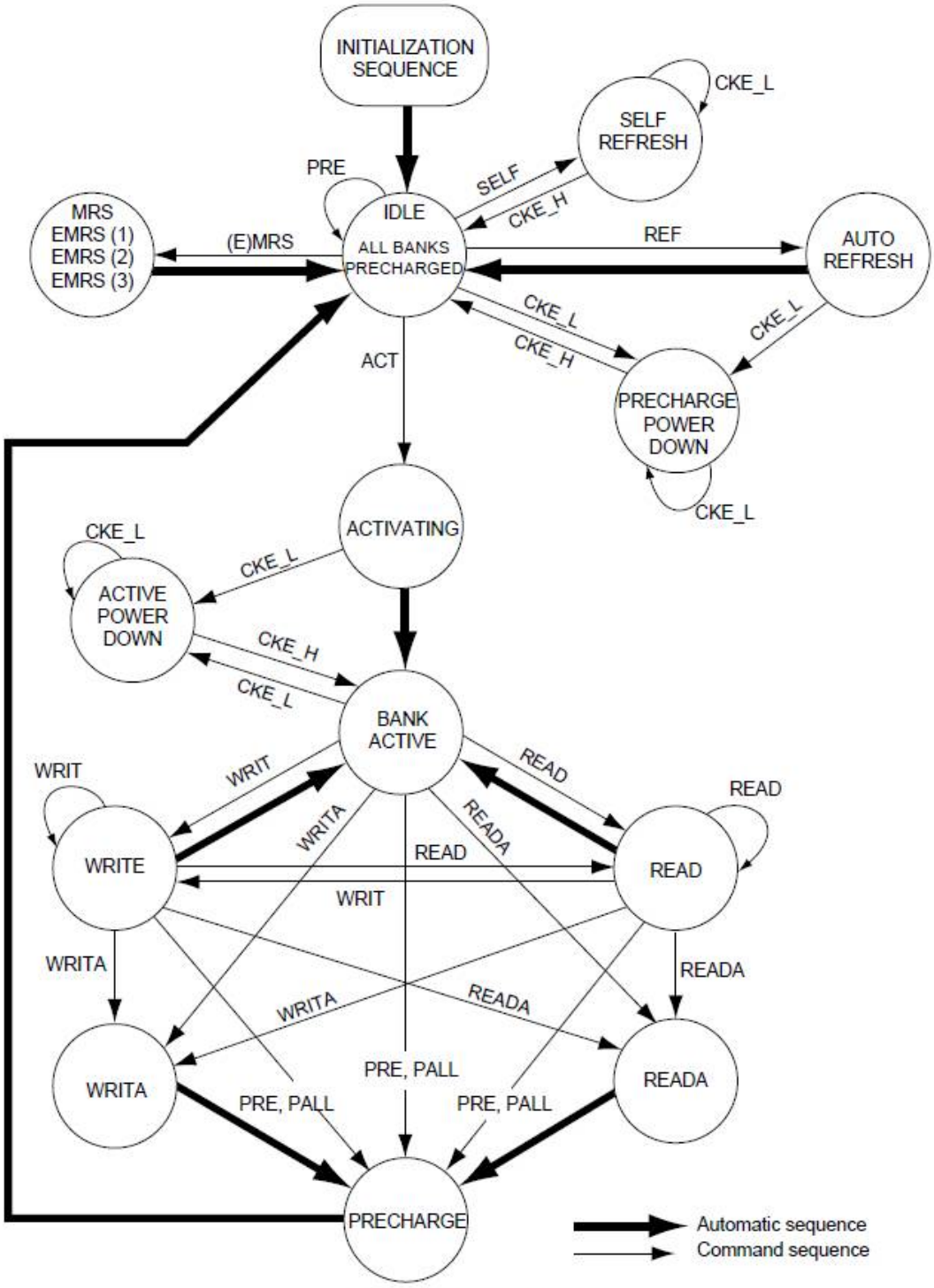
7.3 Data Mask Truth Table

[Refer to section 4 in JEDEC Standard No. JESD79-2F and section 3 in JESD208]

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

8. Functional Description

8.1 Simplified State Diagram



Simplified State Diagram

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

8.2 Basic functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of four or eight in a programmed sequence. Accesses begin with the registration of an active command, which is then followed by a read or write command. The address bits registered coincident with the active command is used to select the bank and row to be accessed (BA0, BA1 and BA2 select the bank; A0 to A13 select the row). The address bits registered coincident with the read or write command are used to select the staring column location for the burs access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization; register definition, command descriptions and device operation.

8.3 Power On and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

8.4 Power-Up and Initialization Sequence

The following sequence is required for power up and initialization

1. Apply power and attempt to maintain CKE below 0.2 x VDDQ (all other inputs may be undefined).
   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95V max, AND
   - VREF tracks VDDQ/2.

     or
   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT and VREF.

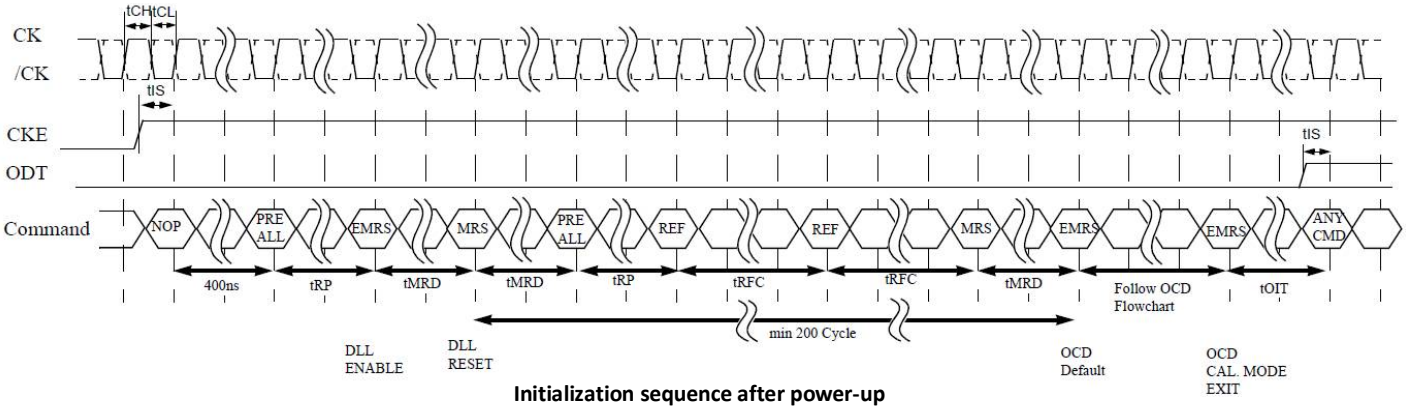
     At least one of these two sets of conditions must be met.
2. Start clock and maintain stable condition
3. For the minimum of 200µs after stable power and clock(CK, /CK), then apply [NOP] or [DESL] and take CKE high.
4. Wait minimum of 400ns then issue precharge all command. [NOP] or [DESL] applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide low to BA0 and BA2, high to BA1)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide low to BA2, high to BA0 and BA1)
7. Issue EMRS(1) to enable DLL. (To issue DLL enable command, provide low to A0, high to BA0 and low to BA1, BA2 and A13)
8. Issue a mode register set command for DLL reset.

(To issue DLL reset command, provide high to A8 and low to BA0, BA1, BA2 and A13)

9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation.

(i.e. to program operating parameters without resetting the DLL.)

12. At least 200 clocks after step 8, issue EMRS (1) command with A9 = A8 = A7 = 1. Then issue EMRS (1) command with A9 = A8 = A7 = 0 with other operating parameters of EMRS (1).
13. The DDR2 SDRAM is now ready for normal operation.



Initialization sequence after power-up

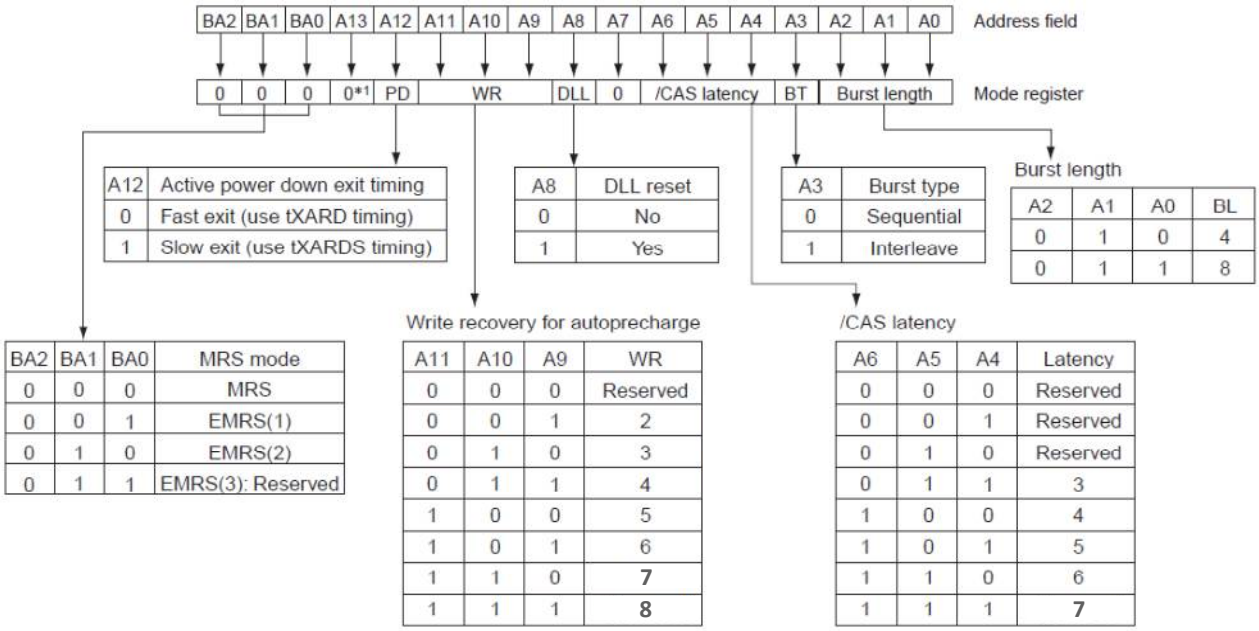
Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

8.5 Programming the Mode Register and Extended Mode Registers

For application flexibility, burst length, burst type, /CAS latency, DLL reset function, write recovery time (tWR) are user defined variables and must be programmed with a mode register set command [MRS]. Additionally, DLL disable function, driver impedance, additive /CAS latency, ODT (On Die Termination), and single-ended strobe are also user defined variables and must be programmed with an extended mode register set command [EMRS]. Contents of the Mode Register (MR) or Extended Mode Registers (EMRS(#)) can be altered by reexecuting the MRS and EMRS commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.
MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

8.6 DDR2 SDRAM Mode Register Set [MRS]

The mode register stores the data for controlling the various operating modes of DDRS2 SDRAM. It controls /CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on /CS, /RAS, /CAS, WE, BA0, BA1 and BA2, while controlling the state of address pins A0 to A13.
The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register.
The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register.
The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 to A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, /CAS latency is defined by A4 to A6. The DDR2 doesn't support half clock latency mode. A8 is used for DLL reset. Write recovery time tWR is defined by A9 to A11. Refer to the table for specific codes.



BA2	BA1	BA0	MRS mode
0	0	0	MRS
0	0	1	EMRS(1)
0	1	0	EMRS(2)
0	1	1	EMRS(3): Reserved

A11	A10	A9	WR
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

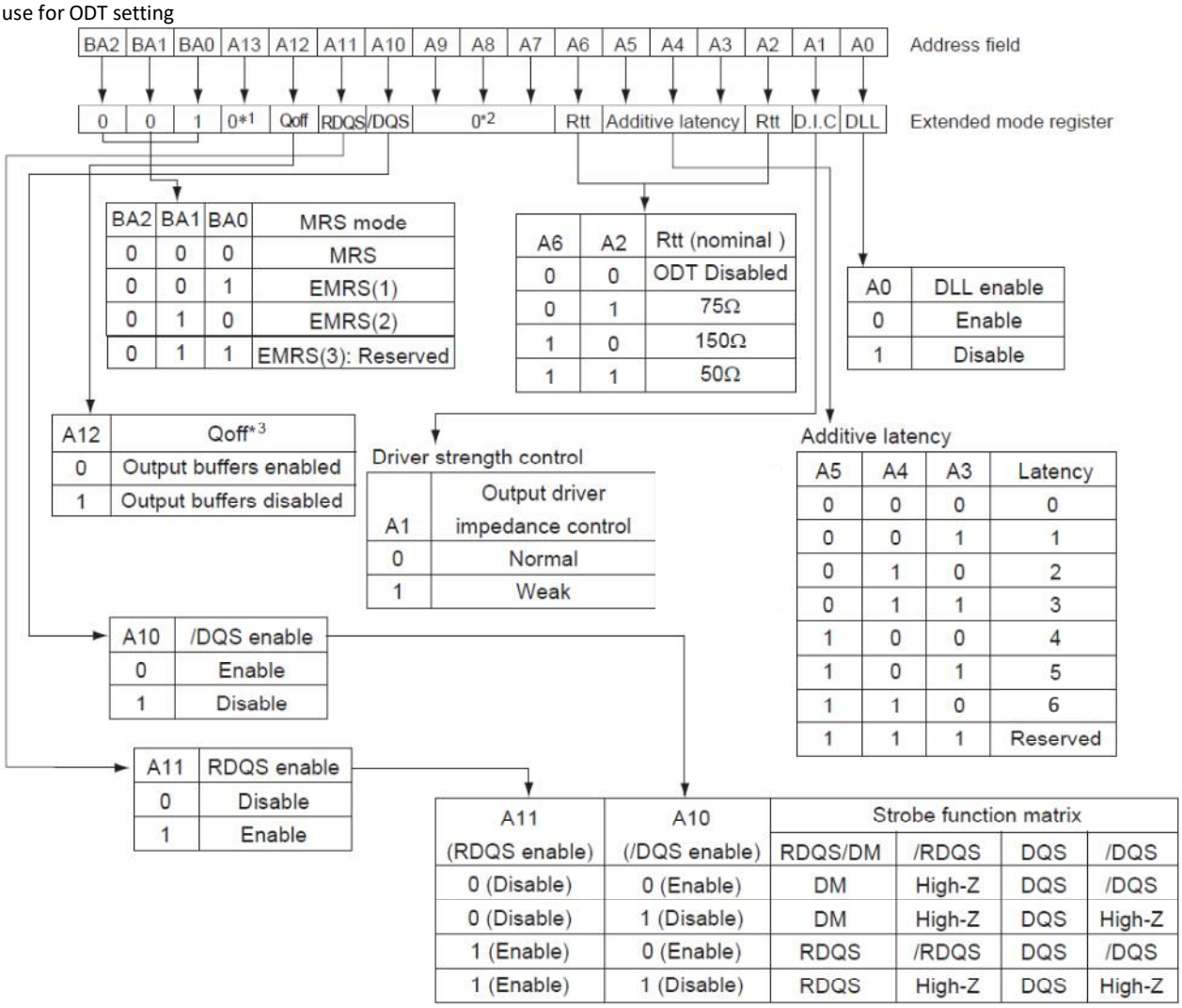
Notes:
1. A13 is reserved for future use and must be programmed to 0 when setting the mode register.
2. WR(min.)(Write Recovery for autoprecharge) is determined by tCK(max.) and WR(max.) is determined by tCK(min.) WR in clock cycles is calculated by dividing tWR(in ns) and rounding up to the next integer. (WR [cycles] = tWR (ns) / tCK (ns))
3. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

8.7 DDR2 SDRAM Extended Mode Register [EMRS]

EMRS (1) Programming

The extended mode register (1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, /DQS disable, RDQS enable. The default value of the extended mode register (1) is not defined, therefore the extended mode register (1) must be written after power-up for proper operation. The extended mode register (1) is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0 and low on BA1, BA2 while controlling the states of address pins A0 to A13. The DDR2 SDRAM should be in all bank percharge with CKE already high prior to writing into the extended mode register (1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for setting output driver strength. A3 to A5 determines the additive latency. A10 is used for /DQS enable or disable. A11 is used for RDQS enable. A2 and A6 are use for ODT setting



Notes:

1. A13 is reserved for future use and must be programmed to 0 when setting the mode register.
2. It must be set to 1 first, and then set to 0 in initialization. Refer to the Power-Up and Initialization Sequence for detailed information.
3. Output disabled – DQ, DQS, /DQS, RDQS, /RDQS. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.

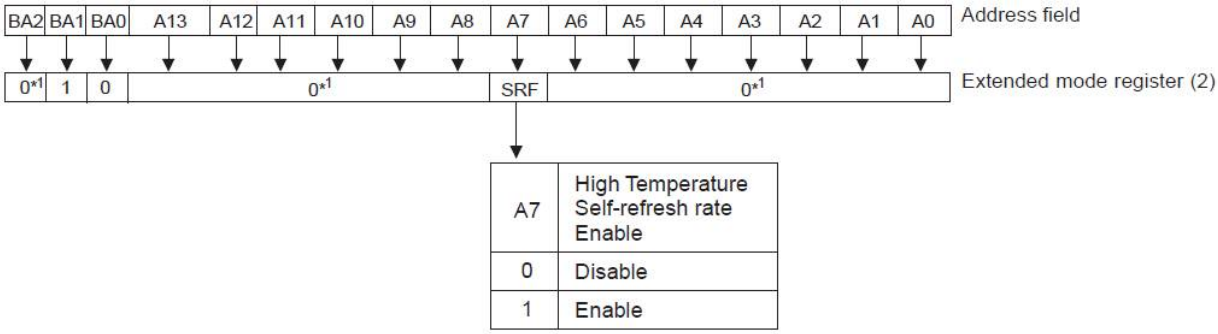
Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self-refresh operation Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

EMRS (2) Programming

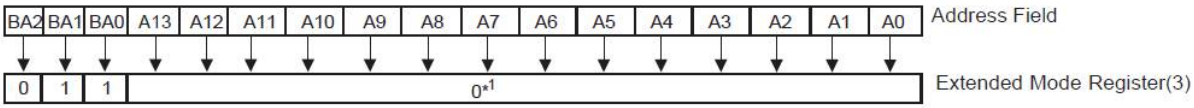
The extended mode register (2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register (2) must be written after power-up for proper operation. The extended mode register (2) is written by asserting low on CS, /RAS, /CAS, /WE, high on BA1 and low on BA0, BA2 while controlling the states of address pins A0 to A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.



Note: 1. The rest bits in EMRS (2) is reserved for future use and all bits in EMRS (2) except A7 must be programmed to 0 when setting the extended mode register (2) during initialization.

EMRS (2)

EMRS (3) Programming: Reserved*1



Note : 1. EMRS (3) is reserved for future use and all bits must be programmed to 0 when setting the extended mode register (3) during initialization.

EMRS (3)

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

8.8 ODT (On Die Termination)

8.9 Bank Activate Command

8.10 Read and write access modes

8.11 Write Data Mask

8.12 Precharge operation

8.13 Auto precharge operation

8.14 Refresh command

8.15 Self refresh operation

8.16 Power-down

8.17 Asynchronous CKE LOW event

8.18 SSC (Spread Spectrum Clocking)

8.19 Input clock frequency change during precharge power down

8.20 No operation command

8.21 Deselect command

[Refer to section 3 in JEDEC Standard No. JESD79-2F and section 2 in JESD208]

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.

Change History			
Document name: A3R1GE340JBF_v(Rev.#)			
Rev. #	**Who**	**When**	**What**
1.6	Jecy	2018-02-13	Changed datasheet template and set IDD6 6mA for -8EPH
1.7	Jerry	2019-04-16	Changed datasheet template
1.8	Porter	2019-10-25	Updated APM and Zentel logo
Document name updated to: DSA3R1GE340JBFF.(Rev.#)			
01	Porter	2020-03-19	Added document number; updated copyright format; removed differences from JEDEC
02	Porter	2020-04-01	Updated copyright format
03	Porter	2020-07-23	Updated PN decoder; updated header; removed note of Operating case temperature range from Specifications
04	Porter	2020-10-13	Updated company logo

Important Notice:

Zentel DRAM products are not intended for medical implementation, airplane and transportation instrument, safety equipment, or any other applications for life support or where Zentel products failure could result in life loss, personal injury, or environment damage. Zentel customers who purchase Zentel products for use in such applications do so in their own risk and fully agree Zentel accepts no liability for any damage from this improper use.

Zentel Japan Corporation reserves the right to change products and/or specifications without notice.
© 2020 Zentel Japan Corporation. All rights reserved.