

85V N-Channel Enhancement Mode MOSFET

Description

The AP140N08NF uses advanced **APM-SGT II** technology

to provide excellent $R_{DS(ON)}$, low gate charge and

operation with gate voltages as low as 10V.

This device is suitable for use as a Battery protection

or in other Switching application.

General Features

$V_{DS} = 85V$ $I_D = 140A$

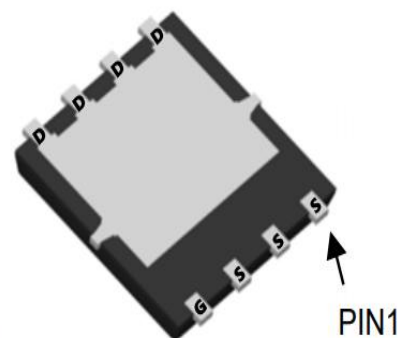
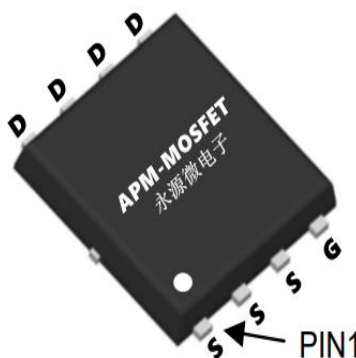
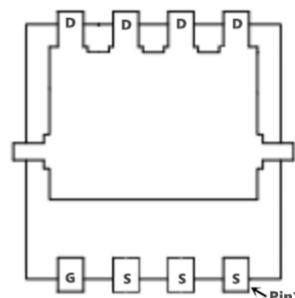
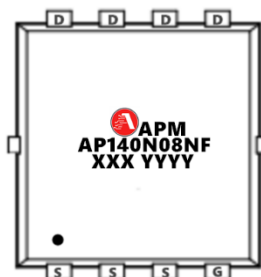
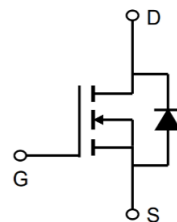
$R_{DS(ON)} < 3.2m\Omega$ $V_{GS}=10V$ (**Type: 2.5m Ω**)

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP140N08NF	PDFN5*6-8L	AP140N08NF XXX YYYY	5000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	85	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	140	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	115	A
I_{DM}	Pulsed Drain Current	700	A
E_{AS}	Single Pulse Avalanche Energy	900	mJ
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	179	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	25	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case	0.7	$^{\circ}C/W$

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Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	85	91		V
VGS(th)	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A, T_J=25^{\circ}\text{C}$	2.0	3.0	4.0	V
IDSS	Zero gate voltage drain current	$V_{DS}=80V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	-	-	1	μA
IDSS	Zero gate voltage drain current	$V_{DS}=80V, V_{GS}=0V, T_J=125^{\circ}\text{C}$	-	-	- 5	μA
IGSS	Gate-source leakage current	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
RDS(on)	Drain-source on-state resistance	$V_{GS}=10V, I_D=20A, T_J=25^{\circ}\text{C}$	-	2.5	3.2	m Ω
gfs	Transconductance	$V_{DS}=5V, I_D=40A$	-	128	-	S
Ciss	Input Capacitance	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$	-	6396	-	pF
Coss	Output Capacitance		-	1224	-	pF
Crss	Reverse Transfer Capacitance		-	23	-	pF
QG	Gate Total Charge	$V_{GS}=10V, V_{DS}=40V, I_D=20A$	-	91	-	nC
Qgs	Gate-Source charge		-	33	-	nC
Qgd	Gate-Drain charge		-	18	-	nC
td(on)	Turn-on delay time	$T_J=25^{\circ}\text{C}, V_{GS}=10V, V_{DS}=40V, R_L=3\Omega$	-	31	-	ns
tr	Rise time		-	35	-	ns
td(off)	Turn-off delay time		-	61	-	ns
tf	Fall time		-	31	-	ns
RG	Gate resistance	$V_{GS}=0V, V_{DS}=0V, f=1\text{MHz}$	-	0.8	-	Ω
VSD	Body Diode Forward Voltage	$V_{GS}=0V, I_{SD}=20A$	-	0.75	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=20A, dI/dt=100A/\mu s$	-	75	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	155	-	nC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、The test cond $\leq 300\mu s$ duty cycle $\leq 2\%$, duty cycle ition is $V_{DD}=64V, V_{GS}=10V, L=0.1mH, I_{AS}=60A$
- 4、The power dissipation is limited by 175°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

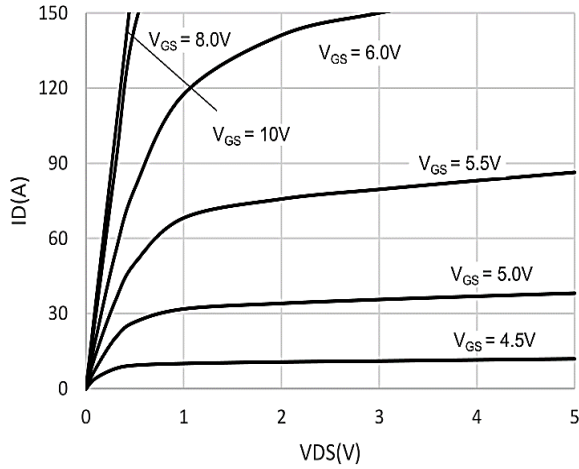


Figure1: Output Characteristics

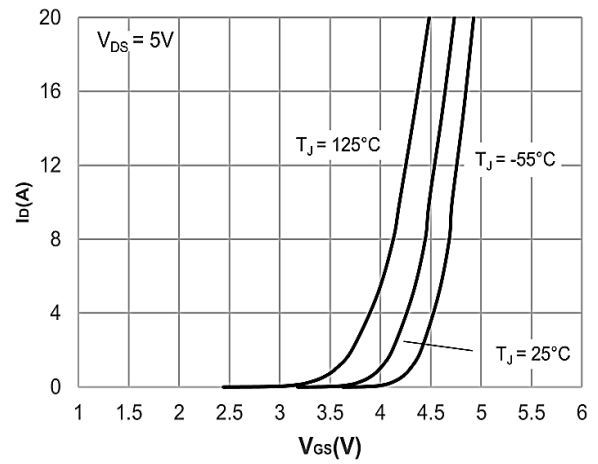


Figure 2: Typical Transfer Characteristics

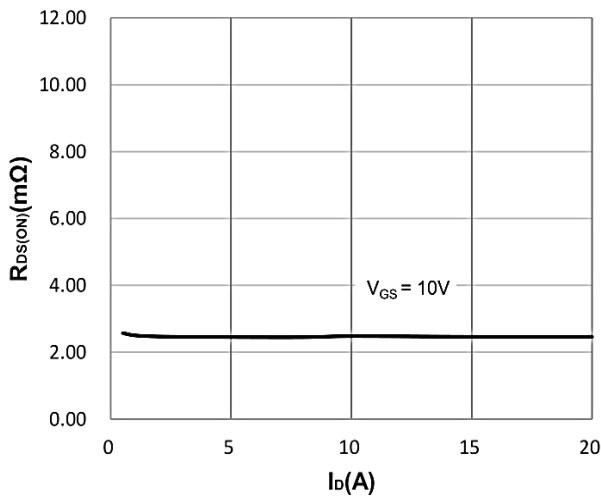


Figure 3: On-resistance vs. Drain Current

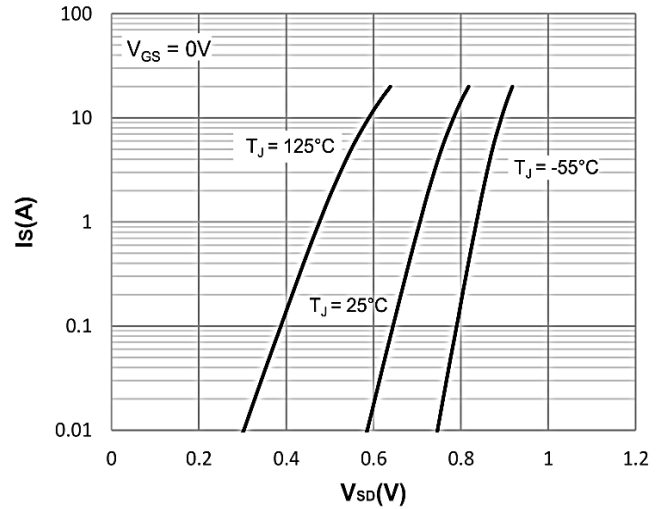


Figure 4: Body Diode Characteristics

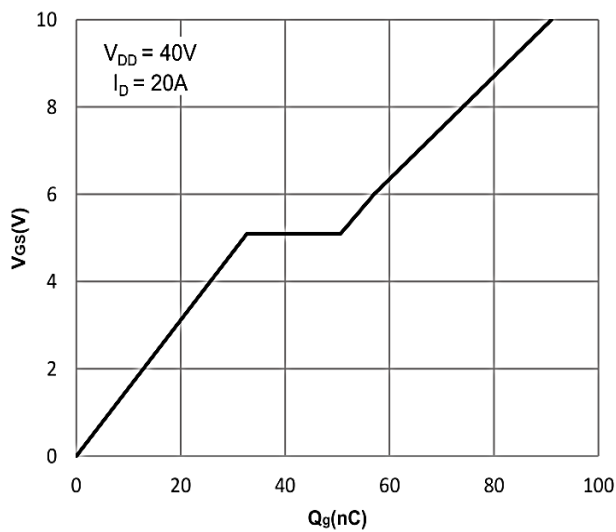


Figure 5: Gate Charge Characteristics

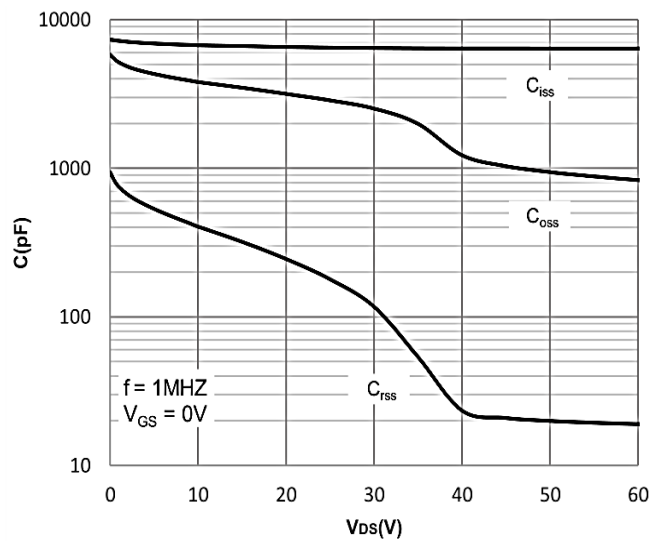


Figure 6: Capacitance Characteristics

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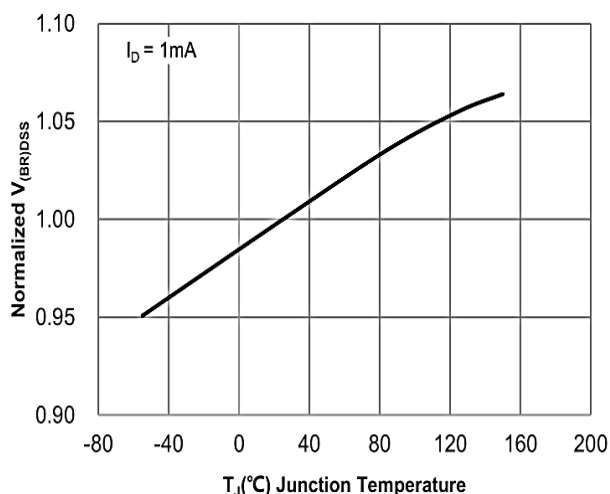


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

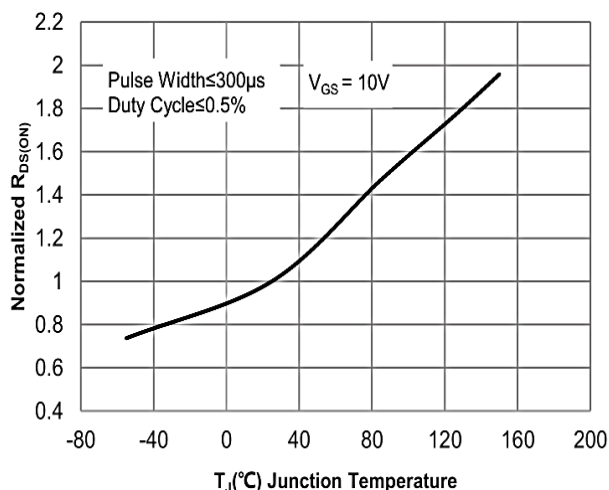


Figure 8: Normalized on Resistance vs. Junction Temperature

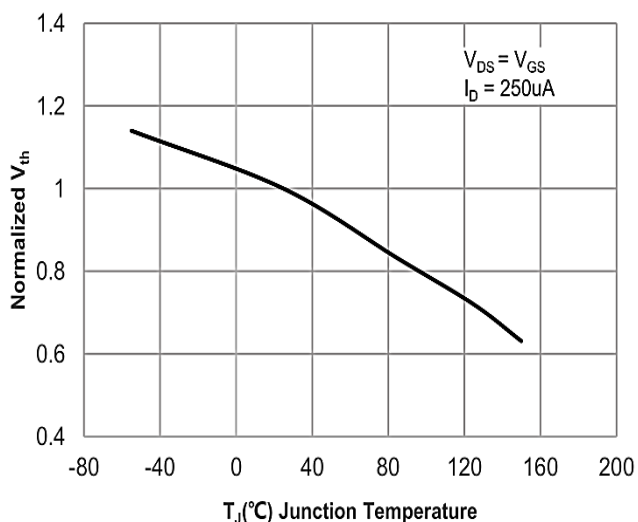


Figure 9: Maximum Safe Operating Area vs. Case Temperature

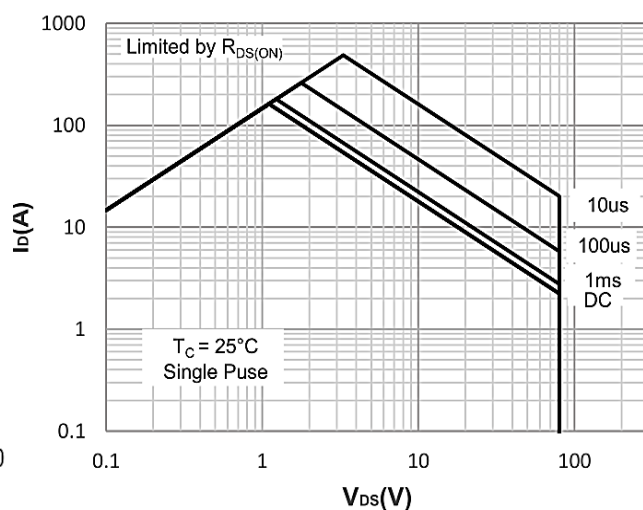


Figure 10: Maximum Safe Operating Area

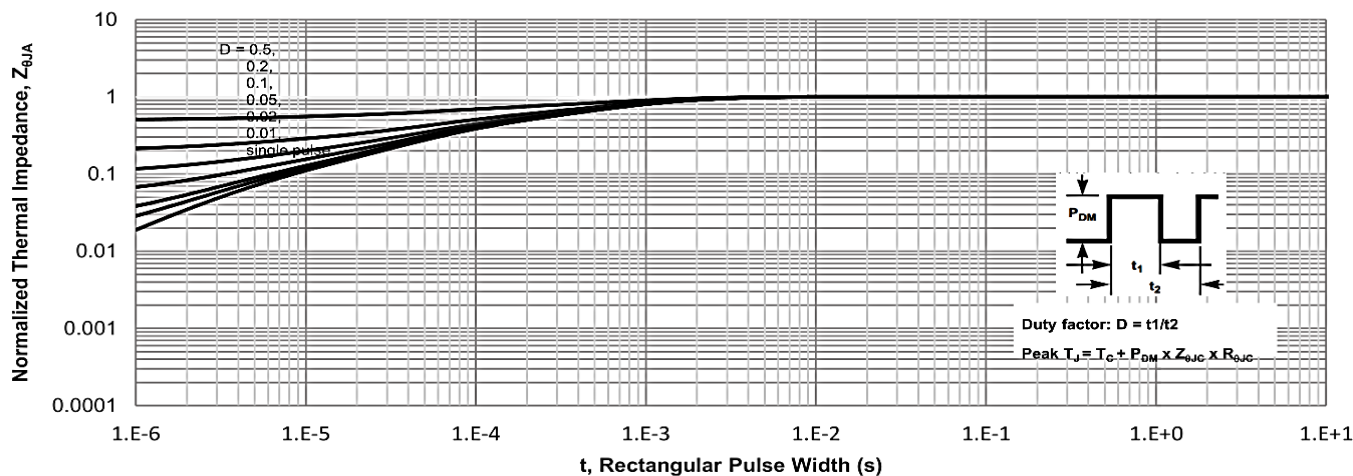
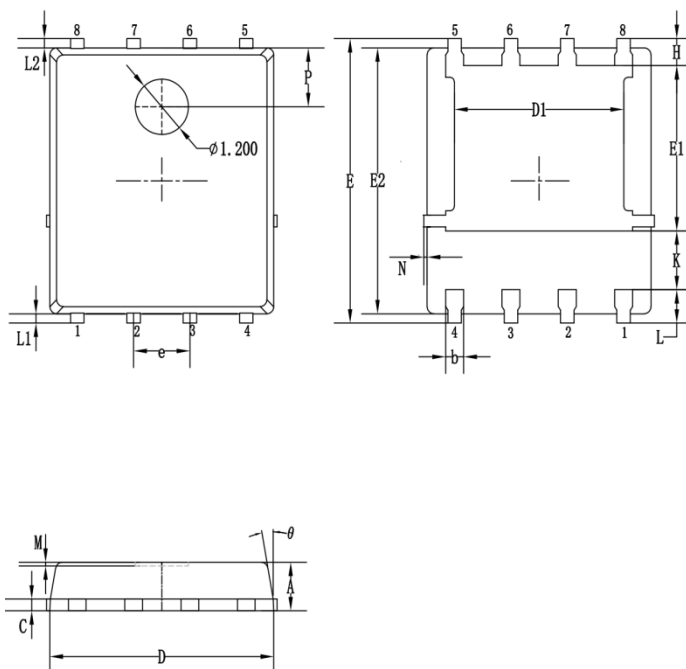


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ca

Package Mechanical Data-PDFN5*6-8L



Symbol	Dimensions In Millimeters		
	min.	typ.	max.
A	0.90	1.05	1.20
b	0.30	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.20
D1	3.72	3.82	4.12
E	5.90	6.10	6.30
E1	3.30	3.50	3.70
E2	5.60	5.75	5.90
e	1.27BSC		
H	0.48	0.58	0.70
K	1.14	1.27	1.40
L	0.54	0.74	0.84
L1/L2	0.10	0.20	0.30
θ	8°	10°	12°
M	0.08REF		
N	0.00		0.15
P	1.28REF		

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Edition	Date	Change
REV1.0	2023/12/31	Initial release

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