

1. DESCRIPTION

The XLISO7220 and XLISO7221 are dual-channel digital isolators. To facilitate PCB layout, the channels are oriented in the same direction in the XLISO7220 and in opposite directions in the XLISO7221. These devices have a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to 4000 V_{PK} per VDE. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received every 4 μs , the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

The small capacitance and resulting time constant provide fast operation with signaling rates available from 0 Mbps (dc) to 25 Mbps.⁽¹⁾ The A-, B- and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device. The M-option devices have CMOS $V_{CC}/2$ input thresholds and do not have the input noise-filter and the additional propagation delay.

These devices require two supply voltages of 2.8 V (C-Grade), 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 2.8-V or 3.3-V supply and all outputs are 4-mA CMOS.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

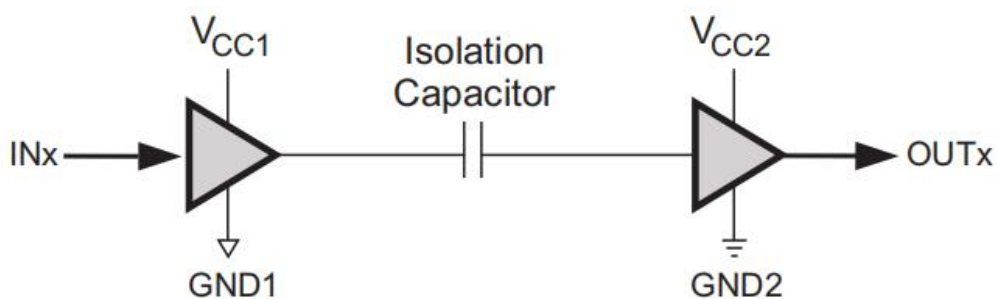
2. FEATURES

- 1, 5, 25Mbps Signaling Rate Options
 - Low Channel-to-Channel Output Skew; 1-ns max
 - Low Pulse-Width Distortion (PWD); 1-ns max
- 50 kV/ μs Typical Transient Immunity
- Operates with 2.8-V (C-Grade), 3.3-V or 5-V Supplies
- 4-kV ESD Protection
- High Electromagnetic Immunity
- Typical 28-Year Life at Rated Voltage

3. APPLICATIONS

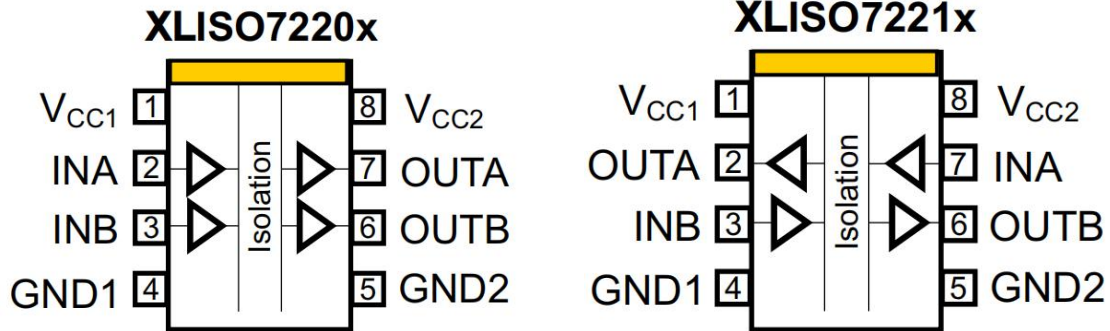
- Industrial Fieldbus
 - Modbus
 - Profibus™
 - DeviceNet™ Data Buses
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

4. SIMPLIFIED SCHEMATIC



5. PIN CONFIGURATION AND FUNCTIONS

SOP Package
8-Pin
Top View



Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	XLISO7220x	XLISO7221x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	8	8	—	Power supply, V_{CC2}

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾ , V_{CC1} , V_{CC2}	-0.5	3	V
V_I	Voltage at IN, OUT	-0.5	3	V
I_O	Output current	-15	15	mA
T_J	Maximum junction temperature		170	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to network ground pin and are peak voltage values.

6.2. Handling Ratings

		MIN	MAX	UNIT	
T _{stg}	Storage temperature range	-65	150	°C	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	-4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	-1	1	
		Machine Model, ANSI/ESDS5.2-1996	-200	200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3. Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage ⁽¹⁾ , V _{CC1} , V _{CC2}	XLISO722xA, XLISO722xB	3		5.5	V
		XLISO722xC	2.8		5.5	
I _{OH}	High-level output current		-4			mA
I _{OL}	Low-level output current				4	mA
t _{ui}	Input pulse width	XLISO722xA	1	0.67		μs
		XLISO722xB	200	100		ns
		XLISO722xC	40	33		
1/t _{ui}	Signaling rate ⁽²⁾	XLISO722xA	0	1500	1000	kbps
		XLISO722xB	0	10	5	Mbps
		XLISO722xC	0	30	25	
V _{IH}	High-level input voltage	XLISO722xA, XLISO722xB, XLISO722xC	2		55	V
V _{IL}	Low-level input voltage		0		0.8	V
T _J	Junction temperature		-40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 & IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

For the 2.8-V operation, V_{CC1} or V_{CC2} is specified at 2.8 V.

(2) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.

6.4. Thermal Information

THERMAL METRIC			XLIS07220x, XLIS07221x	UNIT
			8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Thermal Resistance	212	°C/W
		High-K Thermal Resistance	122	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		69.1	
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	
ψ_{JT}	Junction-to-top characterization parameter		15.2	
ψ_{JB}	Junction-to-board characterization parameter		47.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	

6.5. Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V⁽¹⁾ Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		1	2	mA
	XLISO7221				8.5	17	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		2	3	
	XLISO7221A, XLISO7221B				10	18	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		4	9	
	XLISO7221C				12	22	
I _{CC2}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		16	31	
	XLISO7221x				8.5	17	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		17	32	
	XLISO7221A, XLISO7221B				10	18	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		20	34	
	XLISO7221C				12	22	
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 13	V _{CC} −0.8	4.6		V
			I _{OH} = −20 μA, See Figure 13	V _{CC} −0.1	5		
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 13		0.2	0.4	V
			I _{OL} = 20 μA, See Figure 13		0	0.1	
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current		IN from 0 V to V _{CC}			10	μA
I _{IL}	Low-level input current			-10			
C _i	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πtt)		1		pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 15	25	50		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

6.6. Electrical Characteristics: V_{CC1} at 5 V, V_{CC2} at 3.3 V⁽¹⁾ Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		1	2	mA
	XLISO7221				8.5	17	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		2	3	
	XLISO7221A, XLISO7221B				10	18	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		4	9	
	XLISO7221C				12	22	
I _{CC2}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		8	18	mA
	XLISO7221x				4.3	9.5	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		9	19	
	XLISO7221A, XLISO7221B				5	11	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		10	20	
	XLISO7221C				6	12	
V _{OH}	High-level output voltage	XLISO7220x	I _{OH} = −4 mA, See Figure 13	V _{CC} −0.4			V
		XLISO7221x (5-V side)		V _{CC} −0.8			
			I _{OH} = −20 μA, See Figure 13	V _{CC} −0.1			
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 13			0.4	V
			I _{OL} = 20 μA, See Figure 13			0.1	
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current	IN from 0 V to V _{CC}				10	μA
I _{IL}	Low-level input current			−10			
C _i	Input capacitance to ground	IN at V _{CC} , V _I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V _I = V _{CC} or 0 V, See Figure 15		15	40		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

6.7. Electrical Characteristics: V_{CC1} at 3.3 V, V_{CC2} at 5 V⁽¹⁾ Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		0.6	1	mA
	XLISO7221				4.3	9.5	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		1	2	
	XLISO7221A, XLISO7221B				5	11	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		2	4	
	XLISO7221C				6	12	
I _{CC2}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		16	31	
	XLISO7221x				8.5	17	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		18	32	
	XLISO7221A, XLISO7221B				10	18	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		20	34	
	XLISO7221C				12	22	
V _{OH}	High-level output voltage		XLISO7220x	I _{OH} = −4 mA, See Figure 13	V _{CC} −0.4		V
			XLISO7221x (3.3-V side)		V _{CC} −0.8		
				I _{OH} = −20 μA, See Figure 13	V _{CC} −0.1		
V _{OL}	Low-level output voltage			I _{OL} = 4 mA, See Figure 13		0.4	
				I _{OL} = 20 μA, See Figure 13	0	0.1	
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current		IN from 0 V to V _{CC}			10	μA
I _{IL}	Low-level input current			−10			
C _i	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πrt)		1		pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 15	15	40		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

6.8. Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V⁽¹⁾ Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		0.6	1	mA
	XLISO7221				4.3	9.5	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		1	2	
	XLISO7221A, XLISO7221B				5	11	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		2	4	
	XLISO7221C				6	12	
I _{CC2}	XLISO7220x	Quiescent	V _I = V _{CC} or 0 V, no load		8	18	mA
	XLISO7221x				4.3	9.5	
	XLISO7220A, XLISO7220B	1 Mbps	0.5 MHz Input Clock Signal, no load		9	19	
	XLISO7221A, XLISO7221B				5	11	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		10	20	
	XLISO7221C				6	12	
V _{OH}	High-level output voltage	I _{OH} = −4 mA, See Figure 13		V _{CC} -0.4	3		V
		I _{OH} = −20 μA, See Figure 13		V _{CC} -0.1	3.3		
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, See Figure 13			0.2	0.4	
		I _{OL} = 20 μA, See Figure 13			0	0.1	
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current	IN from 0 V to V _{CC}				10	μA
I _{IL}	Low-level input current			-10			
C _i	Input capacitance to ground	IN at V _{CC} , V _I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V _I = V _{CC} or 0 V, See Figure 15		15	40		kV/μs

(1) For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V

6.9. Electrical Characteristics: V_{CC1} and V_{CC2} at 2.8 V (XLIS0722xC-Only) Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{CC1}	XLISO7220C	Quiescent	V _I = V _{CC} or 0 V, no load		0.4	0.9	mA
	XLISO7221C				3.7	7.5	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		1.5	3.5	
	XLISO7221C				4.5	10	
I _{CC2}	XLISO7220C	Quiescent	V _I = V _{CC} or 0 V, no load		6.8	15	
	XLISO7221C				3.7	7.5	
	XLISO7220C	25 Mbps	12.5 MHz Input Clock Signal, no load		9	17	
	XLISO7221C				4.5	10	
V _{OH}	High-level output voltage		I _{OH} = −4 mA, See Figure 13	V _{CC} -0.6	2.55		V
			I _{OH} = −20 μA, See Figure 13	V _{CC} -0.1	2.8		
V _{OL}	Low-level output voltage		I _{OL} = 4 mA, See Figure 13		0.25	0.6	
			I _{OL} = 20 μA, See Figure 13		0	0.1	
V _{I(HYS)}	Input voltage hysteresis				150		mV
I _{IH}	High-level input current		IN from 0 V to V _{CC}			10	μA
I _{IL}	Low-level input current			-10			
C _i	Input capacitance to ground		IN at V _{CC} , V _I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V _I = V _{CC} or 0 V, See Figure 15	10	30		kV/μs

6.10. Switching Characteristics: V_{CC1} and V_{CC2} at 5 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xA	See Figure 13	280	405	475	ns
PWD	Pulse-width distortion t _{PHL} – t _{PLH} (1)				1	14	
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xB		42	55	70	
PWD	Pulse-width distortion t _{PHL} – t _{PLH} (1)				1	3	
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xC		22	32	42	
PWD	Pulse-width distortion t _{PHL} – t _{PLH} (1)				1	2	
t _{sk(pp)}	Part-to-part skew(2)	XLISO722xA			180	ns	
		XLISO722xB			17		
		XLISO722xC			10		
t _{sk(o)}	Channel-to-channel output skew(3)	XLISO722xA		3	15	ns	
		XLISO722xB		0.6	3		
		XLISO722xC		0.2	1		
tr	Output signal rise time	See Figure 13		1		ns	
tf	Output signal fall time			1			
tfs	Failsafe output delay time from input power loss	See Figure 14		3		μs	

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads

6.11. Switching Characteristics: V_{CC1} at 5 V, V_{CC2} at 3.3 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xA	See Figure 13	285	410	480	ns
PWD	Pulse-width distortion t _{PHL} – t _{PLH} ⁽¹⁾				1	14	
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xB		45	58	75	
PWD	Pulse-width distortion t _{PHL} – t _{PLH} ⁽¹⁾				1	3	
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xC		25	36	48	
PWD	Pulse-width distortion t _{PHL} – t _{PLH} ⁽¹⁾				1	2	
t _{sk(pp)}	Part-to-part skew ⁽²⁾	XLISO722xA			180	ns	
		XLISO722xB			17		
		XLISO722xC			10		
t _{sk(o)}	Channel-to-channel output skew ⁽³⁾	XLISO722xA		3	15		
		XLISO722xB		0.6	3		
		XLISO722xC		0.2	1		
t _r	Output signal rise time	See Figure 13		2		ns	
t _f	Output signal fall time			2			
t _{fs}	Failsafe output delay time from input power loss	See Figure 14		3		μs	

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads

6.12. Switching Characteristics: V_{CC1} at 3.3 V, V_{CC2} at 5 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xA	See Figure 13	285	395	480	ns	
PWD	Pulse-width distortion t _{PHL} – t _{PLH} ⁽¹⁾				1	18		
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xB		45	58	75		
PWD	Pulse-width distortion t _{PHL} – t _{PLH} ⁽¹⁾				1	4		
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xC		25	36	48		
PWD	Pulse-width distortion t _{PHL} – t _{PLH} ⁽¹⁾				1	3		
t _{sk(pp)}	Part-to-part skew ⁽²⁾	XLISO722xA				190		
		XLISO722xB				17		
		XLISO722xC				10		
t _{sk(o)}	Channel-to-channel output skew ⁽³⁾	XLISO722xA			3	15		
		XLISO722xB			0.6	3		
		XLISO722xC			0.2	1		
t _r	Output signal rise time		See Figure 13		1			μs
t _f	Output signal fall time				1			
t _{fs}	Failsafe output delay time from input power loss		See Figure 14		3			

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads

6.13. Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xA	See Figure 13	290	400	485	ns
PWD	Pulse-width distortion t _{PHL} – t _{PLH} (1)				1	18	
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xB		46	62	78	
PWD	Pulse-width distortion t _{PHL} – t _{PLH} (1)				1	4	
t _{PLH} , t _{PHL}	Propagation delay	XLISO722xC		26	40	52	
PWD	Pulse-width distortion t _{PHL} – t _{PLH} (1)				1	3	
t _{sk(pp)}	Part-to-part skew(2)	XLISO722xA				190	
		XLISO722xB				17	
		XLISO722xC				10	
t _{sk(o)}	Channel-to-channel output skew(3)	XLISO722xA			3	15	
		XLISO722xB			0.6	3	
		XLISO722xC			0.2	1	
tr	Output signal rise time		See Figure 13		2		
tf	Output signal fall time				2		
tfs	Failsafe output delay time from input power loss		See Figure 14		3		μs

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads

6.14. Switching Characteristics: V_{CC1} and V_{CC2} at 2.8 V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	XLIS0722xC	See Figure 13	26	45	65	ns
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} ^{(1)}$				1.5	5	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	XLIS0722xC				12	
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	XLIS0722xC			0.2	5	
t_r	Output signal rise time		See Figure 13		2		
t_f	Output signal fall time				2		
t_{fs}	Failsafe output delay time from input power loss		See Figure 14		4.6		μs

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads

6.15. Typical Characteristics

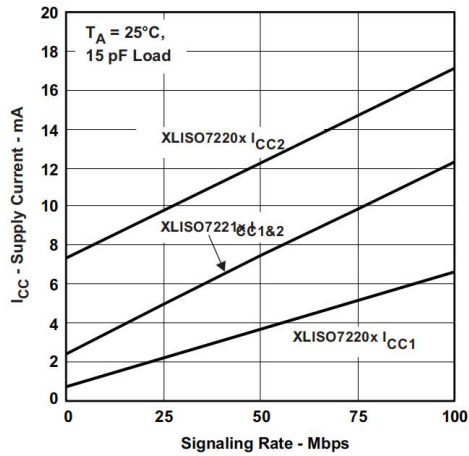


Figure 1. 3.3-V RMS Supply Current vs Signaling Rate (Mbps) (Mbps)

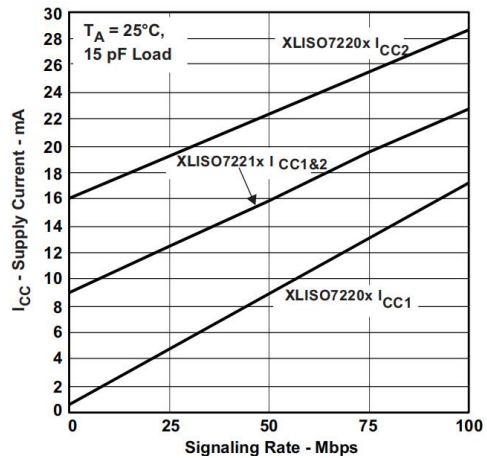


Figure 2. 5-V RMS Supply Current vs Signaling Rate (Mbps)

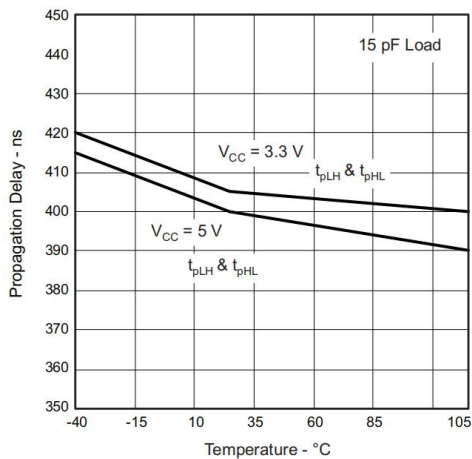


Figure 3. Propagation Delay vs Free-Air Temperature, XLIS0722xA

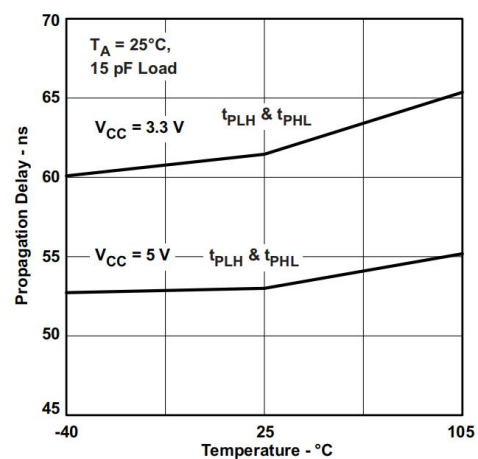


Figure 4. Propagation Delay vs Free-Air Temperature, XLIS0722xB

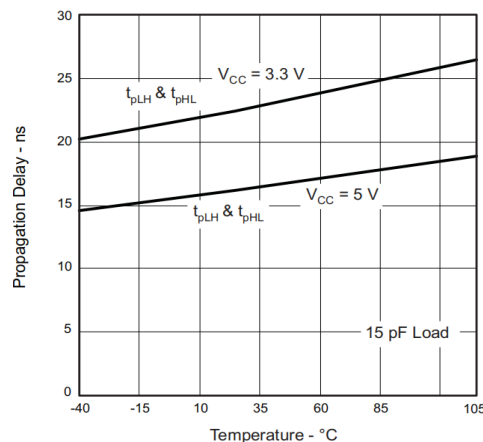


Figure 5. Propagation Delay vs Free-Air Temperature, XLIS0722xC

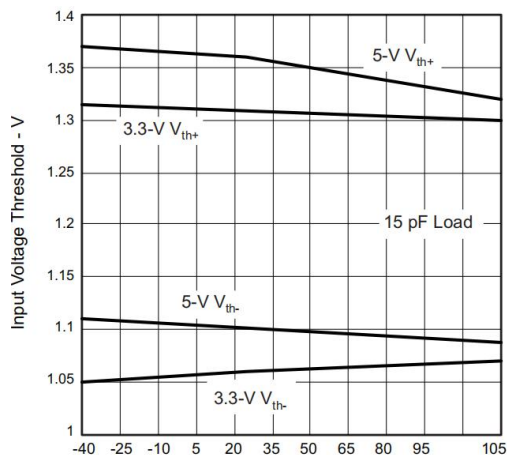


Figure 6. XLIS0722xA, XLIS0722xB and XLIS0722xC Input Voltages vs Free-Air Temperature Low-to-High Switching Threshold vs Free-Air Temperature

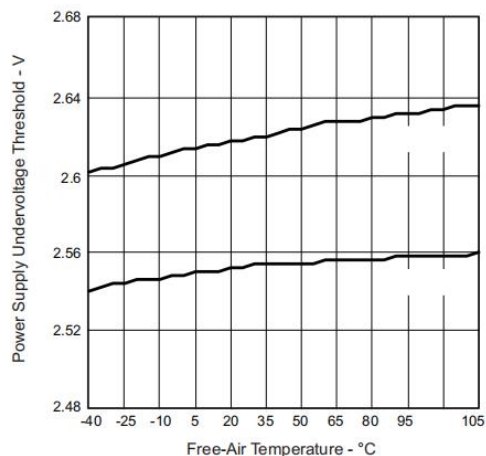


Figure 7. VCC Undervoltage Threshold vs Free-Air Temperature

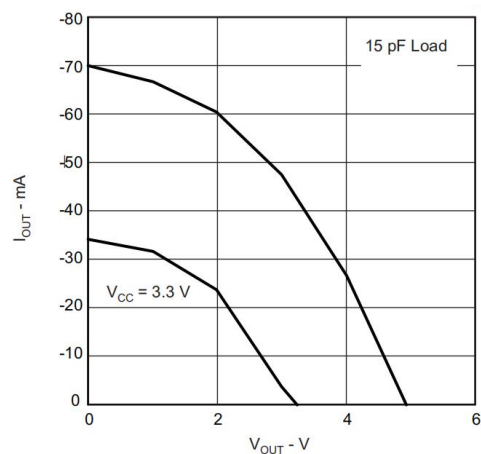


Figure 8. High-Level Output Current vs High-Level Output Voltage

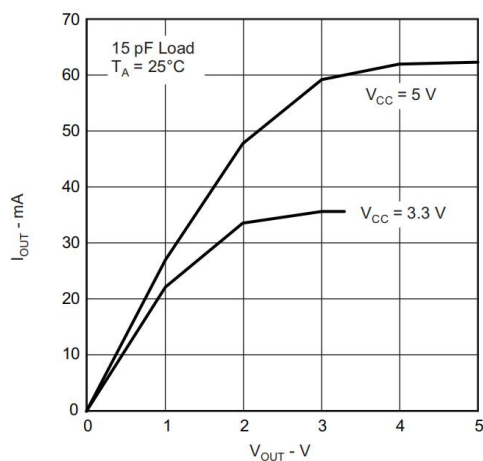


Figure 9. Low-Level Output Current vs Low-Level Output Voltage

8. DETAILED DESCRIPTION

8.1. Overview

The isolator in Figure 17 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2. Functional Block Diagram

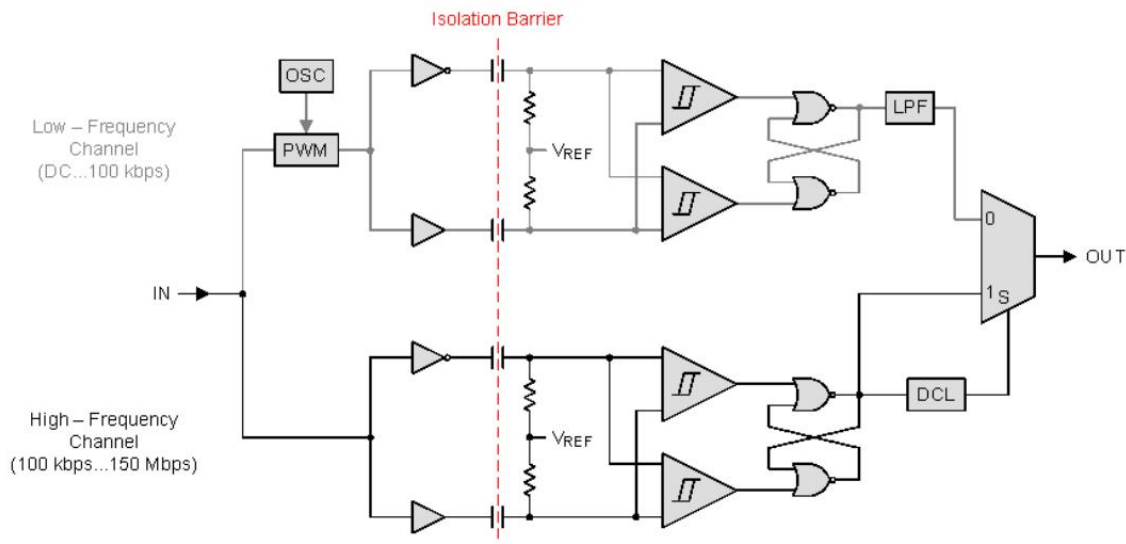


Figure 17. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3. Feature Description

PRODUCT	MAX SIGNALING RATE	INPUT THRESHOLD	CHANNEL DIRECTION
XLISO7220A	1 Mbps	~ 1.5 V (TTL) (CMOS compatible)	Same direction
XLISO7220B	5 Mbps	~ 1.5 V (TTL) (CMOS compatible)	
XLISO7220C	25 Mbps	~ 1.5 V (TTL) (CMOS compatible)	
XLISO7221A	1 Mbps	~ 1.5 V (TTL) (CMOS compatible)	Opposite directions
XLISO7221B	5 Mbps	~ 1.5 V (TTL) (CMOS compatible)	
XLISO7221C	25 Mbps	~ 1.5 V (TTL) (CMOS compatible)	

8.3.1. IEC 60747-5-5 Insulation Characteristics

PARAMETER	TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM} Maximum working insulation voltage		560	VPK
V_{PR} Input to output test voltage	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, $t = 10$ s, Partial discharge < 5 pC	672	
	Method a, After environment tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, $t = 10$ s, Partial discharge < 5 pC	896	
	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with $t = 1$ s, Partial discharge < 5 pC	1050	
V_{IOTM} Transient overvoltage	$V_{TEST} = V_{IOTM}$ $t = 60$ s (qualification) $t = 1$ s (100% production)	4000	
R_S Insulation resistance	$V_{IO} = 500$ V at T_S	>109	Ω
Pollution degree		2	

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage $\leq 150 V_{RMS}$	I-IV
	Rated mains voltage $\leq 300 V_{RMS}$	I-III
	Rated mains voltage $\leq 400 V_{RMS}$	I-II

8.3.2. IEC Package Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01) Minimum air gap (Clearance)	Shortest pin-to-pin distance through air	4.8			mm
L(I02) Minimum external tracking (Creepage)	Shortest pin-to-pin distance across the package surface	4.3			mm
CTI Tracking resistance (Comparative Tracking Index)	IEC 60112	400			V
Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R _{IO} Isolation resistance	Input to output, $V_{IO} = 500 V$, all pins on each side of the barrier tied together creating a two-pin device, $T_A = 25^\circ C$	10^{12}			Ω
	Input to output, $V_{IO} = 500 V$, $100^\circ C \leq T_A \leq \max$	10^{11}			Ω
C _{IO} Barrier capacitance Input to output	$V_I = 0.4 \sin(4E6\pi t)$		1		pF
CI Input capacitance to ground	$V_I = 0.4 \sin(4E6\pi t)$		1		pF

8.3.3. IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipates sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IS Safety input, output, or supply current	$\theta_{JA} = 212^\circ C/W$, $V_I = 5.5 V$, $T_J = 170^\circ C$, $T_A = 25^\circ C$			124	mA
	$\theta_{JA} = 212^\circ C/W$, $V_I = 3.6 V$, $T_J = 170^\circ C$, $T_A = 25^\circ C$			190	
TS Maximum case temperature				150	$^\circ C$

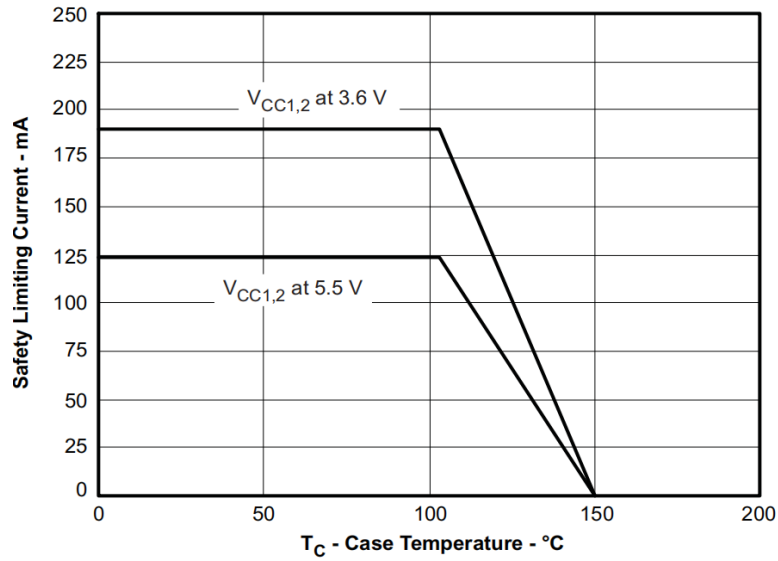


Figure 18. θ_{JC} Thermal Derating Curve per IEC 60747-5-5

8.4. Device Functional Modes

Table 2. XLIS07220x or XLIS07221x⁽¹⁾

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up ($V_{CC} \geq 3.0$ V), PD = Powered Down ($V_{CC} \leq 2.5$ V), X = Irrelevant, H = High Level, L = Low Level

8.4.1. Device I/O Schematics

Internal schematics of input and output pins are shown in Figure 19.

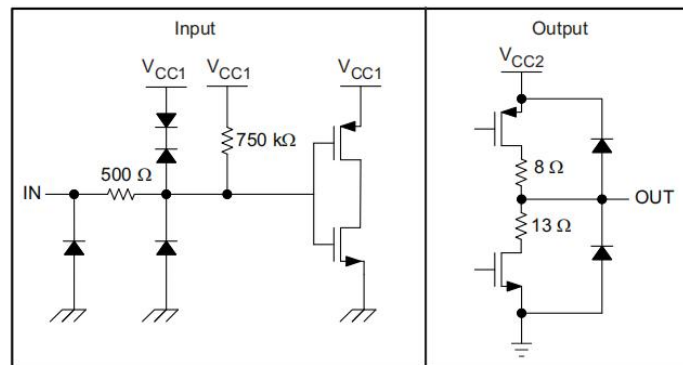


Figure 19. Device I/O Schematics

9. APPLICATION AND IMPLEMENTATION

NOTE

Information in the following applications sections is not part of the XLD component specification, and XLD does not warrant its accuracy or completeness. XLD's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1. Application Information

XLIS0722x use single-ended TTL or CMOS-logic switching technology. Its supply voltage range is from 3 V (2.8 V for C-grade) to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2. Design Requirements

Unlike optocouplers, which need external components to improve performance, provide bias (or limit current), the XLIS0722x devices need only two external bypass capacitors to operate.

9.3. Detailed Design Procedure

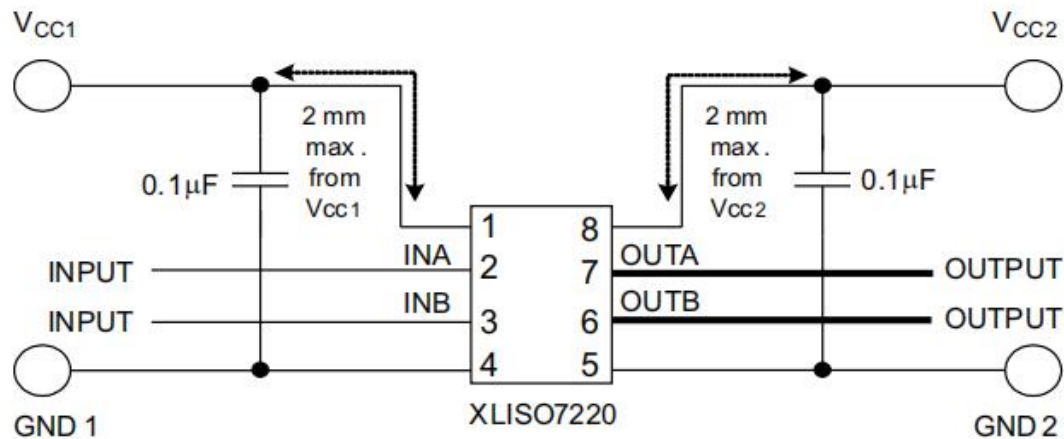


Figure 21. Typical XLIS07220 Circuit Hook-Up

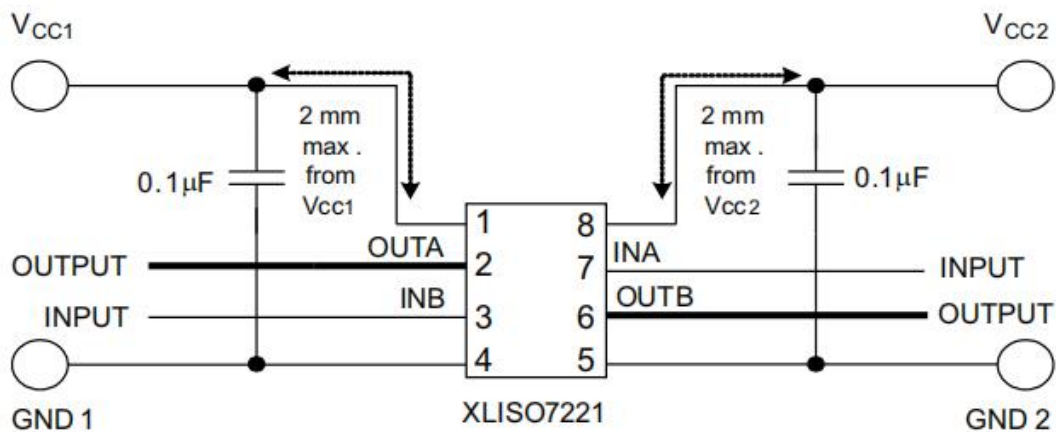


Figure 22. Typical XLIS07221 Circuit Hook-Up

9.4. Application Curve

At maximum working voltage, XLIS0722x isolation barrier has more than 28 years of life.

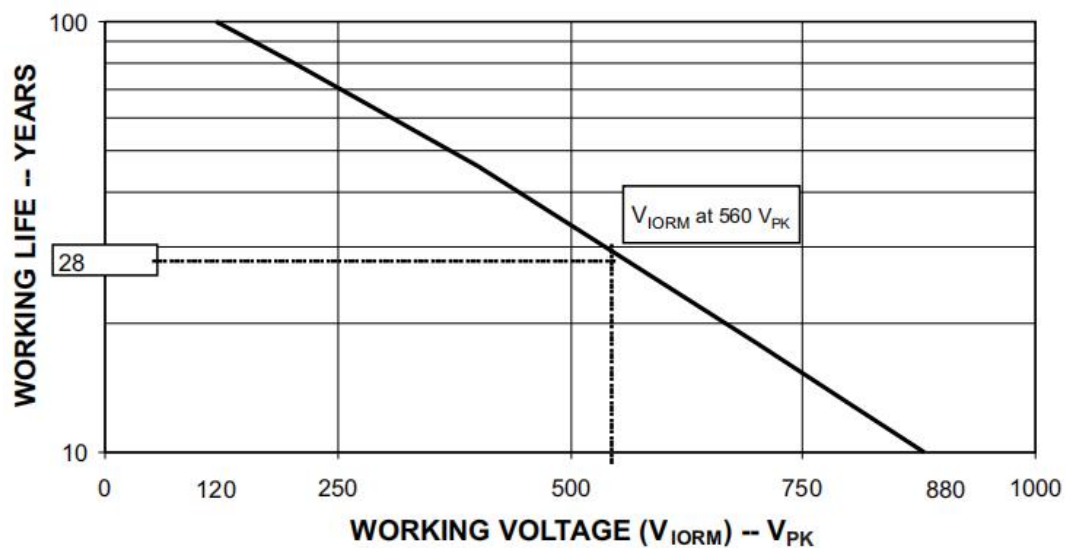


Figure 23. Time Dependent Dielectric Breakdown Test Results

10. Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 μF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible.

11. Layout

11.1. Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 24). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².

Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

12. Layout Example

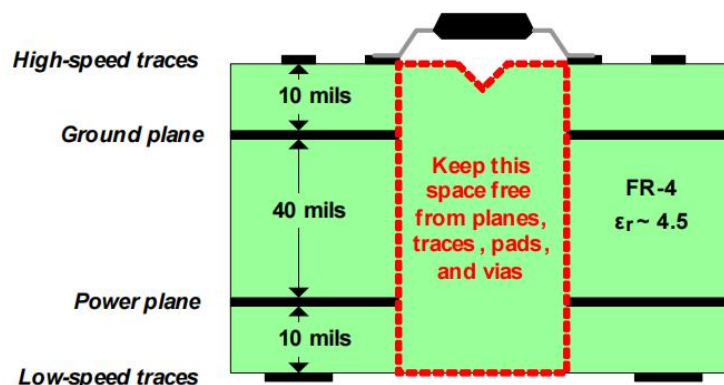


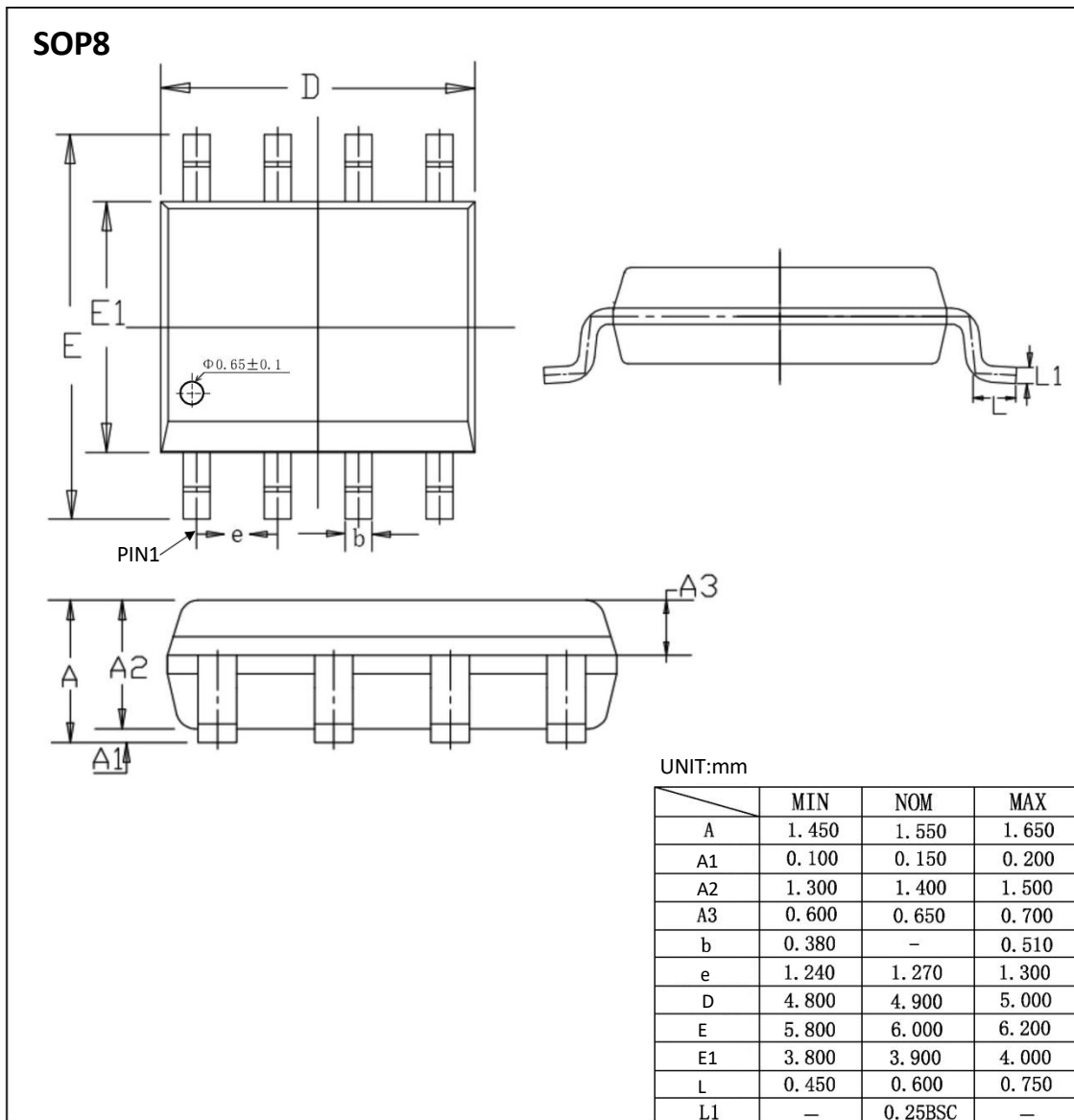
Figure 24. Recommended Layer Stack

13. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLIS07220ADR	XL7220A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLIS07220BDR	XL7220B	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLIS07220CDR	XL7220C	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLIS07221ADR	XL7221A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLIS07221BDR	XL7221B	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLIS07221CDR	XL7221C	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500

14. DIMENSIONAL DRAWINGS



[if you need help contact us. Xinluda reserves the right to change the above information without prior notice]