

650V N-Channel Enhancement Mode MOSFET

Description

The AP7N65F-C is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

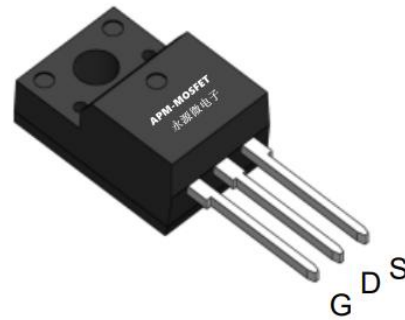
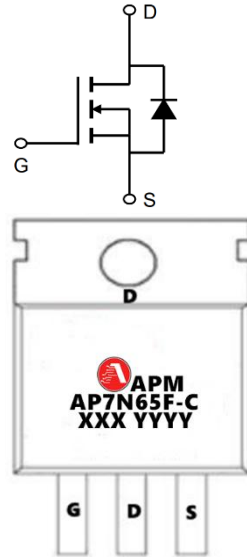
$V_{DS} = 650V$ $I_D = 7A$

$R_{DS(ON)} < 1.4\Omega$ @ $V_{GS}=10V$ (Type: 1.25 Ω)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP7N65F-C	TO220-3L	AP7N65F-C XXX YYYY	2500

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0V$)	650	V
$I_D@T_c=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	7.0	A
$I_D@T_c=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	5.0	A
I_{DM}	Pulsed Drain Current (note1)	26	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy	700	mJ
I_{AS}	Avalanche Current	20	A
P_D	Power Dissipation ($T_c = 25^\circ\text{C}$)	32.9	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^\circ\text{C}$
R_{thJC}	Thermal Resistance, Junction-to-Case	2.05	$^\circ\text{C/W}$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C/W}$



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Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V(\text{BR})_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = 250\mu\text{A}$	650	700	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 650\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 25^{\circ}\text{C}$	--	--	1	μA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}} = \pm 30\text{V}$	--	--	± 100	nA
$V_{\text{GS}}(\text{th})$	Gate-Source Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 250\mu\text{A}$	2.0	3.0	4.0	V
$R_{\text{DS}}(\text{on})$	Drain-Source On-Resistance (Note3)	$V_{\text{GS}} = 10\text{V}, I_{\text{D}} = 3.5\text{A}$	--	1.25	1.40	Ω
C_{iss}	Input Capacitance	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 25\text{V}, f = 1.0\text{MHz}$	--	908	--	pF
C_{oss}	Output Capacitance		--	86	--	
C_{rss}	Reverse Transfer Capacitance		--	5	--	
Q_{g}	Total Gate Charge	$V_{\text{DD}} = 420\text{V}, I_{\text{D}} = 7\text{A}, V_{\text{GS}} = 10\text{V}$	--	20	--	nC
Q_{gs}	Gate-Source Charge		--	17	--	
Q_{gd}	Gate-Drain Charge		--	60	--	
$t_{\text{d}}(\text{on})$	Turn-on Delay Time	$V_{\text{DD}} = 325\text{V}, I_{\text{D}} = 7\text{A}, R_{\text{G}} = 25\Omega$	--	19	--	ns
t_{r}	Turn-on Rise Time		--	17	--	
$t_{\text{d}}(\text{off})$	Turn-off Delay Time		--	59	--	
t_{f}	Turn-off Fall Time		--	22	--	
I_{S}	Continuous Body Diode Current	$T_{\text{C}} = 25^{\circ}\text{C}$	--	--	7.0	A
I_{SM}	Pulsed Diode Forward Current		--	--	28	A
V_{SD}	Body Diode Voltage	$T_J = 25^{\circ}\text{C}, I_{\text{SD}} = 7\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{\text{GS}} = 0\text{V}, I_{\text{S}} = 7\text{A}, di_{\text{F}}/dt = 100\text{A}/\mu\text{s}, V_{\text{DS}} = 320\text{V}$	--	400	--	ns
Q_{rr}	Reverse Recovery Charge		--	3	--	μC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The EAS data shows Max. rating . $I_{\text{AS}} = 4.5\text{A}$, $V_{\text{DD}} = 50\text{V}$, $R_{\text{G}} = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$
- 3、The test condition is Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_{D} and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

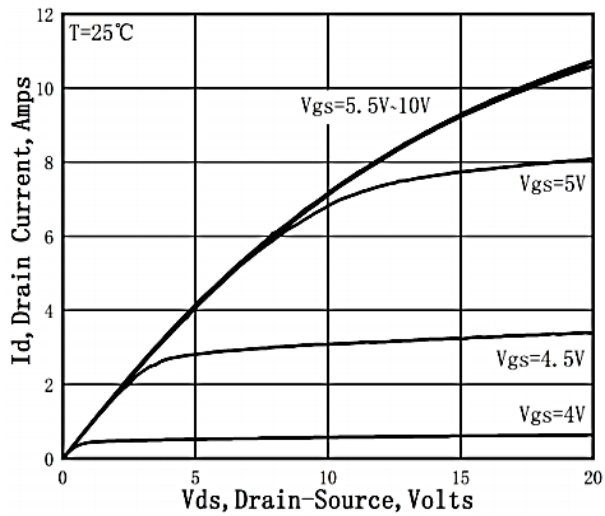


Figure 1. On-Region Characteristics

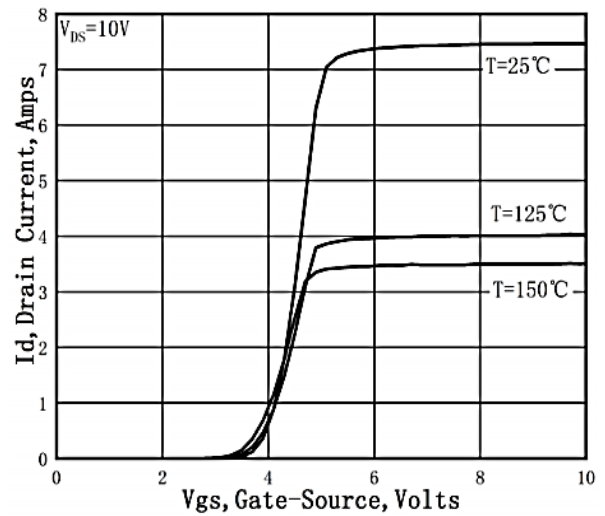


Figure 2. Transfer Characteristics

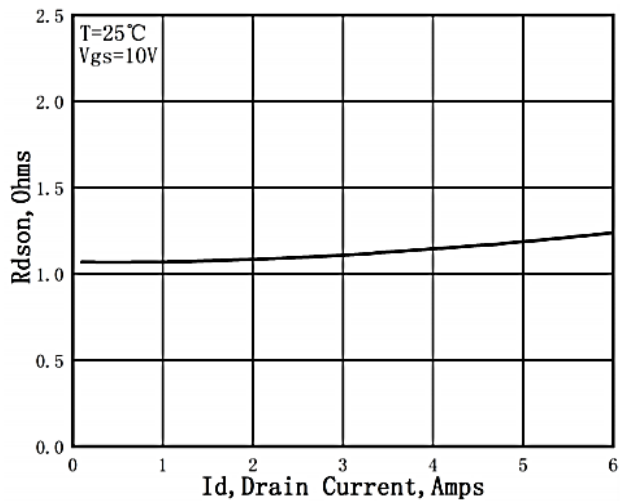


Figure 3. Static Drain-Source On Resistance

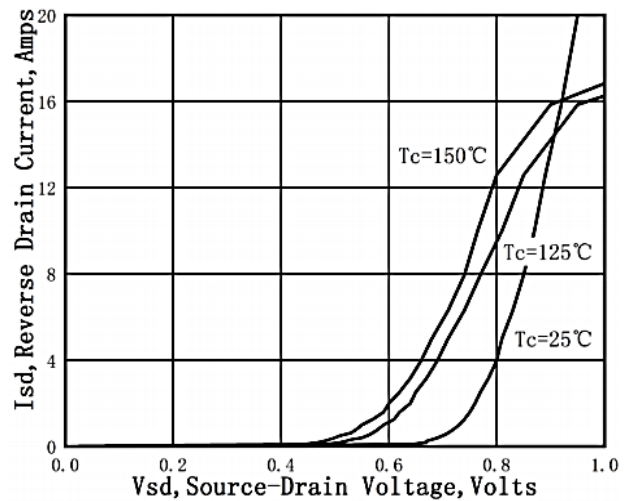


Figure 4. Typical Body Diode Transfer Characteristics

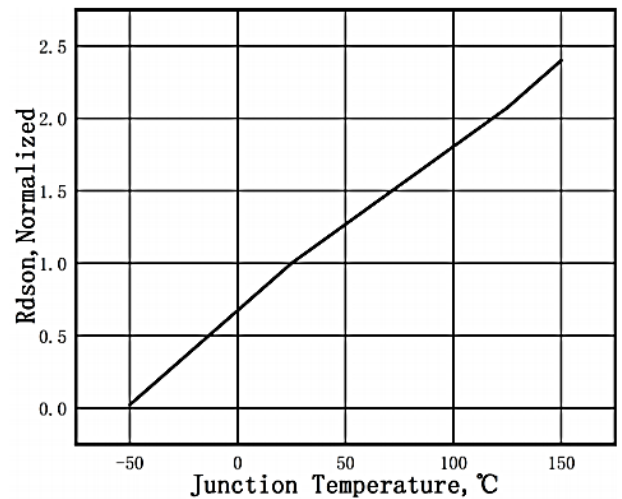


Figure 5. Normalized RDS(on) vs. Temperature

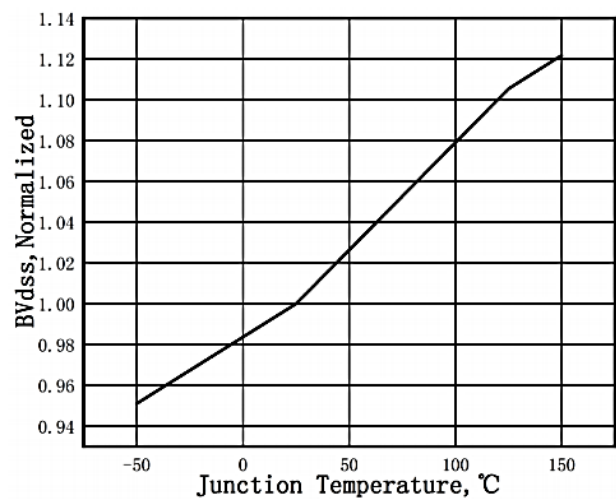


Figure 6. Normalized BVdss vs. Temperature

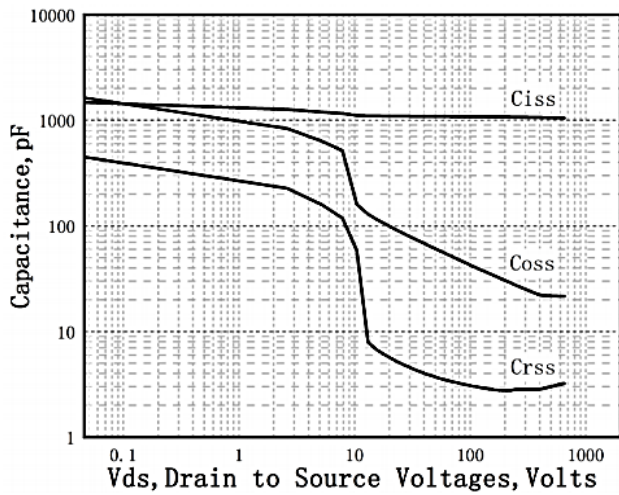


Figure 7. Capacitance Characteristics

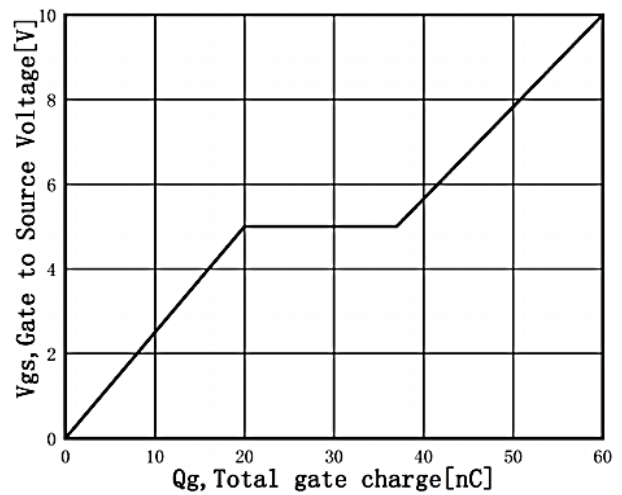


Figure 8. Gate Charge Characteristics

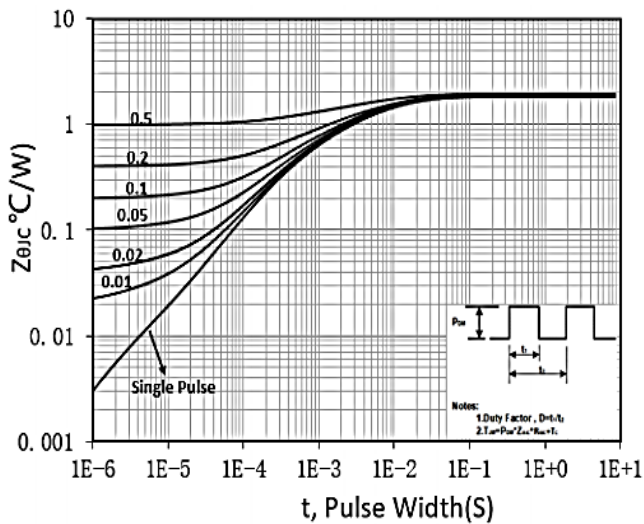


Figure 9. Maximum Safe Operating Area
(TO-220F)

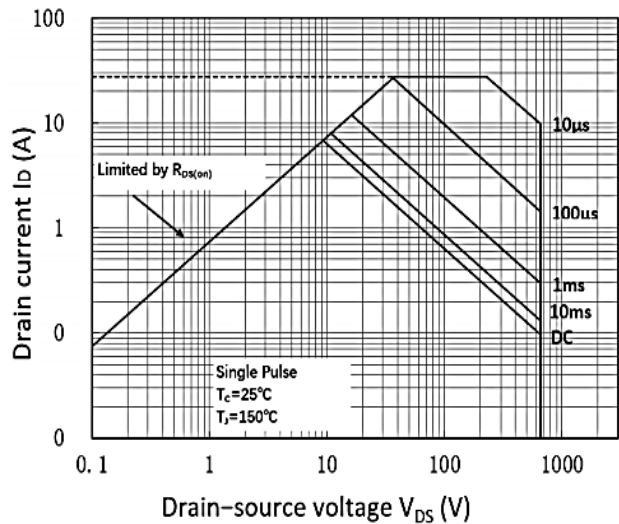
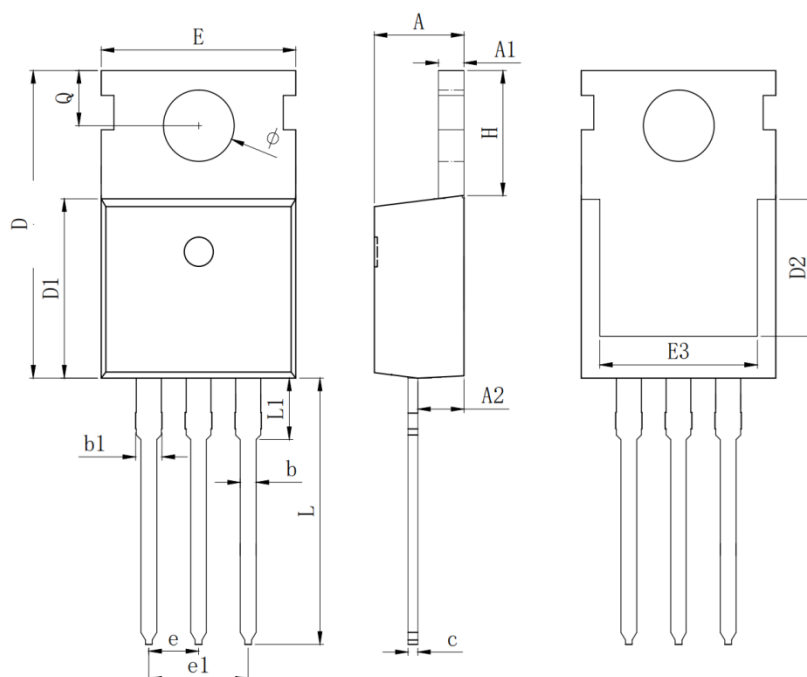


Figure 10. Transient Thermal Response Curve
(TO-220F)

Package Mechanical Data-TO220-3L



Symbol	Dimensions In Millimeters		
	min.	typ.	max.
A	4.25	4.50	4.70
A1	1.15	1.30	1.45
A2	2.15	2.35	2.55
b	0.65	0.80	0.95
b1	1.15	1.35	1.55
c	0.35	0.50	0.65
D	14.30	15.30	16.30
D1	8.80	9.10	9.40
D2	6.3REF		
E	9.70	10.00	10.30
E3	7.00	8.00	9.0
e	2.54BSC		
e1	5.08BSC		
L	12.70	13.50	13.90
L1	2.60	3.10	3.40
H	6.00	6.50	6.85
Q	2.60	2.80	3.00
φ	3.40	3.60	3.80

650V N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2024/1/31	Initial release

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