

1. DESCRIPTION

The XLADUM120x¹ are combining high speed CMOS and monolithic transformer technologies, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocouplers.

By avoiding the use of LEDs and photodiodes, devices remove the design difficulties commonly associated with opto -couplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these products. Furthermore, devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The XLADUM120x isolators provide two independent isolation channels in a variety of channel configurations and data rates(see the Ordering Guide). Both parts operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the XLADUM120x provide low pulse width distortion((the XLADUM120x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

2. FEATURES

- Narrow body, RoHS-compliant, SOP 8-lead package Low power operation
 - 5 V operation
 - 1.1 mA per channel maximum @ 0 Mbps to 2 Mbps
 - 3.7 mA per channel maximum @ 10 Mbps
 - 8.2 mA per channel maximum @ 25 Mbps
 - 3 V operation
 - 0.8 mA per channel maximum @ 0 Mbps to 2 Mbps
 - 2.2 mA per channel maximum @ 10 Mbps
 - 4.8 mA per channel maximum @ 25 Mbps
- Bidirectional communication
- 3 V/5 V level translation
- High data rate: dc to 25 Mbps (NRZ)
- Precise timing characteristics
 - 3 ns maximum pulse width distortion
 - 3 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/μs Qualified for automotive applications

3. APPLICATIONS

- Size-critical multichannel isolation
- SPI interface/data converter isolation
- RS-232/RS-422/RS-485 transceiver isolation
- Digital field bus isolation
- Hybrid electric vehicles, battery monitor, and motor drive

4. FUNCTIONAL BLOCK DIAGRAMS

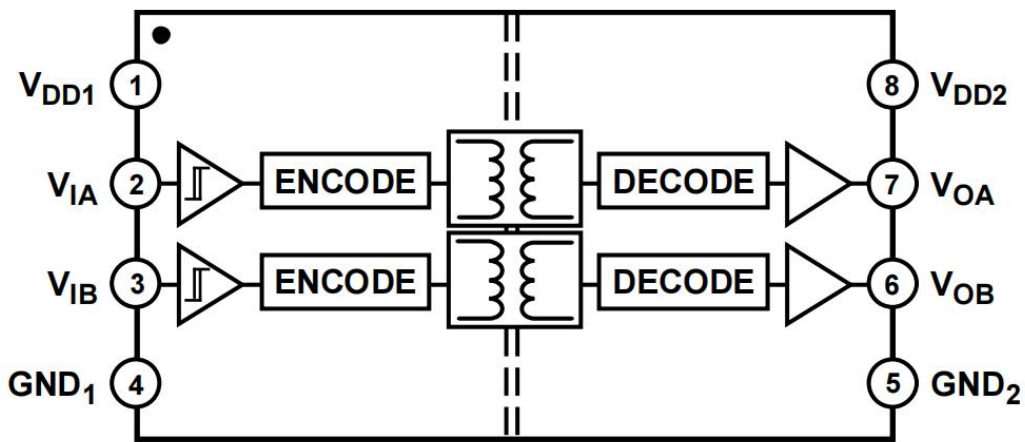


Figure 1.XLADUM1200 Functional Block Diagram

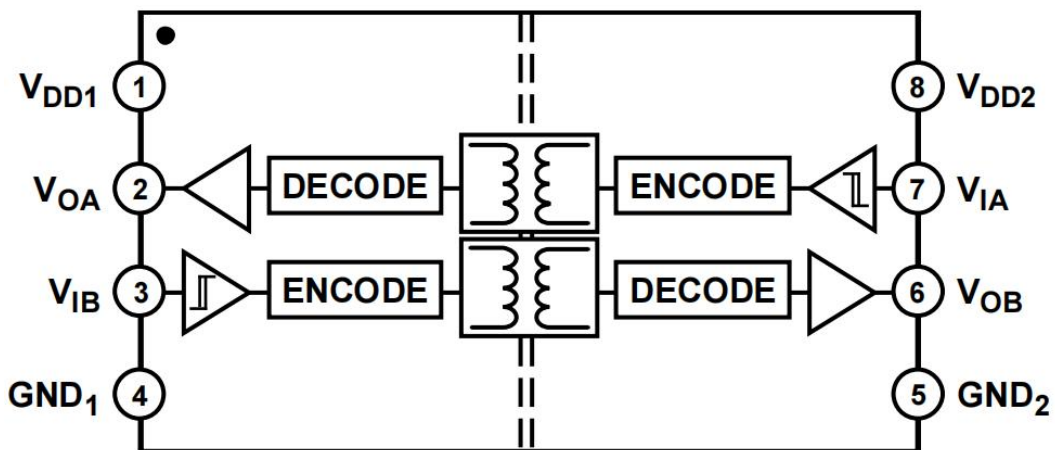


Figure 2.XLADUM1201 Functional Block Diagram

5. SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION

All voltages are relative to their respective ground; $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$		0.50	0.60	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$		0.19	0.25	mA	
XLADUM1200 Total Supply Current, Two Channels¹						
DC to 2 Mbps All Models						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.1	1.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		4.3	5.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		1.3	2.0	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$		10	13	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$		2.8	3.4	mA	12.5 MHz logic signal freq.
XLADUM1201 Total Supply Current, Two Channels¹						
DC to 2 Mbps All Models						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		2.8	3.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		2.8	3.5	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IA}, V_{IB} \leq (V_{DD1} \text{ or } V_{DD2})$
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3(V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) - 0.1 (V_{DD1} or V_{DD2}) - 0.5	5.0 4.8		V	$I_{Ox} = -20\text{ }\mu\text{A}, V_{Ix} = V_{IxH}$ $I_{Ox} = -4\text{ mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0 0.04 0.2	0.1 0.1 0.4	V	$I_{Ox} = 20\text{ }\mu\text{A}, V_{Ix} = V_{IxL}$ $I_{Ox} = 400\text{ }\mu\text{A}, V_{Ix} = V_{IxL}$ $I_{Ox} = 4\text{ mA}, V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
XLADUM120xAR						$C_L = 15\text{ pF}$, CMOS signal levels
Minimum Pulse Width ²	PW	1		1000	ns	
Maximum Data Rate ³		50			Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}			150	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			40	ns	
Change vs. Temperature			11		ps/ $^\circ\text{C}$	
Propagation Delay Skew ⁵	tPSK			100	ns	
Channel-to-Channel Matching ⁶	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	tR/tF		10		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
XLADUM120xBR						
Minimum Pulse Width ²	PW			100	ns	
Maximum Data Rate ³		10			Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD		5	3	ns	
Change vs. Temperature					ps/°C	
Propagation Delay Skew ⁵	t_{PSK}			15	ns	
Channel-to-Channel Matching				3		
Codirectional Channels ⁶	t_{PSKCD}				ns	
Opposing Directional Channels ⁶	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
XLADUM120xCR						
Minimum Pulse Width ²	PW		20	40	ns	
Maximum Data Rate ³		25	50		Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		45	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD		5	3	ns	
Change vs. Temperature					ps/°C	
Propagation Delay Skew ⁵	t_{PSK}			15	ns	
Channel-to-Channel Matching				3		
Codirectional Channels ⁶	t_{PSKCD}				ns	
Opposing Directional Channels ⁶	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F	2.5			ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output ⁷	$ CMH $	25	35		kV/μs	$V_{IX} = V_{DD1}$ or V_{DD2} , $V_{CM} = 1000$ V, transient magnitude = 800 V $V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800V
Logic Low Output ⁷	$ CML $	25	35		kV/μs	
Refresh Rate	f_r		1.2		Mbps	
Dynamic Supply Current per Channel ⁸						
Input	$I_{DDI(D)}$		0.19		mA/ Mbps	
Output	$I_{DDO(D)}$		0.05		mA/ Mbps	

1. The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for XLADUM1200 and XLADUM1201 channel configurations.

2. The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

3. The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

4. t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

5. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

6. Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

7. CMH is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CML is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

8. Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V, 105°C OPERATION

All voltages are relative to their respective ground; $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.0\text{ V}$.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$		0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DD0(Q)}$		0.11	0.20	mA	
XLADUM1200 Total Supply Current, Two Channels¹						
DC to 2 Mbps	$I_{DD1(Q)}$		0.6	1.0	mA	DC to 1 MHz logic signal freq
V_{DD1} Supply Current	$I_{DD2(Q)}$		0.2	0.6	mA	DC to 1 MHz logic signal freq
V_{DD2} Supply Current						
10 Mbps (BR and CR Grades Only)	$I_{DD1(10)}$		2.2	3.4	mA	5 MHz logic signal freq
V_{DD1} Supply Current	$I_{DD2(10)}$		0.7	1.1	mA	5 MHz logic signal freq
V_{DD2} Supply Current						
25 Mbps (CR Grade Only)	$I_{DD1(25)}$		5.2	7.7	mA	12.5 MHz logic signal freq
V_{DD1} Supply Current	$I_{DD2(25)}$		1.5	2.0	mA	12.5 MHz logic signal freq
V_{DD2} Supply Current						
XLADUM1201 Total Supply Current, Two Channels¹						
DC to 2 Mbps	$I_{DD1(Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq
V_{DD1} Supply Current	$I_{DD2(Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq
V_{DD2} Supply Current						
10 Mbps (BR and CR Grades Only)	$I_{DD1(10)}$		1.5	2.2	mA	5 MHz logic signal freq
V_{DD1} Supply Current	$I_{DD2(10)}$		1.5	2.2	mA	5 MHz logic signal freq
V_{DD2} Supply Current						
25 Mbps (CR Grade Only)	$I_{DD1(25)}$		3.4	4.8	mA	12.5 MHz logic signal freq
V_{DD1} Supply Current	$I_{DD2(25)}$		3.4	4.8	mA	12.5 MHz logic signal freq
V_{DD2} Supply Current						
For All Models						
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IA}, V_{IB} \leq (V_{DD1} \text{ or } V_{DD2})$
Logic High Input Threshold	V_{IH}	$0.7(V_{DD1} \text{ or } V_{DD2})$		$0.3(V_{DD1} \text{ or } V_{DD2})$	V	
Logic Low Input Threshold	V_{IL}					
Logic High Output Voltages	V_{OAH}, V_{OBH}	$(V_{DD1} \text{ or } V_{DD2}) - 0.1$	3.0		V	$I_{OX} = -20\text{ }\mu\text{A}, V_{IX} = V_{IXH}$
		$(V_{DD1} \text{ or } V_{DD2}) - 0.5$	2.8		V	$I_{OX} = -4\text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.04	0.1	V	$I_{OX} = 400\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 4\text{ mA}, V_{IX} = V_{IXL}$
SWITCHING SPECIFICATIONS						
XLADUM120xAR						$C_L = 15\text{ pF}$, CMOS signal levels
Minimum Pulse Width ²	PW	1		1000	ns	
Maximum Data Rate ³		50		150	ns	
Propagation Delay ⁴	t_{PHL}, t_{PLH}			40	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD		11		ps/°C	
Change vs. Temperature						
Propagation Delay Skew ⁵	t_{PSK}			100	ns	
Channel-to-Channel Matching ⁶	t_{PSKCD}			50	ns	
	t_{PSKOD}					
Output Rise/Fall Time (10% to 90%)	t_R/t_F		10		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
XLADUM120xBR						
Minimum Pulse Width ²	PW			100	ns	
Maximum Data Rate ³		10			Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		60	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew ⁵	t_{PSK}			22	ns	
Channel-to-Channel Matching						
Codirectional Channels ⁶	t_{PSKCD}			3	ns	
Opposing Directional Channels ⁶	t_{PSKOD}			22	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
XLADUM120xCR						
Minimum Pulse Width ²	PW		20	40	ns	
Maximum Data Rate ³		25	50		Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		55	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew ⁵	t_{PSK}			16	ns	
Channel-to-Channel Matching						
Codirectional Channels ⁶	t_{PSKCD}			3	ns	
Opposing Directional Channels ⁶	t_{PSKOD}			16	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output ⁷	CMH	25	35		kV/μs	$V_{IX} = V_{DD1}$ or V_{DD2} , $V_- = 1000$ V, transient magnitude = 800 V $V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Logic Low Output ⁷	CML	25	35		kV/μs	
Refresh Rate	Fr		1.1		Mbps	
Dynamic Supply Current per Channel ⁸						
Input	$I_{DDI(D)}$		0.10		mA/Mbps	
Output	$I_{DDO(D)}$		0.03		mA/Mbps	

1. The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for XLADUM1200 and XLADUM1201 channel configurations.

2. The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

3. The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

4. t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

5. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

6. Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

7. CMH is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CML is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

8. Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V, 105°C OPERATION

All voltages are relative to their respective ground; 5 V/3 V operation: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$. 3V/5V operation: $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$; $V_{DD1} = 3.0\text{ V}$, $V_{DD2} = 5.0\text{ V}$; or $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 3.0\text{ V}$;

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$					
5 V/3 V Operation			0.50	0.6	mA	
3 V/5 V Operation			0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$					
5 V/3 V Operation			0.11	0.20	mA	
3 V/5 V Operation			0.19	0.25	mA	
XLADUM1200 Total Supply Current, Two Channels¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			1.1	1.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.6	1.0	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.2	0.6	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			4.3	5.5	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.2	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			0.7	1.1	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.3	2.0	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$					
5 V/3 V Operation			10	13	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			5.2	7.7	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$					
5 V/3 V Operation			1.5	2.0	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			2.8	3.4	mA	12.5 MHz logic signal freq.
XLADUM1201 Total Supply Current, Two Channels¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			0.8	1.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.4	0.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.4	0.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.8	1.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			2.8	3.5	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.5	2.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.5	2.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.8	3.5	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$					
5 V/3 V Operation			6.3	8.0	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			3.4	4.8	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$					
5 V/3 V Operation			3.4	4.8	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			6.3	8.0	mA	12.5 MHz logic signal freq.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
For All Models						
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0 V \leq V_{IA}, V_{IB} \leq (V_{DD1} \text{ or } V_{DD2})$
Logic High Input Threshold	V_{IH}	$0.7(V_{DD1} \text{ or } V_{DD2})$			V	
Logic Low Input Threshold	V_{IL}			$0.3 (V_{DD1} \text{ or } V_{DD2})$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$(V_{DD1} \text{ or } V_{DD2}) - 0.1$	$V_{DD1} \text{ or } V_{DD2}$		V	$I_{OX} = -20 \mu A, V_{IX} = V_{IXH}$
		$(V_{DD1} \text{ or } V_{DD2}) - 0.5$	$(V_{DD1} \text{ or } V_{DD2}) - 0.2$		V	$I_{OX} = -4 \text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	$I_{OX} = 20 \mu A, V_{IX} = V_{IXL}$
			0.04	0.1	V	$I_{OX} = 400 \mu A, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 4 \text{ mA}, V_{IX} = V_{IXL}$
SWITCHING SPECIFICATIONS						
XLADUM120xAR						$C_L = 15 \text{ pF}$, CMOS signal levels
Minimum Pulse Width ²	PW			1000	ns	
Maximum Data Rate ³		1			Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}	50		150	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			40	ns	
Change vs. Temperature			11		ps/°C	
Propagation Delay Skew ⁵	t_{PSK}			50	ns	
Channel-to-Channel Matching ⁶	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10%to 90%)	t_R/t_F		10		ns	
XLADUM120xBR						$C_L = 15 \text{ pF}$, CMOS signal levels
Minimum Pulse Width ²	PW			100	ns	
Maximum Data Rate ³		10			Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}	15		55	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew ⁵	t_{PSK}			22	ns	
Channel-to-Channel Matching						
Codirectional Channels ⁶	t_{PSKCD}			3	ns	
Opposing Directional Channels ⁶	t_{PSKOD}			22	ns	
Output Rise/Fall Time (10%to 90%)	t_R/t_F					
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
XLADUM120xCR						$C_L = 15 \text{ pF}$, CMOS signal levels
Minimum Pulse Width ²	PW		20	40	ns	
Maximum Data Rate ³		25	50		Mbps	
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew ⁵	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels ⁶	t_{PSKCD}			3	ns	
Opposing Directional Channels ⁶	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10%to 90%)	t_R/t_F					
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output ⁷	$ CMH $	25	35		kV/ μs	$V_{IX} = V_{DD1} \text{ or } V_{DD2}, V_{CM} = 1000 \text{ V}$, transient magnitude =800 V
Logic Low Output ⁷	$ CML $	25	35		kV/ μs	$V_{IX} = 0 \text{ V}, V_{CM} = 1000 \text{ V}$, transient magnitude =800 V
Refresh Rate	F_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel ⁸	$I_{DDI(D)}$					
5 V/3 V Operation			0.19		mA/	
					Mbps	
3 V/5 V Operation			0.10		mA/	
					Mbps	
Output Dynamic Supply Current per Channel ⁸	$I_{DDO(D)}$					
5 V/3 V Operation			0.03		mA/	
					Mbps	
3 V/5 V Operation			0.05		mA/	
					Mbps	

1. The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for XLADUM1200 and XLADUM1201 channel configurations.
2. The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
3. The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
4. t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
5. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
6. Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
7. CMH is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CML is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8 V$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
8. Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

6. PACKAGE CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output) ¹	R_{I-O}		10 ¹²		Ω	f = 1 MHz
Capacitance (Input-to-Output) ¹	C_{I-O}		1.0		pF	
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		41		°C/W	

1.The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

7. RECOMMENDED OPERATING CONDITIONS

Parameter	Rating
Operating Temperature (T_A)	-40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2}) ¹	3.0 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

1.All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

8. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Storage Temperature (T_{ST})	-55°C to +150°C
Ambient Operating Temperature (T_A)	-40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2}) ¹	-0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}) ^{1, 2}	-0.5 V to $V_{DDI} + 0.5$ V
Output Voltages (V_{OA}, V_{OB}) ^{1, 2}	-0.5 V to $V_{DDO} + 0.5$ V
Average Output Current per Pin (I_O)	-11 mA to +11 mA
Common-Mode Transients (CM_L, CM_H) ³	-100 kV/ μ s to +100 kV/ μ s

1. All voltages are relative to their respective ground.

2. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.

3. Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage

NOTE:

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9. ESD CAUTION

ESD (electrostatic discharge) sensitive device. charged devices and circuit boards can discharge without detection. Although this product features proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD Precautions should be taken to avoid performance degradation or loss of functionality

Table 1.Maximum Continuous Working Voltage

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1

10. PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

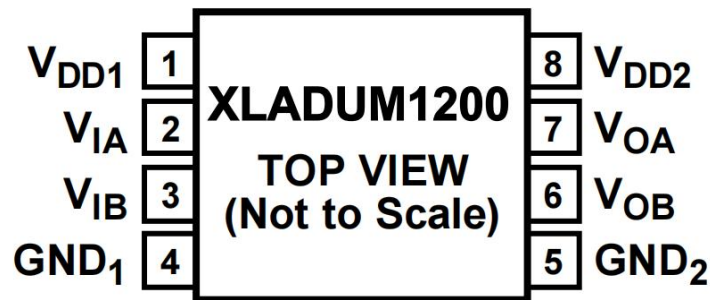


Figure 4.XLADUM1200 Pin Configuration

XLADUM1200 Pin Function Descriptions

PIN NO.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	V _{IA}	Logic Input A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1.Ground Reference for Isolator Side 1.
5	GND ₂	Ground 2.Ground Reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{OA}	Logic Output A.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

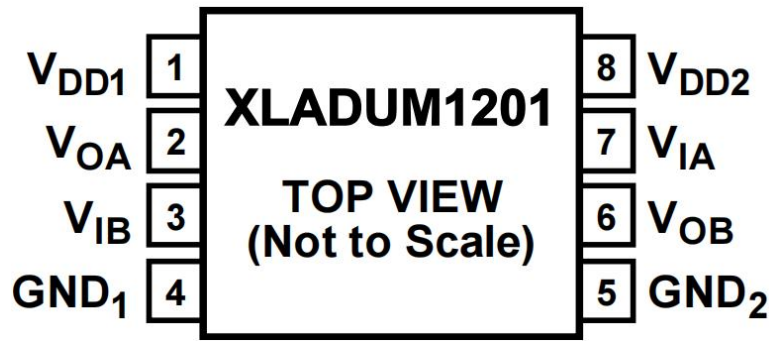


Figure 4.XLADUM1200 Pin Configuration

XLADUM1201 Pin Function Descriptions

PIN NO.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1.Ground Reference for Isolator Side 1.
5	GND_2	Ground 2.Ground Reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

XLADUM1200 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μs of V_{DD2} power restoration.

XLADUM1201 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Unpowered	Indeterminate	H	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X	X	Powered	Powered	H	Indeterminate	Outputs return to the input state within 1 μs of V_{DD2} power restoration.

11. TYPICAL PERFORMANCE CHARACTERISTICS

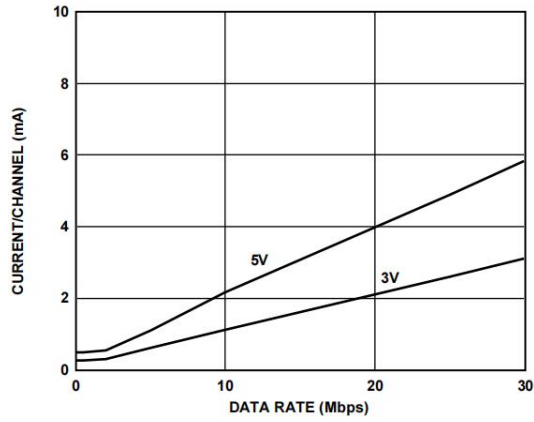


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5V and 3V Operation

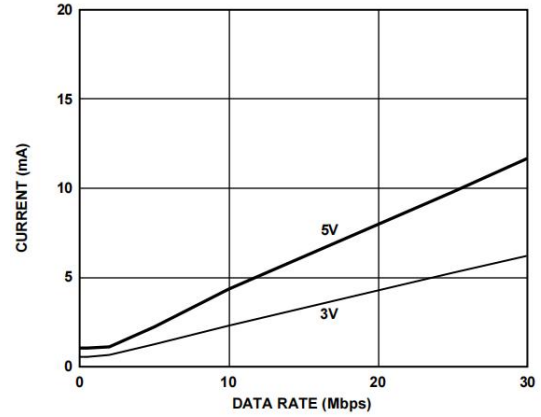


Figure 9. Typical XLADUM1200 V_{DD1} Supply Current vs. Data Rate for 5V and 3V Operation

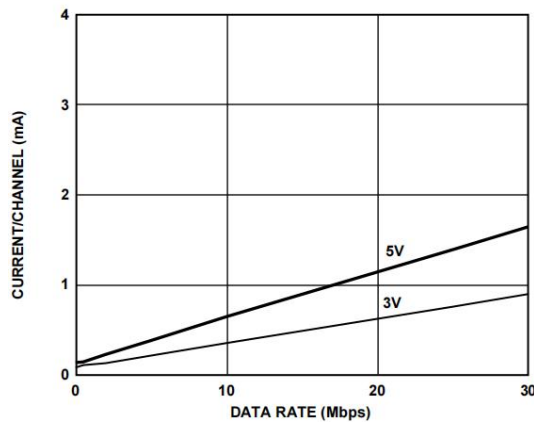


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5V and 3V Operation (No Output Load)

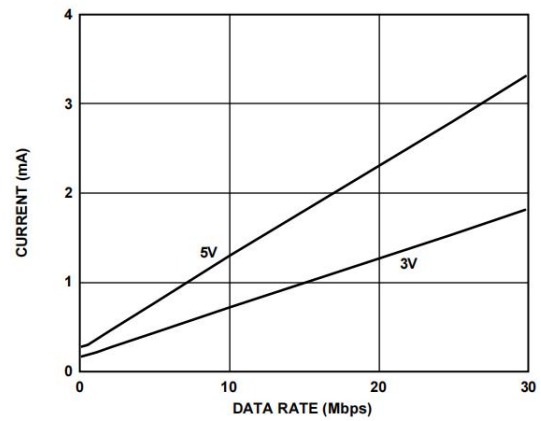


Figure 10. Typical XLADUM1200 V_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation

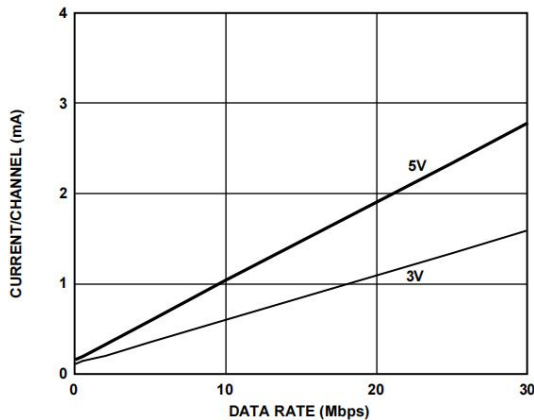


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5V and 3V Operation (15 pF Output Load)

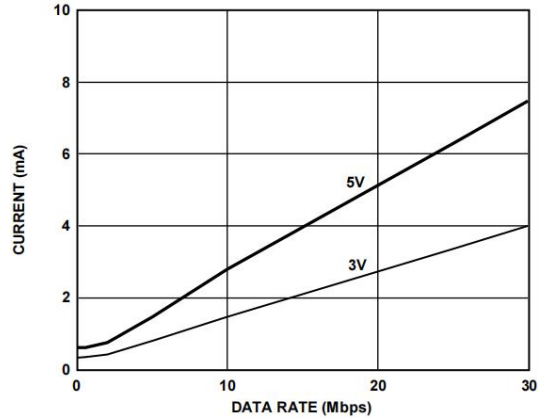


Figure 11. Typical XLADUM1201 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation

12. APPLICATIONS INFORMATION

12.1. PCB LAYOUT

The XLADUM120x digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value should be between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

12.2. PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

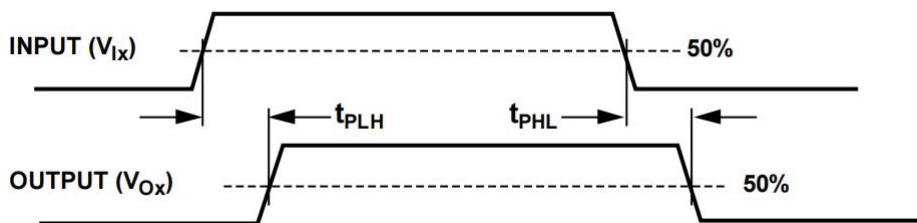


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single XLADUM120x component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple XLADUM120x components operating under the same conditions.

12.3. DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input send narrow (~ 1 ns) pulses to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than ~ 1 μs at the input, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 17 and Table 18) by the watchdog timer circuit.

The XLADUM120x are extremely immune to external magnetic fields. The limitation on the magnetic field immunity of the XLADUM120x is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the XLADUM120x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2; n = 1, 2, \dots, N$$

where:

β is the magnetic flux density (gauss).

N is the number of turns in the receiving coil.

rn is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the XLADUM120x and an imposed requirement that the induced voltage be 50% at most of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

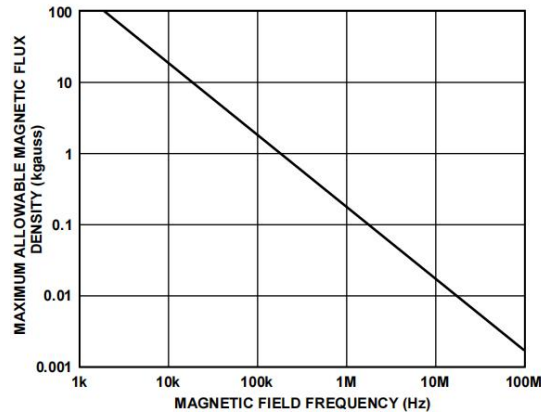


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and has the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the XLADUM120x transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As seen, the XLADUM120x are extremely immune and can be affected only by extremely large currents operating very close to the component at a high frequency. For the 1 MHz example, a 0.5 kA current would have to be placed 5 mm away from the XLADUM120x to affect the operation of the component.

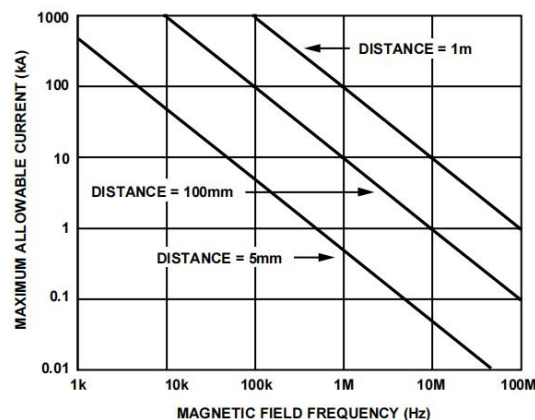


Figure 14. Maximum Allowable Current for Various Current-to-XLADUM120x Spacings

Note that, at combinations of strong magnetic fields and high frequencies, any loops formed by PCB traces can induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

12.4. POWER CONSUMPTION

The supply current at a given channel of the XLADUM120x isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$\begin{aligned} I_{DDI} &= I_{DDI(Q)} & f \leq 0.5f_r \\ I_{DDI} &= I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} & f > 0.5f_r \end{aligned}$$

For each output channel, the supply current is given by

$$\begin{aligned} I_{DDO} &= I_{DDO(Q)} & f \leq 0.5f_r \\ I_{DDO} &= (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} & f > 0.5f_r \end{aligned}$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply currents, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 6 and Figure 7 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 provides perchannel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 11 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for XLADUM1200 and XLADUM1201 channel configurations.

13. INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the XLADUM120x.

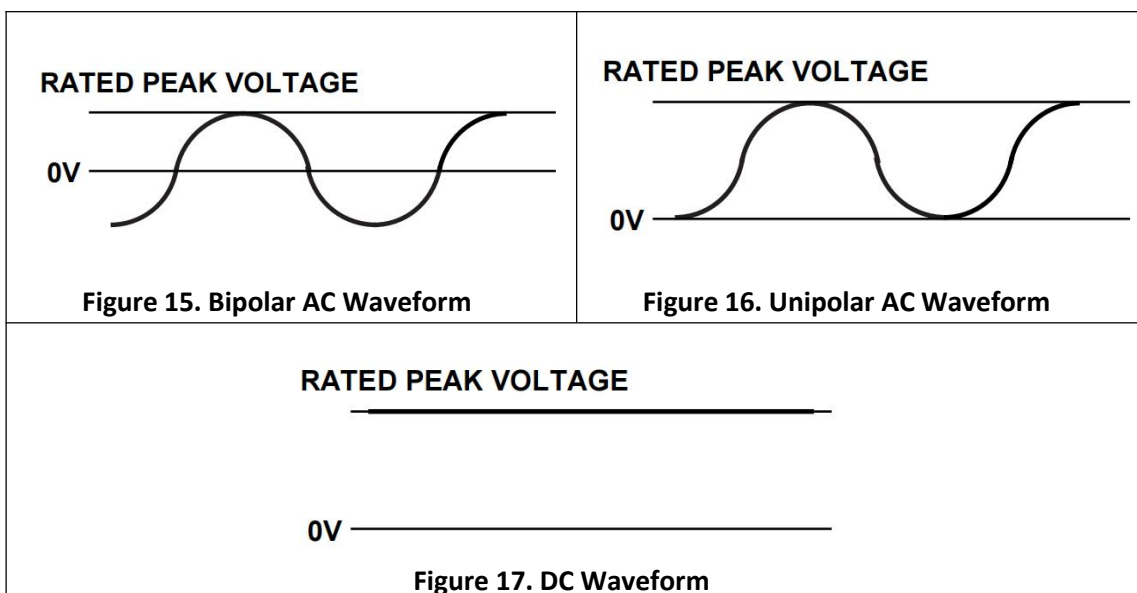
Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 14 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the XLADUM120x depends on the voltage waveform type imposed across the isolation barrier. The insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms, respectively.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages yet still achieves a 50-year service life. The working voltages listed in Table 1 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage cases. Any crossinsulation voltage waveform that does not conform to Figure 16 or Figure 17 is to be treated as a bipolar ac waveform, and its peak voltage is to be limited to the 50-year lifetime voltage value listed in Table 1.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

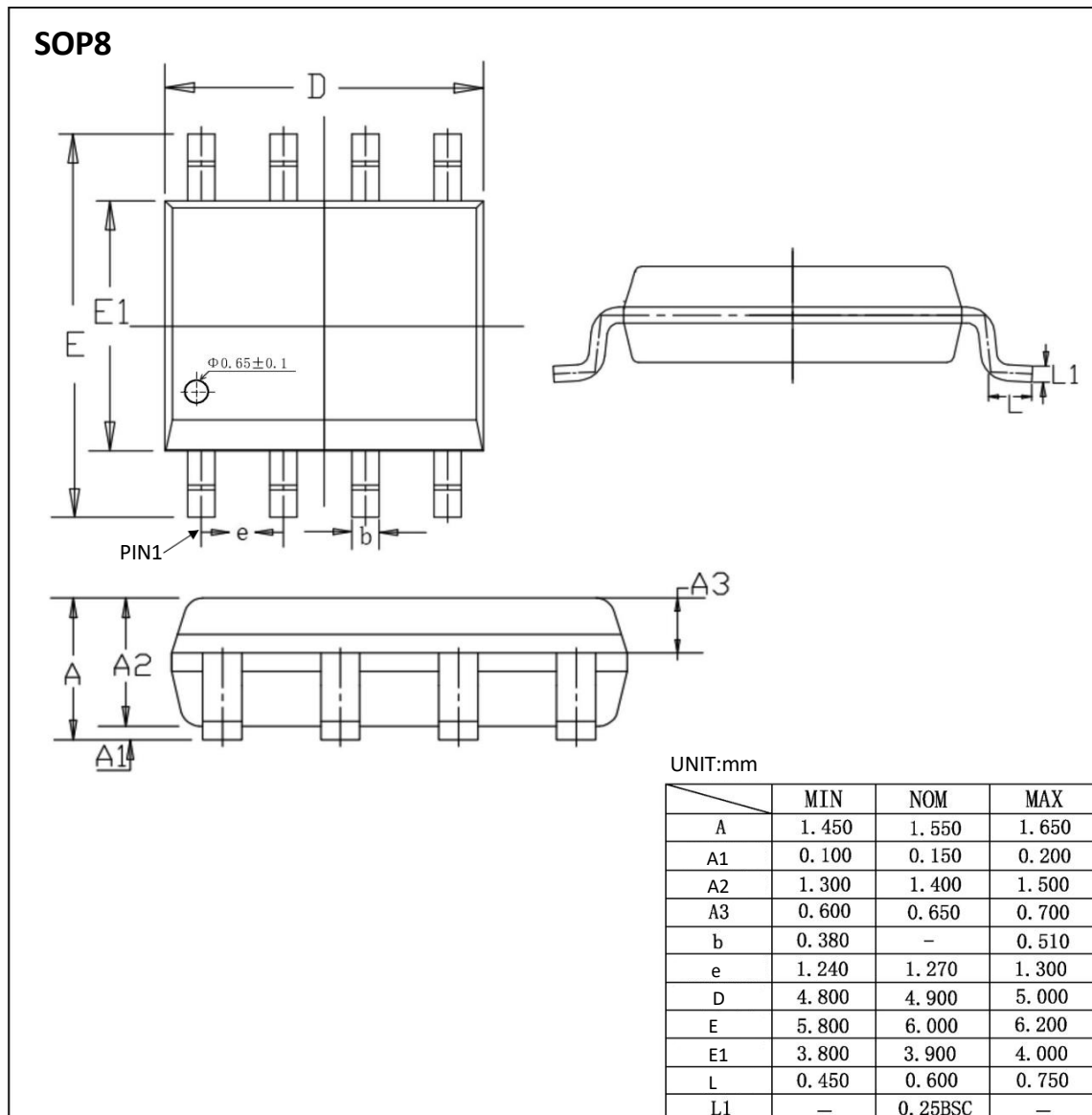


14. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLADUM1200ARZ-RL7	XL1200A	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM1200BRZ-RL7	XL1200B	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM1200CRZ-RL7	XL1200C	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM1201ARZ-RL7	XL1201A	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM1201BRZ-RL7	XL1201B	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM1201CRZ-RL7	XL1201C	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500

15. DIMENSIONAL DRAWINGS



[if you need help contact us. Xinluda reserves the right to change the above information without prior notice]