

1. DESCRIPTION

The XLADUM3200/XLADUM3201 are dual-channel, digital isolators based on . Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these products. Furthermore, devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates. The XLADUM3200/XLADUM3201 isolators provide two independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). They operate with 3.3 V or 5 V supply voltages on either side, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

In comparison to the XLADUM1200/XLADUM1201 isolators, the XLADUM3200/XLADUM3201 isolators contain various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the XLADUM1200/XLADUM1201 or XLADUM3200/XLADUM3201 products is strongly determined by the design and layout of the user board or module.

2. FEATURES

- Enhanced system-level ESD performance per IEC 61000-4-x
- Narrow body, RoHS-compliant, 8-lead SOP
- Low power operation
 - 5 V operation
 - 1.7 mA per channel maximum at 0 Mbps to 2 Mbps
 - 3.7 mA per channel maximum at 10 Mbps
 - 7.0 mA per channel maximum at 25 Mbps
 - 3.3 V operation
 - 1.5 mA per channel maximum at 0 Mbps to 2 Mbps
 - 2.5 mA per channel maximum at 10 Mbps
 - 5.2 mA per channel maximum at 25 Mbps
- Bidirectional communication
- 3.3 V/5 V level translation
- High data rate: dc to 25 Mbps (NRZ)
- Precise timing characteristics
 - 3 ns maximum pulse width distortion
 - 3 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/μs

3. APPLICATIONS

- Size-critical multichannel isolation
- SPI interface/data converter isolation
- RS-232/RS-422/RS-485 transceiver isolation
- Digital field bus isolation
- Hybrid electric vehicles, battery monitor

4. FUNCTIONAL BLOCK DIAGRAMS

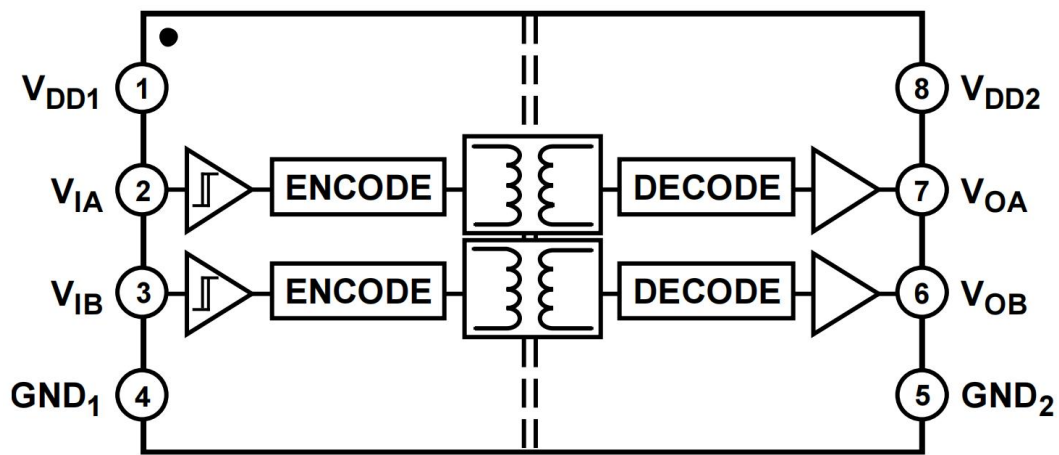


Figure 1. XLADUM3200 Functional Block Diagram

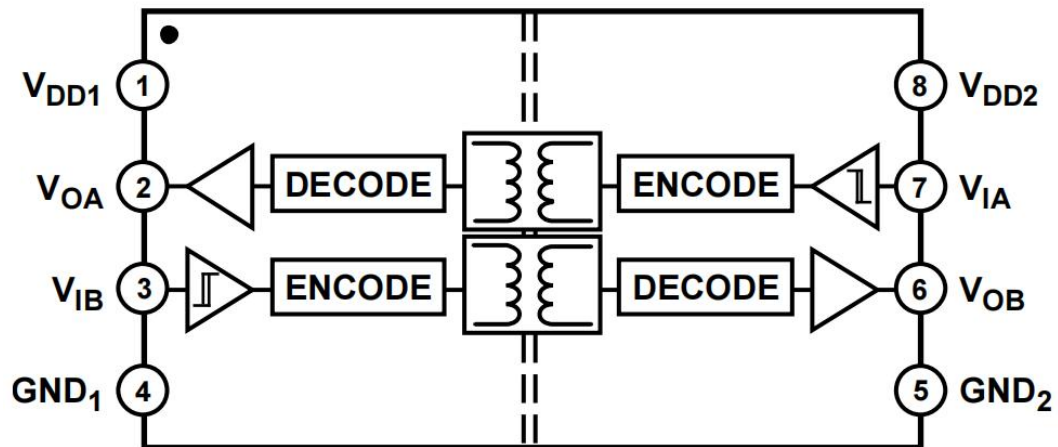


Figure 2. XLADUM3201 Functional Block Diagram

5. SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	symbol	A Grade			B Grade			C Grade			Unit	Test Conditions /Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate	t_{PHL}, t_{PLH}	20		1	20		10	20		25	Mbps	Within PWD limit
Propagation Delay				150			50			45	ns	50% input to 50%output
Pulse Width Distortion				PWD			40			3	3	ns
Change vs.Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	tPSK			100	15		15	ns		Between any two units		
Channel Matching								ns				
Codirectional	tPSKCD			50			3			3	ns	
Opposing-Direction	tPSKOD			50			15			15	ns	
Output Rise/Fall Time	tR/tF		10			2.5			2.5		ns	10% to 90%

Table 2.

Parameter	symbol	1 Mbps—A Grade, B Grade, and C Grade			10 Mbps—A Grade, B Grade, and C Grade			25 Mbps—C Grade			Unit	Test Conditions /Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
XLADUM3200	I _{DD1}		1.3	1.8		3.5	4.6		7.7	10.0	mA	No load
	I _{DD2}		1.0	1.6		2.0	2.8		3.8	4.9	mA	No load
XLADUM3201	I _{DD1}		1.1	1.6		3.1	4.2		6.9	8.9	mA	No load
	I _{DD2}		1.3	1.9		3.1	4.0		6.1	8.3	mA	No load

Table 3.

Parameter	symbol	Min	Typ	Max	Unit	Test Conditions /Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDX}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 V_{DDX}$	V	
Logic High Output Voltages	V_{OH}	$V_{DDX} - 0.1$	V_{DDX}		V	$I_{OX} = -20\text{ }\mu\text{A}, V_{IX} = V_{IXH}$
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	$I_{OX} = -3.2\text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 3.2\text{ mA}, V_{IX} = V_{IXL}$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IX} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity ¹	CM	25	35		kV/ μs	$V_{IX} = V_{DDX}, V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Refresh Rate	fr		1.2		Mbps	

1. |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V, 105°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $CL = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted.

Table.4

Parameter	symbol	A Grade			B Grade			C Grade			Unit	Test Conditions /Comments			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max					
SWITCHING SPECIFICATIONS															
Data Rate	t_{PHL}, t_{PLH} PWD	20		1	20		10			25	Mbps	Within PWD limit 50% input to 50%output			
Propagation Delay							150						60		55
Pulse Width Distortion															
XLADUM3200		6		40	5		3	5	3	ns	$ t_{PLH} - t_{PHL} $				
XLADUM3201				40			4		4	ns	$ t_{PLH} - t_{PHL} $				
Change vs.Temperature										ps/°C					
Pulse Width	PW	1000			100			40		5	ns	Within PWD limit			
Propagation Delay Skew	t_{PSK}									22			16	ns	Between any two units
Channel Matching															
Codirectional	t_{PSKCD}						50			3			3	ns	
Opposing-Direction	t_{PSKOD}						50			22			16	ns	
Output Rise/Fall Time	t_R/t_F		3.0			3.0			3.0		ns	10% to 90%			

Table 5.

Parameter	symbol	1 Mbps—A Grade, B Grade, and C Grade			10 Mbps— B Grade, and C Grade			25 Mbps—C Grade			Unit	Test Conditions /Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
XLADUM3200	IDD1		0.8	1.3		2.2	3.2		4.8	6.4	mA	No load
	IDD2		0.7	1.0		1.3	1.7		2.3	3.0	mA	No load
XLADUM3201	IDD1		0.7	1.3		1.9	2.5		4.1	5.3	mA	No load
	IDD2		0.8	1.6		1.9	2.5		3.7	5.1	mA	No load

Table 6.For All Models

Parameter	symbol	Min	Typ	Max	Unit	Test Conditions /Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDX}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 V_{DDX}$	V	
Logic High Output Voltages	V_{OH}	$V_{DDX} - 0.1$	V_{DDX}		V	$I_{OX} = -20\text{ }\mu\text{A}, V_{IX} = V_{IXH}$
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	$I_{OX} = -3.2\text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 3.2\text{ mA}, V_{IX} = V_{IXL}$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IX} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity ¹	CM	25	35		kV/ μs	$V_{IX} = V_{DDX}, V_{CM} = 1000\text{ V}$, transient magnitude =
Refresh Rate	fr		1.1		Mbps	800 V

1. |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V, 105°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$, and CMOS signal levels, unless otherwise noted.

Table.7

Parameter	symbol	A Grade			B Grade			C Grade			Unit	Test Conditions /Comments		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max				
SWITCHING SPECIFICATIONS														
Data Rate	t _{PHL} , t _{PLH} PWD	15		1	15		10	15		25	Mbps	Within PWD limit		
Propagation Delay				150			55			50	50% input to 50%output			
Pulse Width Distortion				40			3			3	t _{PLH} – t _{PHL}			
Change vs.Temperature	PW tPSK	1000	6		100	5		40	5	ps/°C				
Pulse Width													ns	Within PWD limit
Propagation Delay Skew										50	22	15	ns	Between any two units
Channel Matching											ns			
Codirectional	tPSKCD			50			3			3	ns			
Opposing-Direction	tPSKOD			50			22			15	ns			
Output Rise/Fall Time	tR/tF		3.0			3.0			3.0		ns	10% to 90%		

Table 8.

Parameter	symbol	1 Mbps—A Grade, B Grade, and C Grade			10 Mbps— B Grade, and C Grade			25 Mbps—C Grade			Unit	Test Conditions /Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
XLADUM3200	I _{DD1}		1.3	1.8		3.5	4.6		7.7	10.0	mA	No load
	I _{DD2}		0.7	1.0		1.3	1.7		2.3	3.0	mA	No load
XLADUM3201	I _{DD1}		1.1	1.6		3.1	4.2		6.9	8.9	mA	No load
	I _{DD2}		0.8	1.6		1.9	2.5		3.7	5.1	mA	No load

Table 9. For All Models

Parameter	symbol	Min	Typ	Max	Unit	Test Conditions /Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDX}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 V_{DDX}$	V	
Logic High Output Voltages	V_{OH}	$V_{DDX} - 0.1$	V_{DDX}		V	$I_{OX} = -20\text{ }\mu\text{A}, V_{IX} = V_{IXH}$
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	$I_{OX} = -3.2\text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 3.2\text{ mA}, V_{IX} = V_{IXL}$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IX} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity ¹	CM	25	35		kV/ μs	$V_{IX} = V_{DDX}, V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Refresh Rate	fr		1.2		Mbps	

1. |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V, 105°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 5.0\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted.

Table.10

Parameter	symbol	A Grade			B Grade			C Grade			Unit	Test Conditions /Comments	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
SWITCHING SPECIFICATIONS													
Data Rate	t_{PHL}, t_{PLH} PWD	15		1	15		10	15		25	Mbps ns	Within PWD limit 50% input to 50%output	
Propagation Delay													
Pulse Width Distortion													
XLADUM3200			40		3		3		$ t_{PLH} - t_{PHL} $				
XLADUM3201			40		4		4		$ t_{PLH} - t_{PHL} $				
Change vs.Temperature		1000	6		100	5		40	5	ps/°C ns ns		Within PWD limit Between any two units	
Pulse Width	PW												
Propagation Delay Skew	t_{PSK}												
Channel Matching													
Codirectional	t_{PSKCD}												
Opposing-Direction	t_{PSKOD}			50			3			3	ns		
Output Rise/Fall Time	t_R/t_F		2.5			2.5			2.5		ns	10% to 90%	

Table 11.

Parameter	symbol	1 Mbps—A Grade, B Grade, and C Grade			10 Mbps— B Grade, and C Grade			25 Mbps—C Grade			Unit	Test Conditions /Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
XLADUM3200	I _{DD1}		0.8	1.3		2.2	3.2		4.8	6.4	mA	No load
	I _{DD2}		1.0	1.6		2.0	2.8		3.8	4.9	mA	No load
XLADUM3201	I _{DD1}		0.7	1.3		1.9	2.5		4.1	5.3	mA	No load
	I _{DD2}		1.3	1.9		3.1	4.0		6.1	8.3	mA	No load

Table 12. For All Models

Parameter	symbol	Min	Typ	Max	Unit	Test Conditions /Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDX}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 V_{DDX}$	V	
Logic High Output Voltages	V_{OH}	$V_{DDX} - 0.1$	V_{DDX}		V	$I_{OX} = -20\text{ }\mu\text{A}, V_{IX} = V_{IXH}$
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	$I_{OX} = -3.2\text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 3.2\text{ mA}, V_{IX} = V_{IXL}$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IX} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity ¹	CM	25	35		kV/ μs	$V_{IX} = V_{DDX}, V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Refresh Rate	fr		1.1		Mbps	

1. |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

6. PACKAGE CHARACTERISTICS

Table 13.

Parameter	symbol	Min	Typ	Max	Unit	Test Conditions /Comments
Resistance (Input to Output) ¹	R _{I-O}		10 ¹²		Ω	f = 1 MHz
Capacitance (Input to Output) ¹	C _{I-O}		1.0		pF	
Input Capacitance	C _I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ _{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ _{JCO}		41		°C/W	

1. The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

7. ABSOLUTE MAXIMUM RATINGS

Table 14. Ambient temperature = 25°C, unless otherwise noted.

Parameter	Rating
Storage Temperature (T _{ST})	–55°C to +150°C
Ambient Operating Temperature (T _A)	–40°C to +105°C
Supply Voltages (V _{DD1} , V _{DD2}) ¹	–0.5 V to +7.0 V
Input Voltages (V _{IA} , V _{IB}) ^{1, 2}	–0.5 V to V _{DDI} + 0.5 V
Output Voltages (V _{OA} , V _{OB}) ^{1, 2}	–0.5 V to V _{DDO} + 0.5 V
Average Output Current per Pin (I _O)	–22 mA to +22 mA
Common-Mode Transients (CM _L , CM _H) ³	–100 kV/μs to +100 kV/μs

1. All voltages are relative to their respective ground.

2. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.

3. Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage

NOTE:

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8. ESD CAUTION

ESD (electrostatic discharge) sensitive device. charged devices and circuit boards can discharge without detection. Although this product features proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD Precautions should be taken to avoid performance degradation or loss of functionality

Table 15. Maximum Continuous Working Voltage

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1

Table 16.XLADUM3200 Truth Table (Positive Logic)

V _{IA} Input	V _{IB} Input	V _{DD1} State	V _{DD2} State	V _{OA} Output	V _{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 μ s of V _{DD1} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μ s of V _{DD0} power restoration.

Table 17.XLADUM3201 Truth Table (Positive Logic)

V _{IA} Input	V _{IB} Input	V _{DD1} State	V _{DD2} State	V _{OA} Output	V _{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1 μ s of V _{DD1} power restoration.
X	X	Powered	Powered	H	Indeterminate	Outputs return to the input state within 1 μ s of V _{DD0} power restoration.

9. PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

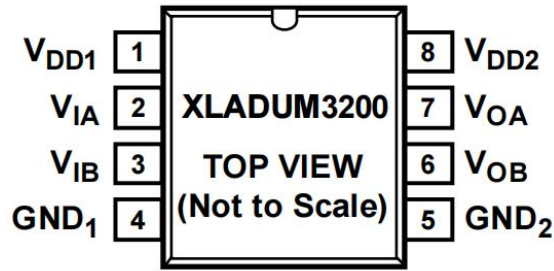


Figure 4.XLADUM3200 Pin Configuration

XLADUM1200 Pin Function Descriptions

PIN NO.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	V _{IA}	Logic Input A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1.Ground Reference for Isolator Side 1.
5	GND ₂	Ground 2.Ground Reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{OA}	Logic Output A.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

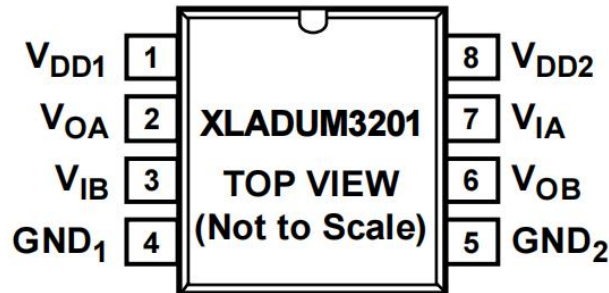


Figure 5.XLADUM3201 Pin Configuration

XLADUM1201 Pin Function Descriptions

PIN NO.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	V _{OA}	Logic Output A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1.Ground Reference for Isolator Side 1.
5	GND ₂	Ground 2.Ground Reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{IA}	Logic Input A.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

10. TYPICAL PERFORMANCE CHARACTERISTICS

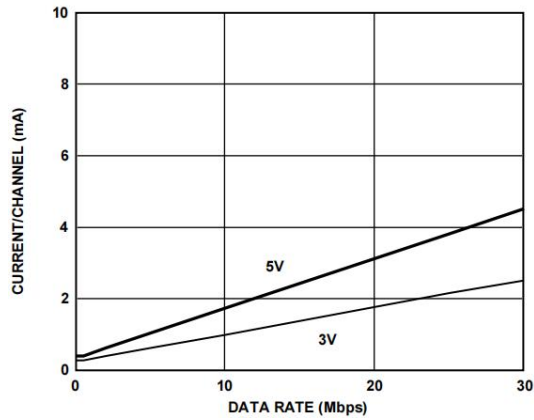


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5V and 3V Operation

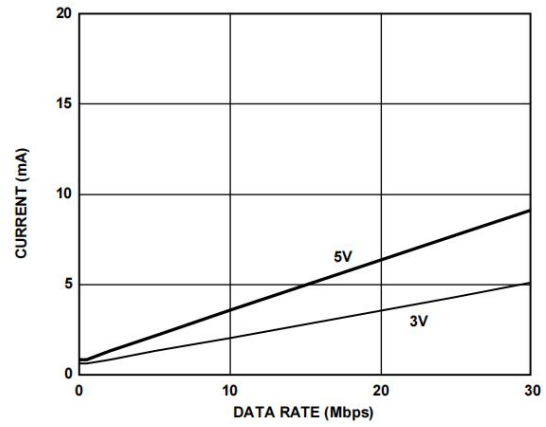


Figure 9. Typical XLADUM3200 I_{DD1} Supply Current vs. Data Rate for 5V and 3V Operation

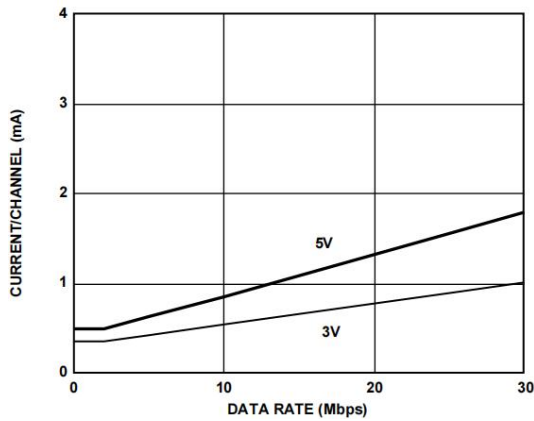


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5V and 3V Operation (No Output Load)

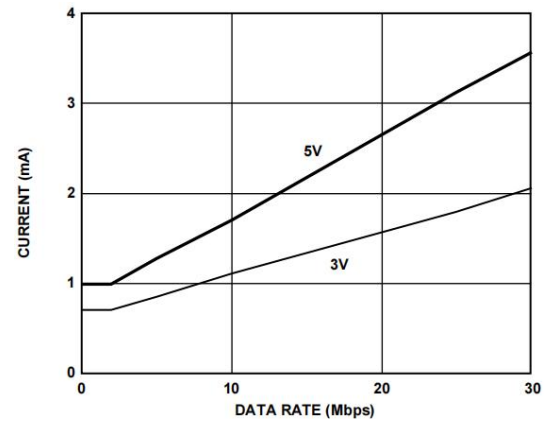


Figure 10. Typical XLADUM3200 I_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation

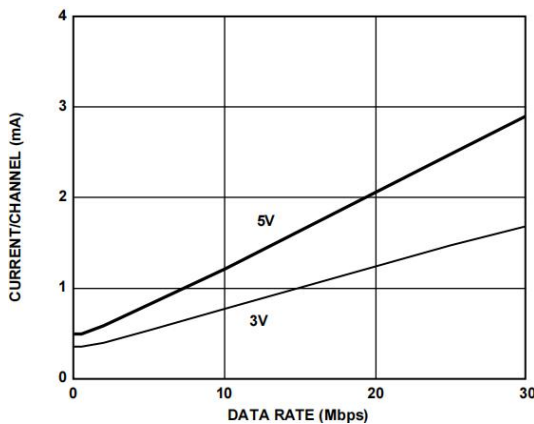


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5V and 3V Operation (15 pF Output Load)

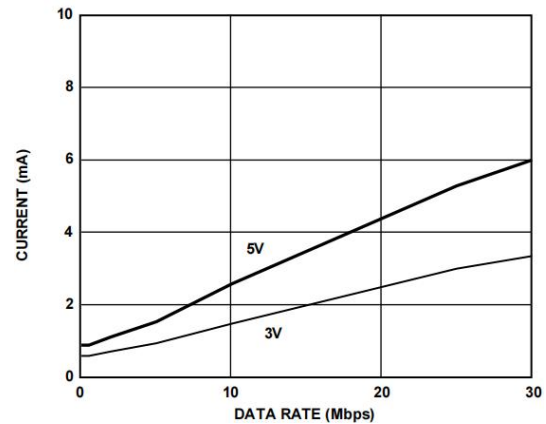


Figure 11. Typical XLADUM3201 I_{DD1} or I_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation

11. APPLICATIONS INFORMATION

11.1. PCB LAYOUT

The XLADUM3200/XLADUM3201 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value must be between $0.01\ \mu\text{F}$ and $0.1\ \mu\text{F}$. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

12. SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design which varies widely by application. The XLADUM3200/XLADUM3201 incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation technique between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and the respective ground.

While the XLADUM3200/XLADUM3201 improve system-level ESD reliability, they are no substitute for a robust system-level design.

13. PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high.

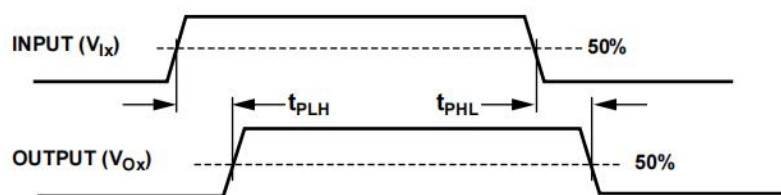


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single XLADUM3200/XLADUM3201 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple XLADUM3200/ XLADUM3201 components operating under the same conditions.

14. DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than ~1 μs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state (see Table 16 and Table 17) by the watchdog timer circuit.

The XLADUM3200/XLADUM3201 are extremely immune to external magnetic fields. The limitation on the XLADUM3200/XLADUM3201 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the XLADUM3200/XLADUM3201 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, n = 1, 2, \dots, N$$

where:

β is the magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n th turn in the receiving coil (cm).

Given the geometry of the receiving coil in the XLADUM3200/XLADUM3201 and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

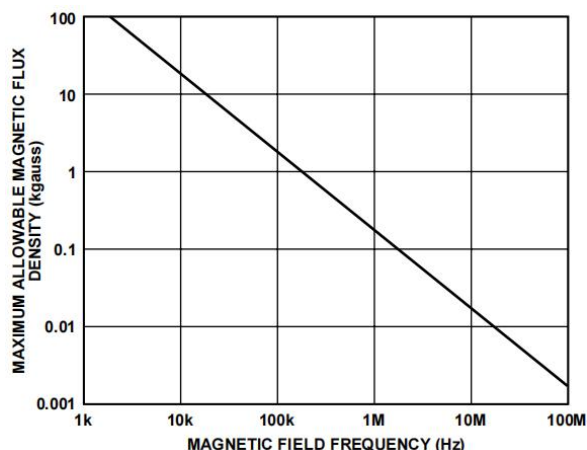


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and had the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

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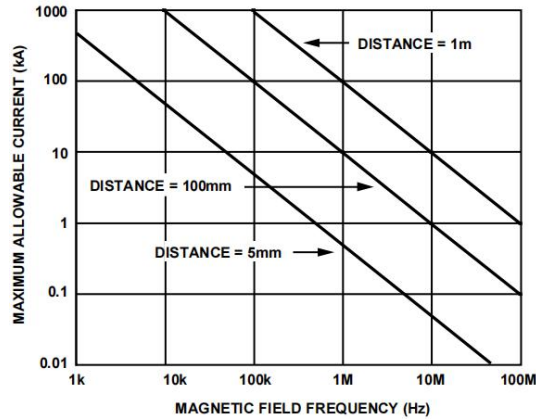


Figure 14. Maximum Allowable Current for Various Current-to-XLADUM3200/XLADUM3201 Spacings

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care must be taken in the layout of such traces to avoid this possibility.

15. POWER CONSUMPTION

The supply current at a given channel of the XLADUM3200/ XLADUM3201 isolator is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5fr$$

$$I_{DDI} = I_{DDI(D)} \times (2f - fr) + I_{DDI(Q)} \quad f > 0.5fr$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5fr$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - fr) + I_{DDO(Q)} \quad f > 0.5fr$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

fr is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 6 provides perchannel input supply currents as a function of data rate.

Figure 7 and Figure 8 provide per-channel output supply currents as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 11 provide total I_{DD1} and I_{DD2} supply current as a function of data rate for XLADUM3200 and XLADUM3201 channel configurations.

16. INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends upon the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the XLADUM3200/XLADUM3201 .

Performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 15 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life.

The insulation lifetime of the XLADUM3200/XLADUM3201 depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 31 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 must be treated as a bipolar ac waveform and the peak voltage must be limited to the 50-year lifetime voltage value listed in Table 15.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

RATED PEAK VOLTAGE

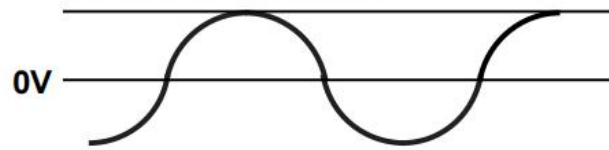


Figure 15. Bipolar AC Waveform

RATED PEAK VOLTAGE

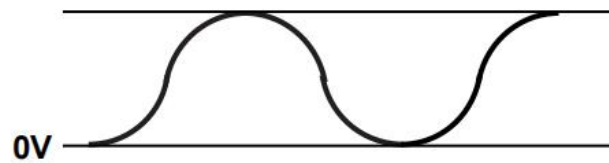


Figure 16. Unipolar AC Waveform

RATED PEAK VOLTAGE

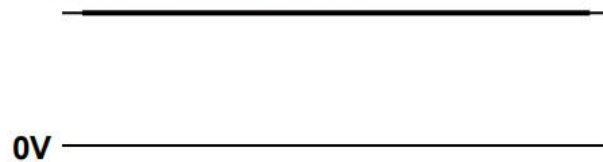


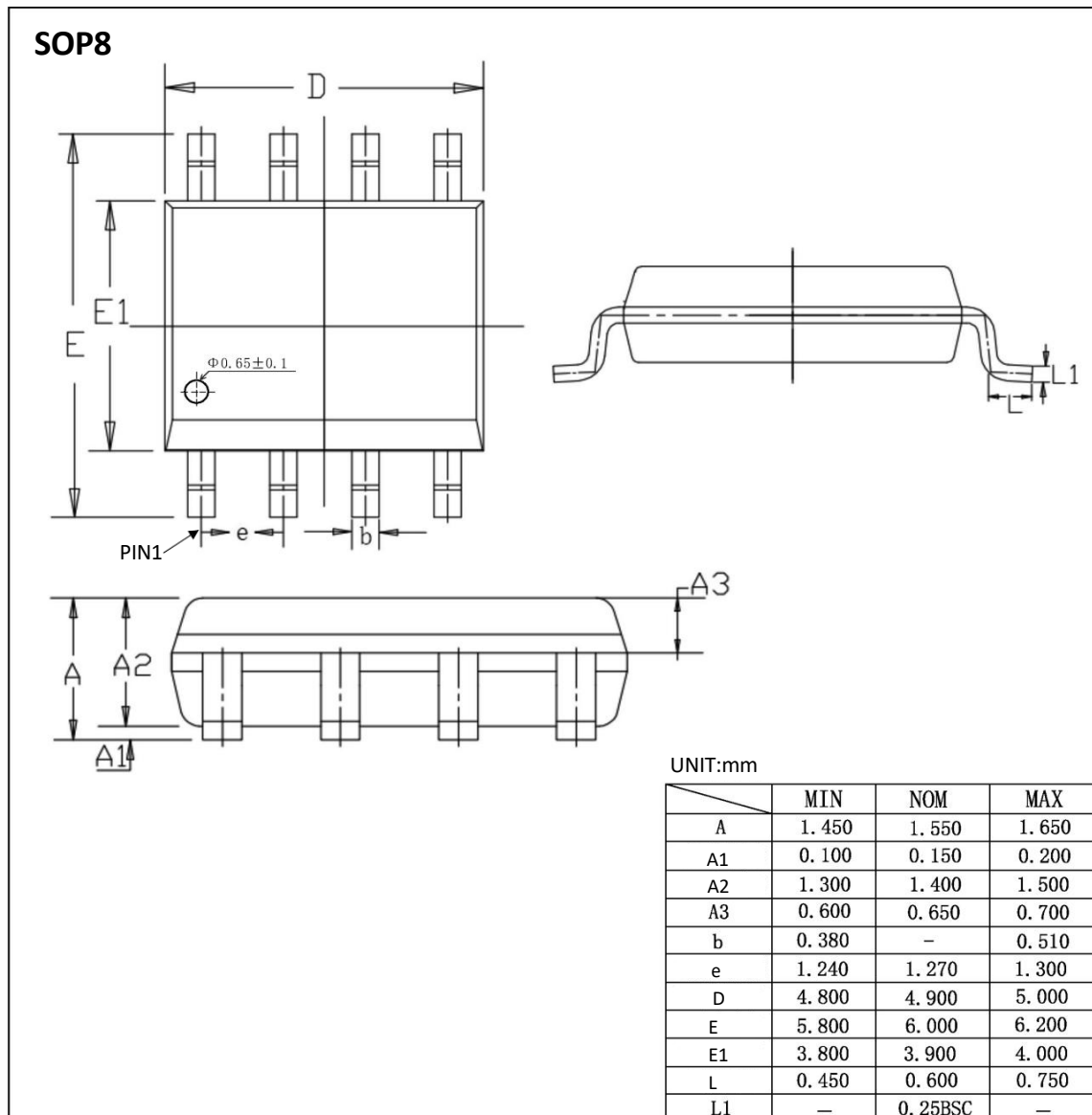
Figure 17. DC Waveform

17. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLADUM3200ARZ-RL7	XL3200A	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM3200BRZ-RL7	XL3200B	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM3200CRZ-RL7	XL3200C	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM3201ARZ-RL7	XL3201A	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM3201BRZ-RL7	XL3201B	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLADUM3201CRZ-RL7	XL3201C	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500

18. DIMENSIONAL DRAWINGS



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