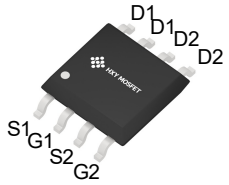
SQ4946CEY-T1_GE3

Dual N-Channel Enhancement Mode MOSFET

Description

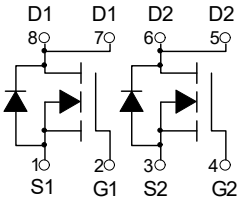
The SQ4946CEY-T1_GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8
(SOIC-8)

General Features

V_{DS} = 60V I_D = 5A
$R_{DS(ON)}$ < 33mΩ @ V_{GS}=10 V
$R_{DS(ON)}$ < 43mΩ @ V_{GS}=4.5V



Dual N-Channel MOSFET

Application

Battery protection

Load switch

Uninterruptible power supply

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SQ4946CEY-T1_GE3	SOP-8	HXY MOSFET	3000

Absolute Maximum Ratings@T_j=25ºC(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 4.5V[3]	5	A
I_D@T_A=100℃	Drain Current, V_{GS} @ 4.5V[3]	3.5	A
I_{DM}	Pulsed Drain Current[1]	20	A
P_D@T_A=25℃	Total Power Dissipation	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	85	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	60	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=60V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1.5	1.57	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[4]	V_{GS}=10V,I_D=4A	---	25	33	mΩ
		V_{GS}=4.5V,I_D=3A	---	33	43	mΩ
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	---	1027	---	pF
C_{oss}	Output Capacitance		---	60	--	
C_{rss}	Reverse Transfer Capacitance		---	45	---	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=30V, I_D=4A, R_{ENG}=3.3Ω,V_{GS}=10V	---	3	---	ns
t_r	Rise Time		---	34	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	23	---	ns
t_f	Fall Time		---	6	---	ns
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=48V, I_D=4A	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	2.6	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	4.1	---	nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_{SD}=1A	---	---	1.2	V
I_S	Continuous Drain Curren	V_D=V_G=0V	---	---	5	A
I_{SM}	Pulsed Drain Current		---	---	20	A
Trr	Reverse Recovery Time	I_F=4A,T_J=25℃ dI/dt=100A/us	---	12.1	---	ns
Qrr	Reverse Recovery Charge		---	6.7	---	nC

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : TJ=25℃,VDD=30V,VG=10V,L=0.1mH
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics

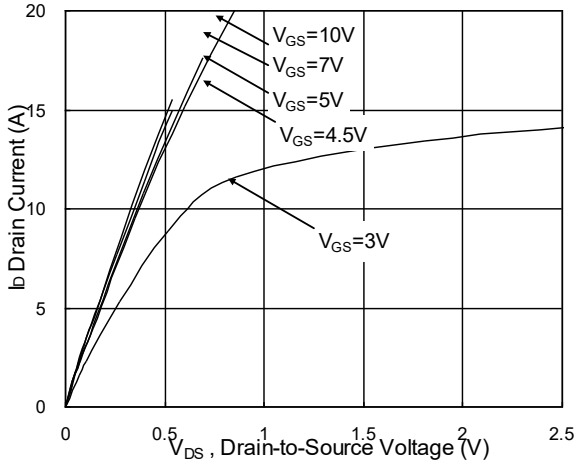


Fig.1 Typical Output Characteristics

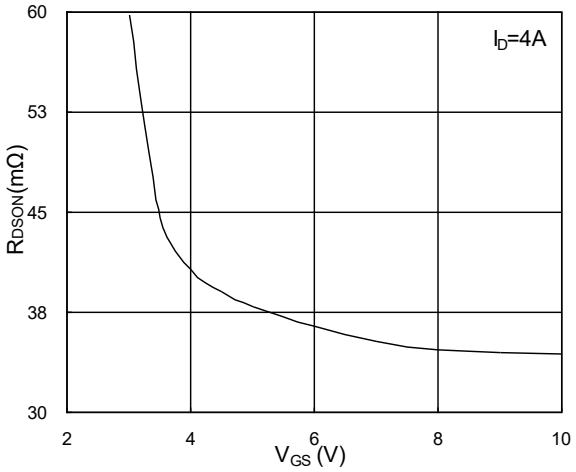


Fig.2 On-Resistance vs. Gate-Source

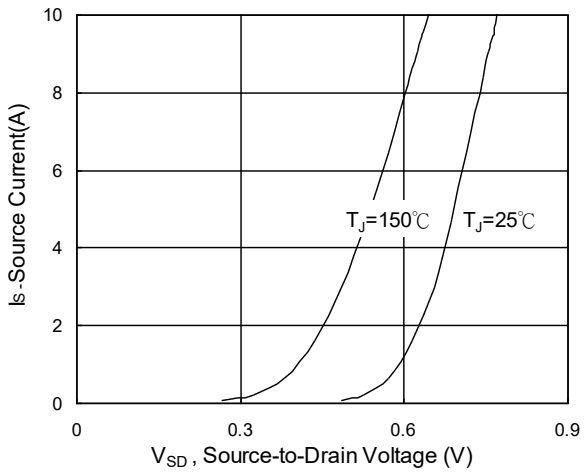


Fig.3 Forward Characteristics Of Reverse

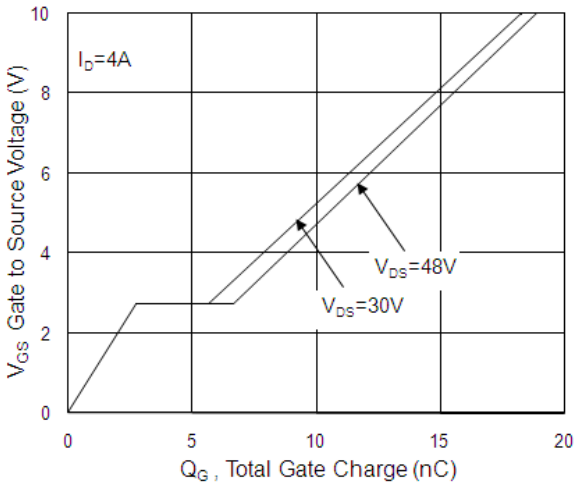


Fig.4 Gate-Charge Characteristics

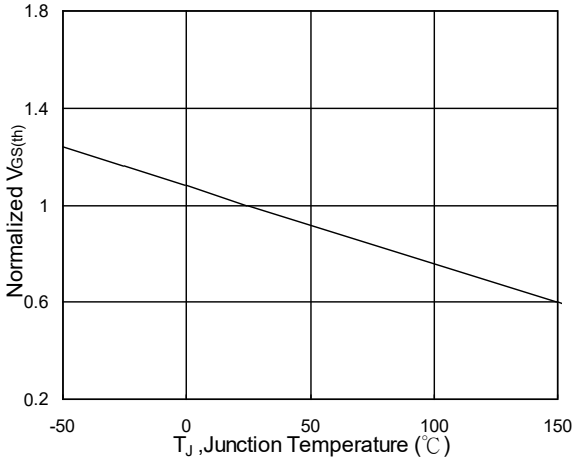


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

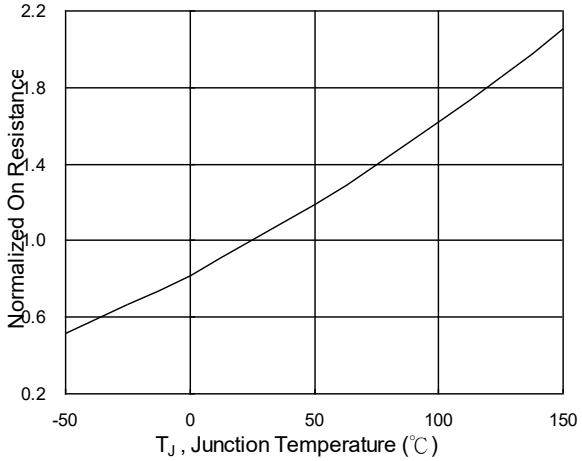


Fig.6 Normalized R_{DSON} vs. T_J

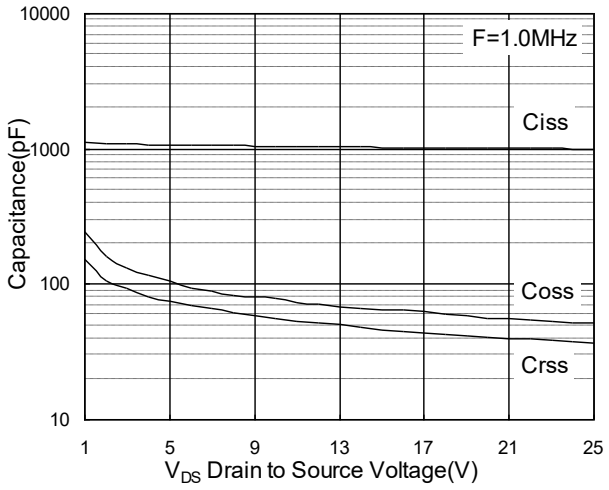


Fig.7 Capacitance

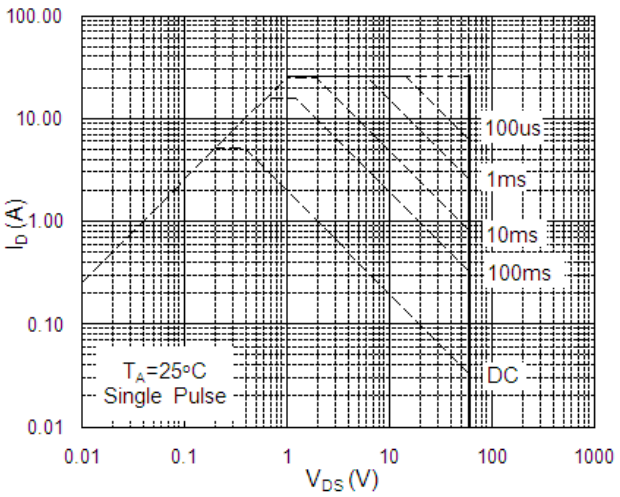


Fig.8 Safe Operating Area

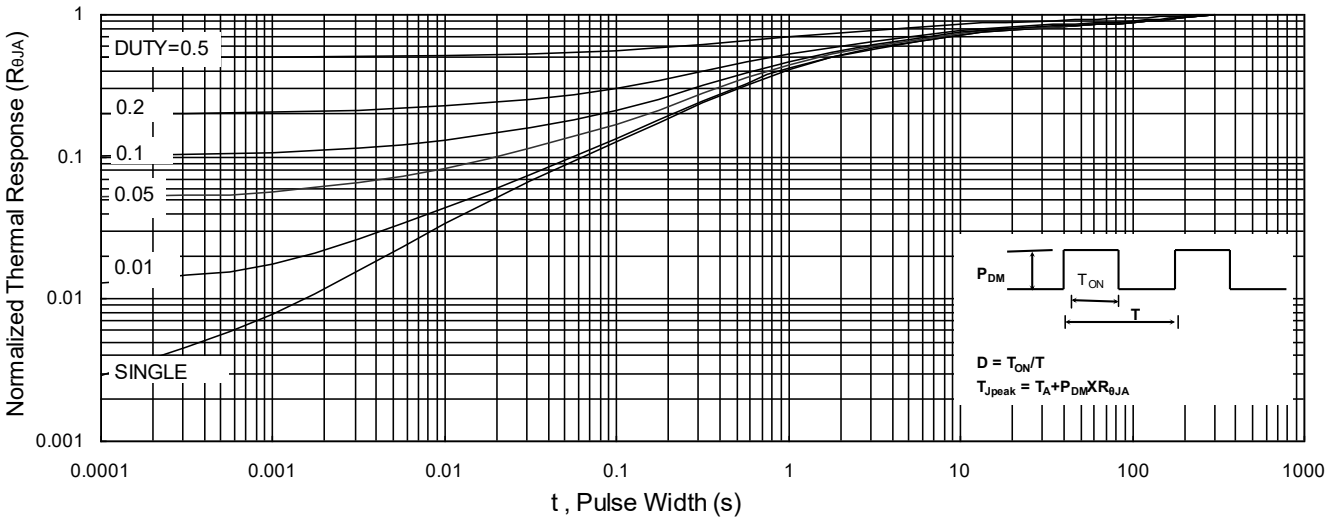


Fig.9 Normalized Maximum Transient Thermal Impedance

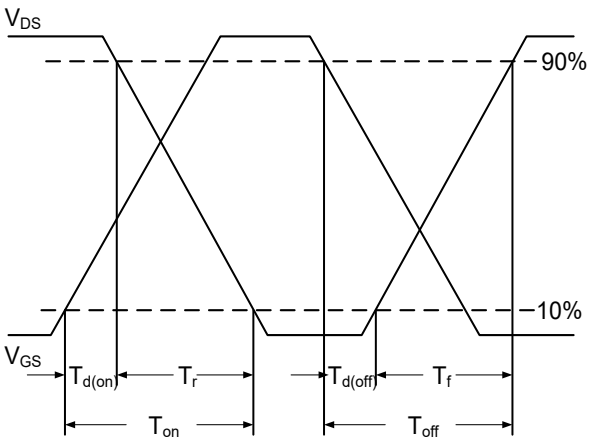


Fig.10 Switching Time Waveform

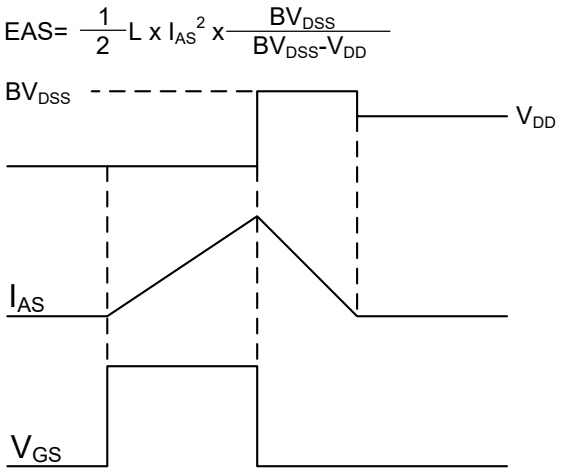
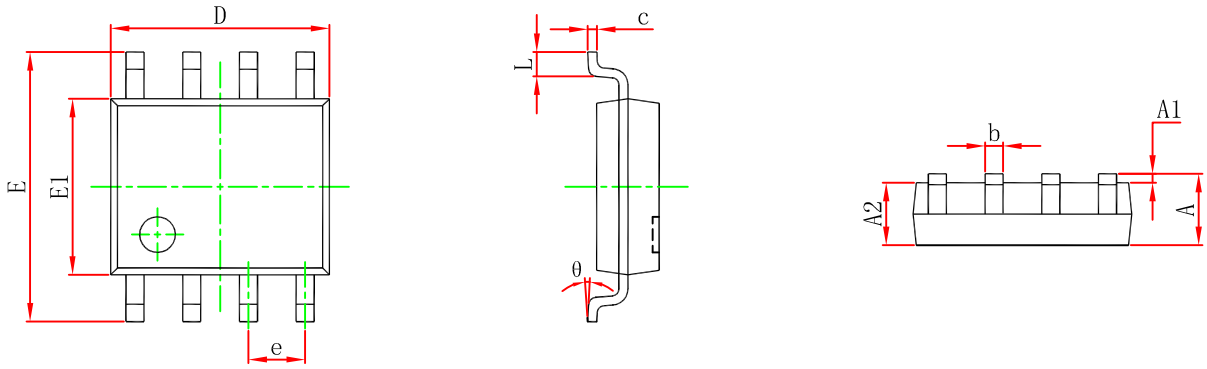
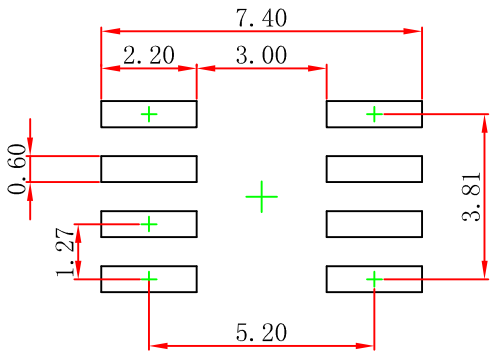


Fig.11 Unclamped Inductive Switching Waveform

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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