1 Description

HT SD NAND Flash is an embedded storage solution for low-power application.The SD NAND consists of the NAND flash and the high-performance controller with the LGA package. 3.3V supply voltage (VCC) is required for the NAND area.The SD NAND Flash is based on an advance 8-pin interface (clock, command, Data*4, power and ground). The SD NAND Flash is fully compliant with SD2.0/SD3.0 interface and operation is similar to SD card.

2 Features

➢ Advance

- Advanced dynamic ECC engine to improve reliability
- Copyrights Protection Mechanism--Complying with highest security of SDMI standard
- Low power consumption, with the standby energy saving management mode automatically
- High-speed Flash Controller inside

➢ Interface

- Support clock frequencies 50MH
- Complies to SD specifications version 2.x/3.x with 1-I/O and 4-I/O
- Supports SPI Mode
- Support UHS-I (SDR50, SDR104, DDR50)

➢ Power Supply and Consumption

- Voltage range: 2.7V ~ 3.6V
- Standby: 100uA (Typical)
- Operating current: 40mA(Typical)

➢ Temperature

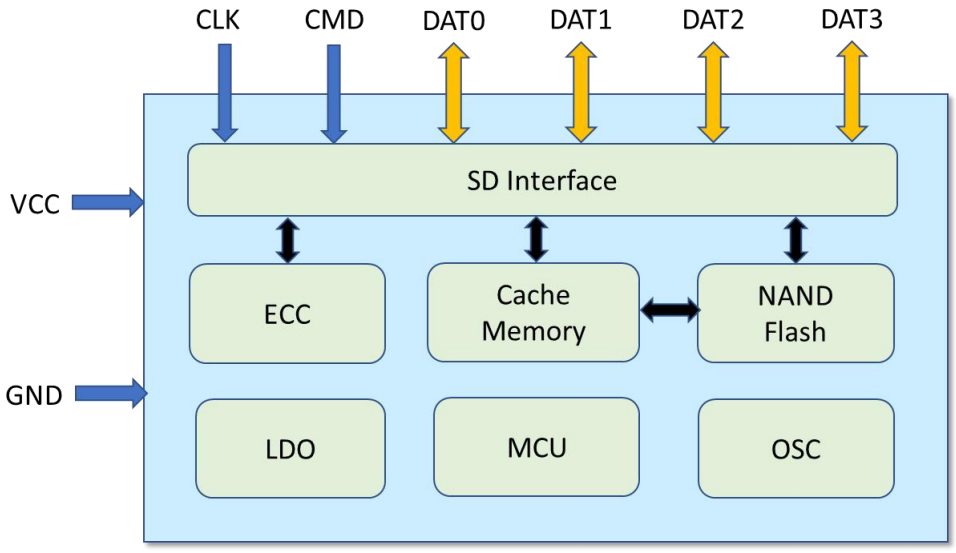
- Operation: -20℃ to 85℃
- Storage: -40℃ to 125℃

➢ Reliability

- P/E cycles with ECC: 3000
- MTBF: 1,000,000hours

Note:The 1Gb-4Gb capacity only supports a clock of 50MHz and is an SD2.0 interface.

3 Block Architecture



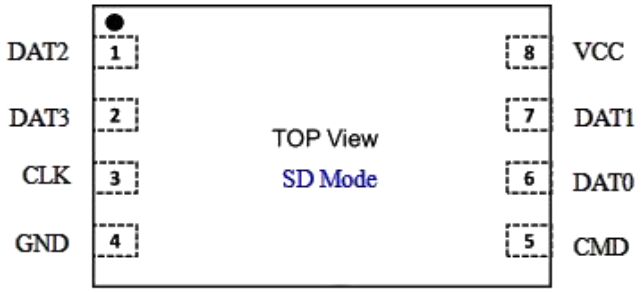
4 Product List

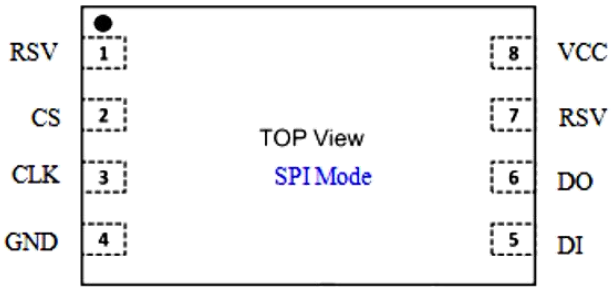
Part Number	Capacity	Sequential Read	Sequential Write	Flash Type	Package
HT5D1G3UPW	1Gb(128MB)	16MB/S	6MB/S	TLC	LGA8-6x8
HT5D2G3UPW	2Gb(256MB)	17MB/S	8MB/S	TLC	LGA8-6x8
HT5D4G3UPW	4Gb(512MB)	18MB/S	8MB/S	TLC	LGA8-6x8
HT5D8G3UPW	8Gb(1GB)	18MB/S	8MB/S	TLC	LGA8-6x8
HT5D16G3UPW	16Gb(2GB)	22MB/S	8MB/S	TLC	LGA8-6x8
HT5D32G3UPW	32Gb(4GB)	40MB/S	10MB/S	TLC	LGA8-6x8
HT5D64G3UPW	64Gb(8GB)	40MB/S	8MB/S	TLC	LGA8-6x8
HT5D128G3UPW	128Gb(16GB)	50MB/S	8MB/S	TLC	LGA8-6x8
HT5D256G3UPW	256Gb(32GB)	60MB/S	8MB/S	TLC	LGA8-6x8
HT5D512G3UPW	512Gb(64GB)	70MB/S	8MB/S	TLC	LGA8-6x8

Note: Different testing environments can lead to differences in read and write speeds.

5 Pin Description

5.1 Device Top View





5.2 Pin Definition

Pin #	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line (bit 2)	RSV	—	Reserved
2	DAT3	I/O/PP	Data Line (bit 3)	CS	I	Chip Select (neg true)
3	CLK	I	Clock	CLK	I	Clock
4	GND	S	Supply Voltage Ground	GND	S	Supply Voltage Ground
5	CMD	PP	Command/Response	DI	I	Data In
6	DAT0	I/O/PP	Data Line (bit 0)	DO	O/PP	Data Out
7	DAT1	I/O/PP	Data Line (bit 1)	RSV	—	Reserved
8	VCC	S	Supply Voltage	VCC	S	Supply Voltage

Note:

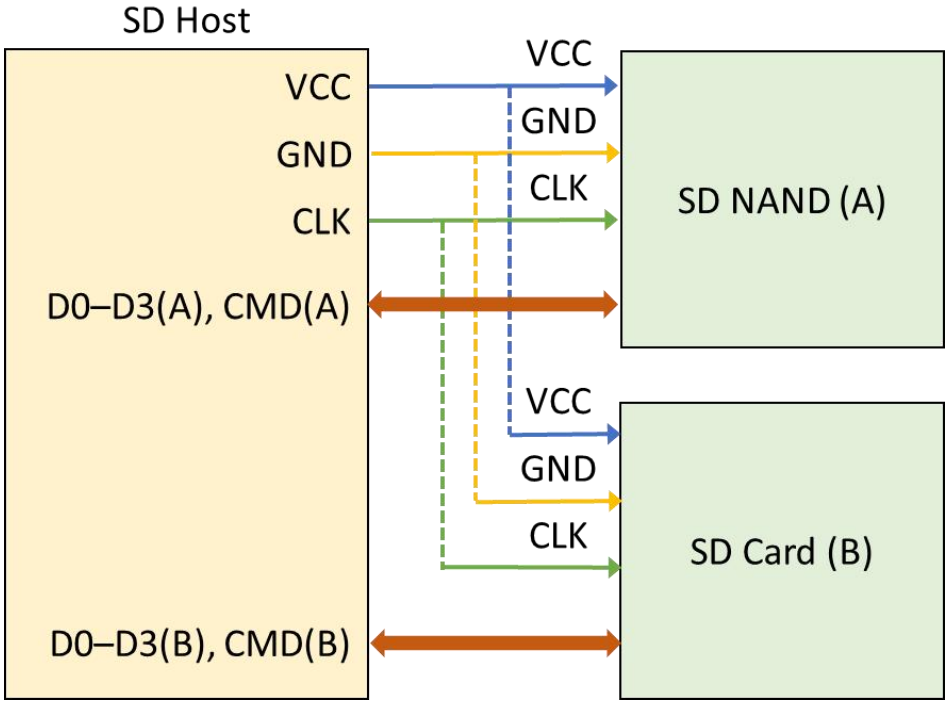
- S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.
- The extended DAT lines(DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to Multimedia Cards.
- After power up this line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT(ACMD42)command.

6 SD Bus Mode Protocol

The SD bus has six communication lines and two supply lines:

- CMD: Command is bi-directional signal.
- DAT0-3: Data lines are bi-directional signals.
- CLK: Host clock signal
- VCC: Power supply.
- GND: Ground

The following figure shows the bus topology with one host in SD Bus mode.



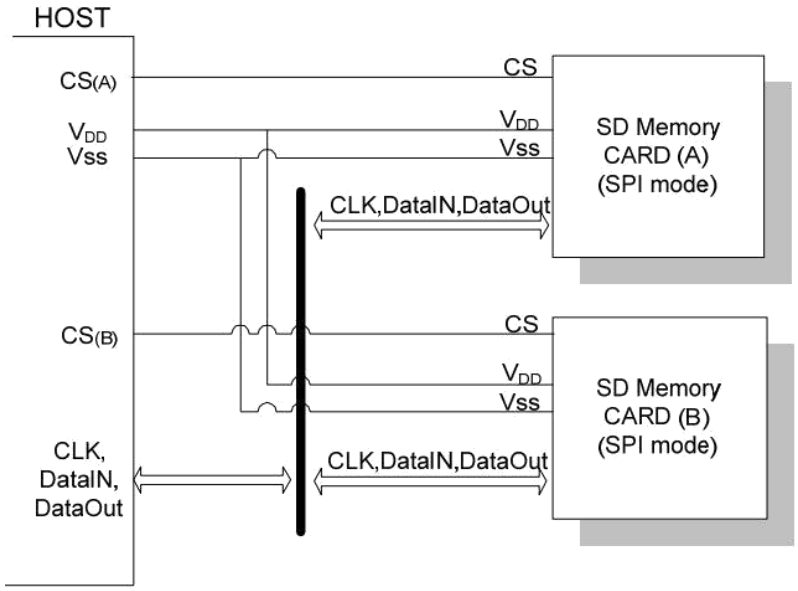
7 SPI Bus Mode Protocol

The SPI mode consists of a secondary communication protocol that is offered by Flash-based SD Memory Cards. This mode is a subset of the SD Memory Card protocol, designed to communicate with a SPI channel, commonly found in Motorola's (and lately a few other vendors') micro controllers. The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.
The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses a subset of the SD Memory Card protocol and command set.

The advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance of the SPI mode versus SD mode (e.g. Single data line and hardware CS signal per card).

The commands and functions in SD mode defined after the Version 2.00 are not supported in SPI mode. The card may respond to the commands and functions even if the card is in SPI mode but host should not use them in SPI mode.

- CS: Chip select signal from host to card.
- CLK: Clock signal from host to card.
- DataIn: Data signal from host to card.
- DataOut: Card to host data signal.



8 Card Initialize

To initialize the SD NAND, follow the following procedure is recommended example.

1).Supply Voltage for initialization

Host System can apply the Operating Voltage from initialization to the card. Apply more than 74 cycles of Dummy-clock to the SD card.

2).Select operation mode (SD mode or SPI mode)

In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to “Low” level. Then, issue CMD0. In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up to “High” normally) Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3).Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.

4).Apply the indicated operating voltage to the card.
Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared. (Bit 31 Busy =1) If response time out occurred, host can recognize not SD Card.

5).Issue the CMD2 and get the Card ID (CID).

6).Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)

7).Issue the CMD7 and move to the transfer state.
If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.

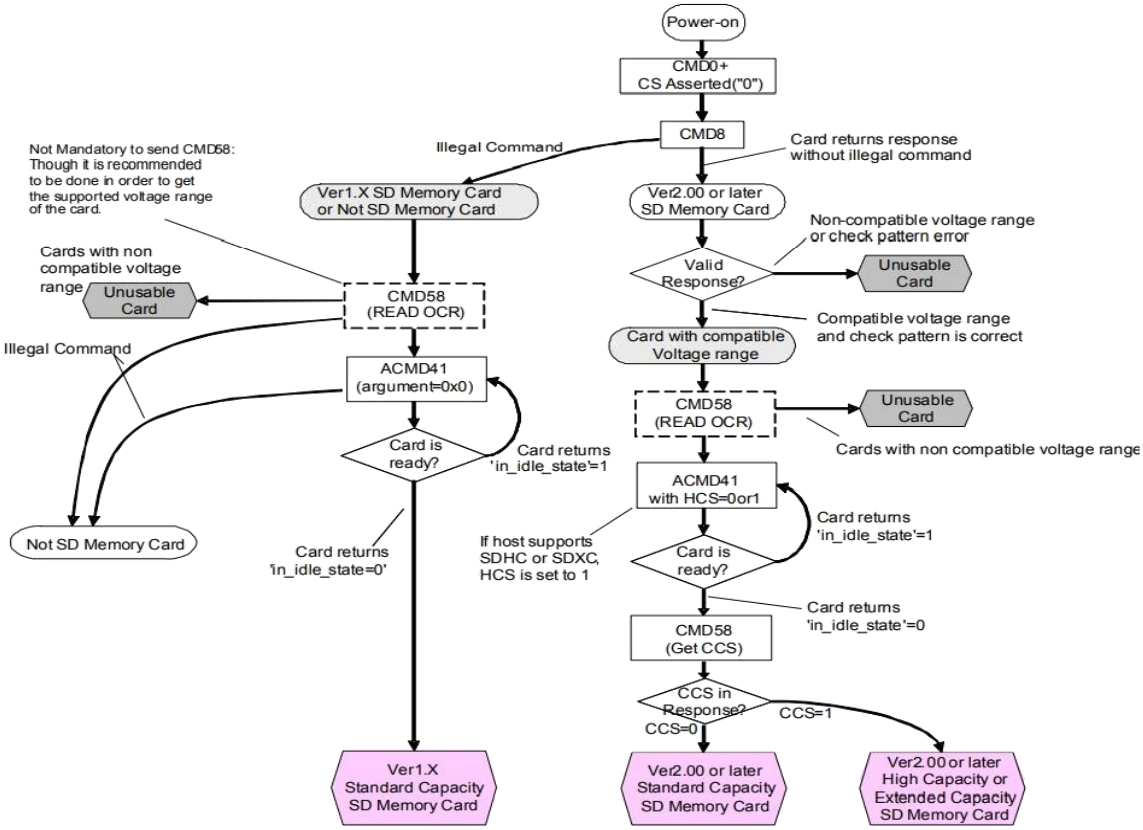
8).Issue the ACMD13 and poll the Card status as SD Memory Card.Check SD_CARD_TYPE value. If significant 8 bits are “all zero”, that means SD Card. If it is not, stop initialization.

9).Issue CMD7 and move to standby state. Issue CMD9 and get CSD. Issue CMD10 and get CID.

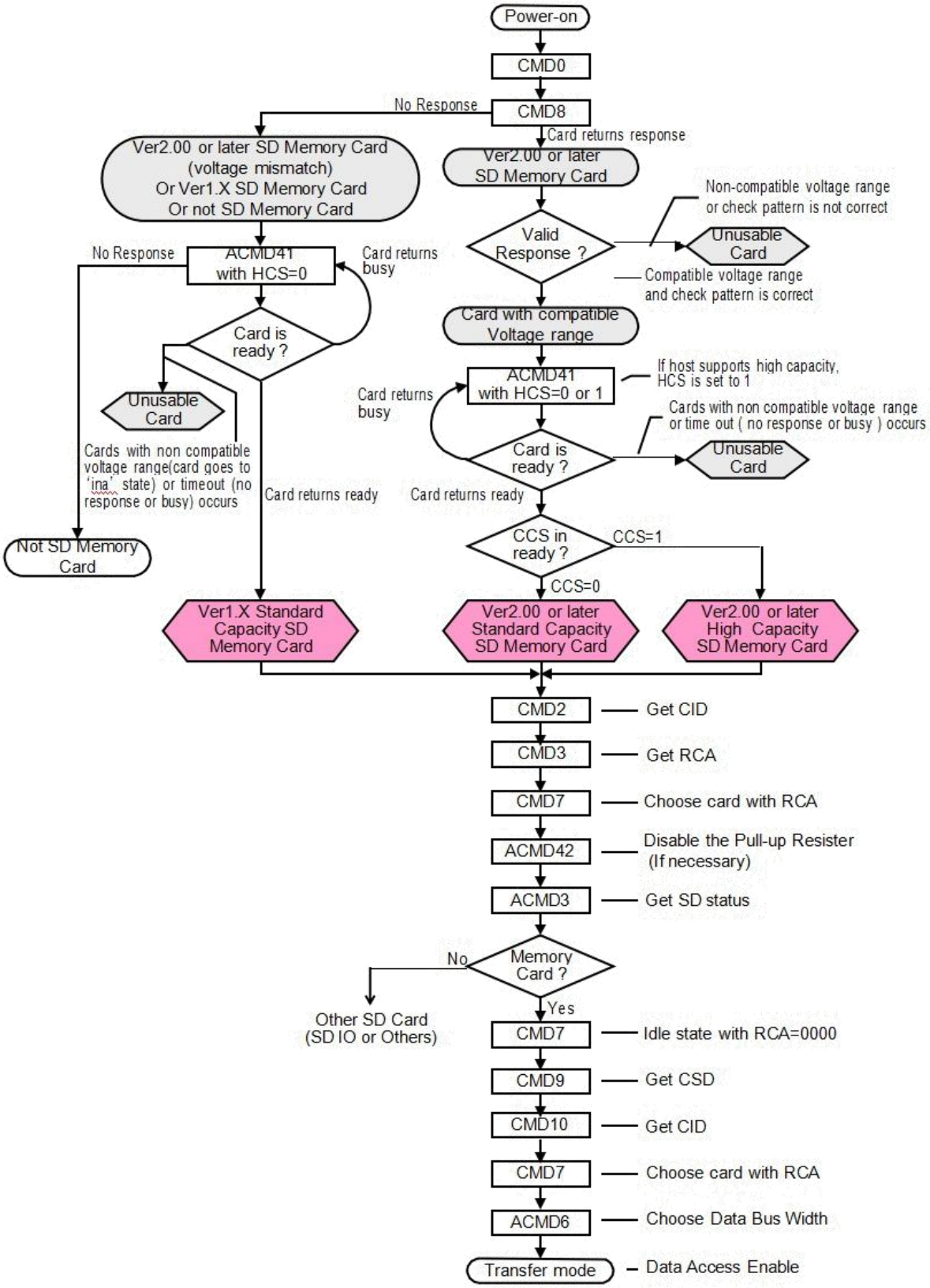
10).Back to the Transfer state with CMD7.

11).Issue ACMD6 and choose the appropriate bus-width.

Then the Host can access the Data between the SD card as a storage device.



SPI Mode Initialization Flow



Normal SD initial flow

9 Function Description

The sector size of the SD NAND Flash is 512-byte which is the same as that in an IDE magnetic disk drive. To write or read a sectors, the host computer software simply issues a Read or Write command to the SD NAND Flash.

9.1 ECC

HT SD NAND Flash provides the internal ECC which can protect user data without other controlling sequence. ECC could use the spare area in NAND FLASH memory and the occupied size is determined by the+ECC protected abilities. The ECC default setting is enabled after device power up.

9.2 Bad Block Manage

The device occasionally contains bad blocks. Please read one word of first page of first spare in each block. HT makes sure that every invalid block has data at this word. If the data of the word is “0”, define the block as a bad block.

9.3 Automatic Sleep Mode

HT SD NAND Flash provides automatic entrance and exit from sleep mode. If no further commands are received within 5msec, chip would enter sleep mode. The host does not have to take any action for this to occur. HT SD NAND Flash provide ultra-low power consumption during sleep mode (around 100uA) and suitable for IoT application.

9.4 Wear Leveling

Wear-leveling is an intrinsic part of the Erase Pooling functionality of SD using NAND memory. The Wear Level command is supported as a NOP operation to maintain backward compatibility with existing software utilities.

10 Registers

Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/ content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.

Register	Width	Comment
OCR	32	Operation Conditions Register
CID	128	Card IDentification
CSD	128	Card-Specific Data
RCA	16	Relative Card Address
DSR	16	Driver Stage Register
SCR	64	SD CARD Configuration Register
SD Status	512	Status Bits and Card Features

10.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile. Additionally, this register includes status information bits. One status bit is set if the power up procedure has been finished. This register includes another status bit indicating the capacity status after set power up status bit.

Bit Position	OCR Fields Definition	Bit Position	OCR Fields Definition
0-3	Reserved	16	2.8 ~ 2.9
4	Reserved	17	2.9 ~ 3.0
5	Reserved	18	3.0 ~ 3.1
6	Reserved	19	3.1 ~ 3.2
7	Reserved for low voltage range	20	3.2 ~ 3.3
8	Reserved	21	3.3 ~ 3.4
9	Reserved	22	3.4 ~ 3.5
10	Reserved	23	3.5 ~ 3.6
11	Reserved	24(1)	Switching to 1.8V Accepted (S18A)
12	Reserved	25-29	Reserved
13	Reserved	30	Card Capacity Status (CCS)(2)
14	Reserved	31	Card power up status bit (busy)(3)
15	2.7 ~ 2.8		

(1) Only UHS-I card supports this bit.

(2) This bit is valid only when the card power up status bit is set.

(3) This bit is set to LOW if the card has not finished the power up routine.

10.2 CID Register

The CID register is 16 bytes long and contains a unique identification number as shown in below table.

Name	Width	CID Slice	Comment
Manufacture ID (MID)	8	[127:120]	The manufacturer IDs are controlled and assigned by the SD Card Association.
OEM/Application ID (OID)	16	[119:104]	Identifies the card OEM and/or the card contents. The OID is assigned by the 3C.*
Product Name (PNM)	40	[103: 64]	5 ASCII characters long
Product Revision (PRV)	8	[63:56]	Two binary coded decimal digits
Serial Number (PSN)	32	[55:24]	32 Bits unsigned integer
Reserved	4	[23:20]	
Manufacture Data Code (MDT)	12	[19:8]	Manufacture date–yym (offset from 2000)
CRC7 checksum (CRC)	7	[7:1]	Calculated
Not used, always 1	1	[0:0]	

10.3 CSD Register

The Card-Specific Data register provides information regarding access to the device contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The types of the entries in the table below are coded as follows: R = readable, W(1) = writable once, W = multiple writable.

Field	Width	Value	Type	CSD-slice
CSD_STRUCTURE	2	00b	R	[127:126]
-	6	00 0000b	R	[125:120]
TAAC	8	xxh	R	[119:112]
NSAC	8	xxh	R	[111:104]
TRAN_SPEED	8	32h or 5Ah	R	[103:96]
CCC	12	01x110110101b	R	[95:84]
READ_BL_LEN	4	xh	R	[83:80]
READ_BL_PARTIAL	1	1b	R	[79:79]
WRITE_BLK_MISALIGN	1	xb	R	[78:78]
READ_BLK_MISALIGN	1	xb	R	[77:77]
DSR_IMP	1	xb	R	[76:76]
-	2	00b	R	[75:74]
C_SIZE	12	xxxh	R	[73:62]
VDD_R_CURR_MIN	3	xxxb	R	[61:59]
VDD_R_CURR_MAX	3	xxxb	R	[58:56]
VDD_W_CURR_MIN	3	xxxb	R	[55:53]
VDD_W_CURR_MAX	3	xxxb	R	[52:50]
C_SIZE_MULT	3	xxxb	R	[49:47]
ERASE_BLK_EN	1	xb	R	[46:46]
SECTOR_SIZE	7	xxxxxxxb	R	[45:39]
WP_GRP_SIZE	7	xxxxxxxb	R	[38:32]
WP_GRP_ENABLE	1	xb	R	[31:31]
-	2	00b	R	[30:29]
R2W_FACTOR	3	xxxb	R	[28:26]
WRITE_BL_LEN	4	xxxxb	R	[25:22]
WRITE_BL_PARTIAL	1	xb	R	[21:21]
-	5	00000b	R	[20:16]
FILE_FORMAT_GRP	1	xb	R/W(1)	[15:15]
COPY	1	xb	R/W(1)	[14:14]
PERM_WRITE_PROTECT	1	xb	R/W(1)	[13:13]
TMP_WRITE_PROTECT	1	xb	R/W	[12:12]
FILE_FORMAT	2	xxb	R/W(1)	[11:10]
-	2	00b	R/W	[9:8]
CRC	7	xxxxxxxb	R/W	[7:1]
-	1	1b	-	[0:0]

10.4 RCA Register

The writable 16-bit relative card address register carries the device address that is published by the device during the identification. This address is used for the addressed host-device communication after the identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7

10.5 DSR Register

The 16-bit driver stage register can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

10.6 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Memory Device's special features that were configured into the given device. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Device manufacturer. The following table describes the SCR register content

Field	Width	Type	CSD-slice
SCR_STRUCTURE	4	R	[63:60]
SD_SPEC	4	R	[59:56]
DATA_STAT_AFTER_ERASE	1	R	[55:55]
SD_SECURITY	3	R	[54:52]
SD_BUS_WIDTHS	4	R	[51:48]
SD_SPEC3	1	R	[47]
-	13		[46:34]
CMD_SUPPORT	14	R	[33:32]
-	32	R	[31:0]

11 Electronic characteristic

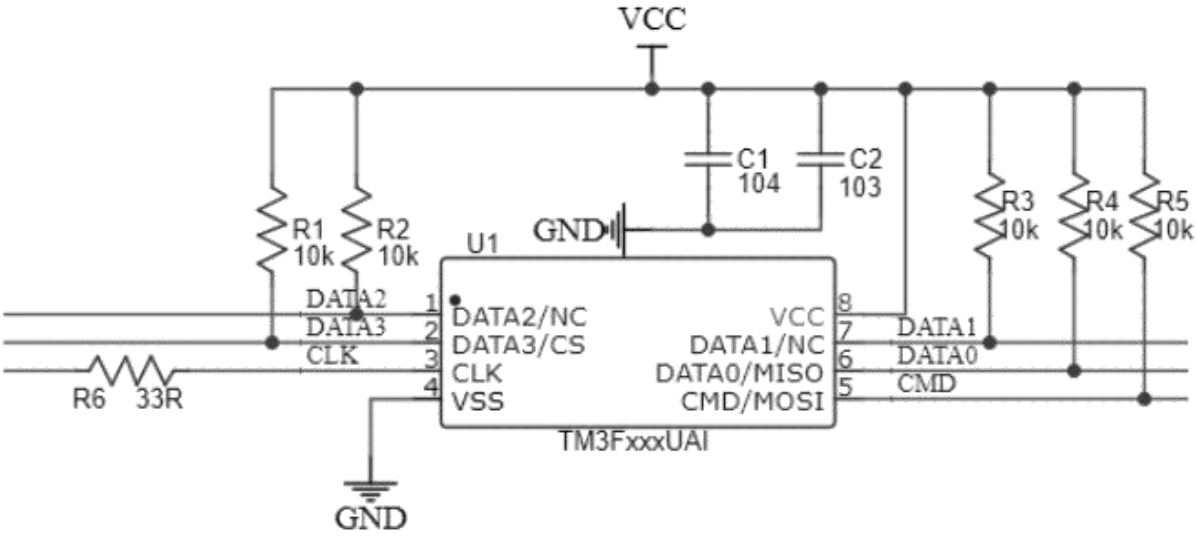
11.1 Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-40°C ~ 125°C
Ambient Operation Temperature	-20°C ~ 85°C
Applied Input/Output Voltage	0V ~ VCC*1.1

11.2 DC Characteristics

Parameters	Min	Typical	Max	UNIT
Supply Voltage (VCC)	2.7	3.3	3.6	V
Input Leakage Current	---	---	5	uA
Output Leakage Current	---	---	5	uA
Operation Current (Read 50MHz)(32Gb)	---	30	---	mA
Operation Current (Write 50MHz)(32Gb)	---	30	---	mA
Standby Current	---	100	---	uA

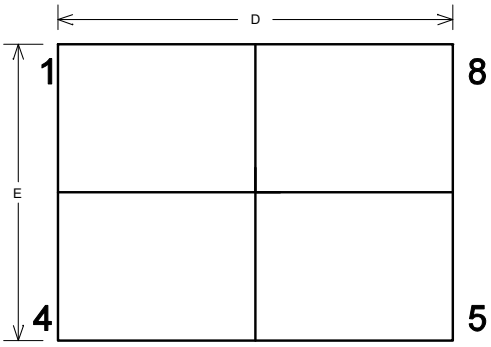
12 Reference Design



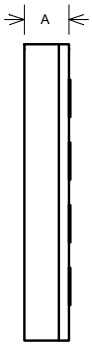
Note：
R_{DAT} and R_{CMD}(10K~100kΩ) are pull-up resistors protecting the CMD and the DAT lines against bus floating when SD NAND is in a high-impedance mode.
The host shall pull-up all DAT0-3 lines by R_{DAT}, even if the host uses the SD NAND as 1-bit mode only in SD mode. It is recommended to have 2.2uF capacitance on VCC.
R_{CLK} reference 0~120 Ω.

13 Package

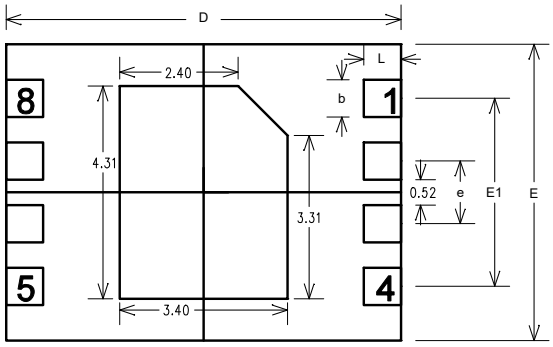
LGA8-6x8



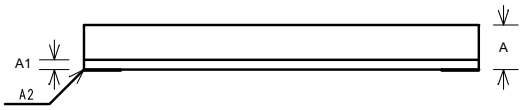
Top View



Side View



Bottom View



Dimensions

Item	D	E	E1	A	A1	A2	b	L	e
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm
Spec	8.10 (8.00) 7.90	6.10 (6.00) 5.90	3.91 (3.81) 3.71	0.95 (0.90) 0.85	0.22 (0.20) 0.18	0.05 (0.02) 0.00	0.80 (0.75) 0.70	0.80 (0.75) 0.70	1.27BSC

The PAD under the chip can be connected to ground.