HT5F1G1UPI

SPI NAND FLASH MEMORY DATASHEET

1 SPI NAND Flash Memory

1.1 FEATURE

1G-bit SPI NAND FLASH

- Page size : 2112 bytes
- Block size : 64 pages
- Device size: 1024 blocks

Advanced security Features

- 16K-Byte OTP Region

Standard, Dual, Quad SPI

- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3

High Speed Clock Frequency

- Quad I/O data transfer reaches 320 Mbits/s
- 2048/64/16 Wrap read operation mode

Program/Erase/Read time

- Page read time: 150us typical(without ECC)
- Page sequential read time: 65us typical(without ECC)
- Page program time: 400us typical(without ECC)
- Block erase time: 3ms typical

Software/Hardware Write Protection

- Write protect all/portion of memory via software
- Register protection with WP# Pin

Enhanced access performance

- 2112 bytes cache

Internal ECC

- 8bits / 512byte

Extended enhancements

- After power-on reset, the data in block 0 and page 0 is automatically loaded into the cache

Superior electrical performance

- Power supply range: 2.7~3.6V
- Operating current<30mA
- Standby current<100uA

Industrial grade standard

- Operating temperature：-40℃~85℃
- Storage temperature：-65℃~150℃

2 SPI NAND Basic characteristics

2.1 CONNECTION DIAGRAM

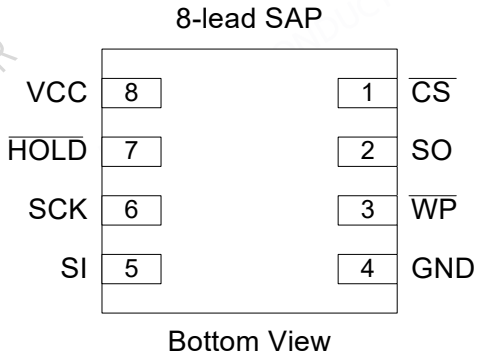


Figure 2-1. Connect Diagram

2.2 PIN DESCRIPTION

Table 2-1 SPI Flash Memory PIN DESCRIPTION

Pin Name	I/O	Description
CS#	I	Chip Select input, active low
SO/SIO1	I/O	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	I/O	Write Protect, active low / Serial Data Input Output 2
VSS	Ground	Ground
SI/SIO0	I/O	Serial Data Input / Serial Data Input Output 0
SCLK	I	Serial Clock input
HOLD#/SIO3	I/O	Hold Input/Serial Data Input Output 3
VCC	Supply	Power Supply

2.3 BLOCK DIAGRAM

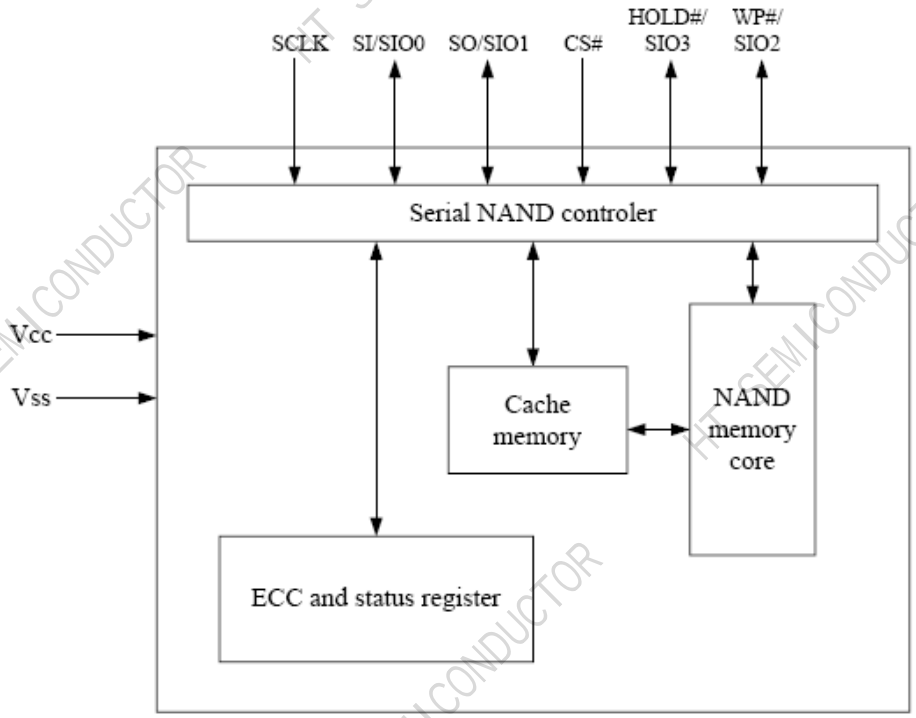


Figure 2-2 SPI NAND Flash Memory BLOCK DIAGRAM

2.4 Storage Array Organization

Table 2-2 SPI NAND Flash Storage Array Organization

capacity	Page organization	Block organization	memory chip
1Gb	2112Bytes	64pages	1024 Blocks

2.5 MEMORY MAPPING

Figure 2-3 shows a schematic diagram of the address mapping structure of a Flash memory with 64 pages per block, and Figure 2-4 shows a schematic diagram of the address mapping structure of a Flash memory with 128 pages per block.

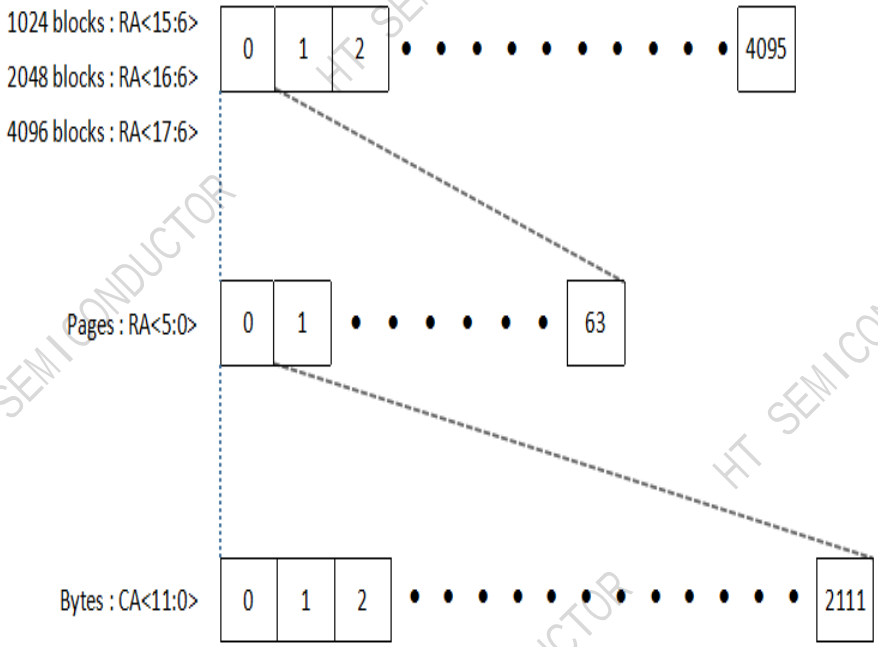


Figure 2-3 SPI NAND Flash(64 pages) MEMORY MAPPING

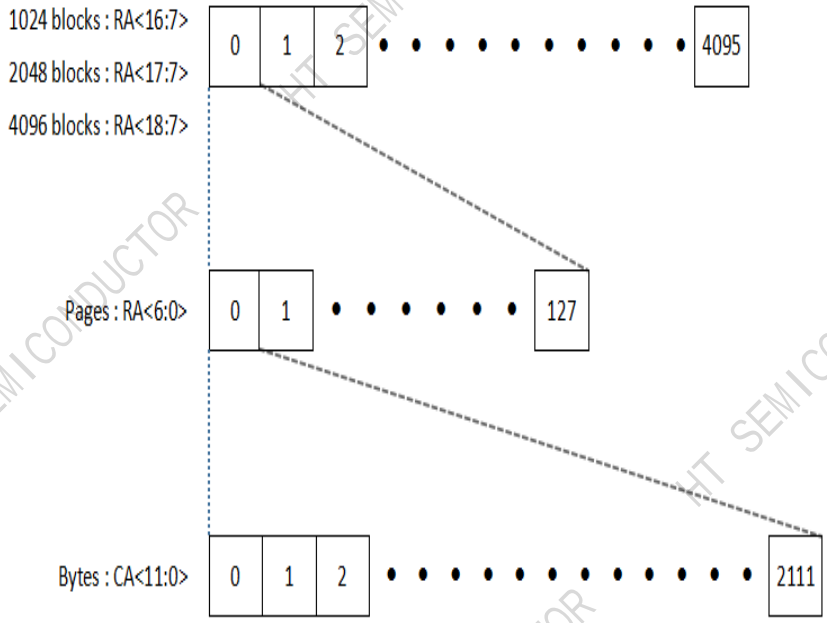


Figure 2-4 SPI NAND Flash(128 pages) MEMORY MAPPING

Note:

CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

3 SPI NAND DEVICE OPERATION

3.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 （Mode 0）
- CPOL = 1, CPHA = 1 （Mode 3）

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. See Figure 3-1 for more details.

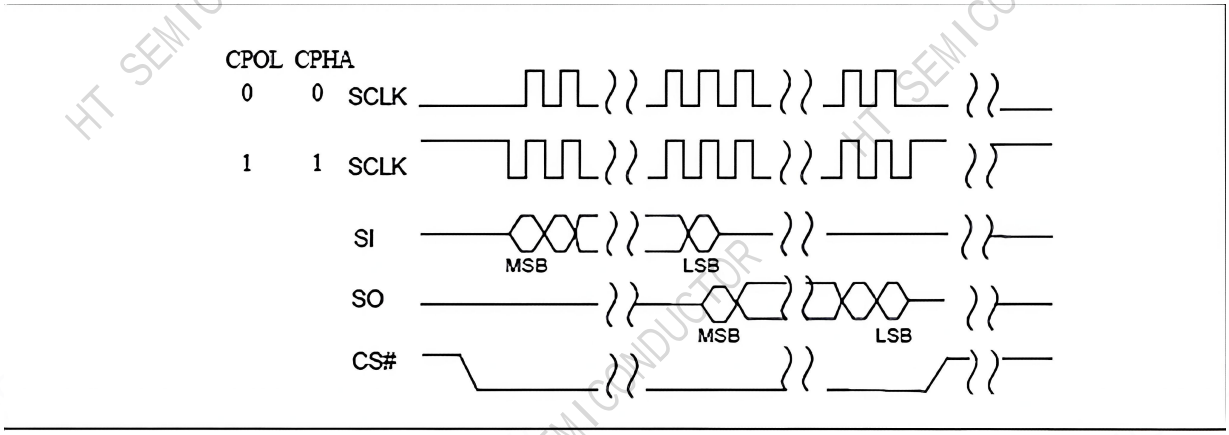


Figure 3-1 SPI Modes Sequence Diagram

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

3.2 HOLD Mode

- The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of reading, programming, or erasing in progress.
- The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low).
- The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).
- The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

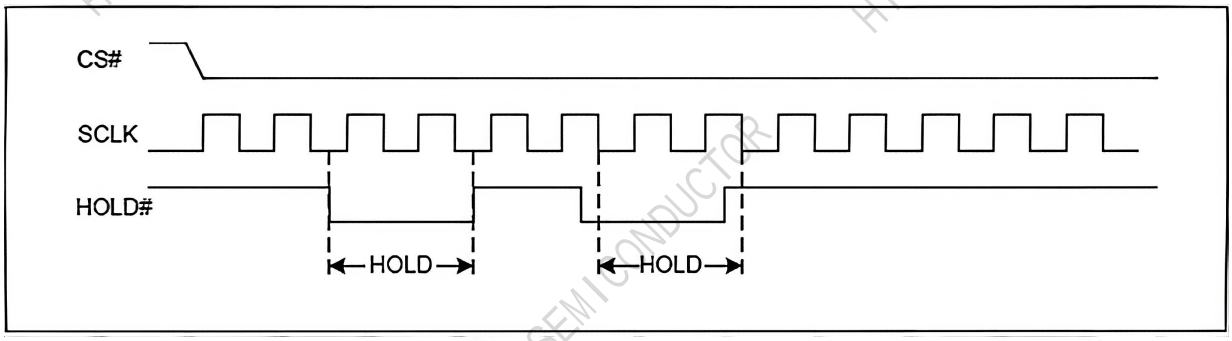


Figure 3-2 HOLD condition

3.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being over written. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered. To enable the Write Protection, the Quad Enable bit (QE) of feature (B0[0]) must be set to 0. See Block Area Protection for details.

4 SPI NAND COMMANDS DESCRIPTION

Table 4-1 commands Set

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	ByteN
Write Enable	06H					
Write Disable	04H					
Get Features	0FH	A7-A0	(D7-D0)			Wrap
Set Feature	1FH	A7-A0	(D7-D0)	Dummy		
Page Read(to cache)	13H	A23-A16	A15-A8	A7-A0		
Read form Cahe	03H/0BH	A15-A8	A7-A0	dummy	(D7-D0)	Wrap
Read form Cahe x 2	3BH	A15-A8	A7-A0	dummy	(D7-D0)x2	Wrap
Read form Cahe x 4	6BH	A15-A8	A7-A0	dummy	(D7-D0)x4	Wrap
Read form Cahe Dual IO	BBH	A15-A0	dummy	(D7-D0)x2		Wrap
Read form Cahe Quad IO	EBH	A15-A0	(D7-D0)x4			Wrap
Read ID	9FH	A7-A0	MID	DID		Wrap
Program Load	02H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load x 4	32H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load random data	84H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load random data x 4	C4H/34H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Load random data Quad IO	72H	A15-A0	(D7-D0)x4	Next byte		Byte N
Block Erase	D8H	A23-A16	A15-A8	A7-A0		
Reset	FFH					

5 SPI NAND COMMAND OPERATIONS

5.1 RESET OPERATION – Reset (FFH)

The RESET (FFH) command stops programming, reading, and erasing operations. The RESET (FFH) command sets the OIP bit to 1 during execution. Use the GET FEATURE (0FH) command to query the OIP bit. If OIP=0, the reset is complete, and the user can then continue to access the SPI NAND FLASH. The RESET (FFH) command will clear P_FAIL/E_FAIL/WEL/ECCS1/ECCS0 after it is received.

(Optional function) After receiving the RESET (FFH) command, it will automatically load the data of block 0 and page 0 into the cache, and ECCS1 and ECCS0 will reflect the BCH error correction results.

The specific command set and command sequence are as follows:

- FFH (RESET)
- 0FH (GET FEATURE)

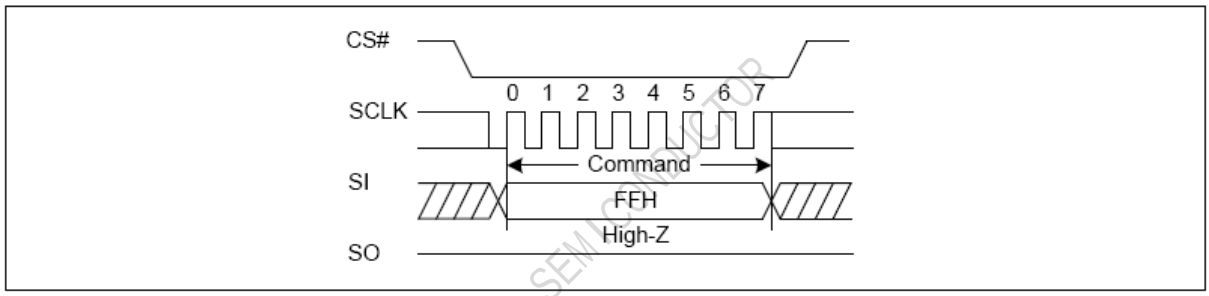


Figure 5-1 Reset Sequence Diagram

Note:

1. It is recommended that users use the RESET (FFH) command + GET FEATURE (0FH) command after powering on the SPI NAND FLASH to confirm that the system power-on initialization is complete (block 0 and page 0 are loaded, and internal initialization is complete). Otherwise, premature command access may lead to unexpected results. If the RESET (FFH) command is not used during power-on, then at least 5ms should be waited before performing other command operations.
2. It is recommended that users use the RESET (FFH) command followed by the GET FEATURE (0FH) command to confirm that the interrupt operation is complete (OIP=0) and that block 0 page 0 has been loaded. Ignoring the OIP status and performing other command operations will lead to unexpected results.

5.2 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device, the READ ID command outputs the Manufacturer ID and the device ID. See Table 5-1 and Figure 5-2 for details.

Table 5-1 READ ID Table

Address	Value	Description
00H	19	MID
01H	03	DID

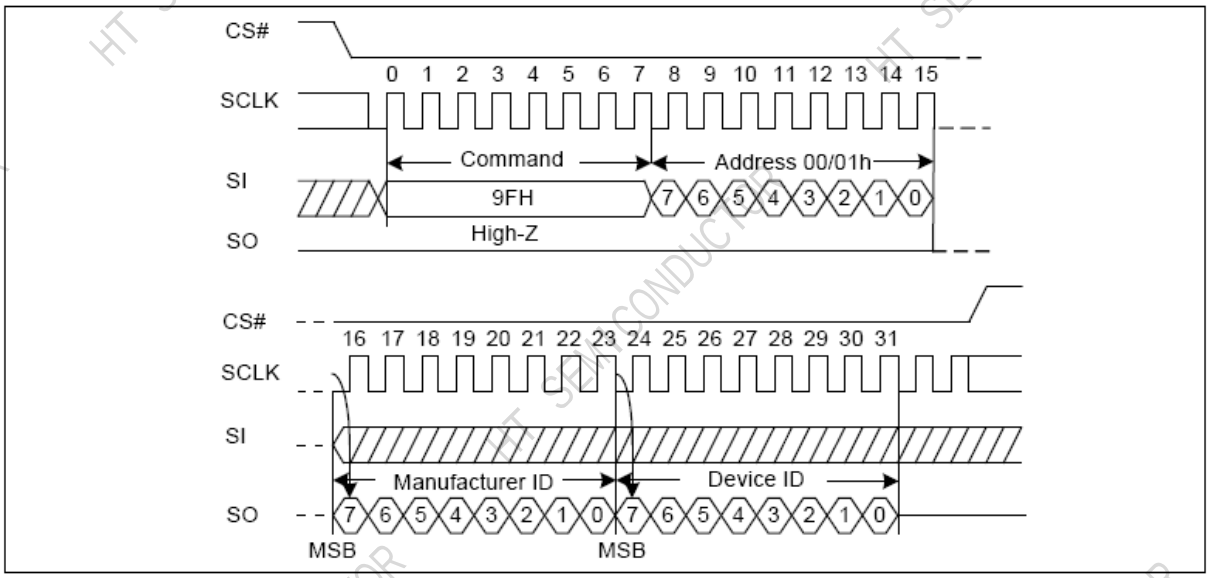


Figure 5-2 Read ID Sequence Diagram

5.3 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

Note:

1. After executing the above command, WEL will be cleared automatically.
2. The WEL bit can be cleared after a reset command.

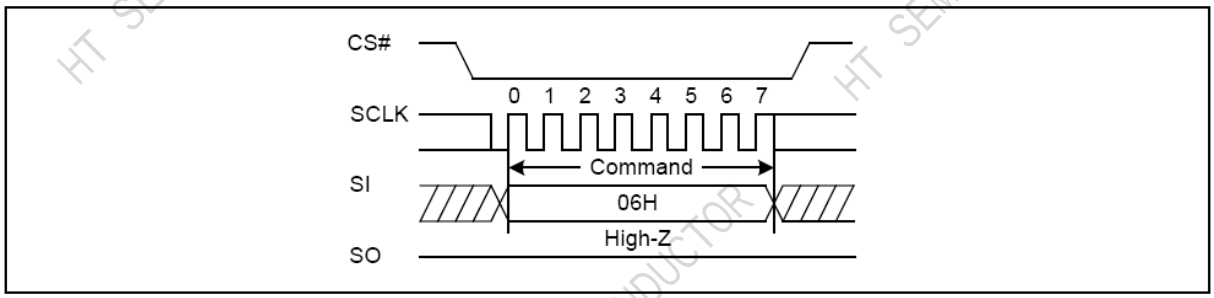


Figure 5-3 Write Enable Sequence Diagram

5.4 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit.

Note:

The WEL bit can be cleared after a reset command.

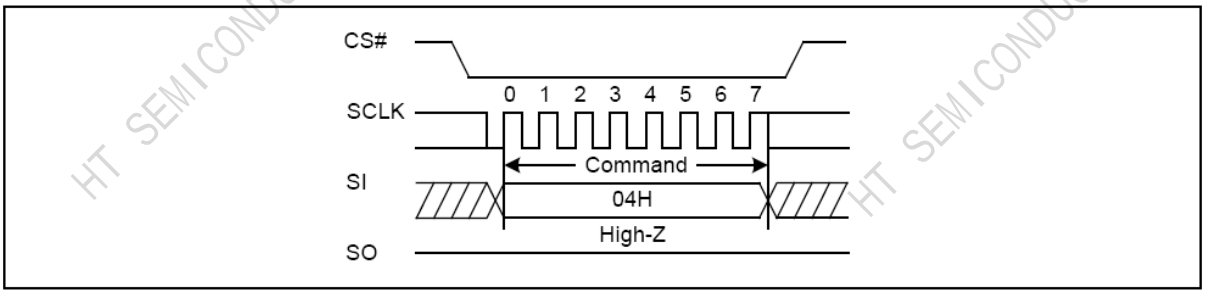


Figure 5-4 Write Disable Sequence Diagram

5.5 Get Features (0FH) and Set Features (1FH)

- The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to monitor the device status and alter the device behavior.
- The addressing registers for the GET FEATURES (0FH) and SET FEATURES (1FH) commands are shown in Table 5-5.
- Except for OTP_PRT, which is a non-volatile bit, all other bits are volatile bits (the value of the non-volatile bit will not change due to power failure).
- All registers will have default values after power-on (except for non- volatile bit).
- After the RESET (FF) command is executed, P_FAIL, E_FAIL, and WEL will be cleared to 0, while the other register bits will remain unaffected.
- All reserved bits return a value of 0 (even if they are set).

Table 5-5 Features Settings

Register	**Addr.**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Protection	A0H	BRWD	reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	reserved	ECC_EN	reserved	reserved	reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FALL	E_FALL	WEL	OIP

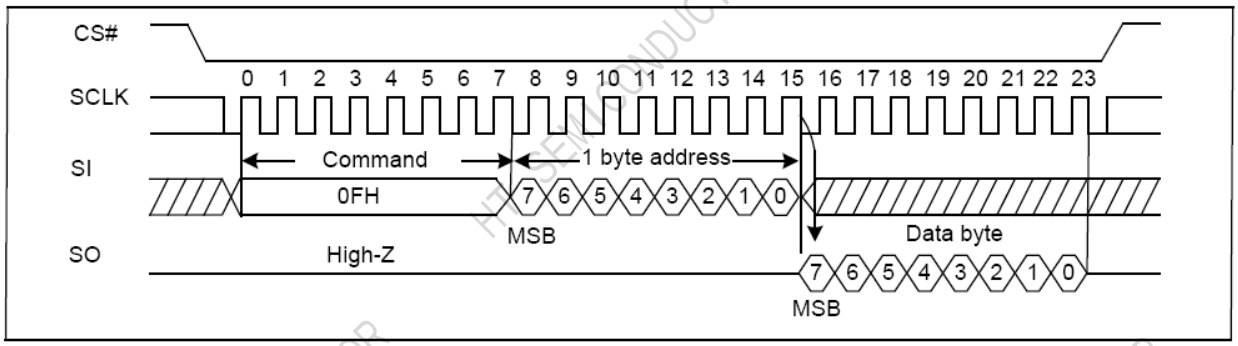


Figure 5-6 Get Features Sequence Diagram

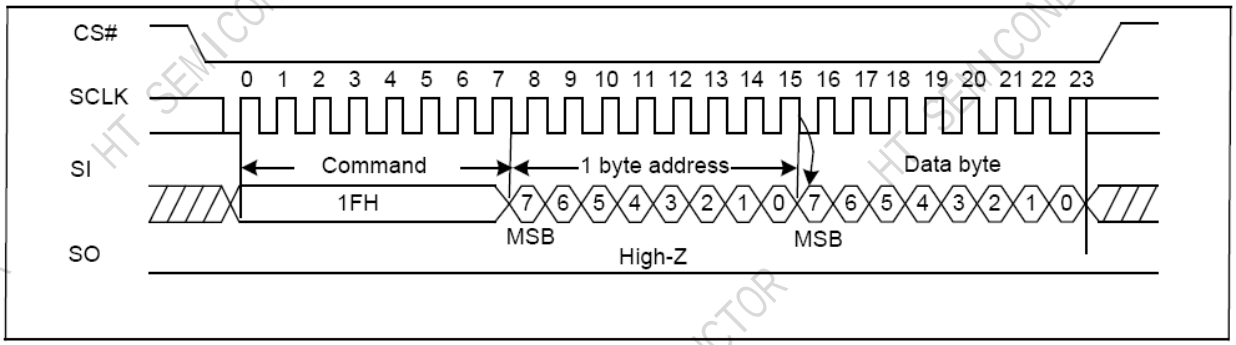


Figure 5-7 Set Features Sequence Diagram

5.6 PAGE READ OPERATIONS

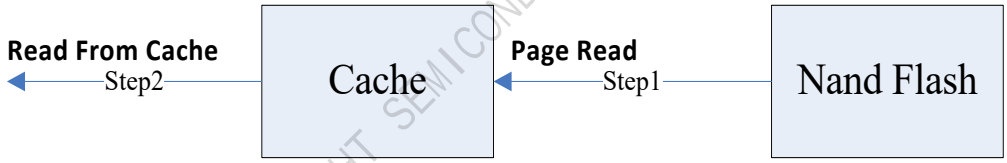


Figure 5-8 Page Read Operations Diagram

Reading data from SPI NAND Flash requires three steps:

1. Use the PAGE READ (13H) command to load the data page into the cache.
2. Use the GET FEATURES (0FH) command to query the status register (C0H), wait for the read to complete (OIP=0), and if ECC_EN is enabled, read ECCS1 and ECCS0 to determine if the read data is correct.
3. Use the Read from cache (03H/0BH/3BH/6BH/BBH/EBH) command to read the data page from the cache.

The Read from cache command address field (16 bits) contains a 4-bit Wrap address to represent the three wrap modes, and a 12-bit column address to specify the cache start address. The 12-bit column start address must be between 0 and 2111. After using the Read from cache command, the cache outputs data sequentially from the specified column address. When it reaches the boundary address of the wrap (2112/2048/64/16-byte) region, it automatically returns to the region start address, and the transmission stops only when CS# goes high.

Table 5-9 Wrap configure bit table

Wrap<3>	Wrap<2>	Wrap<1>	Wrap<0>	Wrap Length(byte)
0	0	X	X	2112
0	1	X	X	2048
1	0	X	X	64
1	1	X	X	16

Page Read to Cache (13H)

The command page read to cache is read the data from flash array to cache register. (If ECC_EN is enabled, data will undergo BCH decoding and error correction before being loaded into the cache). The address field requires 24 bits, where the Page/Block address length varies depending on the Flash specification; refer to Figures 2-3 and 2-4 for the RA address description. After successful SPI NAND FLASH addressing, the corresponding NAND FLASH data will be loaded into the cache; tRD represents the load time. During loading, the OIP status can be queried using the GET FEATURE (0FH) command (OIP = 0 indicates loading is complete). Subsequently, the data can be read from the cache using the Read from cache (03H/0BH/3BH/6BH/BBH/EBH) command.

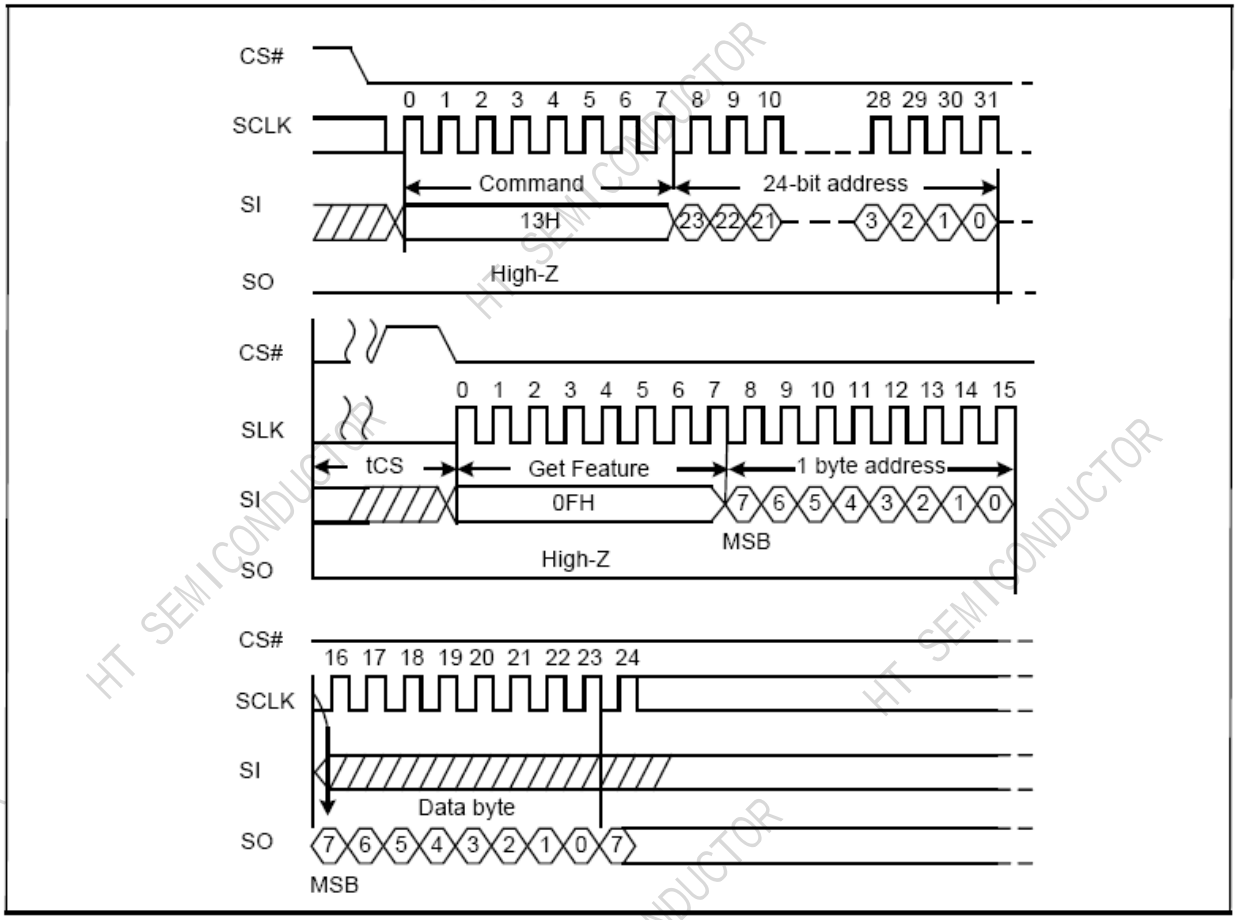


Figure 5-10 Page Read to cache Sequence Diagram

Read From Cache (03H or 0BH)

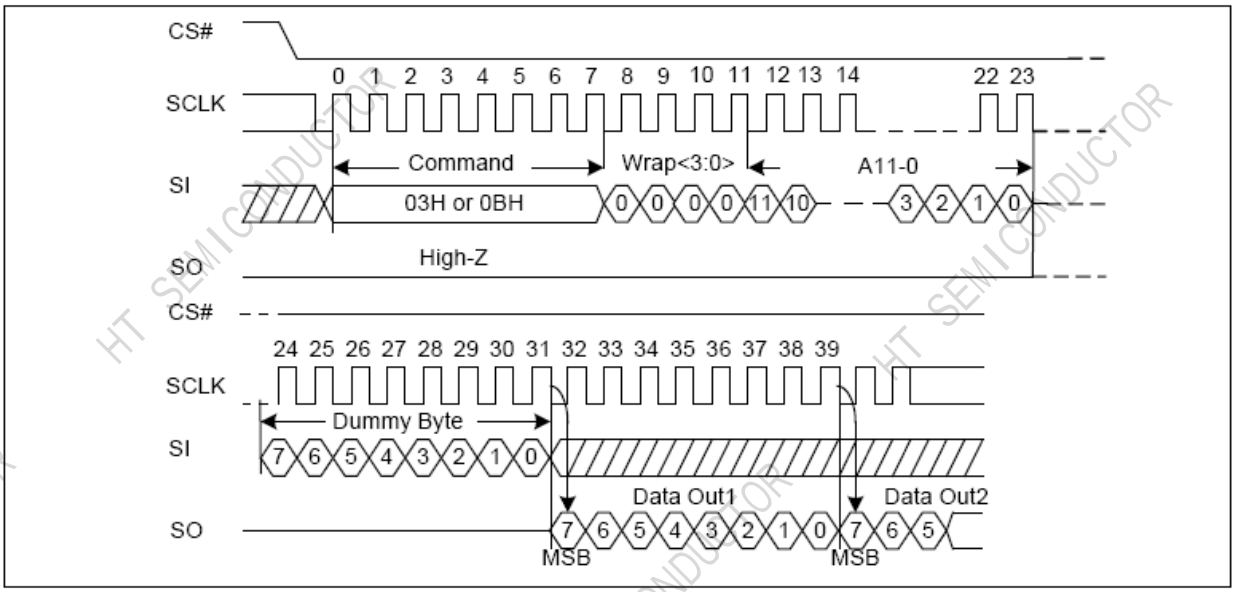


Figure 5-11 Read From Cache Sequence Diagram

Read From Cache x2 (3BH)

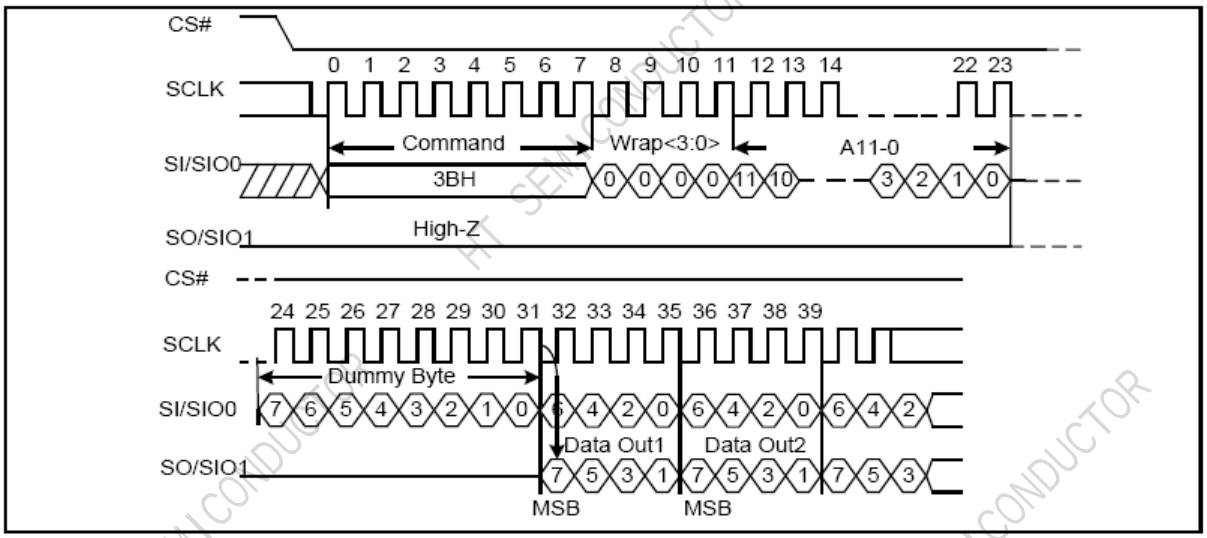


Figure 5-12 Read From Cache x2 Sequence Diagram

Read From Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command.

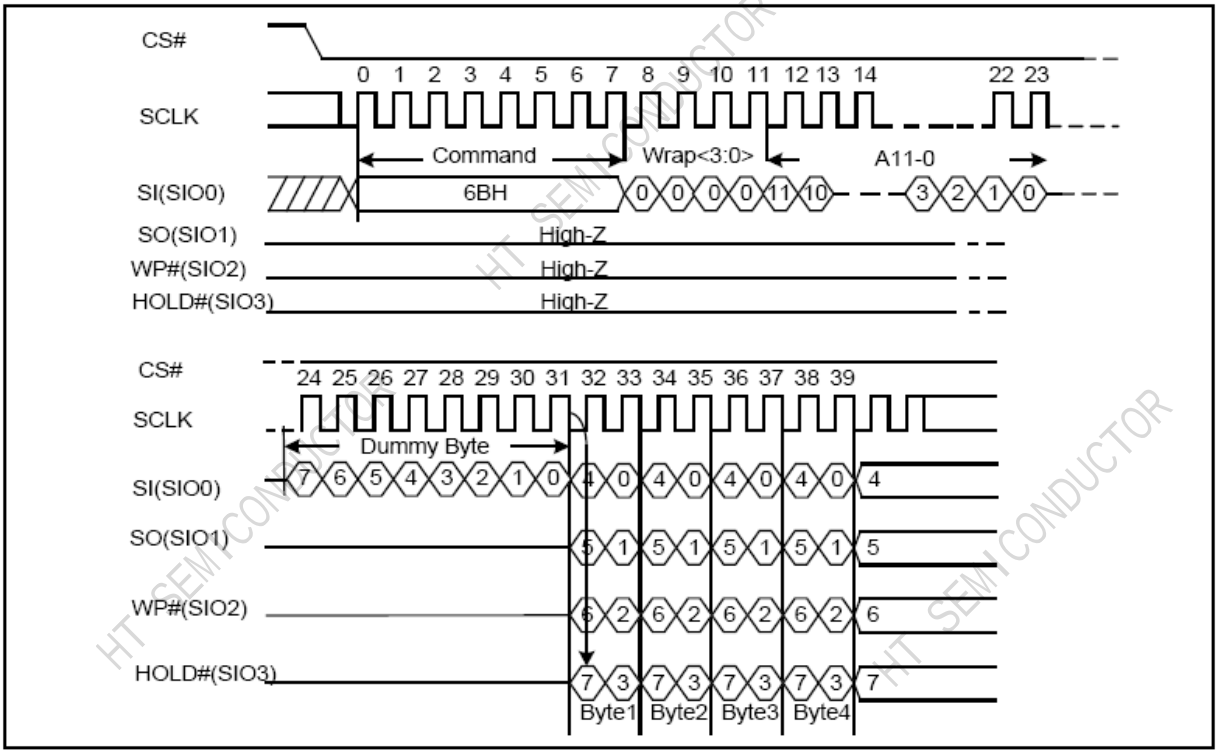


Figure 5-13 Read From Cache x4 Sequence Diagram

Read From Cache Dual IO (BBH)

The Read From Cache Dual I/O command (BBH) is similar to the Read from Cache x2 command (3BH), except that the address field (wrap<3:0> A11-0) is transmitted using SIO0.SIO1.

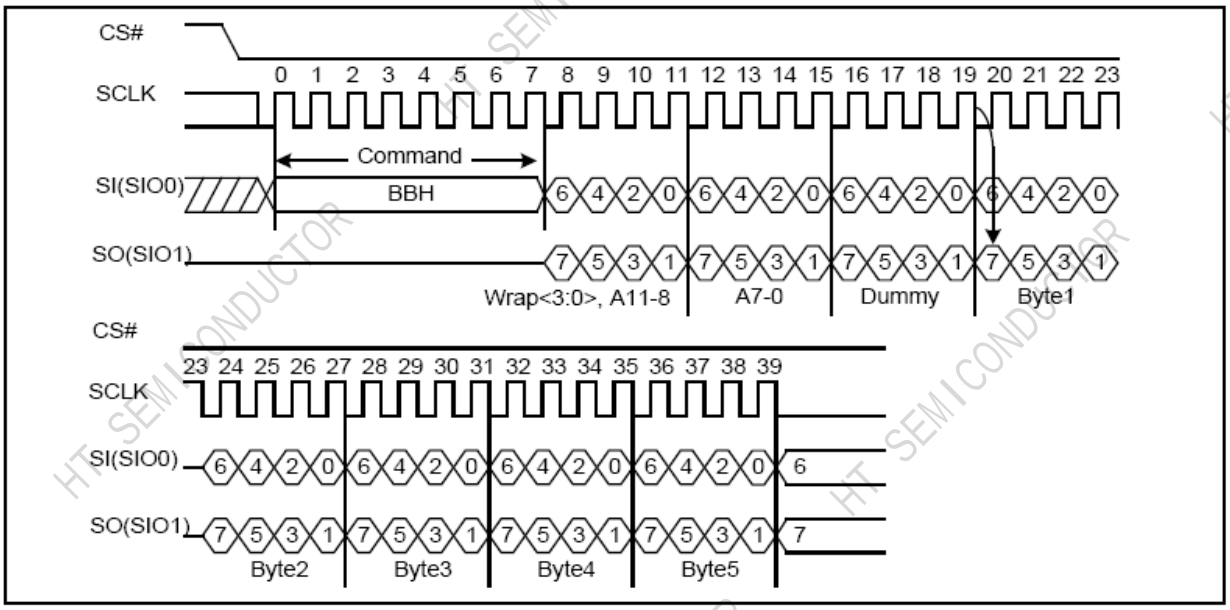


Figure 5-14 Read From Cache Dual IO Sequence Diagram

Read From Cache Quad IO (EBH)

The Read From Cache Quad IO Dual I/O command (EBH) is similar to the Read from Cache x4 command (6BH), and QE must also be set to 1 before using this command. The difference is that the address field (wrap<3:0> A11-0) uses SIO0, SIO1, SIO2, and SIO3 for transmission.

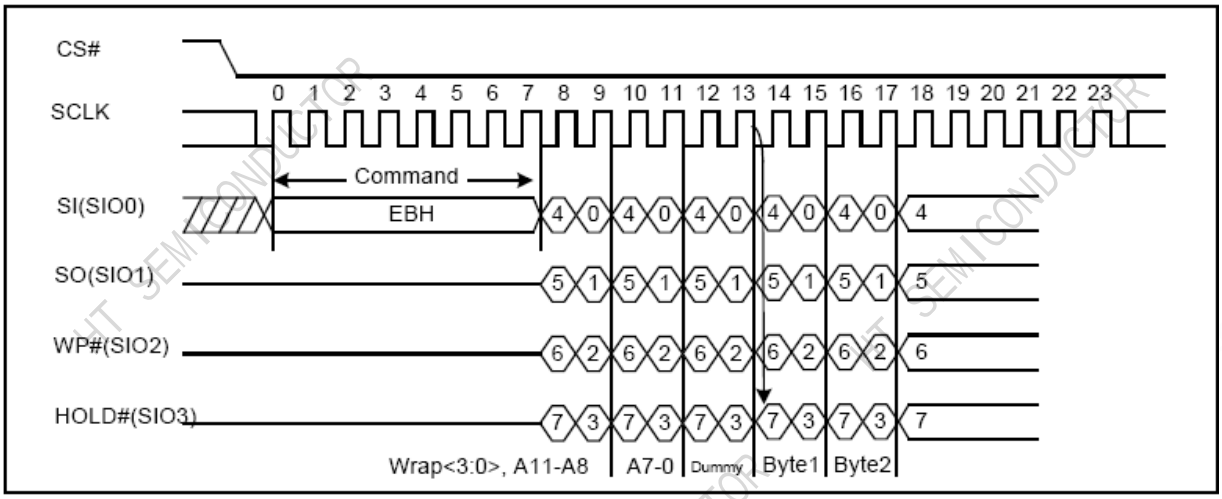


Figure 5-15 Read From Cache Quad IO Sequence Diagram

5.7 PAGE PROGRAM OPERATIONS

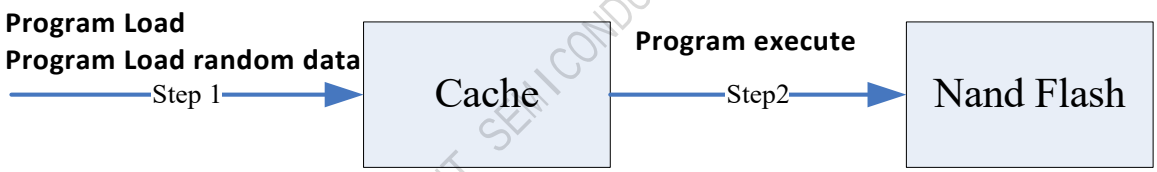


Figure 5-16 Page Program Operations Diagram

Writing data to SPI NAND Flash requires four steps:

1. Load data into the cache using the PROGRAM LOAD (02H/32H) command or the PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command
2. WRITE ENABLE(06H)
3. Use the PROGRAM EXECUTE (10H) command to program the data into the NAND FLASH
4. Use the GET FEATURES (0FH) command to query the status register (C0H), wait for programming to complete (OIP=0), and check P_FAIL to determine whether the data programming was successful (P_FAIL=0 indicates successful programming).

Based on different application programming requirements, the specific command set and command sequence are as follows:

✧ Program Load & Page Program

The PAGE PROGRAM operation sequence programs 1 byte to whole page bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD) / 32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE)

PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The Program address should be in sequential order in a block. The data bytes are loaded into a cache register that is whole page long. If more than one page data are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Use the WRITE ENABLE command (06H) to enable write (WEL=1). If WEL=0, subsequent programming operations will be ignored, and P_FAIL=0. Next, use the PROGRAM EXECUTE command (10H) to write the cached data to the corresponding area of the NAND FLASH. Use GET FEATURE (0FH) to query the programming result. OIP = 0 indicates programming is complete, P_FAIL = 0 indicates programming success, and P_FAIL = 1 indicates programming failure. For the reason for failure, please refer to the description of P_FAIL in the status register.

✧ Internal Data Move & Page Program

The PROGRAM LOAD RANDOM DATA command is used to modify some or all of the data in the cache, similar to the NAND FLASH "Copy back" operation. The command sequence using PROGRAM LOAD RANDOM DATA is as follows:

- 13H (PAGE READ to cache)

- 84H/C4H/ 34H (PROGRAM LOAD RANDOM DATA)
- 84H/C4H/ 34H (PROGRAM LOAD RANDOM DATA)
- ……
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE)

The PAGE READ (13H) command loads the NAND FLASH page data to be modified into the cache. Next, the PROGRAM LOAD RANDOM DATA (84H/C4H/72H) command updates the cached data. The WRITE ENABLE (06H) command enables write operation (WEL=1). If WEL=0, subsequent programming operations will be ignored. The PROGRAM EXECUTE (10H) command programs the cached data into the corresponding NAND FLASH page. The GET FEATURE (0FH) command queries the programming result. OIP = 0 indicates programming is complete, P_FAIL = 0 indicates successful programming, and P_FAIL = 1 indicates programming failure. For the reason for failure, please refer to the description of P_FAIL in the status register.

Program Execute (PE) (10H)

PROGRAM EXECUTE (10H) is used to program cached data into NAND FLASH. The address field requires 24 bits, where the Page/Block address length varies depending on the Flash specification; refer to Figures 2-3 and 2-4 for the RA address description. After successful address addressing, the cached data begins programming, with tPROG indicating the programming time. During programming, the GET FEATURE (0FH) command can be used to query the OIP bit (OIP=0 indicates programming is complete).

Before using the PROGRAM EXECUTE (10H) command, the data needs to be loaded into the cache. There are two ways to load cache data: Program Load and Program Load Random Data.

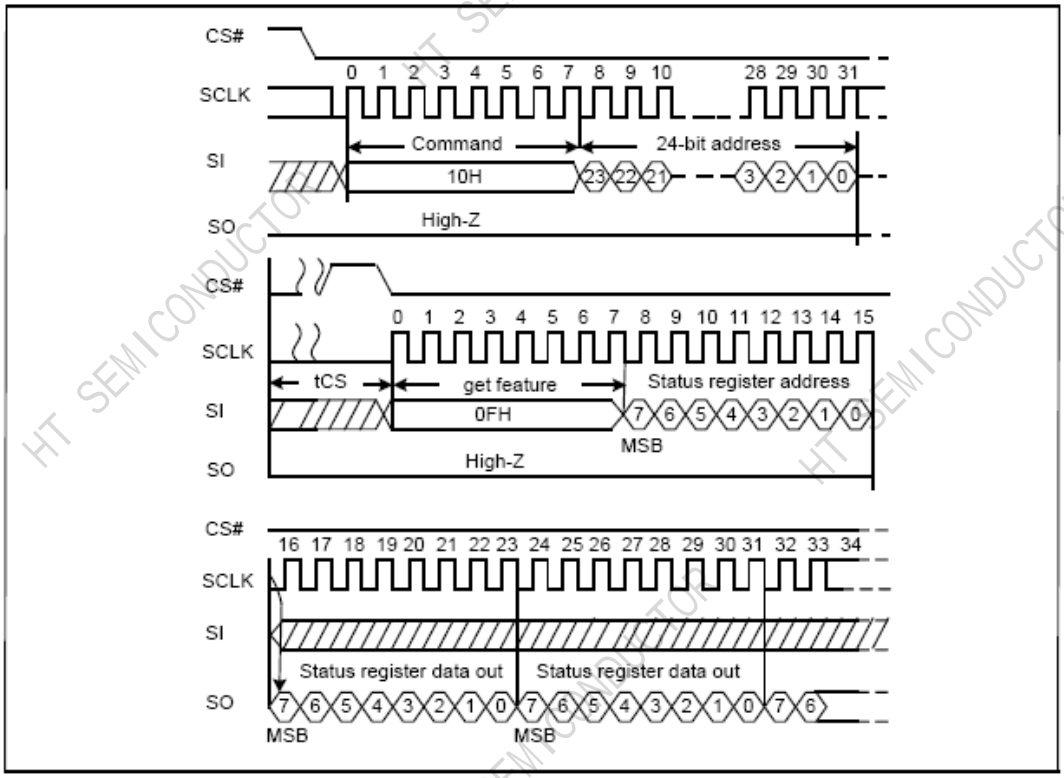


Figure 5-17Program Execute Sequence Diagram

Program Load (PL) (02H)

The address field in the PROGRAM LOAD (02H) command contains a 4-bit dummy address plus a 12-bit column address. The 12-bit column address is used to locate the starting address for writing to the buffer. Input data larger than 2112 will be ignored. CS# must not be pulled high during data transfer; otherwise, the operation will be forcibly terminated.

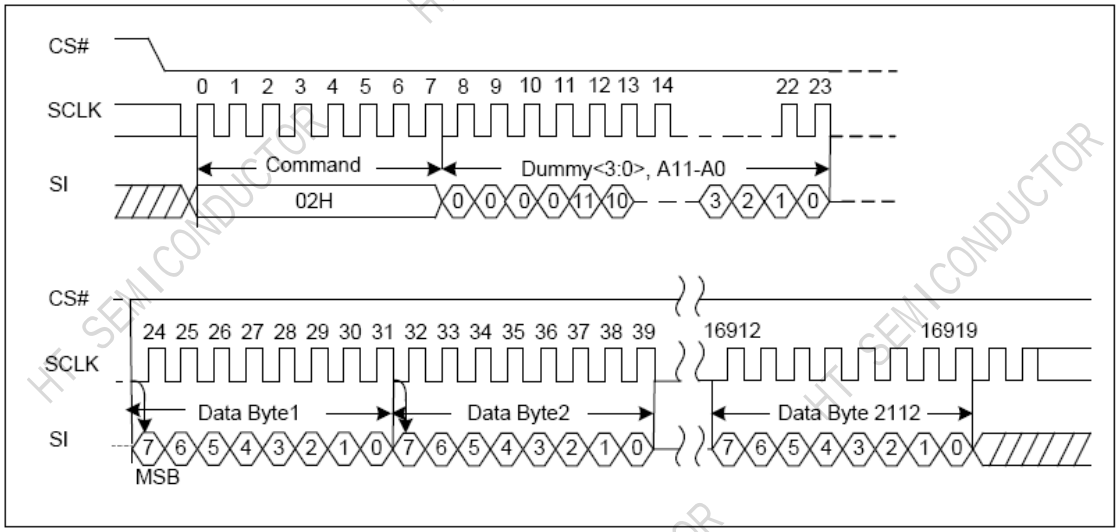


Figure 5-18 Program Load Sequence Diagram

Program Load x4 (PL x4) (32H)

The address field of the PROGRAM LOAD x4 (32H) command contains a 4-bit dummy address plus a 12-bit column address. The 12-bit column address is used to locate the starting address of the write buffer. QE must be set to 1 before using the Program Load x4 command. Input data larger than 2112 will be ignored. CS# must not be pulled high during the write process, otherwise the operation will be forcibly terminated.

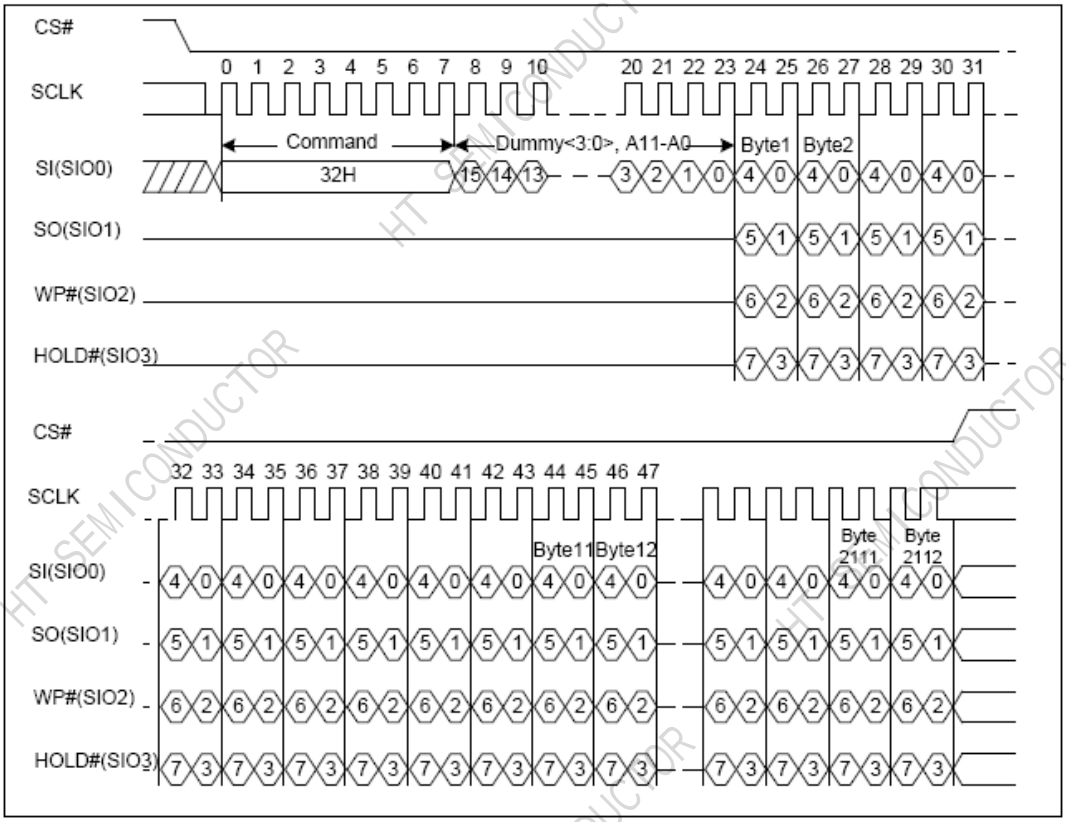


Figure 5-19 Program Load x4 Sequence Diagram

Program Load Random Data (84H)

The PROGRAM LOAD RANDOM DATA (84H) command field contains a 4-bit dummy plus a 12-bit column address. The 12-bit column address is used to locate the starting address of the write buffer. Input data larger than 2112 will be ignored. CS# must not be pulled high during data transfer; otherwise, the operation will be forcibly terminated.

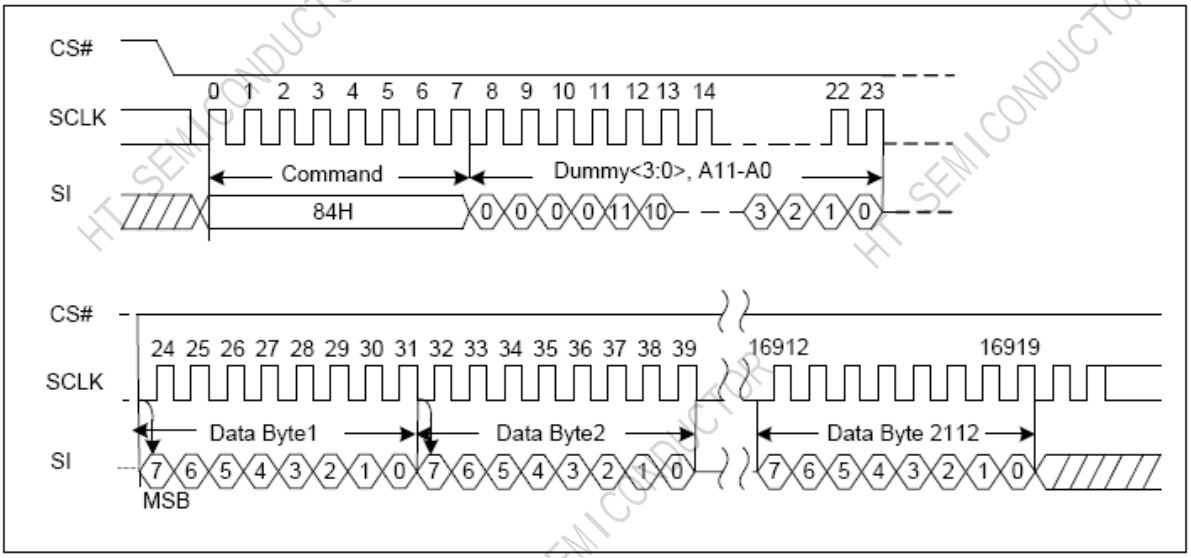


Figure 5-20 Program Load Random Data Sequence Diagram

Program Load Random Data x4 (C4H/34H)

The PROGRAM LOAD RANDOM DATA x4 (C4H/34H) command field contains a 4-bit dummy followed by a 12-bit column address. The 12-bit column address is used to locate the starting address of the write buffer. Input data larger than 2112 will be ignored. CS# must not be pulled high during data transfer; otherwise, the operation will be forcibly terminated. QE must be set to 1 before using the PROGRAM LOAD RANDOM DATA x4 (C4H/34H) command.

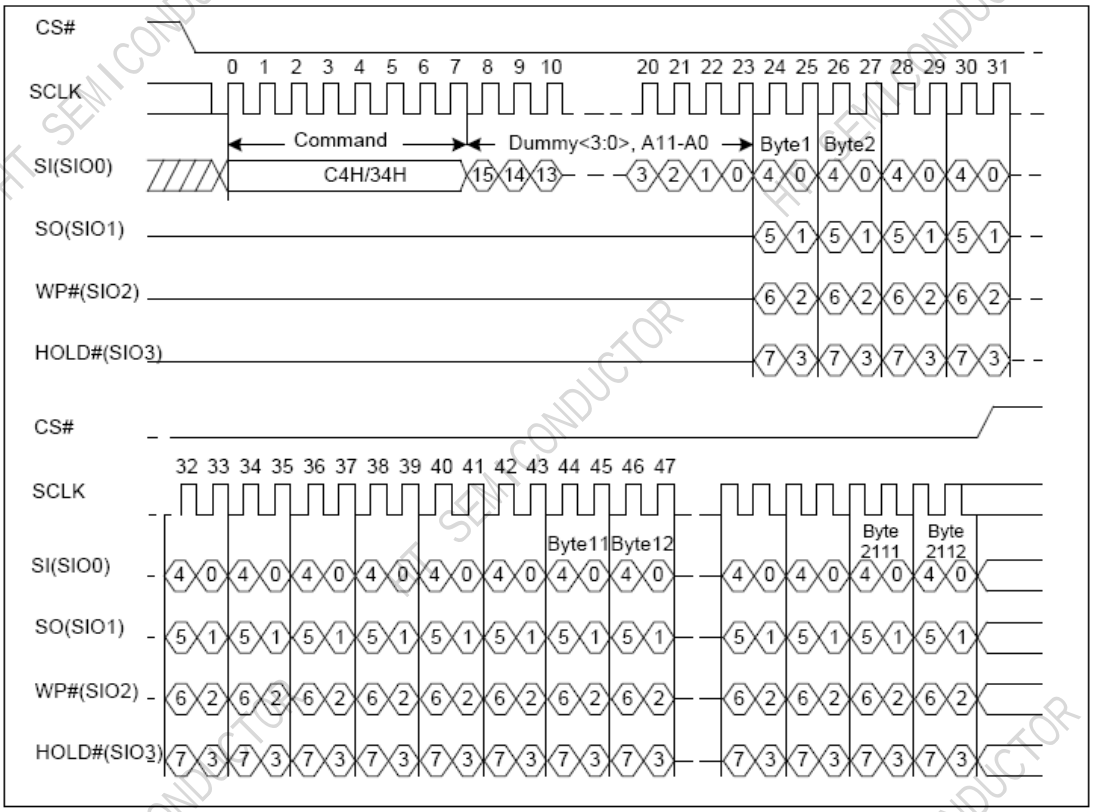


Figure 5-21 Program Load Random Data x4 Sequence Diagram

Program Load Random Data Quad IO (72H)

The Program Load Random Data Quad IO command (EBH) is similar to the PROGRAM LOAD RANDOM DATA x4 (C4H/34H) command; QE must also be set to 1 before using this command. The difference lies in the address field (dummy<3:0> A11-0) using SIO0, SIO1, SIO2, and SIO3 for transmission. Input data larger than 2112 will be ignored. CS# must not be pulled high during data transmission; otherwise, the operation will be forcibly terminated.

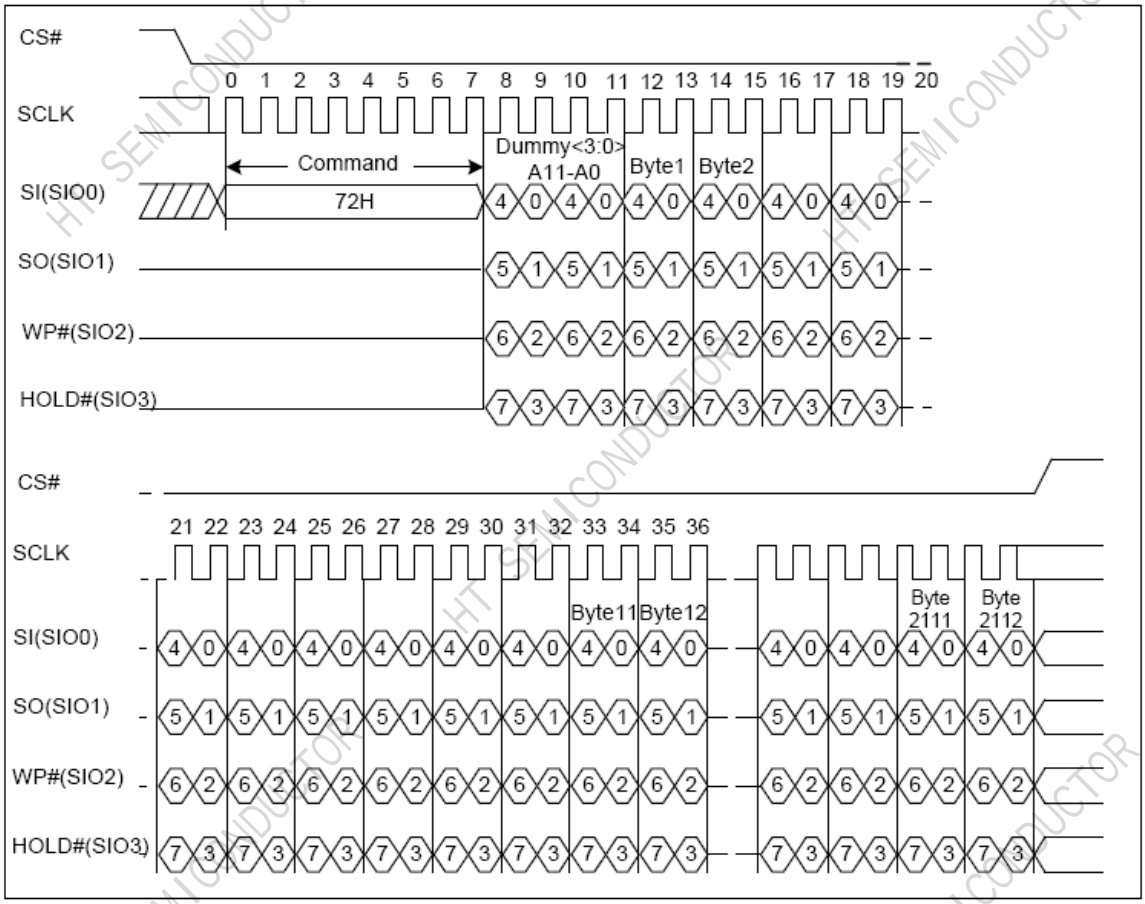


Figure 5-22 Program Load Random Data Quad IO Sequence Diagram

5.8 ERASE OPERATIONS Block Erase (D8H)

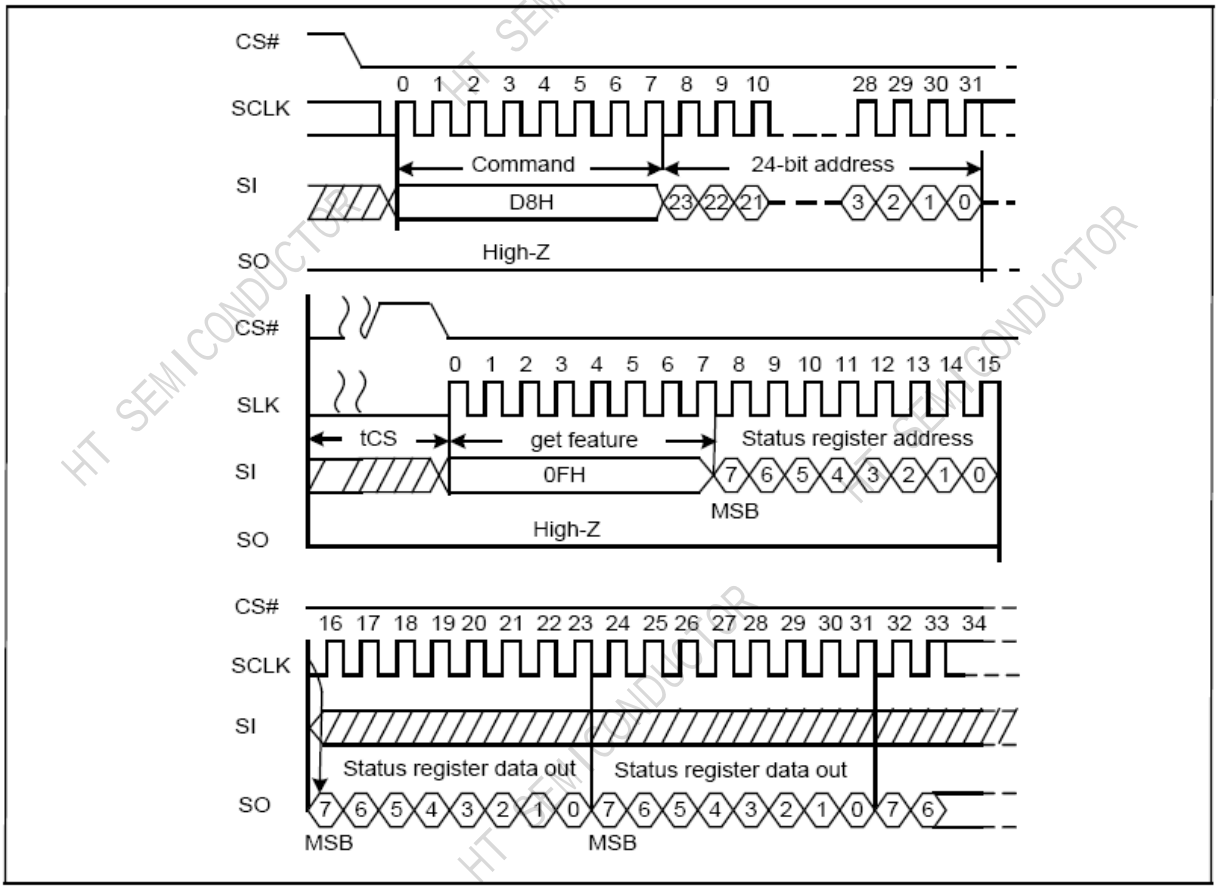


Figure 5-23 Block Erase Sequence Diagram

The BLOCK ERASE (D8H) command erases NAND FLASH blocks. The address field of the BLOCK ERASE (D8H) command contains 24 bits, where the Page/Block address length varies depending on the Flash specification; refer to Figures 2-3 and 2-4 for the RA address description. After successful address addressing, erase operation begins. tERS indicates the erase R/B time. During the erase process, the GET FEATURE (0FH command) can be used to query the OIP bit to monitor the erase result. OIP=0 indicates the erase operation is complete, E_FAIL=0 indicates successful erase, and E_FAIL=1 indicates erase failure. For the reason for failure, please refer to the description of E_FAIL in the status register.

During the execution of the BLOCK ERASE (D8H) command (OIP = 1), users can use the Read From Cache command (03H/0BH/3BH/6BH/BBH/EBH) to perform read operations on the cache, or use the PROGRAM LOAD command (02H/32H/84H/C4H/34H/72H) to perform write operations on the cache.

The command sequence for the BLOCK ERASE operation is as follows:

- 06H (WRITE ENABLE)
- D8H (BLOCK ERASE)
- 0FH (GET FEATURE)

6 SPI NAND FEATURE OPERATIONS

6.1 OTP Region

SPI NAND FLASH offers a protected, One-Time Programmable NAND Flash memory area. 8 full pages are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage.

Table 6-1 Feature Register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Feature	B0H	OTP_PRT	OTP_EN	reserved	ECC_EN	reserved	reserved	reserved	QE
-	-	non-volatile	RW	-	RW	-	-	-	RW

When delivered from factory, feature bit OTP_PRT is 0. To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, pages 00h–07h can be programmed in sequential order by PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands (when not yet protected), and read out by PAGE READ (13h) command and output data by READ from CACHE (03h/0Bh/3Bh/6Bh/BBh/EBh).

Table 6-2 OTP States

OTP_PRT	OTP_EN	State
X	0	Normal Operation
0	1	Access OTP region, read and program data **Note:** OTP_PRT = 0 indicates that the OTP is not locked and can be programmed multiple times. However, an OTP page that has already been programmed cannot be programmed again, otherwise the result will be unknown.
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10h) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data

Enter OTP mode

- Issue the SET FEATURES command (1Fh)
- Set feature (B0H) bit OTP_EN

Access to OTP data

- After into OTP mode，issue PAGE READ command (13H)
- Use the READ FROM CACHE command (03H/0BH/3BH/6BH/BBH/EBH) to read data from the cache.

Write data to OTP (only when OTP_PRT=0)

- Enter OTP mode
- Issue WRITE ENABLE command (06H)
- Use PROGRAM LOAD (02H/32H) or PROGRAM RANDOM (84H/C4H/34H/72H) to write data to the cache.

- Issue PROGRAM EXECUTE (10H)
- Use GET FEATURES (0FH) checks whether the task has been completed (OIP = 0 indicates completion, P_FAIL = 0 indicates success).
- Repeat step 2 and subsequent steps to program the OTP page address.

Protect OTP region

- Issue SET FEATURES (1FH) to set OTP_EN and OTP_PRT bit
- Issue WRITE ENABLE (06H)
- Issue PROGRAM EXECUTE (10H)

Once the OTP region is Protected, the OTP_PRT bit will be permanently set, and the OTP region cannot be erased or reprogrammed thereafter.

6.2 Status Register

The SPI NAND FLASH has an 8-bit status register to indicate the internal operation status, such as the ECC error correction result of the read operation (ECCS1, ECCS0), the result of the programming operation (P_FAIL), and the end of operation (OIP).

The value of this status register can be obtained using the command GET FEATURES(0FH) + address(C0H).

Table 6-3 Status register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Status	C0H	reserved	reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
—	—	—	—	Read only	Read only	Read only	Read only	Read only	Read only

Table 6-4 Status Register Bit Descriptions

bit field	bit name	Description
P_FAIL	Program Fail	P_FAIL = 0： program OK P_FAIL = 1： program FAIL **Note: conditions for P_FAIL = 1:** Programming address out of range Programming locked protected OTP area programming protected areas (BP0, BP1, BP2, INV, CMP) **Note: Conditions for being cleared to 0:** This bit will be cleared to 0 upon receiving the next programming command. This bit is cleared to 0 upon receiving a reset command (FFH).
E_FAIL	Erase Fail	E_FAIL = 0： erase OK E_FAIL = 1： erase FAIL **Note: conditions for E_FAIL = 1:** Erase address out of range Erase locked protected OTP area Erase protected areas (BP0, BP1, BP2, INV, CMP)

bit field	bit name	Description
		Note: Conditions for being cleared to 0: This bit will be cleared to 0 upon receiving the next erase command. This bit is cleared to 0 upon receiving a reset command (FFH).
WEL	Write Enable Latch	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state. When the RESET (FFH) command is executed after power-on, OIP indicates whether internal initialization is complete. When the RESET (FFH) command is executed during operation, the OIP indicates whether the interrupt operation has been completed. **Note: OIP = 0 indicates completion, OIP = 1 indicates that it is still in progress.**
ECCS1,ECSS0	BCH Status	00: Indicates that no errors were found during the execution of PAGE_READ (13H). 10: Found an error, but the error cannot be corrected. **Note: Conditions for being cleared to 0:** This bit is cleared to 0 upon receiving the next PAGE_READ (13H) command. During power-on reset, this bit reflects the loading results of block0 and page0. (The reset command (FFH) and power-on automatically load block0 and page0 into the cache.)

6.3 Assistant Bad Block Management

At the time of manufacture, Nand Flash may contain several bad blocks. The manufacturer will fill the first byte of the OOB area with 00H (Bad Block Mark) to identify bad blocks. Before the first use, the user needs to read the first byte (800H) of the OOB area of the first page of each block. Blocks that return a result other than FFH should be regarded as bad blocks.

6.4 Internal ECC

SPI NAND FLASH offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the “active” state when ECC enable. To enable/disable ECC, perform the following command sequence:

- Issue SET FEATURES (1FH)
- To enable ECC：ECC_EN=1，To disable ECC：ECC_EN=0

When ECC is enabled, during PROGRAM operations, 2K data in the cache is first BCH encoded and then programmed into the NAND FLASH. During READ operations, 2K data read from the NAND FLASH is first BCH decoded, then placed into the cache, and the decoding result is reflected in ECCS1 and ECCS0. For pages that have been erased but not programmed, regardless of whether ECC_EN = 0 or 1, ECCS1 and ECCS0 are always = 0 during read operations. For Flash memory with page sizes of 2176 bytes and 2112 bytes, the protection fields for the data area differ, as shown in Tables 6-5 and 6-6.

Table 6-5-1 **ECC Protection and Spare Area (2176 bytes per page) (version1)**

Min Byte Address	Max Byte Address	ECC Protected	Area	Size	Description
000H	1FFH	Yes	Main0	512	User data 0
200H	3FFH	Yes	Main1	512	User data 1
400H	5FFH	Yes	Main2	512	User data 2
600H	7FFH	Yes	Main3	512	User data 3
800H	832H	Yes	OOB	51	User Meta (800H is also for bad block mark)
833H	83FH	Yes	ECC for OOB	13	ECC for OOB
840H	87FH	Yes	Internal ECC	64	ECC for main(0~3) (prohibited for user)

Note:

1. When ECC is enabled, data written to the ECC for OOB area will be ignored.
2. Regardless of whether ECC is enabled or not, the Internal ECC area is prohibited and is inaccessible.
3. When ECC is disenabled, PAGE SIZE 2112 BYTE can be used.

6.5 Block Protection

Table 6-7 Protection register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Protection	A0H	BRWD	reserved	BP2	BP1	BP0	INV	CMP	reserved
—	—	RW	—	RW	RW	RW	RW	RW	RW

- Use GET FEATURES (0FH) and SET FEATURES (1FH) to access or configure the Protection register.
- SPI NAND provides write protection for the entire/partial block area. After power-on, all blocks are in write-protected state by default (BP2, BP1, BP0 = 1).
- When BRWD = 1 and WP# is low, all protection status bits cannot be modified by the SET FEATURES (1FH) command.
- The PROGRAM/ERASE command will cause an operation error (P_FAIL= 1/EFAIL= 1) when addressing within a protected area.
- Write protection bits (BP0, BP1, BP2, INV, CMP) in different capacity write protection address ranges (taking a 64 pages per block Flash as an example), see Table 6-10

Table 6-8 Block Lock Register Block Protect Bits(64 pages per block)

CMP	INV	BP2	BP1	BP0	Protect page Address （1024 Blocks）	Protect page Address （2048 Blocks）	Protect page Address （4096 Blocks）	Protect Rows
X	X	0	0	0	None	None	None	UNLOCK
X	X	1	1	1	0000H-FFFFH	00000H-1FFFFH	0000H-3FFFFH	LOCK
0	0	0	0	1	FC00H-FFFFH	1F800H-1FFFFH	3F000H-3FFFFH	H 1/64
0	0	0	1	0	F800H-FFFFH	1F000H-1FFFFH	3E000H-3FFFFH	H 1/32
0	0	0	1	1	F000H-FFFFH	1E000H-1FFFFH	3C000H-3FFFFH	H 1/16
0	0	1	0	0	E000H-FFFFH	1C000H-1FFFFH	38000H-3FFFFH	H 1/8
0	0	1	0	1	C000H-FFFFH	18000H-1FFFFH	30000H-3FFFFH	H 1/4
0	0	1	1	0	8000H-FFFFH	10000H-1FFFFH	20000H-3FFFFH	H 1/2
0	1	0	0	1	0000H-03FFH	0000H-07FFH	0000H-0FFFH	L 1/64
0	1	0	1	0	0000H-07FFH	0000H-0FFFH	0000H-1FFFH	L 1/32
0	1	0	1	1	0000H-0FFFH	0000H-1FFFH	0000H-3FFFH	L 1/16
0	1	1	0	0	0000H-1FFFH	0000H-3FFFH	0000H-7FFFH	L 1/8
0	1	1	0	1	0000H-3FFFH	0000H-7FFFH	0000H-FFFFH	L 1/4
0	1	1	1	0	0000H-7FFFH	0000H-FFFFH	0000H-1FFFFH	L 1/2
1	0	0	0	1	0000H-FBFFH	0000H-1F7FFH	0000H-3FFFH	L 63/64
1	0	0	1	0	0000H-F7FFH	0000H-1EFFFH	0000H-3DFFFH	L 31/32
1	0	0	1	1	0000H-EFFFH	0000H-1DFFFH	0000H-3BFFFH	L 15/16
1	0	1	0	0	0000H-DFFFH	0000H-1BFFFH	0000H-37FFFH	L 7/8
1	0	1	0	1	0000H-BFFFH	0000H-17FFFH	0000H-2FFFFH	L 3/4
1	0	1	1	0	0000H~003FH	0000H~003FH	0000H~0003FH	Block0
0	1	0	0	1	0400H-FFFFH	0800H-1FFFFH	1000H-3FFFFH	H 63/64
0	1	0	1	0	0800H-FFFFH	1000H-1FFFFH	2000H-3FFFFH	H 31/32
0	1	0	1	1	1000H-FFFFH	2000H-1FFFFH	4000H-3FFFFH	H 15/16
0	1	1	0	0	2000H-FFFFH	4000H-1FFFFH	8000H-3FFFFH	H 7/8
0	1	1	0	1	4000H-FFFFH	8000H-1FFFFH	10000H-3FFFFH	H 3/4
0	1	1	1	0	0000H~003FH	0000H~003FH	00000H~0003FH	Block0

6.6 Block 0 and Page 0 are automatically loaded into the cache

To ensure compatibility with booting from the SPI interface, the SPI NAND automatically loads block 0 and page 0 data into the cache and performs ECC error correction upon power-up. Data can be read from the cache using the READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command.

To ensure compatibility with some systems where the host uses a "soft shutdown" function (the SPI NAND remains powered on), the host will reboot from block 0, page 0. Upon receiving a reset command, the SPI NAND FLASH will also load the data from block 0, page 0 into the cache and perform ECC error correction (optional).

7 POWER ON TIMING

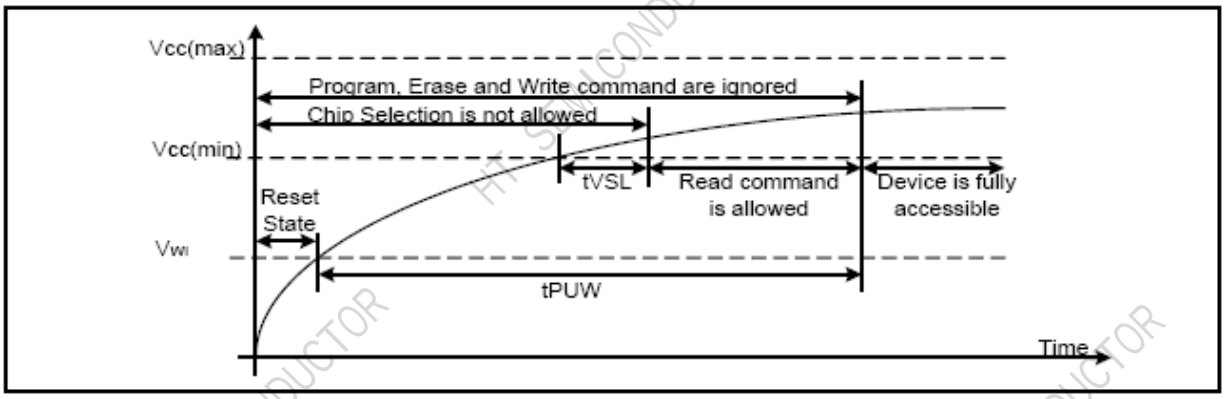


Figure 7-1Power on Timing Sequence

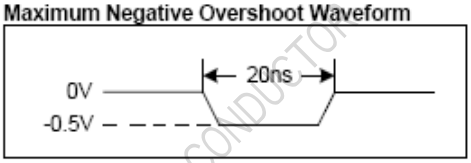
Table 7-1Power-On Timing and Write Inhibit Threshold for 3.3V

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# LOW		1	ms
tPUW	Time Delay From $VCC_{(WI)}$ To Write Instruction		1.5	ms
VWI	Write Inhibit Voltage		2.9	V

Table 7-2ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-55 to 125	℃
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

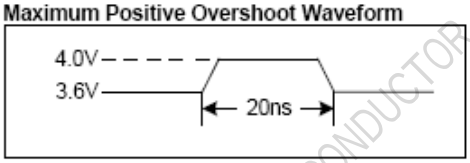
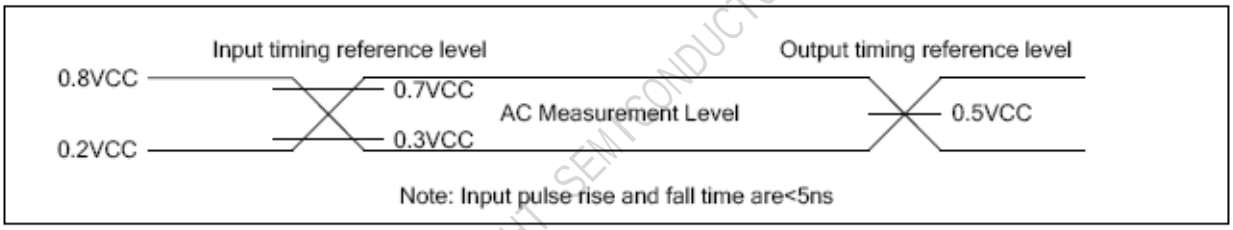


Table 7-3CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	
COUT	Output Capacitance			10	pF	
C_L	Load Capacitance			30	pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.2*VCC		0.8*VCC	V	
	Input Timing Reference Voltage	0.3*VCC		0.7*VCC	V	
	Output Timing Reference Voltage		0.5*VCC		V	


Input timing reference level
Output timing reference level
0.8VCC
0.7VCC
AC Measurement Level
0.5VCC
0.2VCC
0.3VCC
Note: Input pulse rise and fall time are<5ns

8 CHARACTERISTIC

8.1 DC CHARACTERISTIC

Table 8-1 DC Characteristic

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current				±2	uA
I_{LO}	Output Leakage Current				±2	uA
I_{CC1}	Standby Current	CS# = VCC V_{IN} = VCC or VSS			90①/108②/126③	uA
I_{CC2}	Operation Current(Read)	CLK = 0.1VCC/0.9VCC At 104MHz，Q = Open(*1 I/O)				mA
		CLK = 0.1VCC/0.9VCC At 80MHz，Q=Open(*1,*2,*4 I/O)			35	mA
V_{IL}	Input Low Voltage		-0.5		0.3VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.3	V
V_{OH}	Output High Voltage	I_{OH} = 100uA	VCC-0.1			V

(T= -40℃~85℃, VCC=2.7~3.6V)

① 1.8V flash,16bit

② 3.3V flash 16bit

③ 3.3V flash 8bit

8.2 AC CHARACTERISTICS

Table 8-2 AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_C	Serial Clock Frequency For: all command			104	MHz
t_{CH}	Serial Clock High Time	5			ns
t_{CL}	Serial Clock Low Time	5			ns
t_{CLCH}	Serial Clock Rise Time(Slew Rate)	0.5			V/ns
t_{CHCL}	Serial Clock Fall Time(Slew Rate)	0.5			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			10	ns

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLQX}	Output Hold Time	1			ns
t_{DVCH}	Data in Setup Time	3			ns
t_{CHDX}	Data in Hold Time	5			ns
t_{HLCH}	Hold# Low Setup Time(relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time(relative to Clock)	5			ns
t_{CHHL}	Hold# Low Hold Time(relative to Clock)	5.5			ns
t_{CHHH}	Hold# High Hold Time(relative to Clock)	5.5			ns
t_{HLQZ}	Hold# Low to High-Z Output			10	ns
t_{HHQX}	Hold# High to Low-Z Output			10	ns
t_{CLQV}	Clock Low to Output Valid			9	ns
t_{WHSL}	WP# Setup Time Before CS# Low	20			ns
t_{SHWL}	WP# Hold Time After CS# High	100			ns

(T= -40℃~85℃, VCC=2.7~3.6V, C_L=30pf)

8.3 PERFORMANCE TIMING

Table 8-3 PERFORMANCE TIMING

Symbol	Parameter	Min	Typ	Max	Unit
t_{RST}	CS# High To Next Command After Reset(FFh)			500	us
t_{RD}	Read From Array		65	150	us
t_{PROG}	Page Program Time		0.4	1	ms
t_{BERS}	Block Erase Time		3	5	ms

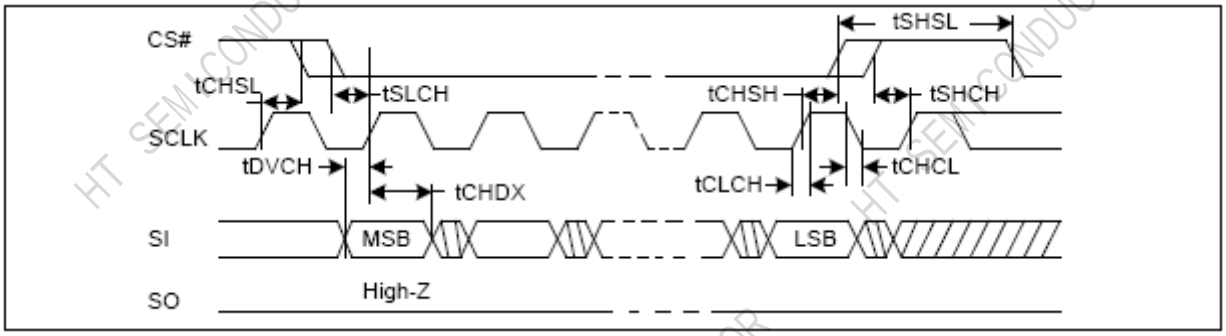


Figure 8-1 Serial Input Timing

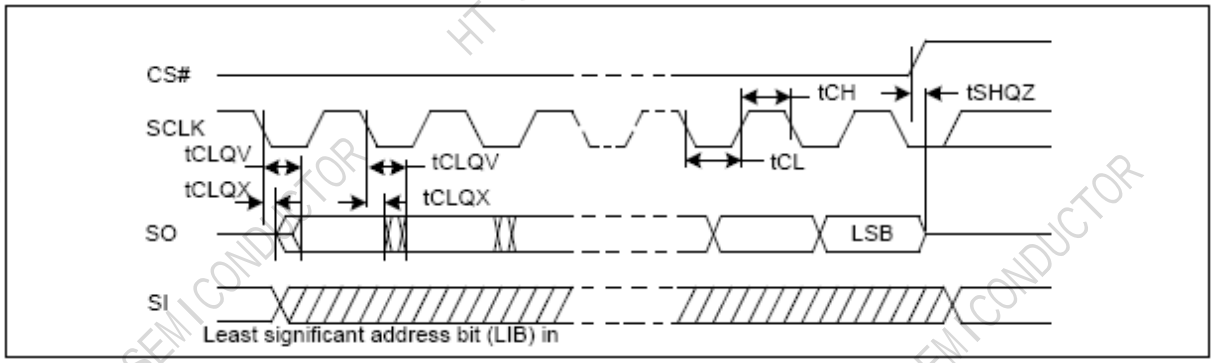


Figure 8-2 Output Timing

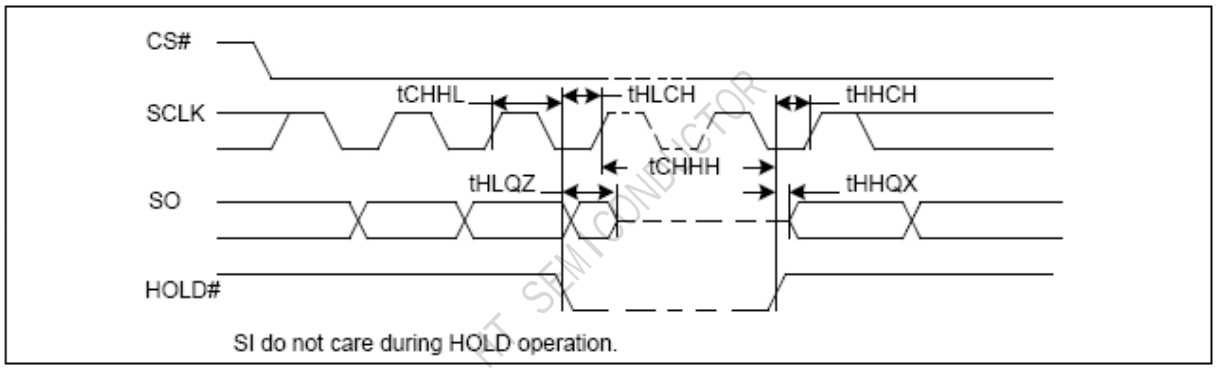
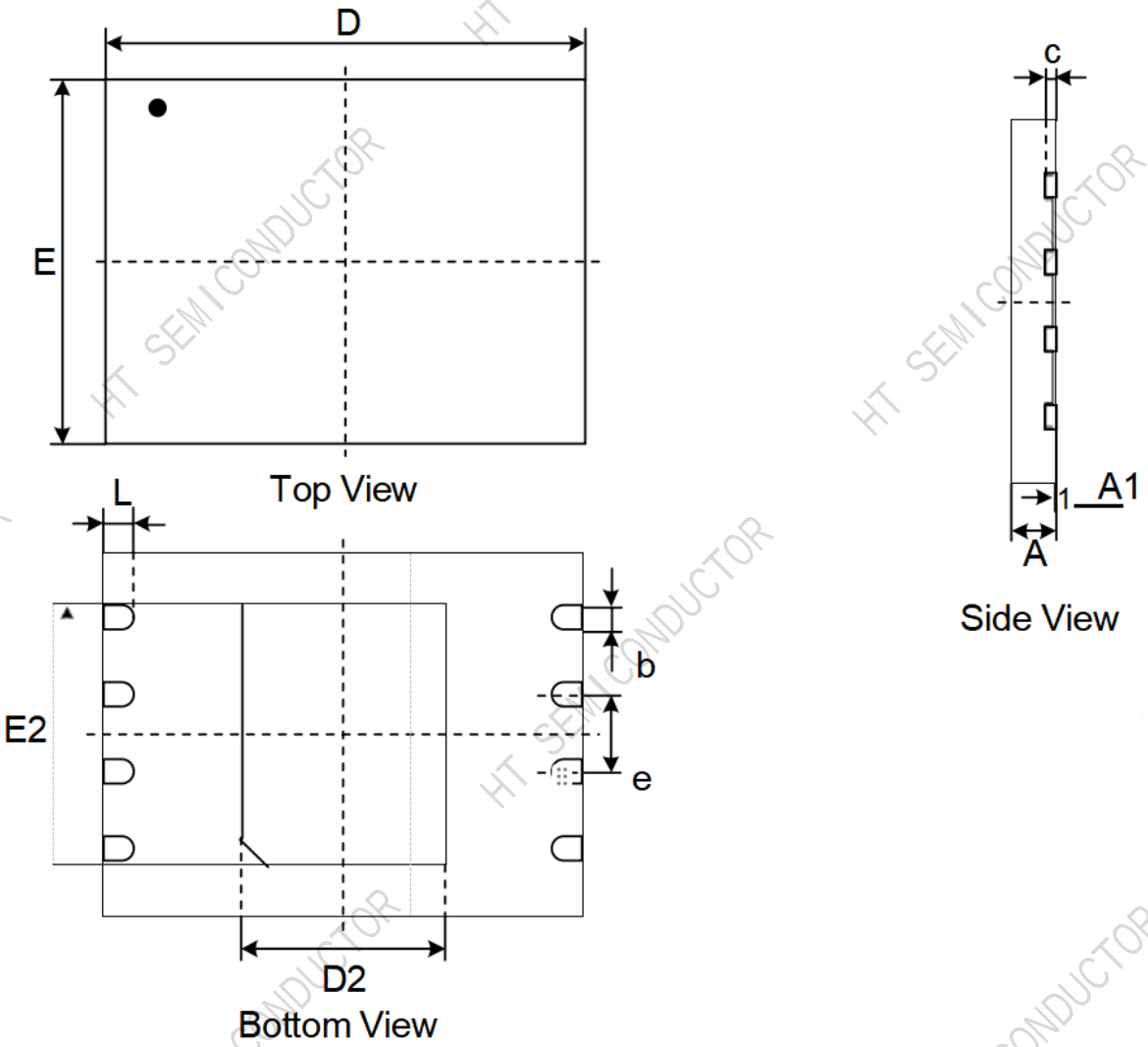


Figure 8-3 Hold Timing

9 PACKAGE INFORMATION



Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022

Figure 17-1. LGA (8x 6 x 0.8mm) Package Outline Drawing Information