Low-Drift, Low-Power, Small-Footprint Series Voltage Reference

Features

Initial accuracy: ±0.15% Maximum

Temperature coefficient: 35ppm/°C Maximum from −40°C to +125°C

Operating temperature range: −40°C to +125°C

Output current: ±10 mA

Low quiescent current: 125 µA

Ultra-low zero load dropout voltage: 200 mV

Input voltage: 2.7 ~ 5.5 V

Long-term stability: 45 ppm/1000 hrs

Small footprint 3 pin SOT-23 package pinouts:

Applications

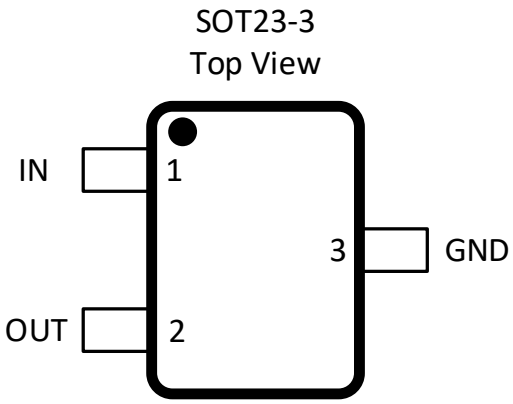
Factory Automation: PLC/Transmitters/DCS

Test Measurement Equipment

Servo driver and Invertor

Precision Reference for MCU`s internal ADC/DAC

PIN Configuration



Pin Configuration and Functions

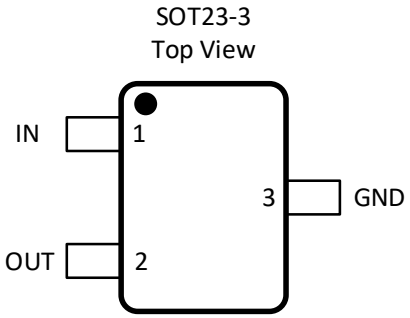


Figure 1. ADR381ARTZ-REEL7
3-Pin SOT-23
Top View

Table 1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	PIN		
IN	1	Power	Input supply voltage connection.
OUT	2	Output	Reference voltage output connection.
GND	3	Ground	Ground connection.

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	IN	-0.3	5.5	V
Output voltage	V_{OUT}	-0.3	5.5	V
Output short circuit current	I_{SC}		30	mA
Operating temperature range	T_A	-55	150	℃
Storage temperature range	T_{stg}	-60	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input voltage	V_{OUT}+ V_{DO} (1)		5.5	V
I_L	Output current	-10		10	mA
T_A	Operating Temperature	-40	25	125	℃

(1) V_{DO} = Dropout voltage

Thermal Information

THERMAL METRIC		SOT23-3	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	285	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115	°C/W

Electrical Characteristics

At V_{IN} = V_{OUT} + V_{DO}, C_L = 1 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40℃ to 125℃;

Typical specifications at T_A = 25℃ (Unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage	TA = 25℃			2.500		V
	Output voltage accuracy	TA = 25℃		-0.15		+0.15	%
	Output voltage temperature coefficient (1)	-40°C ≤ TA ≤ 125°C			15	35	ppm/℃
LINE & LOAD REGULATION							
$\Delta V_O/\Delta V_{IN}$	Line Regulation	V_{IN} = V_{OUT} + V_{DO} (2) to 5.5 V			15		ppm/V
$\Delta V_O/\Delta I_L$	Load Regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT}+ V_{DO} (3)	T_A = 25°C, Sourcing		5		ppm/mA
		I_L = 0 mA - 10mA, V_{IN} = V_{OUT}+ V_{DO}	T_A = 25°C, Sinking		20		
I_{SC}	Short circuit current	V_{OUT} = 0 V at T_A = 25°C			30		mA
NOISE							
e_{np-p}	Low frequency noise	0.1Hz ≤ f ≤ 10Hz			25		μV_{P-P}/V
e_n	Integrated wide band noise	10Hz ≤ f ≤ 10kHz			50		μV_{rms}
LONG TERM STABILITY AND HYSTERESIS							
	Long-term stability	SOT23-3 Package	0 to 1000h at 25°C		45		ppm
	Output voltage thermal hysteresis	SOT23-3 Package	25°C, –40°C,125°C, 25°C Cycle 1		120		ppm
			25°C, –40°C,125°C, 25°C Cycle 2		60		
TURN-ON TIME							
t_{ON}	Turn-on time	0.1% of output voltage settling, C_L = 10 µF			5		ms
CAPACITIVE LOAD							
C_L	Stable output capacitor range	–40°C ≤ TA ≤ 125°C		0.1		10	µF

POWER SUPPLY					
V_{IN}	Input voltage		V_{OUT} + V_{DO}	5.5	V
I_L	Output current capacity	V_{IN} = V_{OUT} + V_{DO} to 5.5 V	-10	10	mA
I_Q	Quiescent current		125		µA
V_{DO}	Dropout voltage	I_L = 0 mA	160		mV
		I_L = 10 mA	250		

(1) Temperature drift is specified according to the box method.
(2) V_{DO} for line regulation test is 300 mV.
(3) V_{DO} for load regulation test is 500 mV.

Typical Characteristics

At T_A = 25° C, V_{IN} = 5.0V, I_L=0mA, C_L=1µF, C_{IN} = 0.1µF (unless otherwise noted).

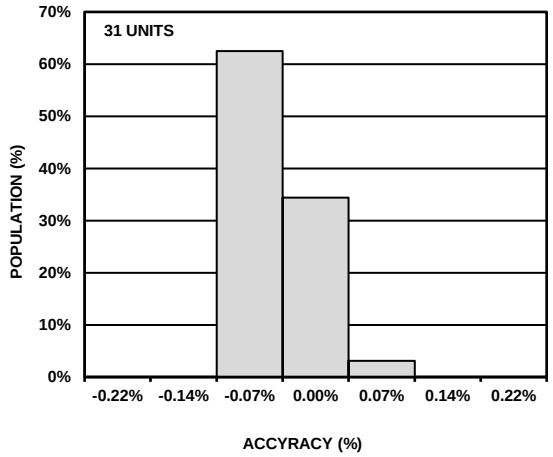


Figure 2: Initial Accuracy

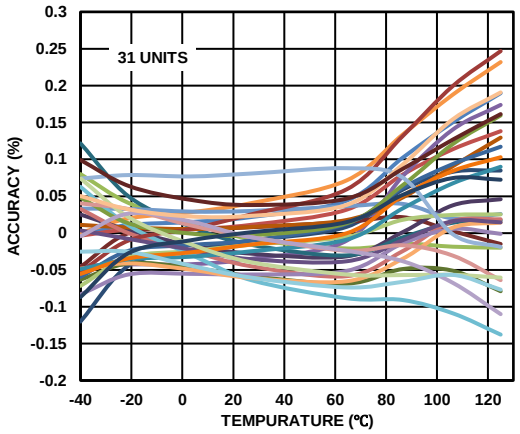


Figure 3: Output Voltage Accuracy vs. Temperature

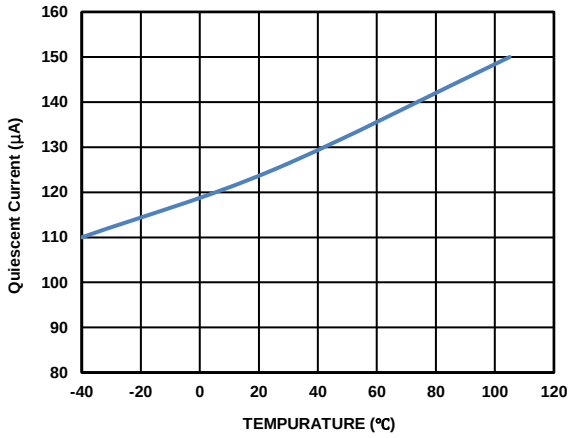


Figure 4: Quiescent Current vs. Temperature

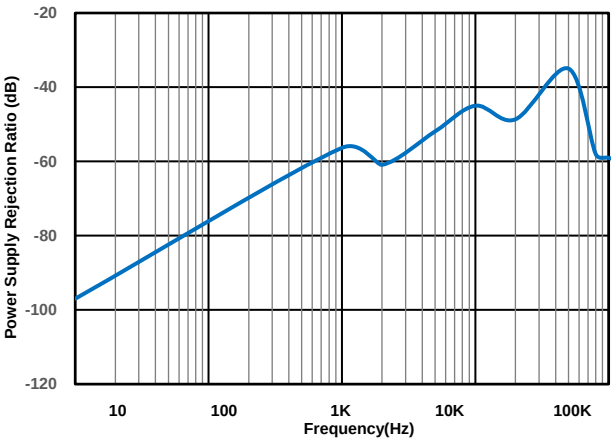


Figure 5: Power-Supply Rejection Ratio vs. Frequency

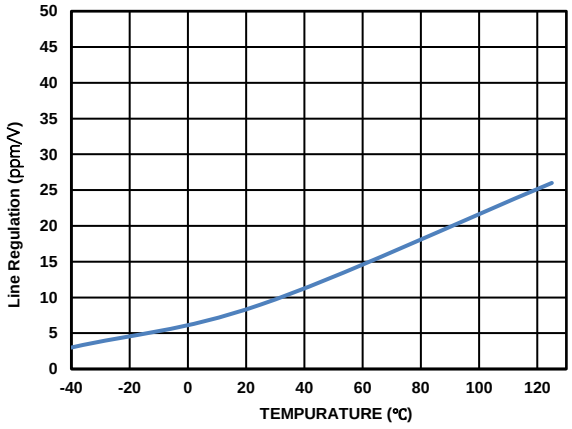


Figure 6: Line Regulation vs. Temperature

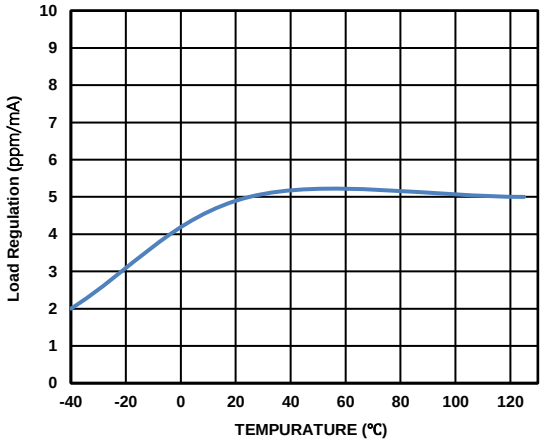


Figure 7: Load Regulation Sourcing

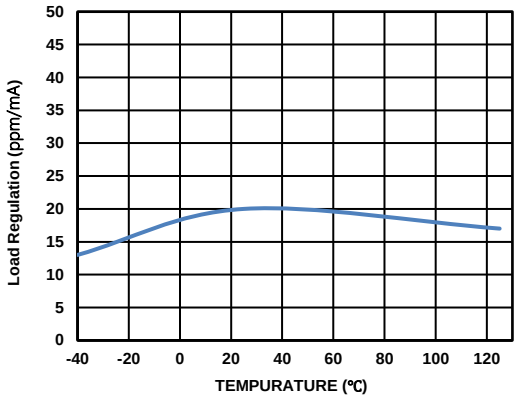


Figure 8: Load Regulation Sinking

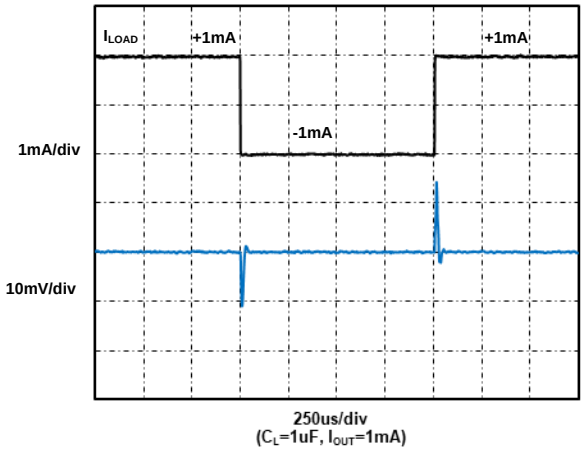


Figure 9: Load Transient

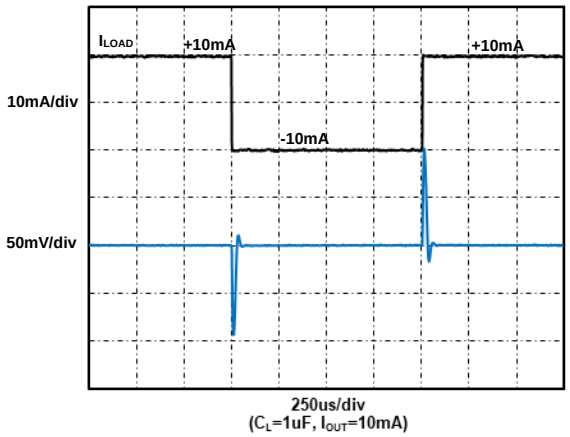


Figure 10: Load Transient

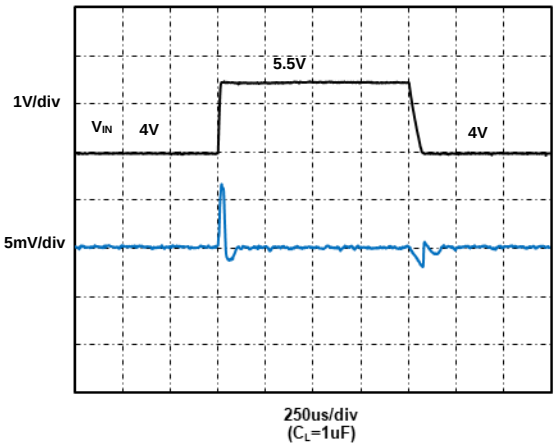


Figure 11: Line Transient

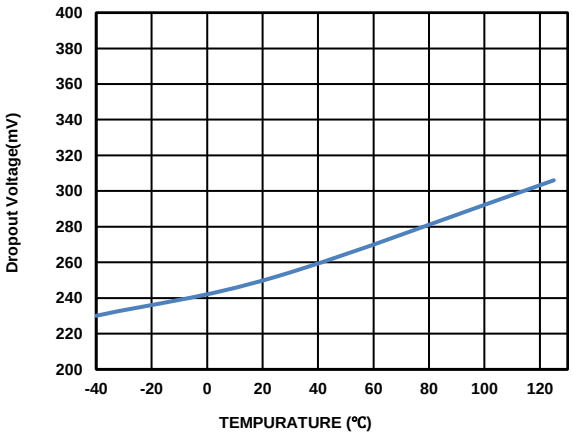


Figure 12: Dropout Voltage(I_{OUT}=10mA)

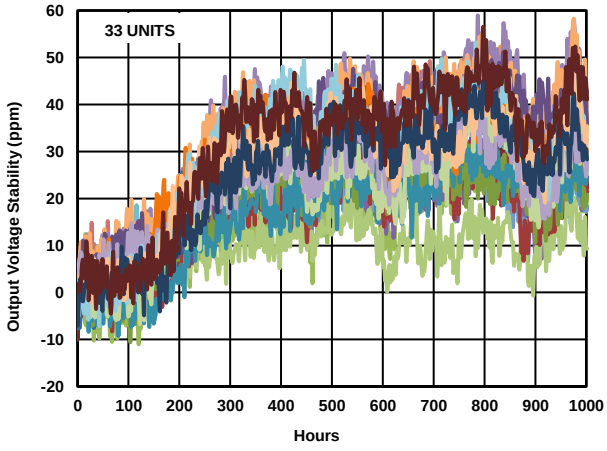


Figure 13: Long Term Stability – 1000 Hours

Parameter Measurement Information

Long-Term Stability

One of the key parameters of the ADR381 references is long-term stability. Typical characteristic expressed as: **Figure 13** shows the typical drift value for the ADR381 is 45 ppm from 0 to 1000 hours. This parameter is characterized by measuring 31 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 30 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time.

Power Dissipation

The ADR381 voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 1:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (1)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

Detailed Description

Overview

The ADR381 is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The section is a simplified block diagram of the ADR381 showing basic band-gap topology.

Functional Block Diagram

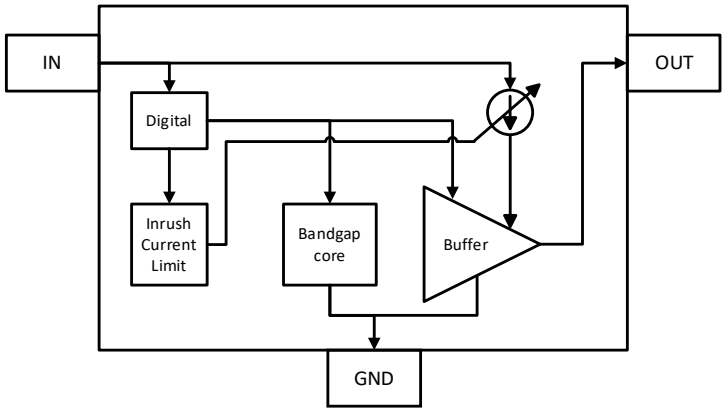


Figure 14: Functional Block Diagram

Feature Description

Supply Voltage

The ADR381 reference features an extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The ADR381 features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 125 µA, and the maximum quiescent current over temperature is just 150 µA. Supply voltages below the specified levels can cause the ADR381 to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

Low Temperature Drift

The ADR381 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 2. For this equation, V_{REF} is V_{OUT} which is the output voltage seen at the junction of OUT_F and OUT_S.

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25℃)} \times \text{Temperature Range}} \right) \times 10^6 \quad (2)$$

Load Current

The ADR381 is specified to deliver a current load of ±10 mA per output. The device temperature increases according to Equation 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

where

- T_J = junction temperature (°C)
- T_A = ambient temperature (°C)
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The ADR381 maximum junction temperature must not exceed the absolute maximum rating of 150°C.

Device Functional Modes

Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the ADR381 can be used to provide a dual-supply reference from a 5V supply. **Figure 15** shows the ADR381 used to provide a 3.3V supply reference voltage. Take care to match the temperature coefficients of R1 and R2.

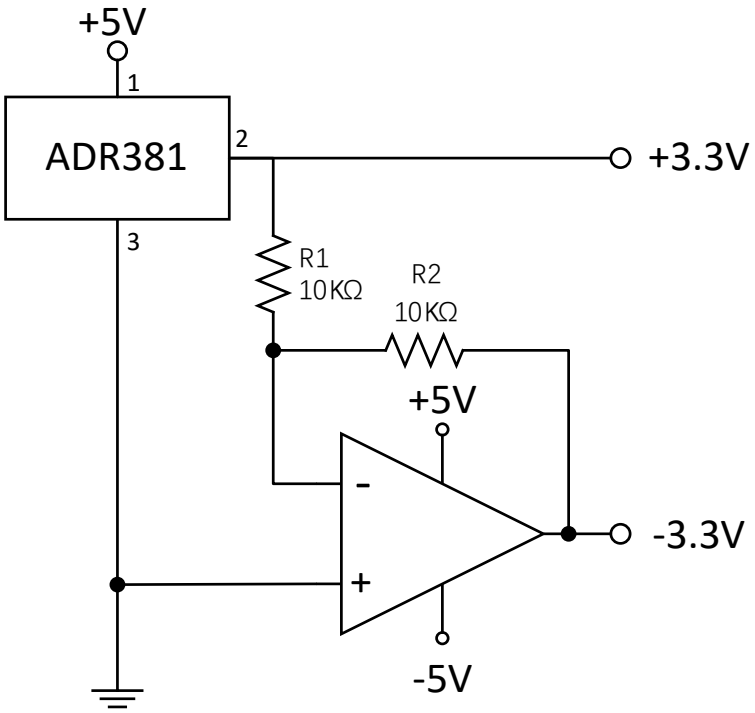


Figure 15: ADR381 Create Positive and Negative Reference Voltages

Power Supply Recommendations

The ADR381 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 250 mV above the output voltage. **Figure 16** shows typical connections required for operation of the ADR381 Sensilicon recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

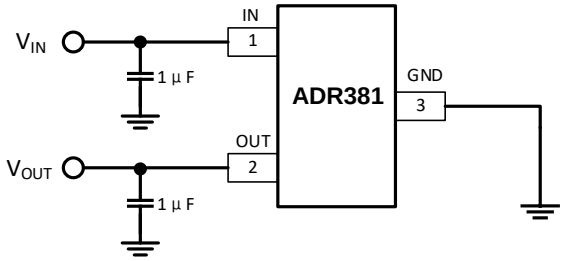


Figure 16: Typical Connections for Operating ADR381

Layout

Layout Guidelines

Figure 17 illustrates an example of a PCB layout for a data acquisition system using the ADR381 .Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at IN, OUT_F, VOUT of the ADR381
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduce electromagnetic interference(EMI)noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect)from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

Layout Example

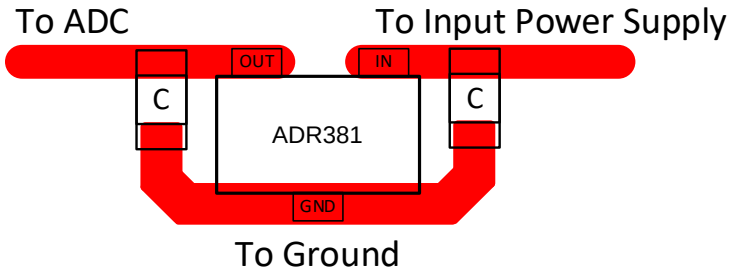
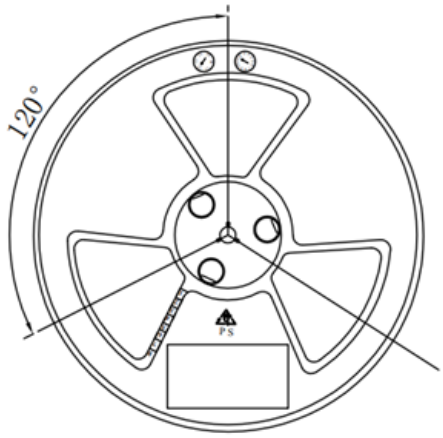
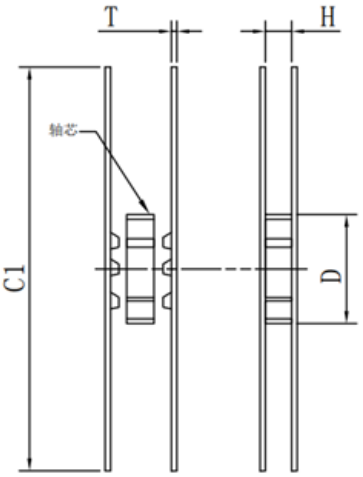
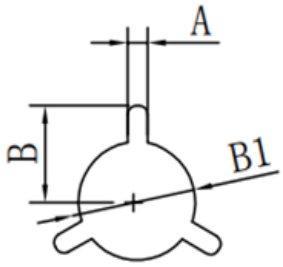


Figure 17: ADR381 PCB Layout Example

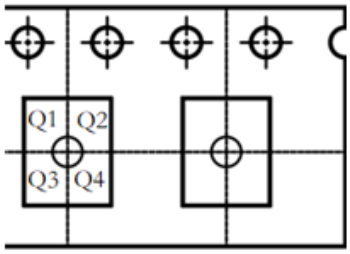
Tape and Reel Information





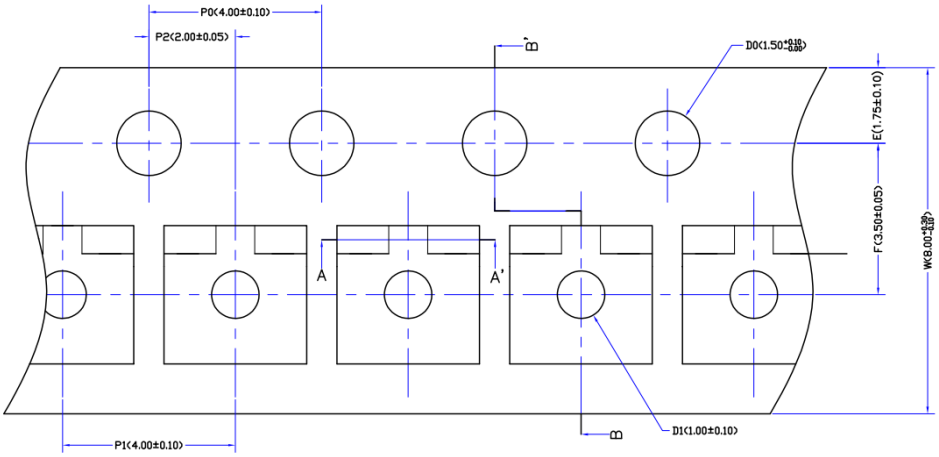


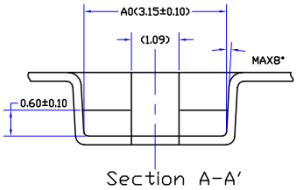
C1	178±1
H	8.4+1/-0
A	2.2±0.5
B	∅13.5±0.2
T	1.2±0.2
D	∅60±0.5
Pin1 Quadrant	Q3



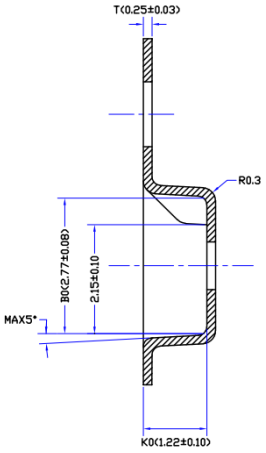
User Direction of Feed

Note: Q1~Q4 is Pocket Quadrants



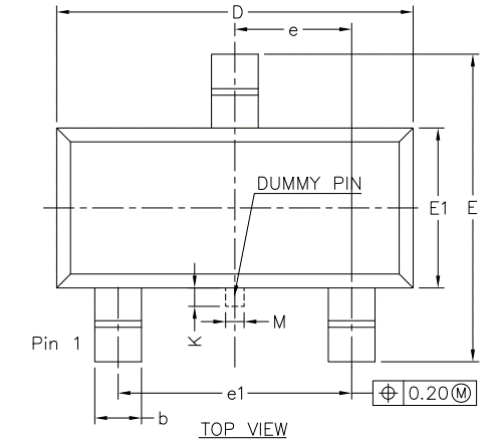


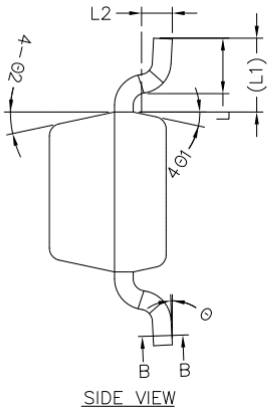
Section A-A'

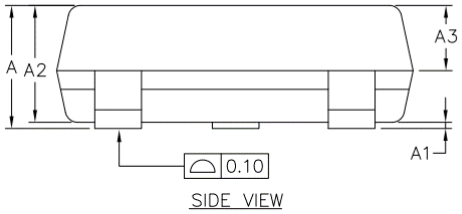


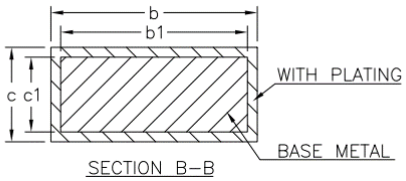
Section B-B'

Package Information









COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.89	–	1.12
A1	0.01	–	0.10
A2	0.88	0.95	1.02
A3	0.43	0.53	0.63
b	0.36	–	0.50
b1	0.35	0.38	0.45
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	2.80	2.90	3.00
E	2.35	2.50	2.64
E1	1.20	1.30	1.40
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.40	0.45	0.60
L1	0.60REF		
L2	0.25BSC		
M	0.10	0.15	0.25
K	0	–	0.25
θ	0°	–	8°
θ1	10°	12°	14°
θ2	10°	12°	14°

Ordering Guide

Orderable Device	Package	Package Qty	MSL-Peak Temp	Lead Fish Plating	Op Temp (°C)	RoHS (Pb Free)
ADR381ARTZ-REEL7	SOT23-3	3000	Level 1-260°C	100%Sn	-40 to 125°C	Yes
ADR381ARTZ-REEL	SOT23-3	250	Level 1-260°C	100%Sn	-40 to 125°C	Yes