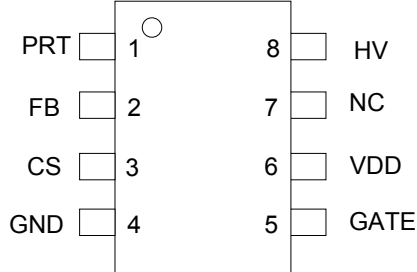


GENERAL INFORMATION

Pin Configuration

The OB5284C is offered in SOP8 package, shown as below.



Ordering Information

Part Number	Description
OB5284CCP	SOP8, Halogen-free in Tube
OB5284CCPA	SOP8, Halogen-free in Taping

Package Dissipation Rating

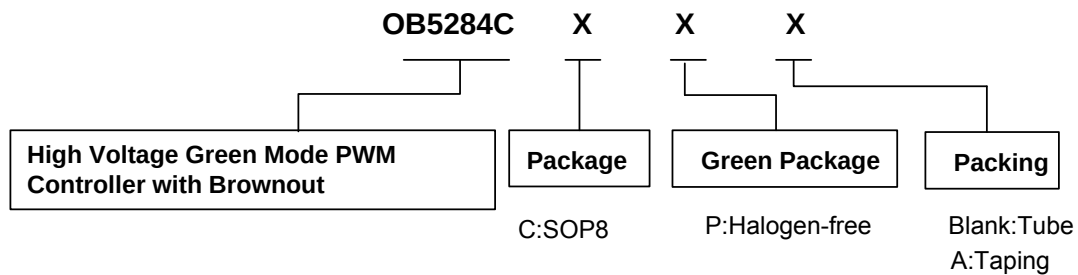
Package	R θ JA(°C/W)
SOP8	90

Absolute Maximum Ratings

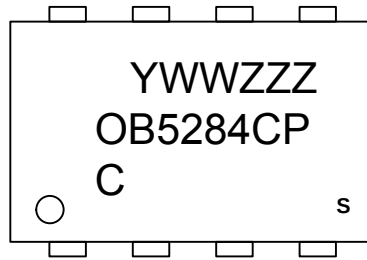
Parameter	Value
VDD DC Supply Voltage	29.5V
High-Voltage Pin, HV	-0.3 to 500 V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T _J	-40 to 150 °C
Operating Ambient Temperature T _A	-40 to 85 °C
Min/Max Storage Temperature T _{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Recommended Operating Condition

Symbol	Parameter	Range
VDD	VCC Supply Voltage	12 to 28V



Marking Information

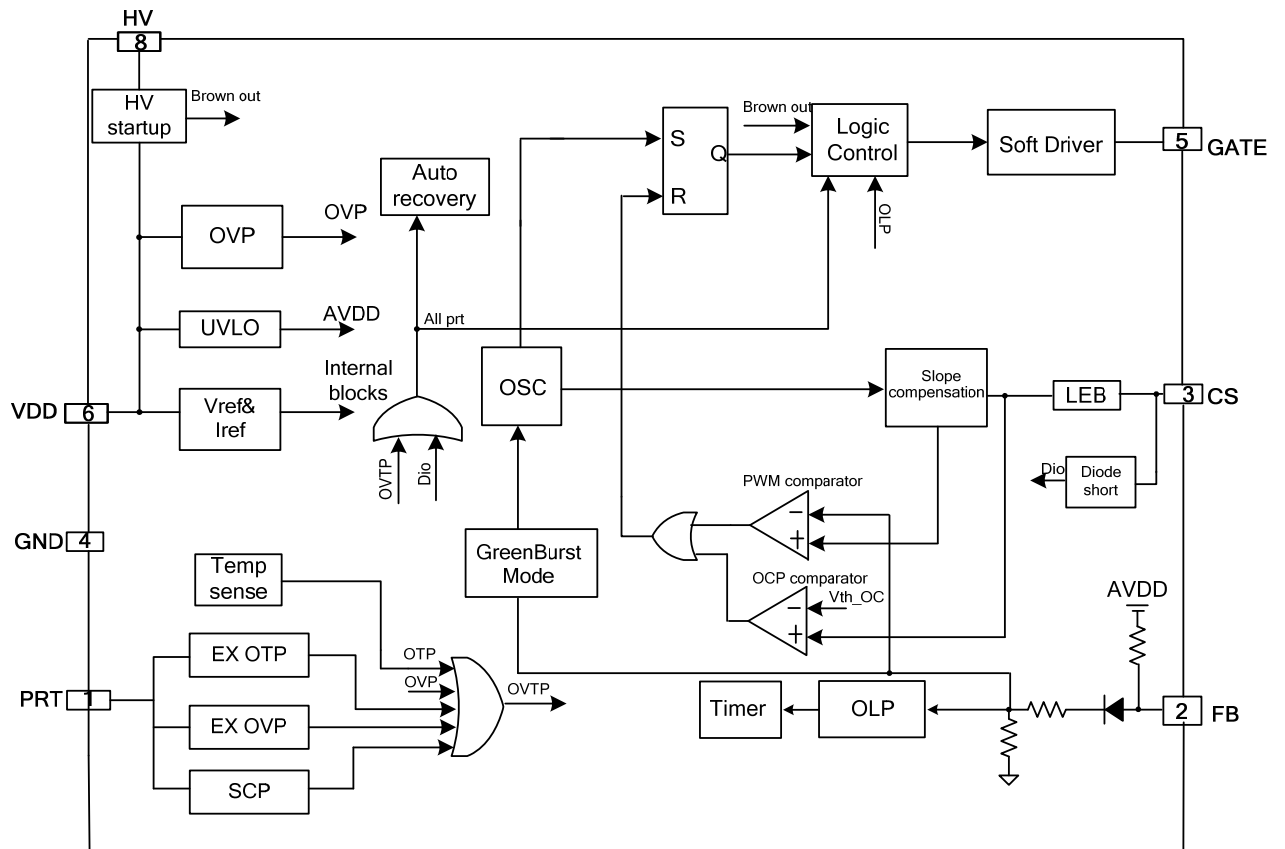


Y:Year Code
 WW:Week Code(01-52)
 ZZZ:Lot Code
 C:SOP8 Package
 P:Halogen-free Package
 C:Character Code
 S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust OVP/SCP trigger voltage and detect transformer core demagnetization. If both OTP and OVP/SCP are needed, a diode should be connected between PRT pin and the NTC resistor. If PRT pin float, output SCP is triggered .
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
3	CS	I	Current sense input
4	GND	P	Ground
5	Gate	O	Totem-pole gate driver output for power Mosfet
6	VDD	P	Power Supply
7	NC		
8	HV	P	Connected to the line input via resistors and diodes for startup and x-cap discharge, this PIN allows the brownout detection as well.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

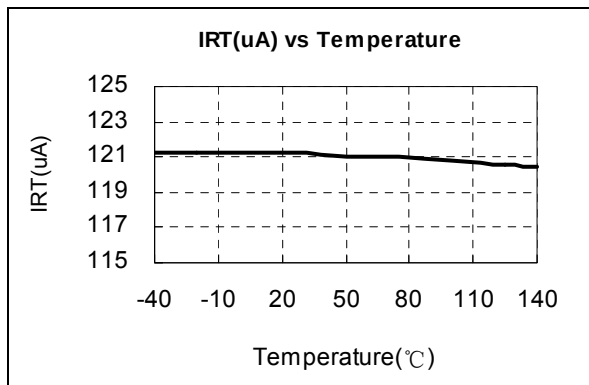
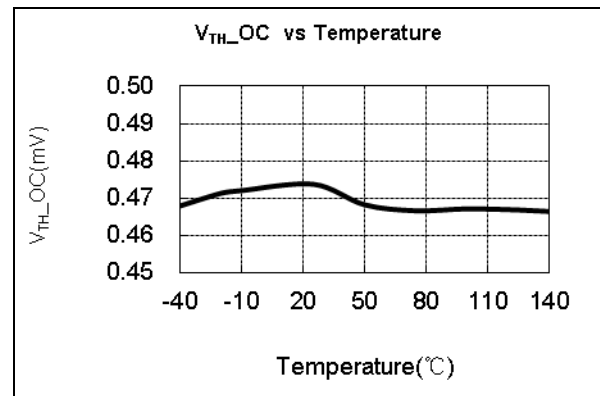
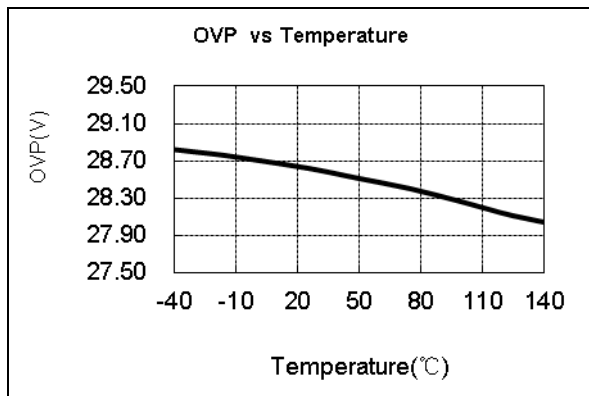
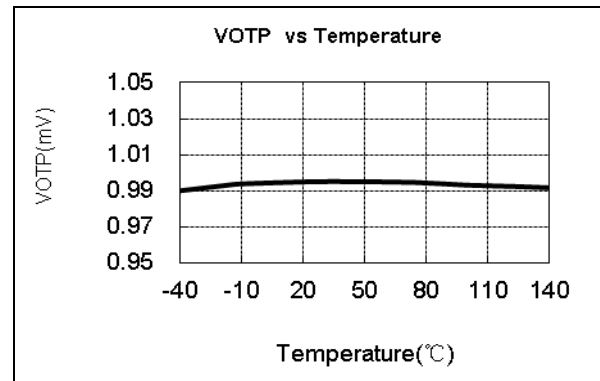
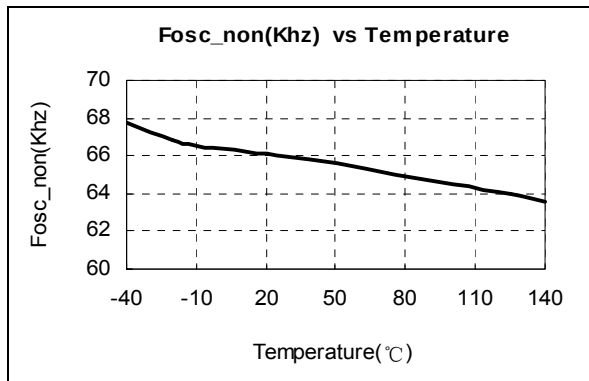
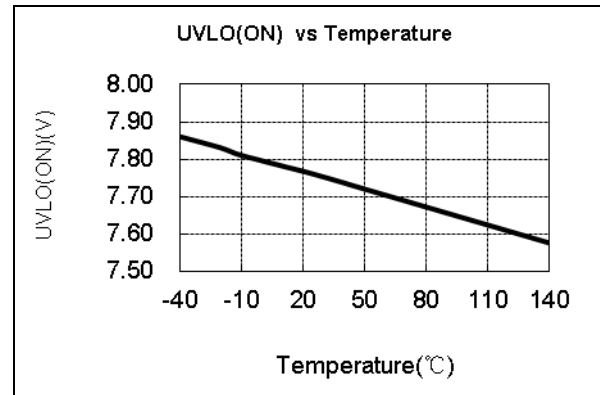
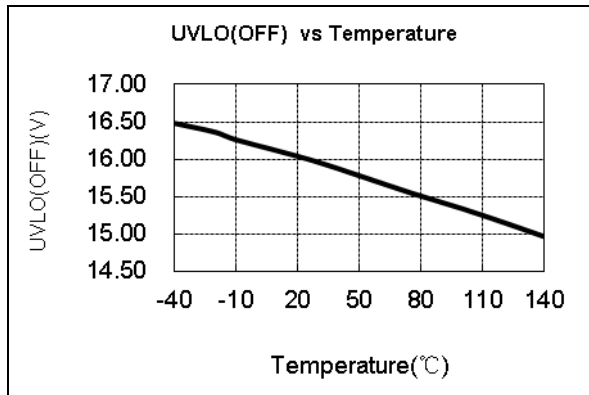
(T_A = 25°C, VDD=15V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
IHV1	Supply current from HV pin @VDD>1V	VDD=2V, HV=100V	1	2	3.5	mA
IHV2	Supply current from HV pin @VDD<1V	VDD=0.5V, HV=100V	0.3	0.57	0.85	mA
leakage	HV pin leakage current after startup	VDD=18V, HV=500V			10	uA
Supply Voltage (VDD)						
Istartup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	20	uA
I_VDD_Operation	Normal Operation Current	V _{FB} =3V, CL=1nF		2.5	3	mA
I_VDD_Burst	Burst Operation Current	V _{FB} =0.5V, CL=1nF		0.7	0.8	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		7.3	7.8	8.3	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		15	16	17	V
Vpull-up	Pull-up PMOS active			11		V
OVP	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	27.5	28.5	29.5	V
T _{D_rst}	Restart time for OCP / peak power protection occurs			1.4		s
Feedback Input Section(FB Pin)						
V _{FB} Open	V _{FB} Open Loop Voltage			5.1		V
Avcs	PWM input gain ΔVFB/ΔVCS			3.5		V/V
Maximum duty cycle	Max duty cycle @ VDD=14V, VFB=3V, VCS=0.3V		75	80	85	%
Vref_green	The threshold enter green mode			1.5		V
Vref_burst_H	The threshold exit burst mode			1.2		V
Vref_burst_L	The threshold enter burst mode			0.75		V
I _{FB_Short}	FB pin short circuit current	Short FB pin to GND and measure current		180		uA
V _{TH_OLP}	OLP FB Threshold Voltage		4.2	4.4		V
T _{D_OLP}	OLP Debounce Time		54	60	66	ms
Z _{FB_IN}	Input Impedance			30		KΩ
Current Sense Input(CS Pin)						
SST_CS	Soft start time of CS threshold			2.5		ms
T _{blanking}	Leading edge blanking time			320		ns
T _{D_OC}	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		80		ns
V _{TH_OC}	Internal Current Limiting Threshold Voltage with zero duty cycle		0.45	0.475	0.50	V
V _{TH_OC_clamp}	CS voltage clamping		0.725	0.755	0.785	V
Oscillator						

F _{OSC}	Normal Oscillation Frequency	VDD=15V, FB=3V,	60	65	70	KHz
Δf _{OSC}	Frequency jittering			+/-7		%
F _{shuffling}	Shuffling frequency			60		Hz
Δf _{Temp}	Frequency Temperature Stability			1		%
Δf _{VDD}	Frequency Voltage Stability			1		%
F _{Burst}	Burst Mode Switch Frequency			25		KHz
Gate driver						
VOL	Output low level @ VDD=15V, I _o =20mA				1	V
VOH	Output high level @ VDD=15V, I _o =20mA		8			V
V _{clamping}	Output clamp voltage			12		V
T _r	Output rising time 1.2V ~ 10.8V @ CL=1000pF			100		ns
T _f	Output falling time 10.8V ~ 1.2V @ CL=1000pF			50		ns
Brownout protection						
V _{th_bo_L}	Threshold voltage for Brownout	RHV=200 KΩ	63	70	77	VAC
V _{th_bo_H}	Threshold voltage for Brownout release	RHV=200 KΩ	70	77	85	VAC
T _{d_brownout}	Brownout debounce time		27	32	37	ms
PRT pin						
I _{bias}	Output bias current expect during OVP detection			20		uA
I _{RT}	Output current for external OTP detection		114	120	126	uA
V _{OTP}	Threshold voltage for external OTP		0.95	1.0	1.05	V
T _{d_ex_OTP}	EX OTP debounce time			60		Cycles
I _{output_ovp}	Current threshold for adjustable output OVP		170	180	190	uA
T _{d_output_ovp}	Output OVP debounce time			8		Cycles
I _{output_scp}	Current threshold for output short protection			42		uA
T _{d_scp_blank}				20		mS
On Chip OTP						
OTP Level				150		°C
OTP exit				125		°C

CHARACTERIZATION PLOTS

VDD = 18V, TA = 25°C condition applies if not otherwise noted.



OPERATION DESCRIPTION

OB5284C is a highly integrated current mode PWM control IC optimized for high performance, low standby power consumption and cost effective offline flyback converter applications. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Internal High Voltage Startup and Under Voltage Lockout (UVLO)

OB5284C integrates HV startup circuit, and provides about 2mA current to charge VDD pin during power on state from HV pin. When VDD voltage is higher than UVLO(OFF), the charge current is switched off. At this moment, the VDD capacitor provides current to OB5284C until the auxiliary winding of the main transformer starts to provide the operation current.

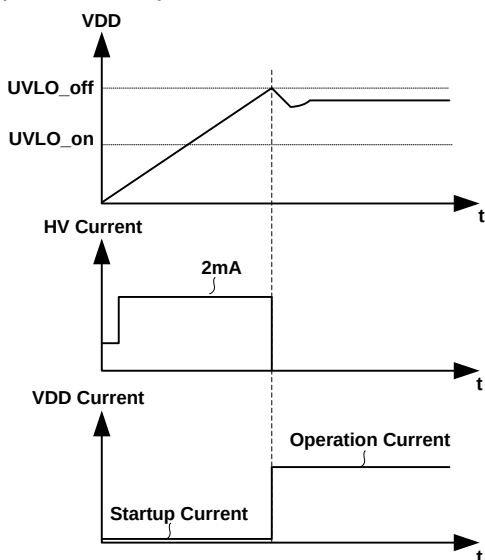


Fig1 Startup current timing

Operating Current

The typical operating current of OB5284C is 2.5mA. Good efficiency is achieved with this low operating current together with the 'Extended burst mode' control features.

Soft Start

OB5284C features an internal 2.5ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0V to the maximum level. Every restart up begins with a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in OB5284C. The

oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Oscillator Operation

During the full load power operation, OB5284C operates at a 65KHz (typical) fixed frequency. The efficiency and system cost is controlled at an optimal level. At light load, OB5284C enters the light load mode, where the output current is reduced. The switching losses are reduced by lowering the switching frequency.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB5284C current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic

oscillation and thus reduces the output ripple voltage.

Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Dual Function of External OTP and Output OVP/SCP

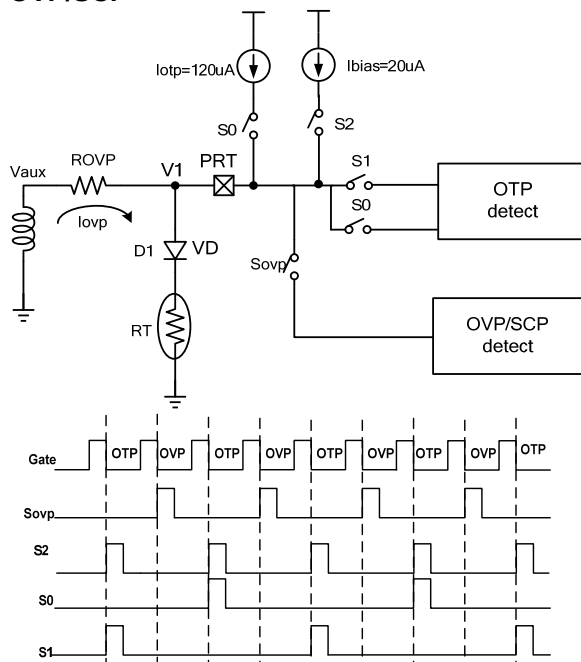


Fig2 PRT Pin protection timing

On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the fig2.

There is a 20uA(typical) bias current outflow when S2=1, that's S0= "1" or S1= "1". For external OTP detection, when switch control signal S1= "1", the 20uA (typical) current flows out from PRT pin. When switch control signal S0= "1", another 120uA (typical IRT) current flows out from PRT pin in addition to 20uA.

So the PRT pin voltage V1(s0) at phase S1="1" is:

$$V1(s1) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP \cdot 20\mu A}{ROVP + RT}$$

The PRT pin voltage V1(s1) at phase S0="1" is

$$V1(s0) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP(20\mu A + 120\mu A)}{ROVP + RT}$$

Vaux is the auxiliary winding demagnetization voltage.

VD is D1 forward voltage.

ROVP and RT are shown in fig2.

Voltage difference of ΔVotp at phase S0 and S1 phase is

$$\Delta V_{otp} = V1(s0) - V1(s1) = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 120\mu A$$

This voltage difference cancels the effect of D1 diode forward voltage.

When ΔVotp < VOTP (1.0V typical), external OTP auto recovery protection is triggered after 60(typical) PWM cycles debounce.

For output OVP detection, when Sovp= "1", loutput is equal to Vo/ROVP. If loutput is larger than 180uA (typical loutput_ovp), output OVP is triggered. The output OVP is calculated as

$$V_{outovp} = \frac{180\mu A \cdot N_{sec} \cdot ROVP}{N_{aux}} - V_{diode}$$

Nsec is transformer secondary winding turns, Naux is transformer auxiliary winding turns, Vdiode is the secondary output diode forward voltage.

OVP auto-recovery protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

For output SCP detection, when Sovp= "1", loutput is equal to Vo/ROVP. If loutput is always lower than 42uA (typical loutput_scp) within startup 20mS, output SCP is triggered. The SCP detection is disabled after startup 20mS.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including OCP, Over Temperature Protection (OTP), VDD and output Over Voltage Protection (OVP), output short Protection(SCP) and Under Voltage Lockout on VDD (UVLO).

With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output OCP limit over the universal input voltage range and its dependency on primary inductance and frequency is removed.

At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

OCP output Current Controls

At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter.

When primary side inductor current exceeds the OCP threshold, OCP timer will begin counting. After 60ms (typical), OCP protection occurs.

When OCP protection occurs, no GATE output and VDD begins discharging and charging until the duration is longer than 1.4S. Then VDD begins dropping until to UVLO(on) and later restarts.

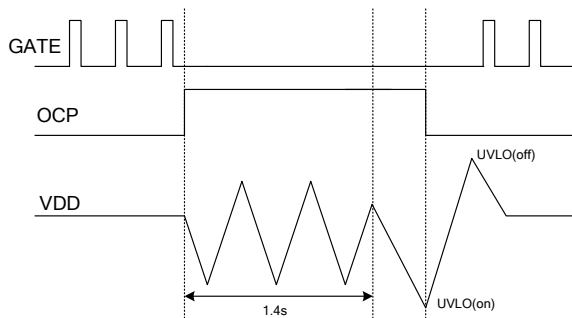


Fig3 Restart Timing when OCP occurs

Pin Floating and Short Protection

OB5284C provides PIN floating protection for all the pins and pin short protection for adjacent pins. In the cases when a pin is floating or two adjacent pins are shorted, Gate switching is disabled.

Intelligent AC off Detect with X-CAP discharge function

The HV pin is also used for AC off detection. When AC is off, the AC off state can be detected through HV pin. Then IC will provide a discharge path from HV pin to GND for the X-CAP discharge.

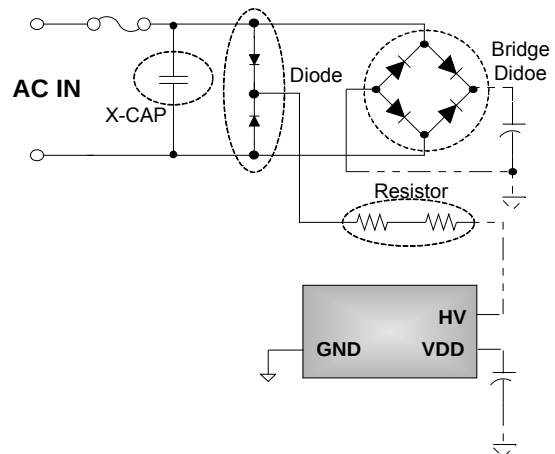


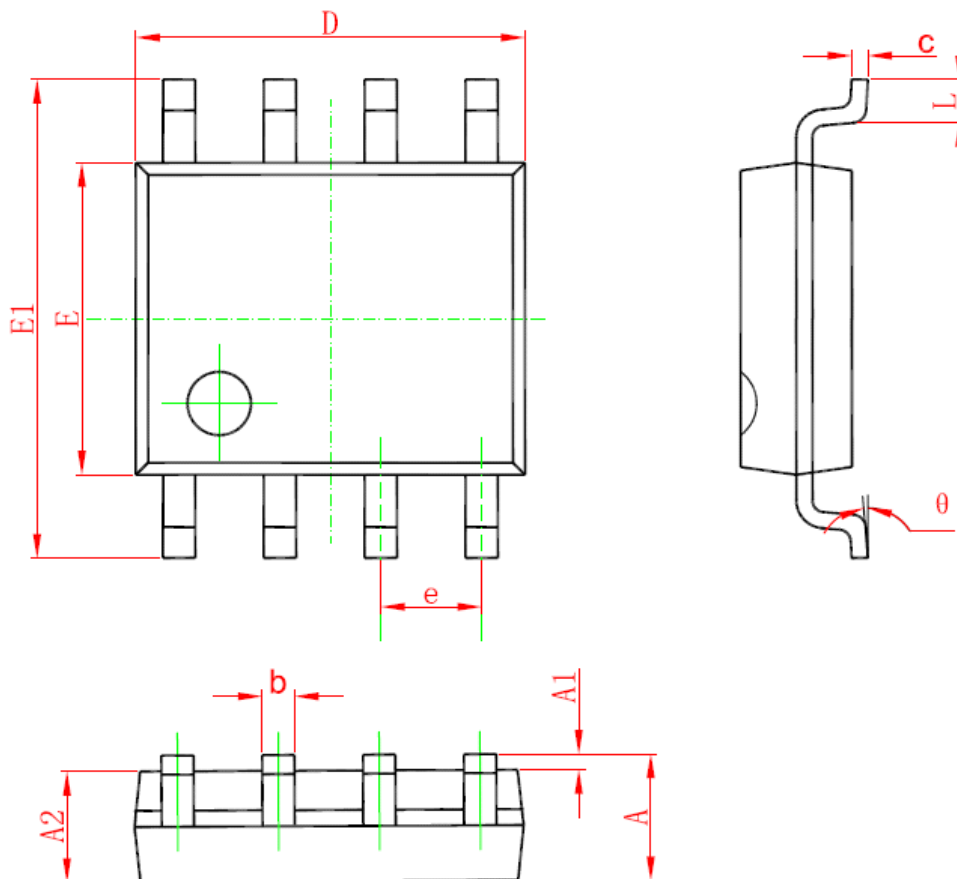
Fig4 X-CAP discharge circuit

Discharge circuit main components selection

Components	Voltage/Current Stress Range
Bridge Diode	≥600V ≥2A
Diode	≥1000V ≥1A
Resistor	R1206(1/4W)×2 Total impedance 200kΩ
X-CAP	0.1uF – 1.36uF

PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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