AXP15060 PMIC For Multi-Core High-Perfor---ance System

1. Features

- 6 DCDCs
  DCDC1: 1.5~3.4V, IMAX=2A
  DCDC2: 0.5~1.54V, IMAX=4A, DVM
  DCDC3: 0.5~1.54V, IMAX=4A, DVM
  DCDC4: 0.5~1.54V, IMAX=2.5A, DVM
  DCDC5: 0.8~1.84V, IMAX=2.5A, DVM
  DCDC6: 0.5~3.4V, IMAX=2.5A
  DCDC2 &DCDC3 can be set to dual-phase;
  DCDC4 & DCDC6 can be set to dual-phase.
  DVM(Dynamic Voltage scaling Management) ramp rate: 1step/15.625us and 1step/31.250us.
- 16 LDOs, 1 Switch
  RTCLDO: 1.8V/3.3V,IMAX=100mA
  ALDO1: 0.7~3.3V, IMAX=600mA
  ALDO2: 0.7~3.3V, IMAX=300mA
  ALDO3: 0.7~3.3V, IMAX=200mA
  ALDO4: 0.7~3.3V, IMAX=300mA
  ALDO5: 0.7~3.3V, IMAX=300mA
  BLDO1: 0.7~3.3V, IMAX=300mA
  BLDO2: 0.7~3.3V, IMAX=500mA
  BLDO3: 0.7~3.3V, IMAX=300mA
  BLDO4: 0.7~3.3V, IMAX=400mA
  BLDO5: 0.7~3.3V, IMAX=600mA
  CLDO1: 0.7~3.3V, IMAX=200mA
  CLDO2: .7~3.3V, IMAX=200mA
  CLDO3: 0.7~3.3V, IMAX=300mA
  CLDO4: 0.7~4.2V, IMAX=200mA
  CPUSLDO:V_{DDR}/2(source/sink),0.7~1.4V,IMAX=200mA, input is DCDC5.
  Switch: 0.1ohm switch, input is DCDC1, IMAX=1A, soft turn on.
- TWSI(Two Wire Serial Interface) supporting standard mode (100kHz) and quick mode (400kHz), slave address is 0x36 or 0x37(7 bits) by customer
- RSB(Reduced Serial Bus) supporting for Allwinner platform, slave address is 0x03A2 or 0x04E6 by customer
- Internal temperature sensor and protection
- Monitor DCDCs output voltage, send interrupt and over/under voltage protection
- Customization for start up sequence and default voltage

2. Applications

- VR, Tablet, Smartphone, Smart TV
- UMPC-like, Student Computer

3. Description

AXP15060 is a highly integrated power management IC targeting at applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate r quirements of power control.

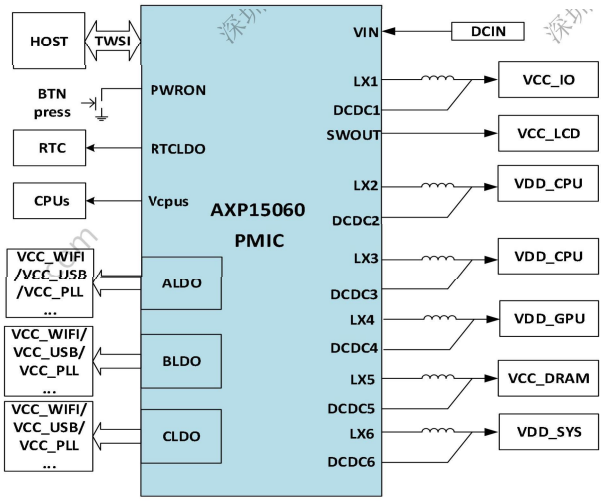
AXP15060 supports 23 channel power outputs (including 6 channel DCDC). To ensure the security and stability of the power system, AXP15060 integrates protection circuits such as over-voltage protection (OVP), under-voltage protection (UVP) and over temperature protection(OTP).

AXP15060 supports TWSI and RSB for system to dynamically adjust output voltages, enable power outputs and configure interrupt condition.

Device Information

Part Number	Package	Body Size
AXP15060	QFN-52	6mm * 6mm

Simplified Application Diagram



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4. Revision History

Revision	Date	Description
V 1.0	May 10,2018	Initial version
V 1.1	Aug.24,2018	1. Add ESD Ratings, Recommended Operating Conditions, Thermal Information, Application Information , PCB Layout Guideline, Storage and Baking. 2. Update Electrical Characteristics.
V 1.2	Feb.15,2019	1. Update Electrical Characteristics , Multi-Power Outputs and Register.
V 1.3	Jul.8,2020	1. Update Power On/Off & Reset and Function Block Diagram.
V 1.4	Dec.15,2020	1. Update Electrical Characteristics and Baking.

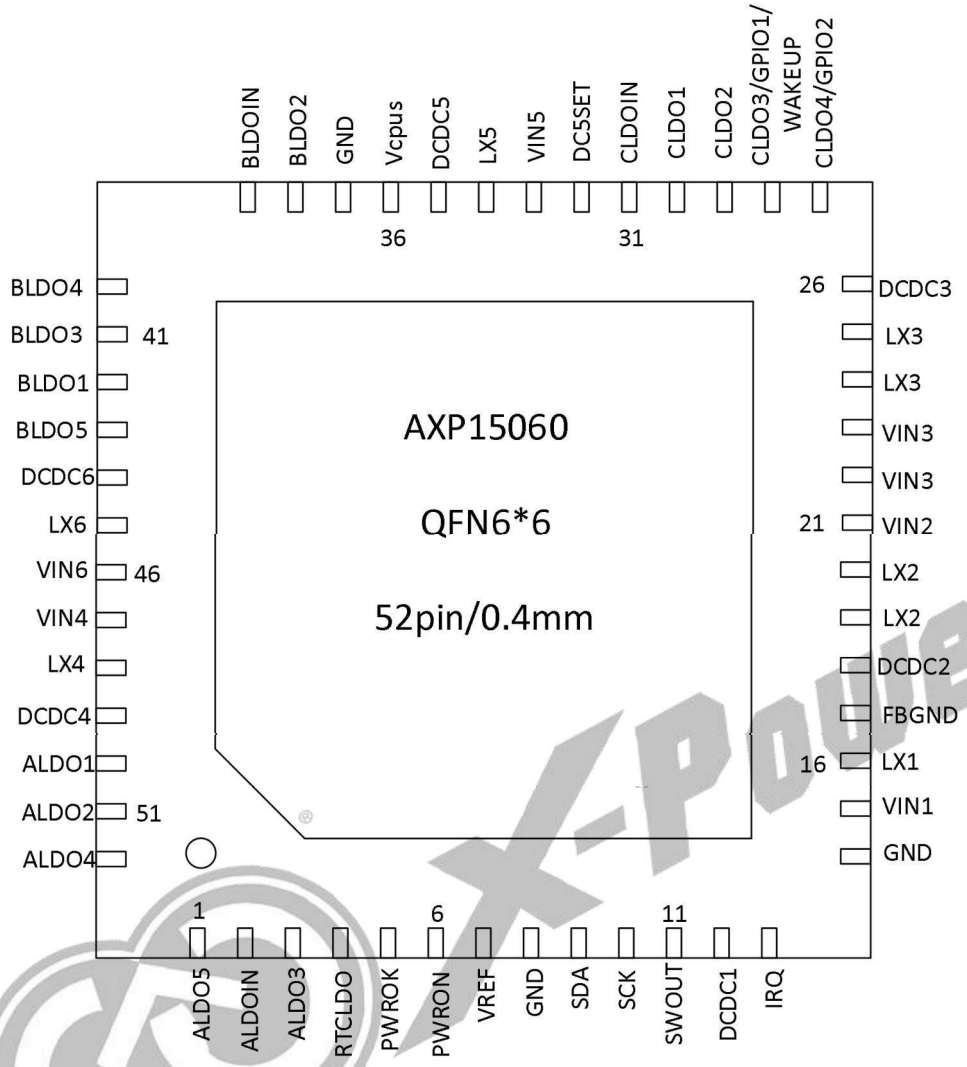
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5. Pin Configuration and Functions



Pin Description

Pin		I/O(1)	Description
NO.	Name		
1	ALDO5	PO	Output pin of ALDO5.
2	ALDOIN	PI	ALDO input source and internal analog power .
3	ALDO3	PO	Output pin of ALDO3.
4	RTCLDO	PO	RTC power output.
5	PWROK	DO	Power good indication output.
6	PWRON	IO	Power On-Off key input. Internal 100k pulled up.
7	VREF	AIO	Internal reference voltage.
8	GND	G	GND for internal analog circuit.
9	SDA	DIO	Data pin for serial interface. Connect SDA to the logic rail through a 2.2kΩ resistor.

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10	SCK	DI	Clock pin for serial interface. Connect SCL to the logic rail through a 2.2kΩ resistor.
11	SWOUT	PO	DCDC1 Switch output pin.
12	DCDC1	PI	DCDC1 feedback pin and Switch input source.
13	IRQ	PIO	IRQ output. Connect the IRQ to a logic rail via a 4.7kΩ resistor. The IRQ pin sends a low level signal to host to report device status and fault.
14	GND	G	GND for internal analog circuit.
15	VIN1	PI	DCDC1 input source.
16	LX1	PIO	Inductor pin for DCDC1.
17	FBGND	AI	Remote feedback signal of DCDC2GND. 1.If used, connect to the GND of DCDC2 load. 2.If not used, just connect to the nearby GND.
18	DCDC2	AI	DCDC2 feedback pin.
19、20	LX2	PIO	Inductor pin for DCDC2.
21	VIN2	PI	DCDC2 input source.
22、23	VIN3	PI	DCDC3 input source.
24、25	LX3	PIO	Inductor pin for DCDC3.
26	DCDC3	AI	DCDC3 feedback pin.
27	CLDO4/GPIO2	PO/GPIO	Output pin of CLDO4 or GPIO2 configured by REG 2CH[2:0].
28	CLDO3/GPIO1 /WAKEUP	PO/GPIO	Output pin of CLDO3 or GPIO1 or WAKEUP input pin configured by REG 2BH[6:5].
29	CLDO2	PO	Output pin of CLDO2.
30	CLDO1	PO	Output pin of CLDO1.
31	CLDOIN	PI	CLDO input source . Connected to PS or DCDC output.
32	DC5SET	AI	Setting DCDC5 default output voltage.
33	VIN5	PI	DCDC5 input source.
34	LX5	PIO	Inductor pin for DCDC5.
35	DCDC5	PI	DCDC5 feedback pin and CPUSLDO input source.
36	VCPUS	PO	Output pin of CPUSLDO.
37	GND	G	GND for internal analog circuit.
38	BLDO2	PO	Output pin of BLDO2.
39	BLDOIN	PI	BLDO input source. Connected to PS or DCDC output.
40	BLDO4	PO	Output pin of BLDO4.
41	BLDO3	PO	Output pin of BLDO3.
42	BLDO1	PO	Output pin of BLDO1.
43	BLDO5	PO	Output pin of BLDO5.
44	DCDC6	AI	DCDC6 feedback pin.
45	LX6	PIO	Inductor pin for DCDC6.
46	VIN6	PI	DCDC6 input source.

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47	VIN4	PI	DCDC4 input source.
48	LX4	PIO	Inductor pin for DCDC4.
49	DCDC4	AI	DCDC4 feedback pin.
50	ALDO1	PO	Output pin of ALDO1 and RTC input source .
51	ALDO2	PO	Output pin of ALDO2.
52	ALDO4	PO	Output pin of ALDO4.
EP	EP	PG	Exposed Pad, need to be connected to system ground.

(1)**O** for output, **I** for input, **IO** for input/output, **D** for digital, **A** for analog, **P** for power, and **G** for ground.

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6. Specifications

6.1 Absolute Maximum Ratings(1)

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
ALDOIN/BLDOIN/CLDOIN/VIN1/VIN2/VIN3/VIN4/VIN5/VIN6	Input Voltage	-0.3	7.5	V
Ta	Operating Temperature Range	-40	85	℃
T_J	Junction Temperature Range	-40	125	℃
Ts	Storage Temperature Range	-40	150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)		300	℃

(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Human body model(HBM)(1)	±3000	V
	Charged device model(CDM)(2)	±750	V

(1) Reference:ESDA/JEDEC JS-001-2014. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) Reference:ESDA/JEDEC JS-002-2014. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VIN	Input voltage	3.0	5.5	V

6.4 Thermal Information

Thermal Metric(1)		VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	34.2	℃/W
θ_{JB}	Junction-to-board thermal resistance	17.5	
θ_{JC}	Junction-to-case(top) thermal resistance	12.7	

(1)Thermal metrics are calculated refer to JEDEC document JESD51.

6.5 Electrical Characteristics

V_{IN} =5V, T_A= -40℃~85℃

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
PMIC Under Voltage						
V_{OFF}	PMIC Under Voltage Power off		2.6		3.0	V

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Off Mode Current						
I_{OFF}	OFF Mode Current	ALDOIN=5V		30		μA
Logic						
V_{IL}	Logic Low Input Voltage			0.3		V
V_{IH}	Logic High Input Voltage			1.2		V
RSB						
ADDRESS	Slave Address			0x03A2		
TWSI						
V_{CC}	Input Supply Voltage			3.3		V
ADDRESS	TWSI Slave Address (7 bits)			0x36		
f_{SCK}	Clock Operating Frequency			400		kHZ
t_f	Clock Data Fall Time	2.2kΩ Pull High		60		ns
t_r	Clock Data Rise Time	2.2kΩ Pull High		100		ns
DCDC						
f_{OSC}	Oscillator Frequency	Default		3		MHz
DCDC1						
V_{IN1}	VIN1 Input Voltage		V_{OFF}		5.5	V
I_{VIN1}	Input Current	PFM Mode I_{DC1OUT} =0		60		μA
I_{DC1OUT}	Available Output Current			2000		mA
V_{DC1OUT}	Output Voltage Range		1.5		3.4	V
V_{DC1_STEP}	Output Voltage Step			100		mV/step
V_{DC1_RIPPLE}	Output Voltage Ripple	PFM Mode	-30		+30	mV
		PWM Mode	-10		+10	mV
V_{DC1_ACC}	Output Voltage Accuracy	PFM	-2%		+4%	
		PWM	-2.5%		+2.5%	
V_{DC1_OVP}	Over Voltage Protection			120%* V_{DC1OUT}		V
V_{DC1_UVP}	Under Voltage Protection			85%* V_{DC1OUT}		V
DCDC2						
V_{IN2}	VIN2 Input Voltage		V_{OFF}		5.5	V
I_{VIN2}	Input Current	PFM Mode I_{DC2OUT} =0		70		μA
I_{DC2OUT}	Available Output Current			4000		mA
V_{DC2OUT}	Output Voltage Range		0.5		1.54	V
V_{DC2_STEP}	Output Voltage Step	V_{DC2OUT}=0.5~1.2V		10		mV/step
		V_{DC2OUT}=1.22~1.54V		20		mV/step
V_{DC2_RIPPLE}	Output Voltage Ripple	PFM Mode	-30		+30	mV
		PWM Mode	-10		+10	mV
V_{DC2_ACC}	Output Voltage Accuracy	PFM V_{DC2OUT}<=1V	-20		+40	mV
		PFM V_{DC2OUT}>1V	-2%		+4%	

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		PWM	V_{DC2OUT}<=1V	-15		+15	mV
			V_{DC2OUT}>1V	-1.5%		+1.5%	
V_{DC2_OVP}	Over Voltage Protection				130%* V_{DC2OUT}		V
V_{DC2_UVP}	Under Voltage Protection				85%* V_{DC2OUT}		V
DCDC3							
V_{IN3}	VIN3 Input Voltage			V_{OFF}		5.5	V
I_{VIN3}	Input Current	PFM Mode I_{DC3OUT} =0			60		uA
I_{DC3OUT}	Available Output Current				4000		mA
V_{DC3OUT}	Output Voltage Range			0.5		1.54	V
V_{DC3_STEP}	Output Voltage Step	V_{DC3OUT}=0.5~1.2V			10		mV/step
		V_{DC3OUT}=1.22~1.54V			20		mV/step
V_{DC3_RIPPLE}	Output Voltage Ripple	PFM Mode		-30		+30	mV
		PWM Mode		-10		+10	mV
V_{DC3_ACC}	Output Voltage Accuracy	PFM	V_{DC3OUT}<=1V	-20		+40	mV
			V_{DC3OUT}>1V	-2%		+4%	
		PWM	V_{DC3OUT}<=1V	-15		+15	mV
			V_{DC3OUT}>1V	-1.5%		+1.5%	
V_{DC3_OVP}	Over Voltage Protection				130%* V_{DC3OUT}		V
V_{DC3_UVP}	Under Voltage Protection				85%* V_{DC3OUT}		V
DCDC4							
V_{IN4}	VIN4 Input Voltage			V_{OFF}		5.5	V
I_{VIN4}	Input Current	PFM Mode I_{DC3OUT} =0			60		uA
I_{DC4OUT}	Available Output Current				2500		mA
V_{DC4OUT}	Output Voltage Range			0.5		1.54	V
V_{DC4_STEP}	Output Voltage Step	V_{DC4OUT}=0.5~1.2V			10		mV/step
		V_{DC4OUT}=1.22~1.54V			20		mV/step
V_{DC4_RIPPLE}	Output Voltage Ripple	PFM Mode		-30		+30	mV
		PWM Mode		-10		+10	mV
V_{DC4_ACC}	Output Voltage Accuracy	PFM	V_{DC4OUT}<=1V	-20		+40	mV
			V_{DC4OUT}>1V	-2%		+4%	
		PWM	V_{DC4OUT}<=1V	-15		+15	mV
			V_{DC4OUT}>1V	-1.5%		+1.5%	
V_{DC4_OVP}	Over Voltage Protection				130%* V_{DC4OUT}		V
V_{DC4_UVP}	Under Voltage Protection				85%*		V

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				V_{DC4OUT}		
DCDC5						
V_{IN5}	VIN5 Input Voltage		V_{OFF}		5.5	V
I_{VIN5}	Input Current	PFM Mode I_{DC3OUT} =0		60		uA
I_{DC5OUT}	Available Output Current			2500		mA
V_{DC5OUT}	Output Voltage Range		0.8		1.84	V
V_{DC5_STEP}	Output Voltage Step	V_{DC5OUT}=0.8~1.12V		10		mV/step
		V_{DC5OUT}=1.14~1.84V		20		mV/step
V_{DC5_RIPPLE}	Output Voltage Ripple	PFM Mode	-30		+30	mV
		PWM Mode	-10		+10	mV
V_{DC5_ACC}	Output Voltage Accuracy	PFM V_{DC5OUT}<=1V	-20		+40	mV
		PFM V_{DC5OUT}>1V	-2%		+4%	
		PWM V_{DC5OUT}<=1V	-15		+15	mV
		PWM V_{DC5OUT}>1V	-1.5%		+1.5%	
V_{DC5_OVP}	Over Voltage Protection			130%* V_{DC5OUT}		V
V_{DC5_UVP}	Under Voltage Protection			85%* V_{DC5OUT}		V
DCDC6						
V_{IN6}	VIN6 Input Voltage		V_{OFF}		5.5	V
I_{VIN6}	Input Current	PFM Mode I_{DC3OUT} =0		60		uA
I_{DC6OUT}	Available Output Current			2500		mA
V_{DC6OUT}	Output Voltage Range		0.5		3.4	V
V_{DC6_STEP}	Output Voltage Step			100		mV/step
V_{DC6_RIPPLE}	Output Voltage Ripple	PFM Mode	-30		+30	mV
		PWM Mode	-10		+10	mV
V_{DC6_ACC}	Output Voltage Accuracy	PFM V_{DC6OUT}<=1V	-20		+40	mV
		PFM V_{DC6OUT}>1V	-2%		+4%	
		PWM V_{DC6OUT}<=1V	-25		+25	mV
		PWM V_{DC6OUT}>1V	-2.5%		+2.5%	
V_{DC6_OVP}	Over Voltage Protection	V_{DC6OUT}<1.5V		130%* V_{DC6OUT}		V
		V_{DC6OUT}>=1.5V		120%* V_{DC6OUT}		
V_{DC6_UVP}	Under Voltage Protection			85%* V_{DC6OUT}		V
RTCLDO						
V_{RTCLDO}	Output Voltage	I_{RTC_VCC}=1mA	-3.0%	1.8/ 3.3	3.0%	V

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I_{RTCLDO}	Output Current			100		mA
ALDO						
V_{ALDOIN}	ALDOIN Input Voltage		V_{OFF}		5.5	V
ALDO1						
V_{ALDO1}	Output Voltage Range	I_{ALDO1}=1mA	0.7		3.3	V
V_{ALDO1_STEP}	Output Voltage Step			100		mV/step
V_{ALDO1_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{ALDO1}	Output Current			600		mA
I_Q	Quiescent Current			120		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO1}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
ALDO2						
V_{ALDO2}	Output Voltage Range	I_{ALDO2}=1mA	0.7		3.3	V
V_{ALDO2_STEP}	Output Voltage Step			100		mV/step
V_{ALDO2_ACC}	Output Voltage Accuracy		-2.0%		+2.0%	
I_{ALDO2}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO2}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
ALDO3						
V_{ALDO3}	Output Voltage Range	I_{ALDO3}=1mA	0.7		3.3	V
V_{ALDO3_STEP}	Output Voltage Step			100		mV/step
V_{ALDO3_ACC}	Output Voltage Accuracy		-2.0%		+2.0%	
I_{ALDO3}	Output Current			200		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO3}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
ALDO4						
V_{ALDO4}	Output Voltage Range	I_{ALDO4}=1mA	0.7		3.3	V
V_{ALDO4_STEP}	Output Voltage Step			100		mV/step
V_{ALDO4_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{ALDO4}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO4}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
ALDO5						

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V_{ALDO5}	Output Voltage Range	I_{ALDO5}=1mA	0.7		3.3	V
V_{ALDO5_STEP}	Output Voltage Step			100		mV/step
V_{ALDO5_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{ALDO5}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO5}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
BLDO						
V_{BLDOIN}	BLDOIN Input Voltage		V_{OFF}		5.5	V
BLDO1						
V_{BLDO1}	Output Voltage Range	I_{BLDO1}=1mA	0.7		3.3	V
V_{BLDO1_STEP}	Output Voltage Step			100		mV/step
V_{BLDO1_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{BLDO1}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO1}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
BLDO2						
V_{BLDO2}	Output Voltage Range	I_{BLDO2}=1mA	0.7		3.3	V
V_{BLDO2_STEP}	Output Voltage Step			100		mV/step
V_{BLDO2_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{BLDO2}	Output Current			500		mA
I_Q	Quiescent Current			80		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO2}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
BLDO3						
V_{BLDO3}	Output Voltage Range	I_{BLDO3}=1mA	0.7		3.3	V
V_{BLDO3_STEP}	Output Voltage Step			100		mV/step
V_{BLDO3_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{BLDO3}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO3}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
BLDO4						
V_{BLDO4}	Output Voltage Range	I_{BLDO4}=1mA	0.7		3.3	V

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V_{BLDO4_STEP}	Output Voltage Step			100		mV/step
V_{BLDO4_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{BLDO4}	Output Current			400		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO4}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
BLDO5						
V_{BLDO5}	Output Voltage Range	I_{BLDO5}=1mA	0.7		3.3	V
V_{BLDO5_STEP}	Output Voltage Step			100		mV/step
V_{BLDO5_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{BLDO5}	Output Current			600		mA
I_Q	Quiescent Current			90		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO5}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
CLDO						
V_{CLDOIN}	CLDOIN Input Voltage		V_{OFF}		5.5	V
CLDO1						
V_{CLDO1}	Output Voltage Range	I_{CLDO1}=1mA	0.7		3.3	V
V_{CLDO1_STEP}	Output Voltage Step			100		mV/step
V_{CLDO1_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{CLDO1}	Output Current			200		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO1}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
CLDO2						
V_{CLDO2}	Output Voltage Range	I_{CLDO2}=1mA	0.7		3.3	V
V_{CLDO2_STEP}	Output Voltage Step			100		mV/step
V_{CLDO2_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{CLDO2}	Output Current			200		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO2}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
CLDO3						
V_{CLDO3}	Output Voltage Range	I_{CLDO3}=1mA	0.7		3.3	V
V_{CLDO3_STEP}	Output Voltage Step			100		mV/step

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V_{CLDO3_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{CLDO3}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO3}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
CLDO4						
V_{CLDO4}	Output Voltage Range	I_{CLDO4}=1mA	0.7		4.2	V
V_{CLDO4_STEP}	Output Voltage Step			100		mV/step
V_{CLDO4_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{CLDO4}	Output Current			200		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO4}=10mA, 1kHz		70		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
CPUSLDO						
V_{CPUS}	Output Voltage	As reference of V_{DDR}		V_{DDR}/2		
		As General Purpose LDO, I_{CPUS}=1mA	0.7		1.4	V
V_{CPUS_STEP}	Output Voltage Step	As General Purpose LDO		50		mV/step
V_{CPUS_ACC}	Output Voltage Accuracy		-3.0%		+3.0%	
I_{CPUS}	Output Current	As reference of V_{DDR}		30		mA
		As General Purpose LDO		200		mA
I_Q	Quiescent Current	As General Purpose LDO		70		μA
PSRR	Power Supply Rejection Ratio	V_{DC5OUT}=1.84V, I_{CPUS}=10mA, 1kHz		60		dB
e_N	Output Noise,0-80kHz			40		μV_{RMS}
SWOUT						
R_{SWOUT}	Internal Ideal Resistance	PIN to PIN		100		mΩ

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6.6 Typical Characteristics

Table 6-1 Typical Characteristics

DCDC1 Efficiency VS Different Load	Figure 6-1
DCDC2 Efficiency VS Different Load	Figure 6-2
DCDC3 Efficiency VS Different Load	Figure 6-3
DCDC4 Efficiency VS Different Load	Figure 6-4
DCDC5 Efficiency VS Different Load	Figure 6-5
DCDC6 Efficiency VS Different Load	Figure 6-6

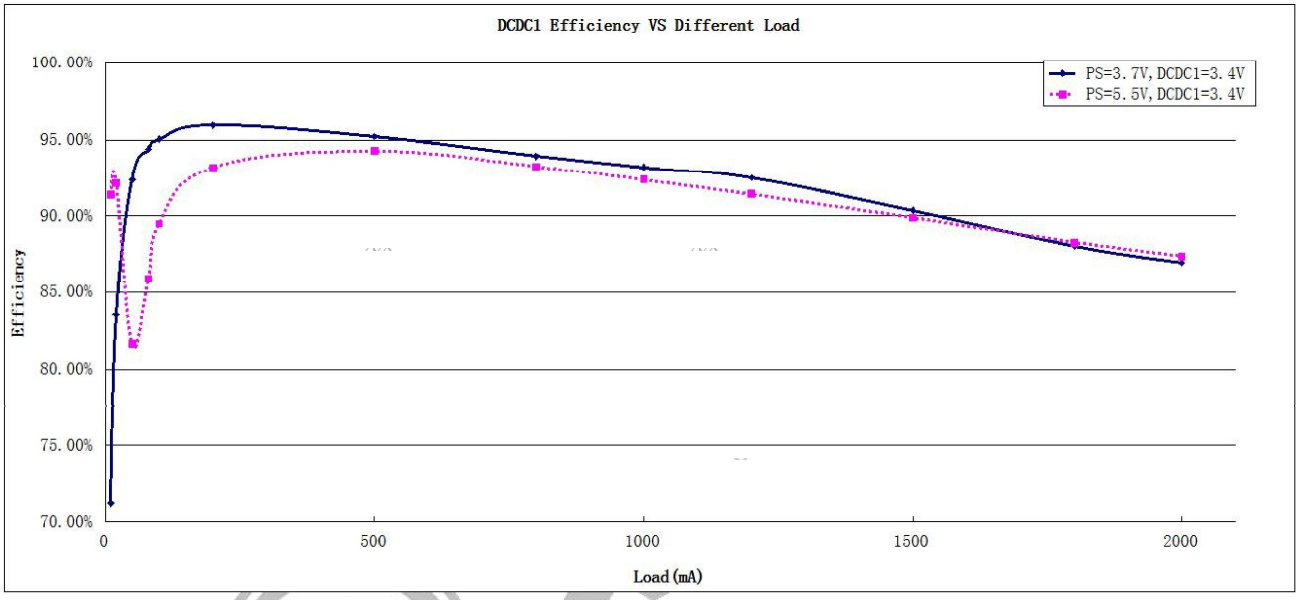


Figure 6-1 DCDC1 Efficiency VS Different Load

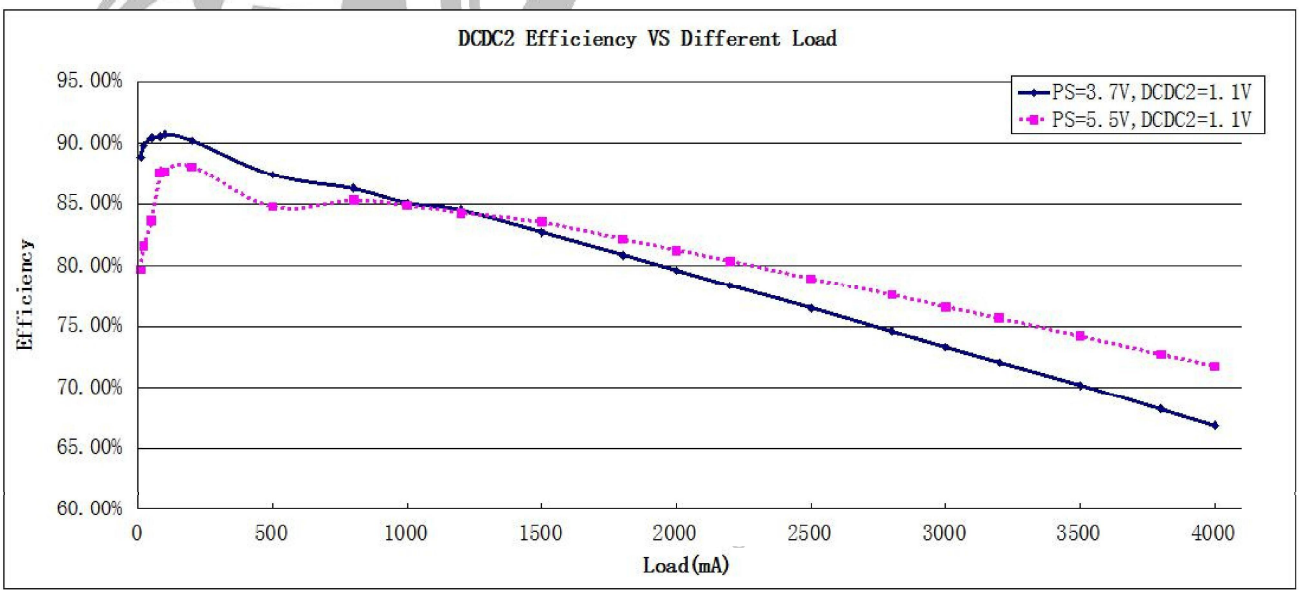


Figure 6-2 DCDC2 Efficiency VS Different Load

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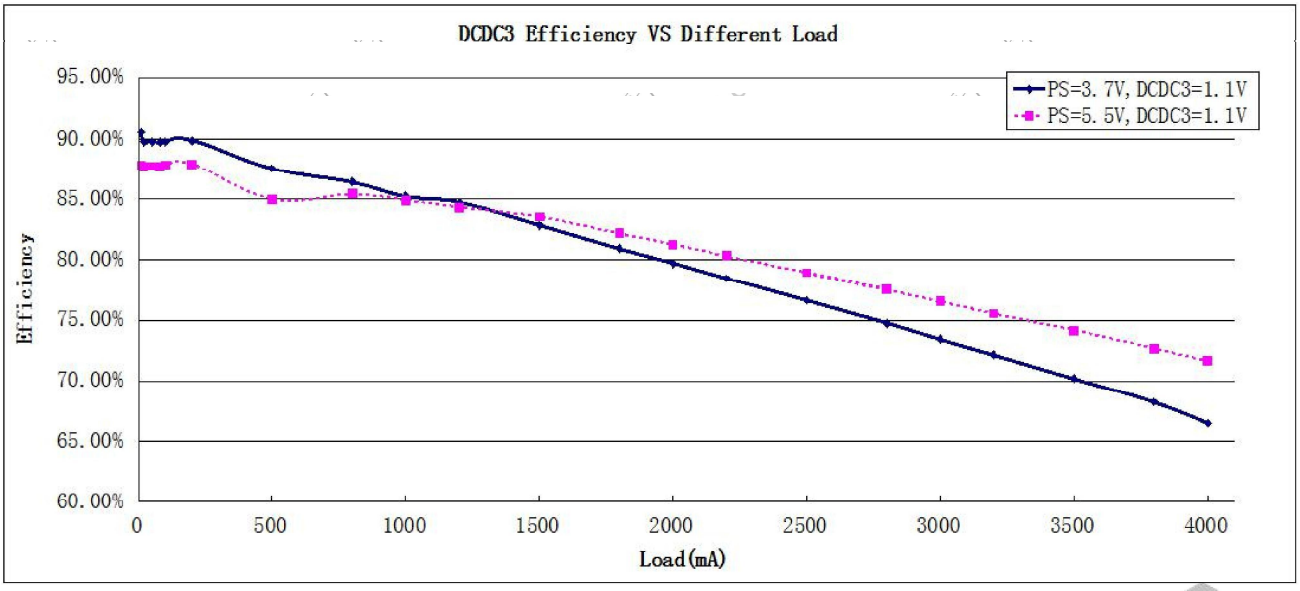


Figure 6-3 DCDC3 Efficiency VS Different Load

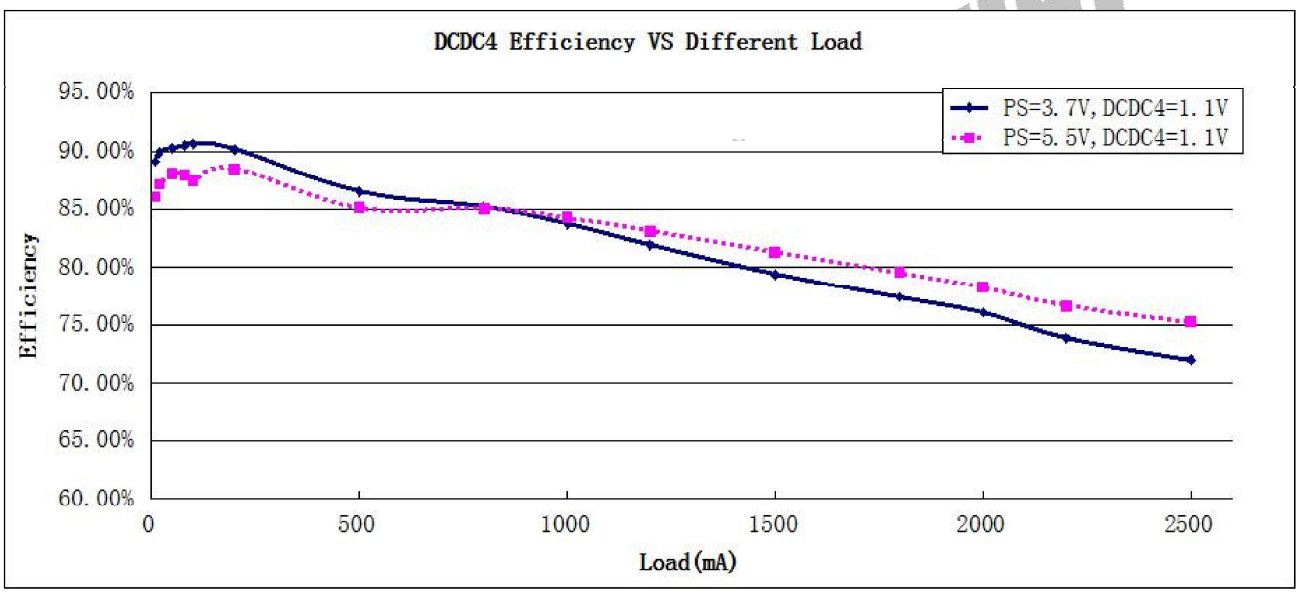


Figure 6-4 DCDC4 Efficiency VS Different Loa

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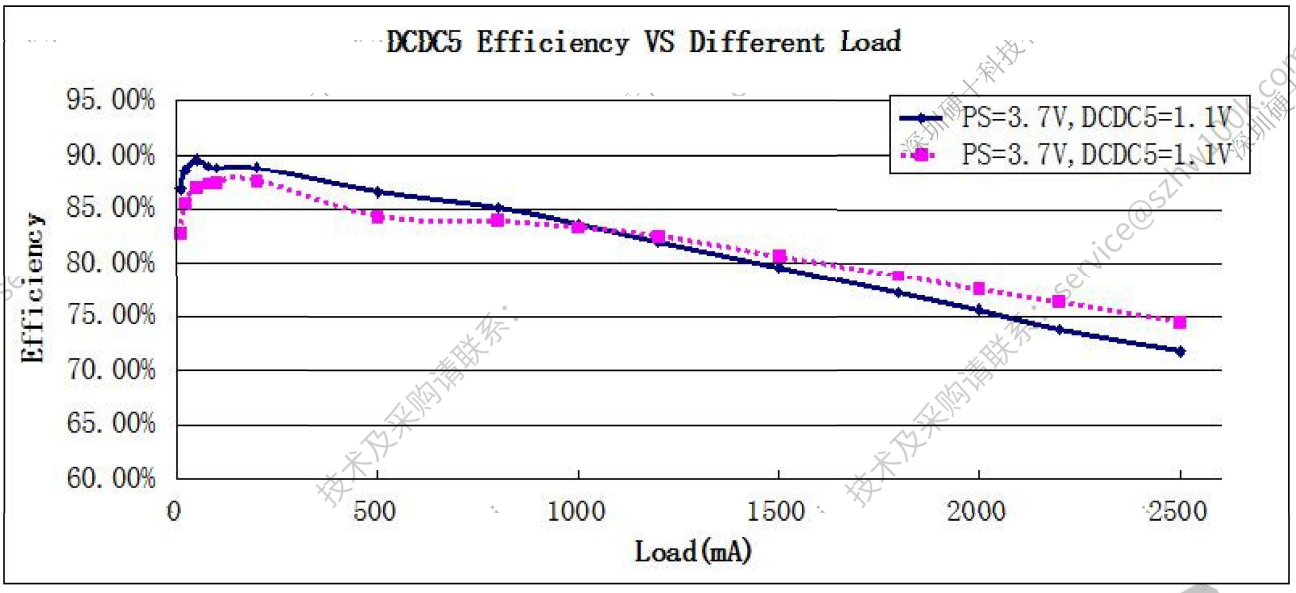


Figure 6-5 DCDC5 Efficiency VS Different Load

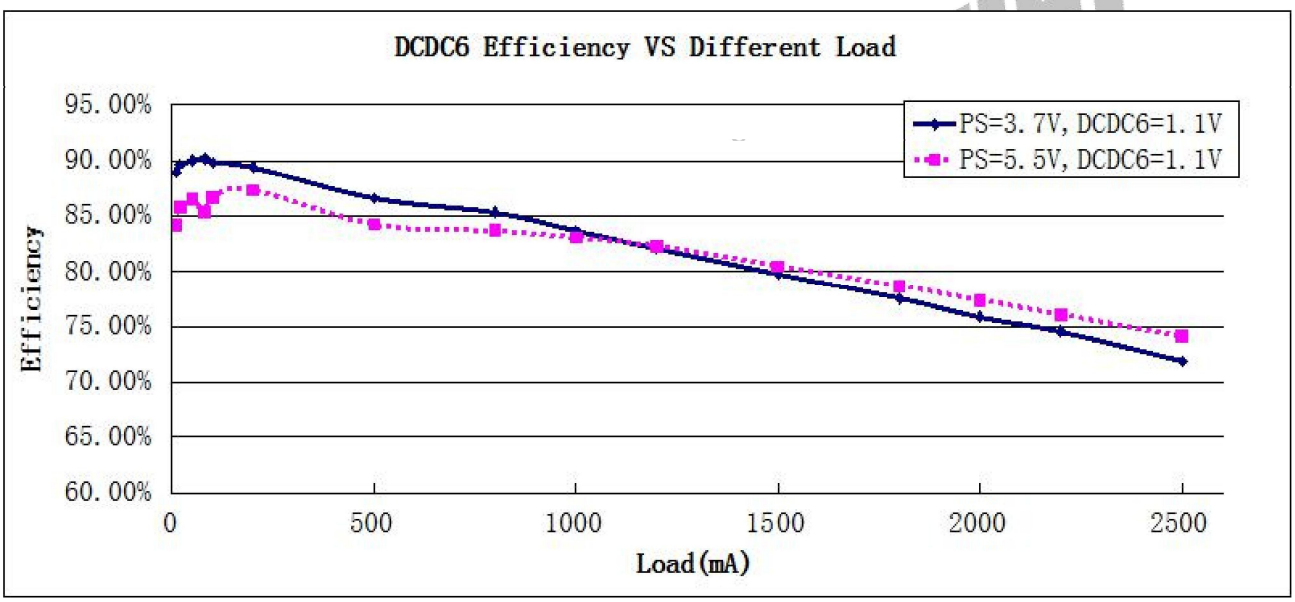


Figure 6-6 DCDC6 Efficiency VS Different Load

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7. Detail Description

7.1 Overview

AXP15060 is a highly integrated power management IC targeting at applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

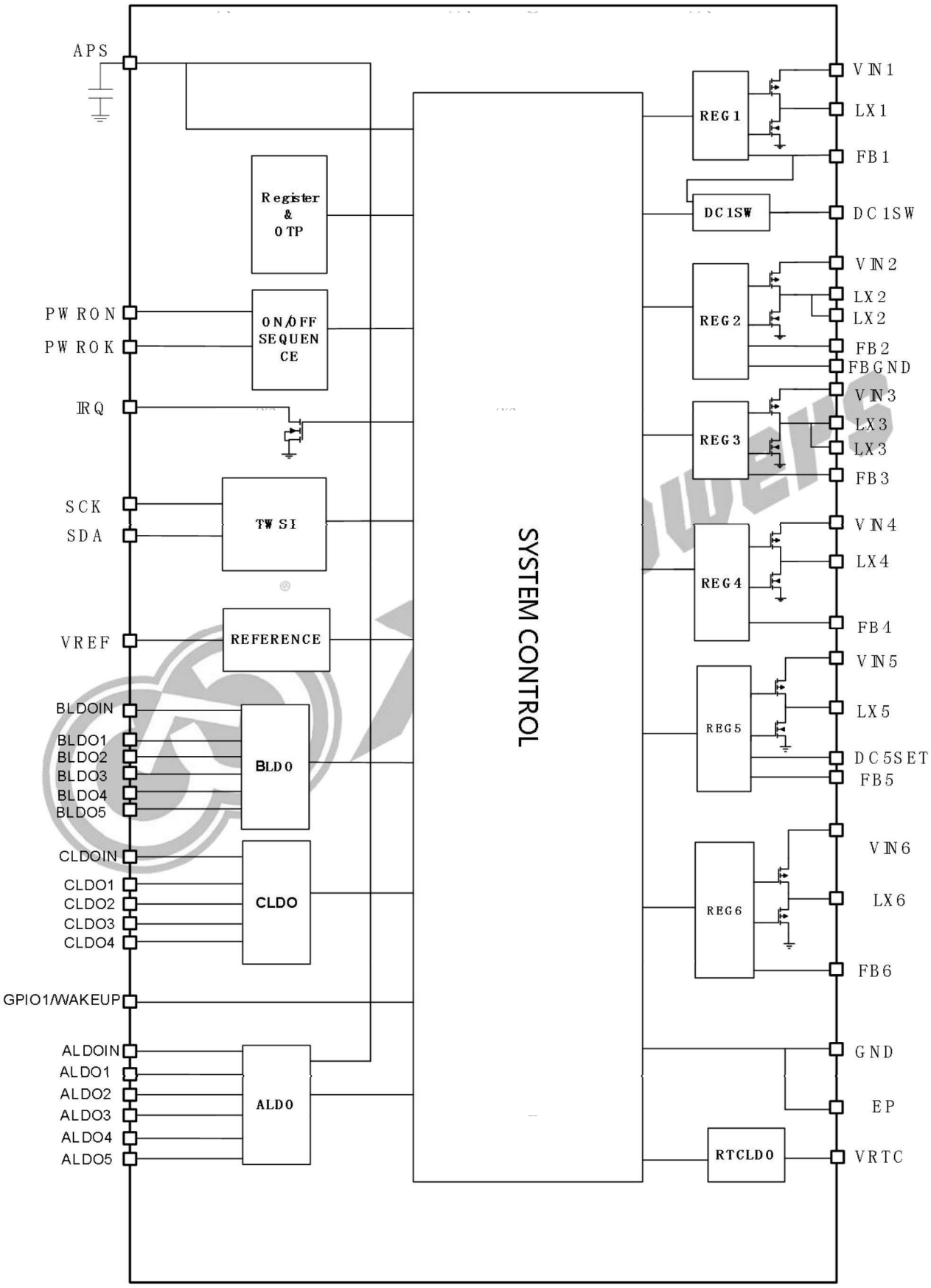
AXP15060 supports 23 channel power outputs(including 6 channel DCDC).To ensure the security and stability of the power system, AXP15060 integrates protection circuits such as over-voltage protection(OVP), under-voltage protection(UVP) and over-temperature protection(OTP).

AXP15060 provides a fast interface(Two Wire Serial Interface, TWSI) for system to dynamically adjust output voltages, enable power outputs and configure interrupt condition.

AXP15060 is available in 6mm x 6mm 52-pin QFN package.

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7.2 Function Block Diagram



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7.3 Serial Interface Communi ation

AXP15060 supports TWSI protocol and performs as a TWSI slave device with address 0x6C/0x6D or 0x6E/0x6F by customer. When AXP15060 powers on, SCK/SDA pin of TWSI will be pulled up to IO Power and then Host can adjust and monitor AXP15060 with rich feedback information.

Besides, AXP15060 supports RSB for Allwinner platform with address 0x03A2 or 0x04E6 by customer.

Note: “Host” here refers to system processor.

7.4 Power On/Off & Reset

PMIC has power off and power on status. When at off state, all voltage outputs are turned off except RTCLDO and VREF. At this time, the total power consumption is typically 30uA.

Power on-off Key (POK)

EN/PWRON pin can be configured as PWRON pin or EN pin by customization. The default is PWRON pin. The Power on-off Key (POK) can be connected between PWRON pin and GND of AXP15060. AXP15060 can automatically identify the four status(Long-press ,Short- ress ,Negative edge, Positive edge) and then correspond respectively.

Power on

1.When EN/PWRON pin is customized as PWRON pin, power on sources include:

(1).POK. AXP15060 can be powered on by pressing and holding POK for a period of time that longer than “ONLEVEL”.

(2).ALDOINGOOD low go high. The function can be configured by customization.

(3).IRQ Low level. When REG1FH[7]=1 and IRQ pin is low level for more than 16ms, AXP15060 will be powered on

2.When EN/PWRON pin is customized as EN pin , AXP15060 can be powered on by EN pin from low to high(>0.6V).

After power on, DC-DC and LDO will be soft booted in preset timing sequence.

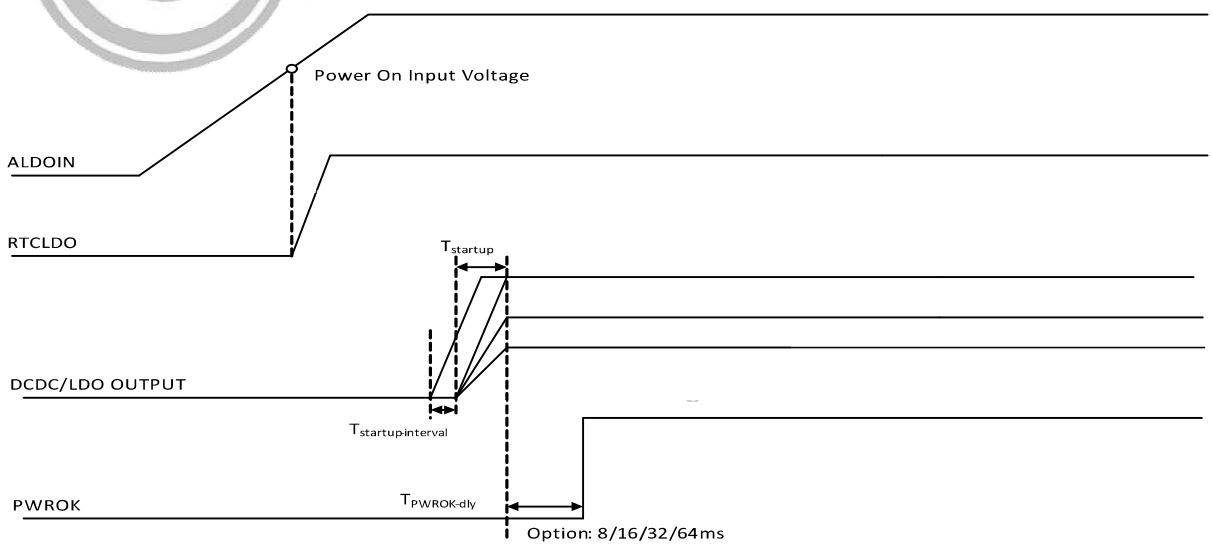


Figure 7-1 Power On Sequence

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Power Off

1.When EN/PWRON pin is customized a PWRON pin, power off sources include:

(1).POK. AXP15060 can be powered off by pressing and holding POK for a period of time that longer than "OFFLEVEL". The function can be configured by REG36H[3] and REG36H[2] decides whether the PMIC auto turns on or not when it shuts down after OFFLEVEL POK.

(2).Write "1" to REG32H[7] .

(3).ALDOINGOOD high go low. When ALDOIN<VOFF or ALDOIN>5.8V, AXP15060 will be powered off. The default of VOFF is 2.6V which can be configured by REG1FH[5:3].

(4).The output voltage of DCDC is 15% lower than the setting value. The function can be configured by REG1EH[6:1].

(5).The output voltage of DCDC is much larger than their setting. The function can be configured by REG1EH[0].

(6).Die temperature is over the warning level2(125℃)。The function can be configured by REG32H[1].

2.When EN/PWRON pin is customize as EN pin , AXP15060 can be powered off by EN pin from hig to low.

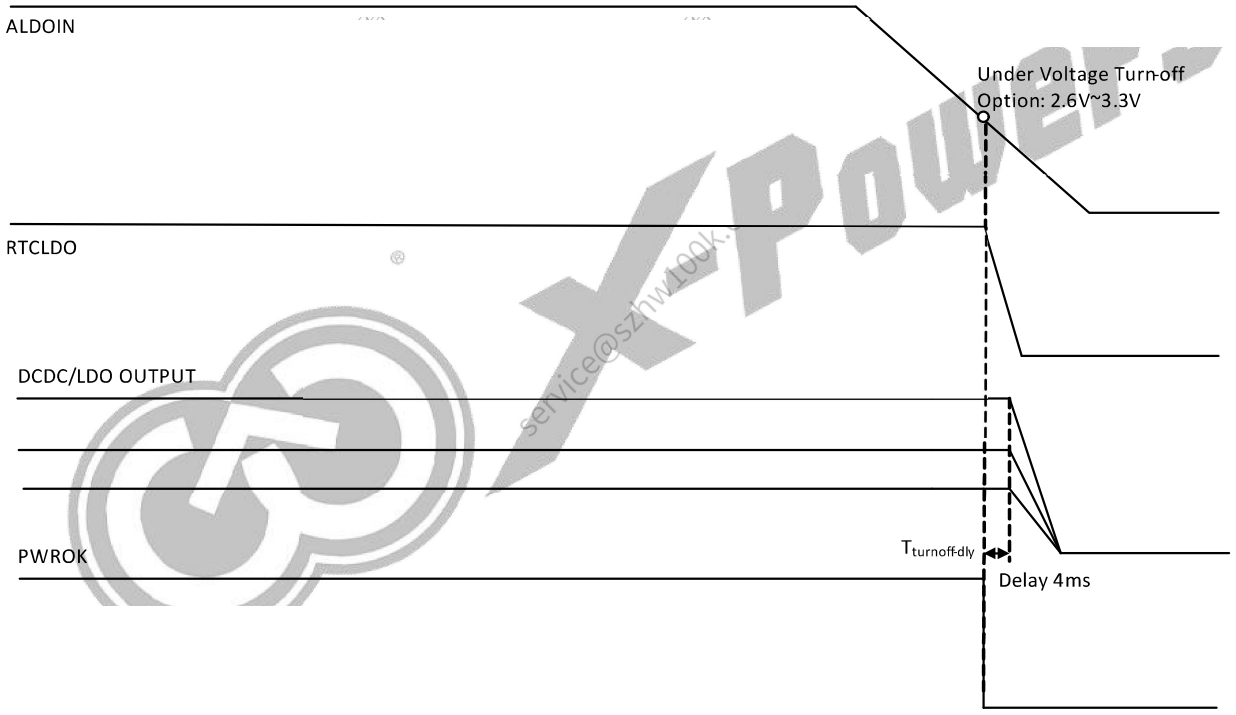


Figure 7-2 Power Off Sequence

Sleep and wakeup

When the running system needs to enter Sleep mode, Maybe one or several power outputs should be disabled or changed to other voltage. Wakeup can be initiated by the following sources:

1.Software wakeup (REG31H[5] is set to 1)

2.POK negative edge IRQ(EN/PWRON pin is configured as PWRON pin and REG41H[3] is set to 1)

3.POK long press IRQ(EN/PWRON pin is configured as PWRON pin and REG41H[0] is set to 1)

4.IRQ pin wakeup(REG1FH[7]=1 and IRQ pin is low level for more than 16ms)

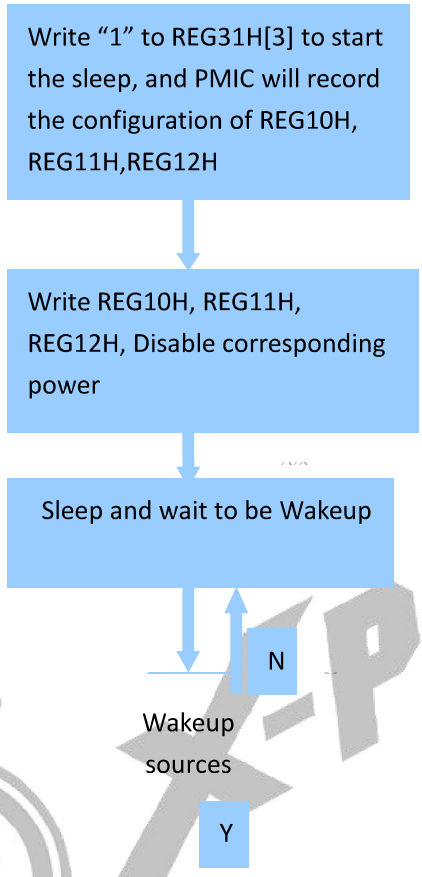
5.Wakeup pin input(REG2BH[6:5]=11 and the active level is detected; the active level can be configured by REG2BH[7])

These sources will make the all PMIC power outputs resume to the default voltage or the setting voltage, which is

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configured by REG31H[6], and all shutdown powers will resume by the startup sequence. The voltage can be set at any time before wakeup.

See the control process under sleep and wakeup modes as below:



eset

The PMIC has system reset and power on reset.

- System reset

System reset means the registers will be reset when PMIC powers off. When at system reset state, all voltage outputs are turned off except RTCLDO and VREF. There are two ways of system reset.

(1).PWROK drive low.

The PWROK pin can be used as the reset signal of application system. During AXP15060 startup, PWROK outputs low level, which will be pulled up to startup the system after output voltage reaches the regulated value.

When application system works normally, If the PWROK pin is driven low by external key or other reasons, the PMIC will be restarted. The function can be configured by REG32H[4].

(2).Write “1” to REG32H[6] to restart the PMIC.

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- Power on reset

Power on reset means the registers will be reset when ALDOIN voltage drops below 2.1V. When at power on reset state, all voltage outputs are turned off including RTCLDO and VREF. There are two ways of power on reset.
(1).POK. Press and hold POK for a period of time that longer than 16s. The function is configured by REG32H[0].
(2).Remove the power and then power on again.

7.5 Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP15060.

Output Path	Type	Default Voltage	Startup Sequence	Application Suggestion	Load Capacity(Max)
DCDC1	BUCK	Customization	Customization	IO/USB	2000mA
DCDC2	BUCK			CPU	4000mA
DCDC3	BUCK			GPU	4000mA
DCDC4	BUCK			SYS	2500mA
DCDC5	BUCK			DDR	2500mA
DCDC6	BUCK			LDO	2500mA
ALDO1	LDO			N/A	600mA
ALDO2	LDO			N/A	300mA
ALDO3	LDO			N/A	200mA
ALDO4	LDO			N/A	300mA
ALDO5	LDO			N/A	300mA
BLDO1	LDO			N/A	300mA
BLDO2	LDO			N/A	500mA
BLDO3	LDO			N/A	300mA
BLDO4	LDO			N/A	400mA
BLDO5	LDO			N/A	600mA
CLDO1	LDO			N/A	200mA
CLDO2	LDO			N/A	200mA
CLDO3	LDO			N/A	300mA
CLDO4	LDO			N/A	200mA
VCPUS	LDO			CPUs/Reference of DDR	200mA
RTC-LDO	LDO		Always on	RTC	100mA
DC1SW	Switch	OFF	OFF	N/A	1000mA

AXP15060 includes six synchronous step-down DCDCs, sixteen LDOs and one switch. The work frequency of DC-DC is 3MHz. External small inductors and capacitors can be connected. In addition, 6-ch DCDCs can be set in fixed PWM mode or auto mode (automatically switchable according to the load). See register REG1BH.

DCDC2/3/4/5 has DVM enable option. In DVM mode, when there is a change in the output voltage, DCDC will change to the new targeted value step by step. It supports two kinds of DVM slope:1step/15.625us and 1step/31.250us. The slope can be chosen by REG1AH[5].

DCDC2 and DCDC3 as well as DCDC4 and DCDC6 can be configured as dual phase DCDC to meet the high current requirement. When DCDC2/3 and DCDC4/6 are working as dual phase DCDC, the parameter setting is only

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controlled by the registers of DCDC2 and DCDC4.

DCDC5 voltage configuration is depended on the DC5SET pin and customization. When the DC5SET pin is connected to 1.8V, the default output is 1.5V. When a resistor(Rs) is connected between the DC5SET pin and GND, the default output is 1.1V. When DC5SET pin is connected to GND, the default output is 1.2V. When the DC5SET pin is floating, the default output is depended on customization.

DC5SET	GND	1.8V	Rs (20k~200k)	floating
Default voltage of DCDC5	1.2V	1.5V	1.1V	Customization

AXP15060 can configure the default voltage, the startup sequence and other control of all power output.
Startup sequence:The startup sequence has eight levels from 0 to 7. When the sequence is 0, it means the output is booted at the first step. When the sequence code is 1, it means the output is booted at the second step. When the sequence is 7, it means the output is not booted.
Default voltage setting: The default voltage of each channel can be set to each step within the output range.

7.6 Multi-Function Pin Description

EN/PWRON

EN/PWRON can be configured as EN pin or PWRON PIN by customization. When it is configured as PWRON pin, a Power on-off Key (POK) can be connected between PWRON pin and GND. When it is configured as EN pin, it can be used for dial switch.

CLDO4/GPIO2

It can be configured as LDO or GPIO. Please refer to REG2CH[2:0] Instruction for details.

CLDO3/GPIO1/WAKEUP

It can be configured as LDO or GPIO or WAKEUP pin. Please refer to REG2BH[6:5] Instruction for details.

7.7 Interrupt

PMIC Interrupt Controller monitors the trigger events such as over voltage, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enable bits are set to 1 (Refer to registers REG40H and REG41H), corresponding IRQ status will be set to 1 (Refer to registers REG48H and REG49H), and IRQ pin (open drain) will be pulled down. When host detects triggered IRQ signal, host will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing “1” to status bit.

The input edge IRQ of GPIO will only function when CLDO3/GPIO1/WAKEUP and CLDO4/GPIO2 are set as GPIO.

Bit	IRQ	DESCRIPTION
REG48_[7]	IRQ1	DCDC6 under voltage
REG48_[6]	IRQ2	DCDC5 under voltage
REG48_[5]	IRQ3	DCDC4 under voltage
REG48_[4]	IRQ4	DCDC3 under voltage
REG48_[3]	IRQ5	DCDC2 under voltage

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REG48_[2]	IRQ6	DCDC1 under voltage
REG48_[1]	IRQ7	IC temperature over level2
REG48_[0]	IRQ8	IC temperature over level1
REG49_[5]	IRQ9	GPIO2 IRQ
REG49_[4]	IRQ10	POK positive edge
REG49_[3]	IRQ11	POK negative edge
REG49_[2]	IRQ12	GPIO1 IRQ
REG49_[1]	IRQ13	POK short press
REG49_[0]	IRQ14	POK long press

7.8 Register

7.8.1 Register List

Address	Description	R/W	Default
00	Power ON Source	R	
04-07	4 data buffers	R/W	00H
10	on-off control1	R/W	XXH
11	on-off control2	R/W	XXH
12	on-off control3	R/W	XXH
13	DCDC1 Voltage control	R/W	XXH
14	DCDC2 Voltage control	R/W	XXH
15	DCDC3 Voltage control	R/W	XXH
16	DCDC4 Voltage control	R/W	XXH
17	DCDC5 Voltage control	R/W	XXH
18	DCDC6 Voltage control	R/W	XXH
19	ALDO1 Voltage control	R/W	XXH
1A	DCDC mode control1	R/W	X0H
1B	DCDC mode control2	R/W	00H
1E	output monitor control & off discharge	R/W	81H
1F	IRQ & PWROK & Voff setting	R/W	07H
20	ALDO2 Voltage control	R/W	XXH
21	ALDO3 Voltage control	R/W	XXH
22	ALDO4 Voltage control	R/W	XXH
23	ALDO5 Voltage control	R/W	XXH
24	BLDO1 Voltage control	R/W	XXH
25	BLDO2 Voltage control	R/W	XXH
26	BLDO3 Voltage control	R/W	XXH
27	BLDO4 Voltage control	R/W	XXH
28	BLDO5 Voltage control	R/W	XXH
29	CLDO1 Voltage control	R/W	XXH
2A	CLDO2 Voltage control	R/W	XXH

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Address	Description	R/W	Default
2B	CLDO3 voltage control & CLDO3/GPIO1/Wakeup control	R/W	XXH
2C	CLDO4/GPIO2 control	R/W	00H
2D	CLDO4 Voltage control	R/W	XXH
2E	CPUSLDO Voltage control	R/W	0XH
31	power wakeup CTRL	R/W	00H
32	power disable & power down sequence	R/W	24H
36	POK setting	R/W	59H
3E	Interface mode select	RW	00H
40	IRQ Enable1	R/W	03H
41	IRQ Enable2	R/W	03H
48	IRQ Status1	R/W	00H
49	IRQ Status2	R/W	00H

7.8.2 Register Description

REG 00H：Power ON source indication

Reset：system reset

Bit	Description	R/W
7-6	Reserved	R
5	Startup by ALDOINGOOD from L go H when EN is High	R
4	Startup by EN from L go H when ALDOINGOOD is High	R
3	Startup by IRQ pin	R
2	Startup by PWRON Press	R
1	Reserved	R
0	Startup by ALDOIN from L go H	R

REG 04H-07H：4 Data Buffers

Default：00H

Reset：Power on reset

REG 10H：Output power on-off control 1

Default：XXH

Reset：system reset

Bit	Description		R/W	Default
7-6	Reserved		RW	0
5	DCDC-6 on-off control	0-off; 1-on	RW	Customization
4	DCDC-5 on-off control	0-off; 1-on	RW	
3	DCDC-4 on-off control	0-off; 1-on	RW	
2	DCDC-3 on-off control	0-off; 1-on	RW	
1	DCDC-2 on-off control	0-off; 1-on	RW	
0	DCDC-1 on-off control	0-off; 1-on	RW	

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REG 11H：Output power on-off control 2

Default：XXH

Reset：system reset

Bit	Description		R/W	Default
7	BLDO3 on-off control	0-off; 1-on	RW	Customization
6	BLDO2 on-off control	0-off; 1-on	RW	
5	BLDO1 on-off control	0-off; 1-on	RW	
4	ALDO5 on-off control	0-off; 1-on	RW	
3	ALDO4 on-off control	0-off; 1-on	RW	
2	ALDO3 on-off control	0-off; 1-on	RW	
1	ALDO2 on-off control	0-off; 1-on	RW	
0	ALDO1 on-off control	0-off; 1-on	RW	

REG 12H：Output power on-off control 3

Default：XXH

Reset：system reset

Bit	Description		R/W	Default
7	Switch on-off control	0-off; 1-on	RW	0
6	CPUSLDO on-off control	0-off; 1-on	RW	Customization
5	CLDO4 on-off control	0-off; 1-on	RW	
4	CLDO3 on-off control	0-off; 1-on	RW	
3	CLDO2 on-off control	0-off; 1-on	RW	
2	CLDO1 on-off control	0-off; 1-on	RW	
1	BLDO5 on-off control	0-off; 1-on	RW	
0	BLDO4 on-off control	0-off; 1-on	RW	

REG 13H：DC/DC 1 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	DCDC-1 voltage setting bit4-0: 1.5~3.4V，100mV/step，20steps	RW	Customization

REG 14H：DC/DC 2 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-2 voltage setting bit6-0: 0.5~1.2V，10mV/step，71steps 1.22~1.54V，20mV/step，17steps	RW	Customization

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REG 15H：DC/DC 3 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-3 voltage setting bit6-0: 0.5~1.2V，10mV/step，71steps 1.22~1.54V，20mV/step，17steps	RW	Customization

REG 16H：DC/DC 4 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-4 voltage setting bit6-0: 0.5~1.2V，10mV/step，71steps 1.22~1.54V，20mV/step，17steps	RW	Customization

REG 17H：DC/DC 5 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-5 voltage setting bit6-0: 0.8~1.12V，10mV/step，33steps 1.14~1.84V，20mV/step，36steps	RW	Customization

REG 18H：DC/DC 6 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	DCDC-6 voltage setting bit4-0: 0.5~3.4V，100mV/step，30steps	RW	Customization

REG 19H：ALDO1 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO1 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 1AH：DCDC mode control 1

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Default：X0H

Reset：system reset

Bit	Description		R/W	Default
7	DCDC 4&6 poly-phase control 0：no poly-phase；　1：poly-phase		RW	Customization
6	DCDC 2&3 poly-phase control 0：no poly-phase；　1：poly-phase		RW	
5	DCDC DVM voltage ramp control	0：1step/15.625us 1：1step/31.250us	RW	0
4	Reserved		RW	0
3	DCDC-5 DVM on-off control	0：disable 1：enable	RW	0
2	DCDC-4 DVM on-off control		RW	0
1	DCDC-3 DVM on-off control		RW	0
0	DCDC-2 DVM on-off control		RW	0

REG 1BH：DCDC mode control 2

Default：00H

Reset：system reset

Bit	Description		R/W	Default
7-6	Reserved		RW	0
5	DCDC-6 PFM/PWM control	0：auto switch 1：always PWM	RW	0
4	DCDC-5 PFM/PWM control		RW	0
3	DCDC-4 PFM/PWM control		RW	0
2	DCDC-3 PFM/PWM control		RW	0
1	DCDC-2 PFM/PWM control		RW	0
0	DCDC-1 PFM/PWM control		RW	0

REG 1EH：Output monitor control & Discharge

Default：81H

Reset：Power on reset

Bit	Description	R/W	Default
7	Internal off-Discharge enable for Buck & LDO & SWITCH 0: disable　1: enable	RW	1
6	DCDC-6 85% low voltage turn off PMIC function 0: disable　1: enable	RW	0
5	DCDC-5 85% low voltage turn off PMIC function 0: disable　1: enable	RW	0
4	DCDC-4 85% low voltage turn off PMIC function 0: disable　1: enable	RW	0
3	DCDC-3 85% low voltage turn off PMIC function 0: disable　1: enable	RW	0
2	DCDC-2 85% low voltage turn off PMIC function 0: disable　1: enable	RW	0

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1	DCDC-1 85% low voltage turn off PMIC function 0: disable 1: enable	RW	0
0	If voltage of DCDC is over 20%(30%) of the setting value， the PMIC shutdown or not.（OVP） 0: not shutdown 1: shutdown	RW	1

REG 1FH： IRQ & PWROK & VOFF setting

Default：07H

Reset：Power on reset

Bit	Description	R/W	Default
7	IRQ pin turn on or wakeup AXP15060 function enable 0: disable 1: enable	RW	0
6	Reserved	RW	0
5-3	VOFF setting bit2-0: 2.6~3.3V，0.1V/step，8steps	RW	000
2	Enable for 4ms delay when PMIC power off normally 0：disable 1：enable	RW	1
1-0	Delay time between PWROK signal and power good time 00：8ms；01：16ms；10：32ms；11：64ms	RW	11

REG 20H： ALDO2 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO2 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 21H： ALDO3 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO3 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 22H： ALDO4 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO4 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

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REG 23H：ALDO5 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO5 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 24H：BLDO1 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO1 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 25H：BLDO2 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO2 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 26H：BLDO3 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO3 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 27H：BLDO4 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO4 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 28H：BLDO5 voltage control

Default：XXH

Reset：system reset

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Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO5 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 29H：CLDO1 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	CLDO1 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 2AH：CLDO2 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	CLDO2 voltage setting bit4-0: 0.7~3.3V，100mV/step，27steps	RW	Customization

REG 2BH：CLDO3 voltage control & CLDO3 /GPIO1/Wakeup control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7	When REG2B[6:5]= 11, the active level: 0: low active 1: high active	RW	0
6-5	CLDO3/GPIO1/Wakeup pin function control: 00: CLDO3 01: GPIO1, Output low 10: GPIO1, Output high, high level set by REG2B[4:0],1.25V~3.3V 11: Wakeup, Input, threshold voltage is 1.2V	RW	00
4-0	CLDO3 voltage setting(GPIO1 high level) bit4-0: 0.7~3.3V, 100mV/step, 27steps	RW	Customization

REG 2CH：CLDO4/GPIO2

Default：00H

Reset：bit[2] power on reset, others system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0
3	When REG2C[2:0]=011, the GPIO2 input edge trigger IRQ setting	RW	0

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	0: the negative edge 1: high positive edge		
2-0	CLDO4/GPIO2 pin function control: 000: CLDO4 001: GPIO2, Output low 010: GPIO2, Output high, high level set by REG2D[5:0], 1.25V~3.3V 011: GPIO2, Input, threshold voltage is 1.2V 100~101: Reserved 110~111: floating	RW	000

REG 2DH：CLDO4 voltage control

Default：XXH

Reset：system reset

Bit	Description	R/W	Default
7-6	Reserved	RW	0
5-0	CLDO4 voltage setting (GPIO2 high level) bit5-0: 0.7~4.2V, 100mV/step, 36steps	RW	Customization

REG 2EH：CPUSLDO voltage control

Default：0XH

Reset：system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0
3-0	CPUSLDO voltage setting bit3-0: 0.7~1.4V, 50mV/step, 15steps; Vddr/2, 0b'1111.	RW	Customization

REG 31H：Power wakeup CTRL

Default：00H

Reset：bit[3] is System reset，the others is Power on reset

Bit	Description	R/W	Default
7	PWROK drive low or not when Power wake up and REG31[3]=1. 0: not drive low 1: drive low in wake up period	RW	0
6	Voltage recovery control when AXP15060 wakeup 0: recovery to the default 1: Do nothing to the voltage	RW	0
5	Soft Power wakeup, write 1 to this bit, the output power will be waked up, and this bit will clear itself	RW	0
4	Control bit for IRQ output and wake up trigger when reg31[3] is 1 0 : IRQ pin is masked and IRQ can wake up AXP15060 1 : IRQ pin is normal and IRQ can not wake up AXP15060	RW	0
3	Enable bit for the function that output power be waked up by REG31_[5]、POKNIRQ、POKLIRQ、or IRQ pin is Low. 0: Wakeup function Off	RW	0

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	1: Wakeup function On It self-clear after wakeup		
2-0	Reserved	RW	0

REG 32H：Power disable & Power down sequence

Default：24H

Reset：bit [7:6] is System reset，the others is Power on reset

Bit	Description	R/W	Default
7	Power disable control. Write 1 to this bit will power off the PMIC，and this bit will clear itself	RW	0
6	Host restart the PMIC and clear itself	RW	0
5	Enable for PMIC to monitor the status of PWROK pin to judge whether PMIC starts up normally 0: disable 1: enable	RW	1
4	Enable to restart the PMIC by PWROK drive low 0: disable 1: enable	RW	0
3	Output power down sequence control 0: at the same time 1: the reverse of the start up sequence	RW	0
2	Die temperature detect enable 0 : disable 1: enable	RW	1
1	The PMIC shut down or not when die temperature is over the warning level 2 0: not shutdown 1: shutdown	RW	0
0	Enable for 16s POK to power on reset 0: disable 1: enable	RW	0

REG 36H：POK setting

Default：59H

Reset：bit3 is System reset，the others is Power on reset

Bit	Description	R/W	Default
7-6	ONLEVEL setting 00: 128ms 01: 1s 10: 2s 11: 3s	RW	01
5-4	IRQLEVEL setting 00: 1s 01: 1.5s 10: 2s 11: 2.5s	RW	01
3	Enable bit for the function which will shut down the PMIC when POK is larger than OFFLEVEL 0: disable 1: enable	RW	1
2	The PMIC auto turn on or not when it shut down after OFFLEVEL POK 0: not turn on 1: auto turn on	RW	0
1-0	OFFLEVEL setting 00: 4s 01: 6s 10: 8s 11: 10s	RW	01

REG 3EH: Interface mode select

Default: 00H

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Reset: power on reset

Bit	Description	R/W	Default
7-0	Interface mode select 8'H7C : select RSB Others : select TWSI	RW	00H

REG 40H：IRQ Enable1

Default：03H

Reset：System reset

Bit	Description	R/W	Default
7	Voltage of DCDC-6 is under 85% of setting IRQ enable	RW	0
6	Voltage of DCDC-5 is under 85% of setting IRQ enable	RW	0
5	Voltage of DCDC-4 is under 85% of setting IRQ enable	RW	0
4	Voltage of DCDC-3 is under 85% of setting IRQ enable	RW	0
3	Voltage of DCDC-2 is under 85% of setting IRQ enable	RW	0
2	Voltage of DCDC-1 is under 85% of setting IRQ enable	RW	0
1	Die temperature is over the warning level 2 IRQ enable	RW	1
0	Die temperature is over the warning level 1 IRQ enable	RW	1

REG 41H：IRQ Enable2

Default：03H

Reset：System reset

Bit	Description	R/W	Default
7-6	Reserved	RW	0
5	GPIO2 IRQ enable	RW	0
4	POKPIRQ enable	RW	0
3	POKNIRQ enable	RW	0
2	GPIO1 IRQ enable	RW	0
1	POKSIRQ enable	RW	1
0	POKLIRQ enable	RW	1

REG 48H：IRQ Status1

Default：00H

Reset：System reset

Bit	Description	R/W	Default
7	Voltage of DCDC-6 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
6	Voltage of DCDC-5 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
5	Voltage of DCDC-4 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
4	Voltage of DCDC-3 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0

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3	Voltage of DCDC-2 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
2	Voltage of DCDC-1 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
1	Die temperature is over the warning level 2 Write 1 to it or temperature drop to level 2 will clear it	RW	0
0	Die temperature is over the warning level 1 Write 1 to it or temperature drop to level 1 will clear it	RW	0

REG 49H： IRQ Status2

Default： 00H

Reset： System reset

Bit	Description	R/W	Default
7-6	Reserved	RW	0
5	GPIO2 IRQ, write 1 to it will clear it	RW	0
4	POKPIRQ,write 1 to it will clear it	RW	0
3	POKNIRQ,write 1 to it will clear it	RW	0
2	GPIO1 IRQ,write 1 to it will clear it	RW	0
1	POKSIRQ,write 1 to it will clear it	RW	0
0	POKLIRQ,write 1 to it will clear it	RW	0

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8. Application Information

8.1 DCDC/LDO Design

1. Output capacitance of LDO is not smaller than 4.7uF.
2. For unused LDO, the output pin just stays floating and dose not need an external capacitor.
3. Each DCDC uses a 1uH inductor. Its saturation current of inductor should be 30% higher than the load current, and the internal resistance is less than 30mohm.
4. Output capacitance of each DCDC is not smaller than 22uF.
5. layout：Inductors of DCDC are close to PMIC, output capacitors are close to inductors and input inductors are close to input pins.

8.2 Internal LDO Design

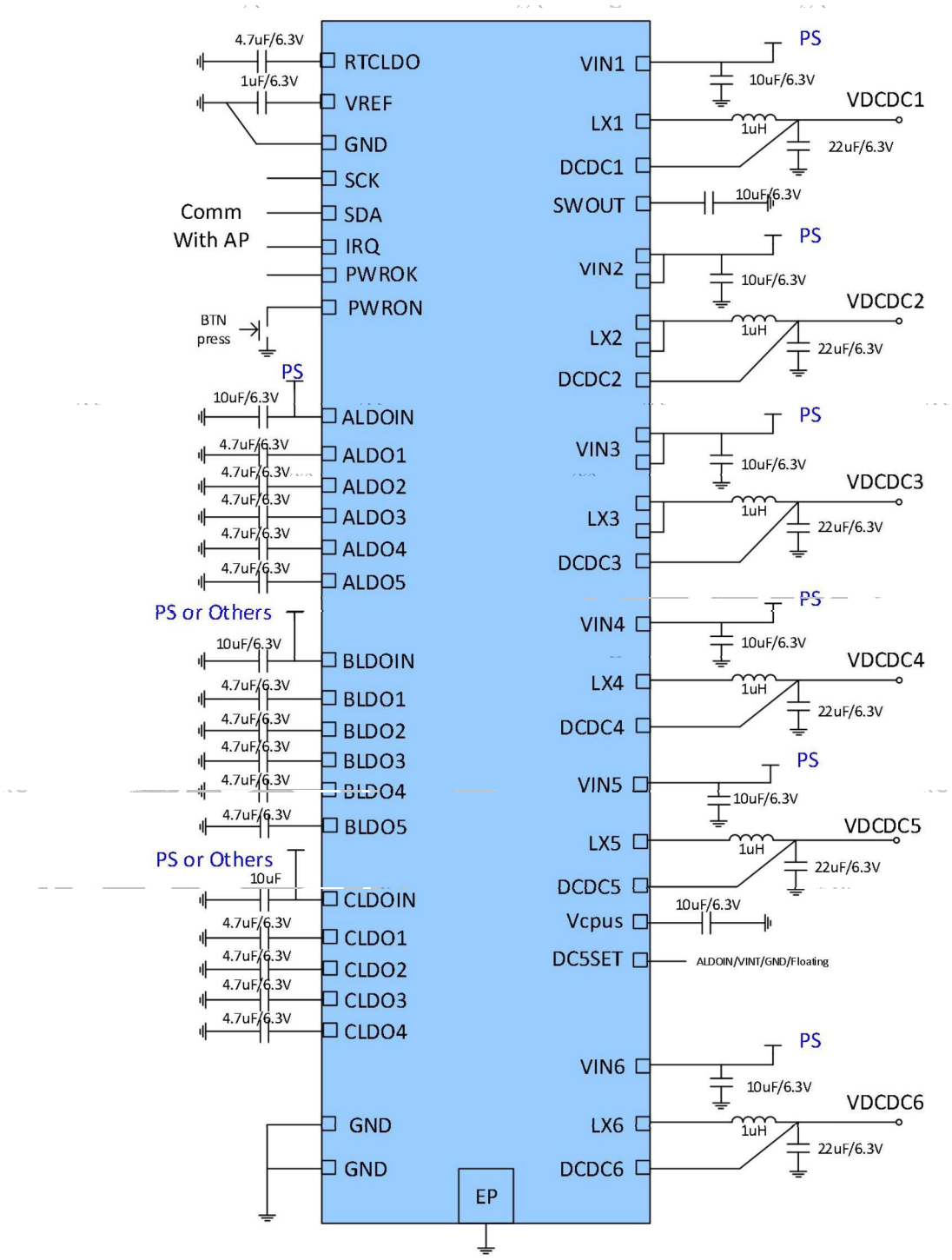
1. VREF is a high accuracy reference voltage of AXP15060. Connect a 1uF capacitor to VREF pin to ensure the accuracy of all output voltage. The capacitor should be close to VREF pin and away from DCDC to avoid interference.

8.3 IO Design

1. TWSI: Pull up SDA and SCK to a source, such as RTCLDO.
2. Pull up IRQ with a 4.7kΩ resistor to a source, such as RTCLDO.
3. If the system needs a reset key, just connect a key between PWROK pin and GND.
4. Connect the PWRON key between PWRON pin and GND directly.

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8.4 Typical Application



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9. PCB Layout Guideline

Line width of high current path such as power input and output need to be widened to reduce line impedance, voltage drop and loss.

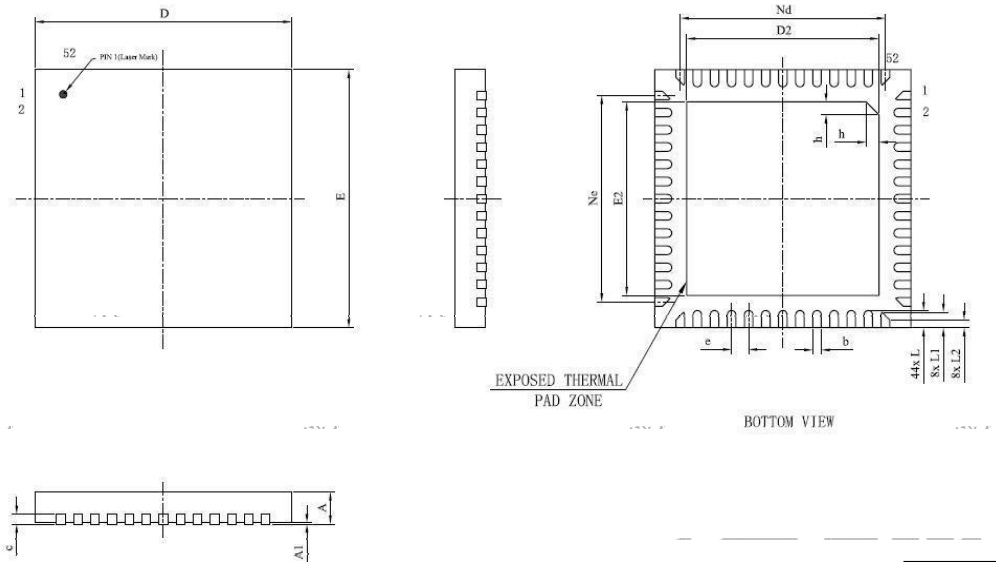
- Line width of DCDC input and output: >=120mil; In particular, Line width of SWOUT: >=30mil.
- Feedback line of DCDC1 provides power to SWOUT, line width: >=50mi.
- Line width of LDO input: >=80mil; Line width of output depends on load current.

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10. Package and Ordering Information

10.1 Package Information

AXP15060 package is QFN6*6, 52-pin. Figure 10-1 shows AXP15060 package.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 10-1 Package Information

10.2 Marking information

Figure 10-2 shows AXP15060 marking.

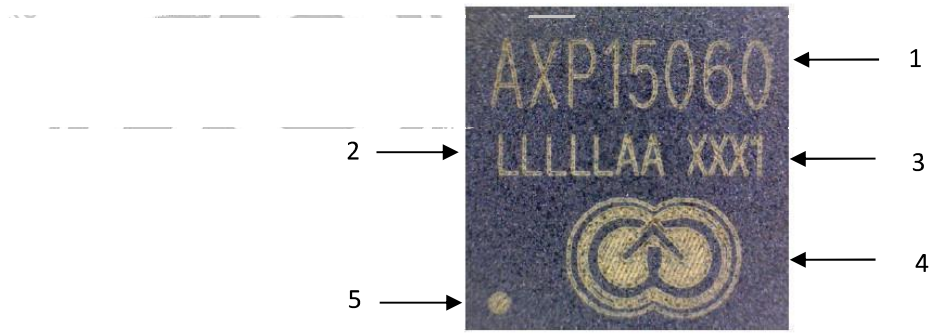


Figure 10-2 AXP15060 Marking

Table 10-1 describes AXP15060 marking information.

Table 10-1 AXP15060 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP15060	Product name	Fixed
2	LLLLLAA	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

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10.3 Carrier

Table 10-2 shows AXP15060 tray carrier information

Table 10-2 Tray Carrier Information

Item	Color	Size
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm
Pearl cotton cushion (The Gap between vacuum bag and inside box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm
Inside Box	White	396mm x 196mm x 96mm
Outside Box	White	420mm x 410mm x 320mm

Figure 10-3 shows tray dimension drawing of AXP15060.

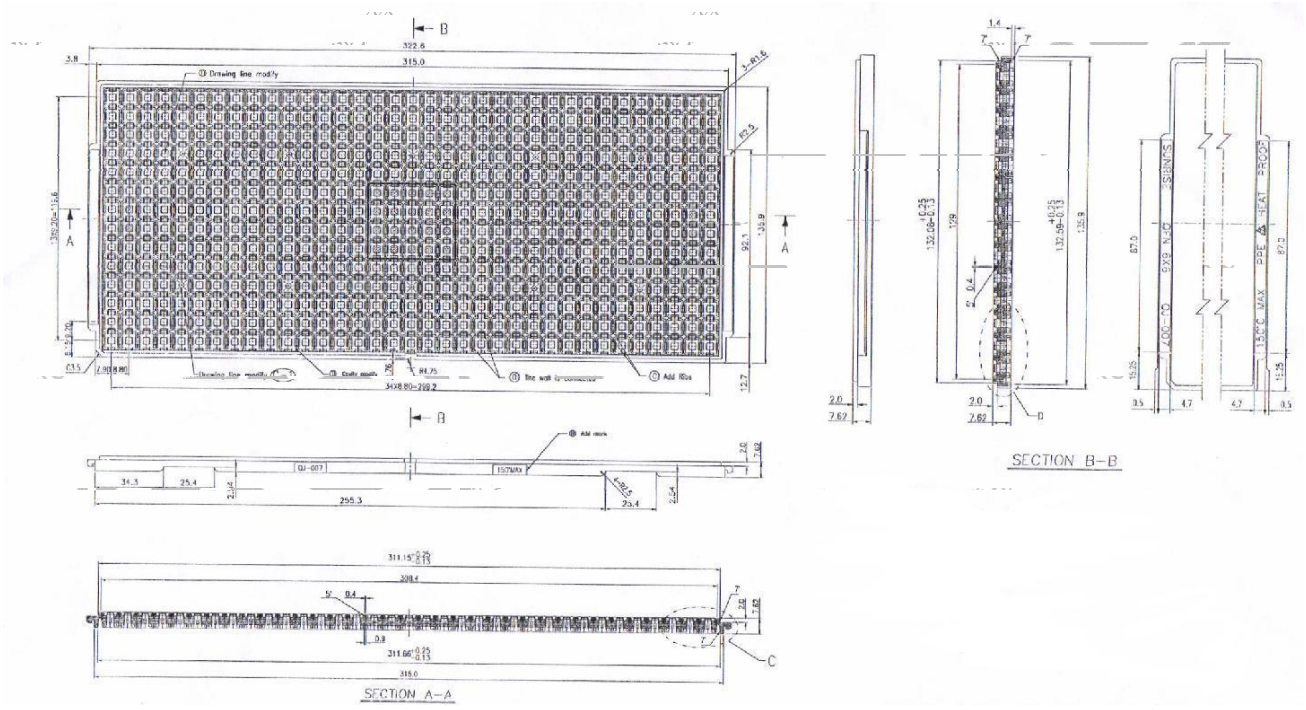


Figure 10-3 Tray Dimension Drawing

Table 10-3 shows AXP15060 packing quantity.

Table 10-3 Packing Quantity Information

Type	Quantity	Part Number
Tray	490pcs/Tray 10trays/Package	AXP15060

10.4 Storage

10.4.1 Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factor floor longer than a high MSL device sample. ALL MSL are defined in Table 10-4.

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Table 10-4 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30℃/85%RH
2	1 year	≤30℃/60%RH
2a	4 weeks	≤30℃/60%RH
3	168 hours	≤30℃/60%RH
4	72 hours	≤30℃/60%RH
5	48 hours	≤30℃/60%RH
5a	24 hours	≤30℃/60%RH
6	Time on Label(TOL)	≤30℃/60%RH

AXP15060 device samples are classified as MSL3.

10.4.2 Bagged Storage Conditions

The shelf life of AXP15060 are defined in Table 10-5.

Table 10-5

Packing mode	Vacuum packing
Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Shelf life	6 months

10.4.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP15060 is as follows.

Table 10-6 Out-of-bag Duration

Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

10.5 Baking

It is not necessary to bake AXP15060 if the conditions specified in Section 10.4.2 and Section 10.4.3 have not been exceeded. It is necessary to bake AXP15060 if any condition specified in Section 10.4.2 and Section 10.4.3 have been exceeded.

Table 10-7 Baking Conditions

Surrounding	Condition	Note
Nitrogen	125℃/8 hours	Recommended condition. It is recommended to bake once, no more than three times.
CAUTION： If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature		

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11 Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

Figure 11-1 shows the typical reflow profile of AXP15060 device sample.

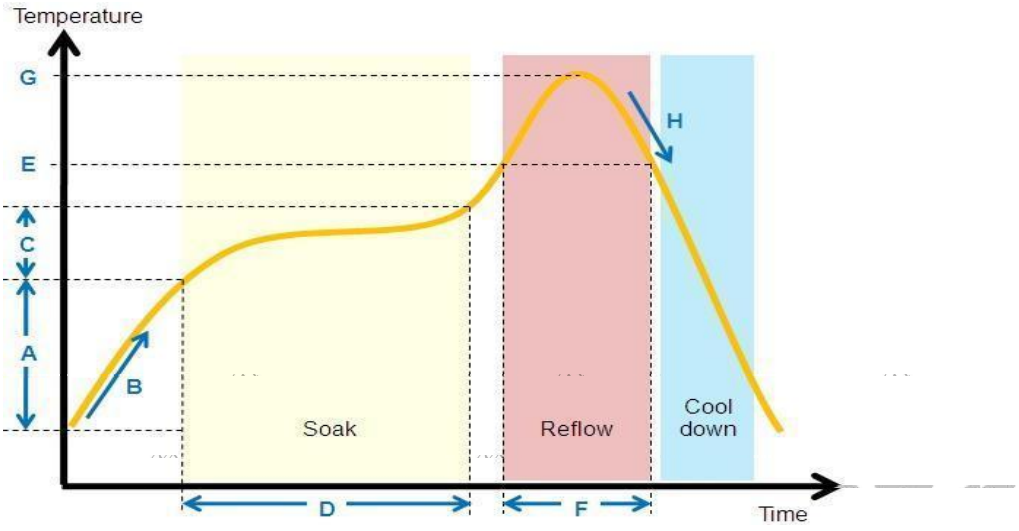


Figure 11-1 AXP15060 Typical Reflow Profile

Reflow profile conditions of AXP15060 device sample is given in Table 11-1.

Table 11-1 AXP15060 Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25℃ -> 150℃
B	Preheat ramp up rate	1.5~2.5 ℃/sec
C	Soak temperature range	150 -> 190℃
D	Soak time	80~110 sec
E	Liquidus temperature	217℃
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250℃
H	Cool down temperature rate	≤4℃/sec

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