

BSS10N4R7SA1

N-Channel Power MOSFET

100 V, 107 A , 4.7 mΩ



Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency. It has been optimized for low gate charge, low RDSon, fast switching speed.

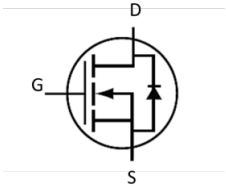
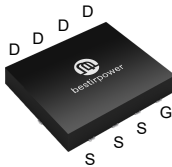
Features

$BV_{DSS} @ T_{J,max}$	I_D	$R_{DS(on),max}$	$Q_{g,typ}$
100V	107 A	4.7mΩ	59 nC

- Shielded-gate trench technology
- Low on-resistance and low gate-charge
- RoHS compliant
- 100% avalanche tested

Applications

- High-frequency DC-to-DC converters
- Motor controllers
- Battery management and protection
- Server power



Absolute Maximum Ratings (T_J = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		100	V
V _{GSS}	Gate to Source Voltage		±20	V
I _D	Drain Current ¹⁾	T _C = 25°C	107	A
		T _C = 100°C	68	
I _{DM}	Drain Current ²⁾		448	A
E _{AS}	Single Pulsed Avalanche Energy ³⁾		165	mJ
I _{AR}	Avalanche Current ⁴⁾		45	A
P _{tot}	Power Dissipation		114	W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R _{θJC}	Thermal Resistance, Junction to Case (T _C = 25 °C)	-	-	1.1	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient ⁵⁾ (T _C = 25 °C)	-	-	45	
T _{sold}	Soldering temperature, wave soldering only allowed at leads	-	-	260	°C

Electrical Characteristics⁶⁾ ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$	-	3.9	4.7	mΩ
R_G	Gate resistance	F=1MHz open drain	-	0.8	-	Ω
g_{fs}	Transconductance	$V_{DS}=5\text{V}, I_D=30\text{A}$	-	58	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$ $f = 1\text{ MHz}$	-	4800	-	pF
C_{oss}	Output Capacitance		-	1200	-	pF
C_{rss}	Reverse Transfer Capacitance		-	10	-	pF
$Q_{g(tot)}$	Gate Charge Total	$V_{DD} = 50\text{ V}, I_D = 50\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V}$	-	59	-	nC
Q_{gs}	Gate to Source Charge		-	19	-	nC
Q_{gd}	Gate to Drain Charge		-	8	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 50\text{ A}$ $V_{GS} = 10\text{ V}, R_G = 3.0\Omega$	-	8	-	ns
t_r	Turn-On Rise Time		-	32	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	68	-	ns
t_f	Turn-Off Fall Time		-	19	-	ns

Source-Drain Diode Characteristics

V_{SD}	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_F = 50\text{ A}$	-	0.8	-	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 25\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	70	-	ns
Q_{rr}	Reverse Recovery Charge		-	170	-	nC

1) Rated according to $R_{\theta JC}$ 2) Limited by maximum T_J 3) Starting $T_J = 25^\circ\text{C}$, $L = 0.1\text{ mH}$, $V_{DD} = 50\text{ V}$, $V_{GS} = 10\text{ V}$ 4) Pulse width limited by maximum T_J 5) Surface-mounted on 1 inch² FR4 board, 2 oz Cu6) $T_J = 25^\circ\text{C}$ unless otherwise specified

Typical Performance Characteristics

Figure 1. Output characteristics

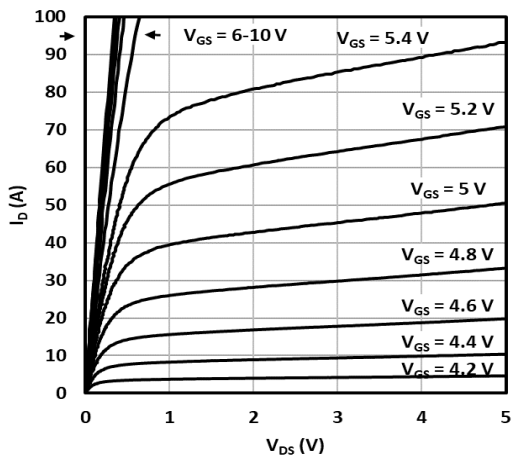


Figure 2. Transfer characteristics

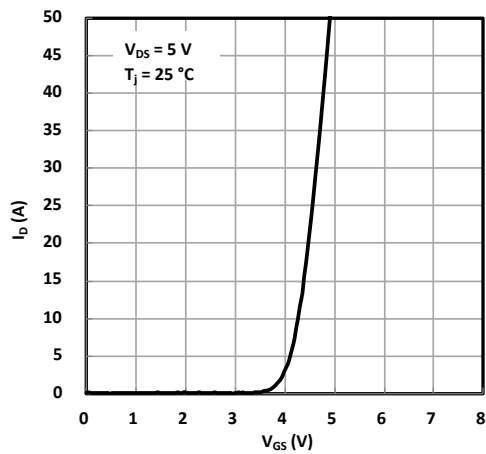


Figure 3. On-resistance vs. gate voltage

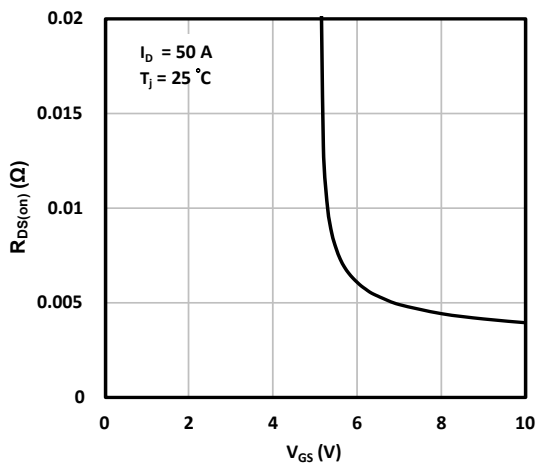


Figure 4. On-resistance vs. drain current

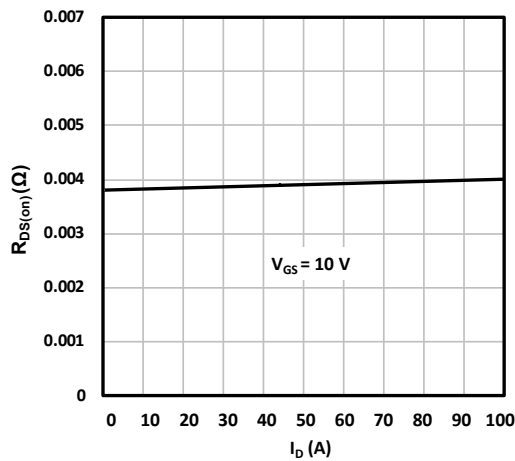


Figure 5. Source-to-drain diode forward characteristics

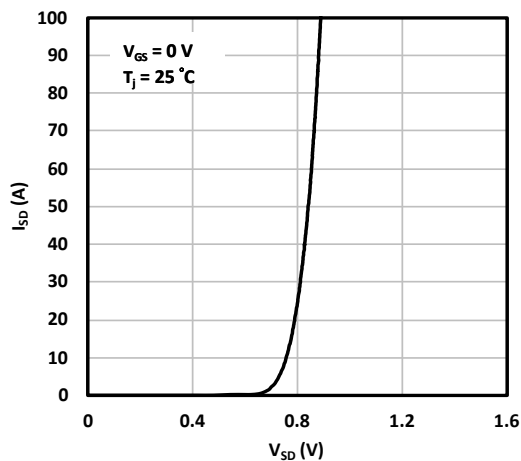
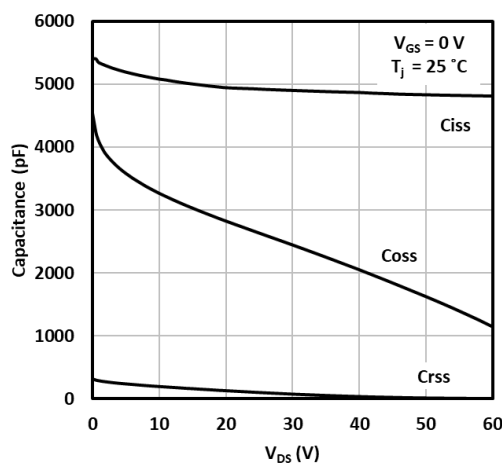


Figure 6. Capacitance vs. drain-to-source voltage



Typical Performance Characteristic

Figure 7. Gate-to-source voltage vs. gate charge

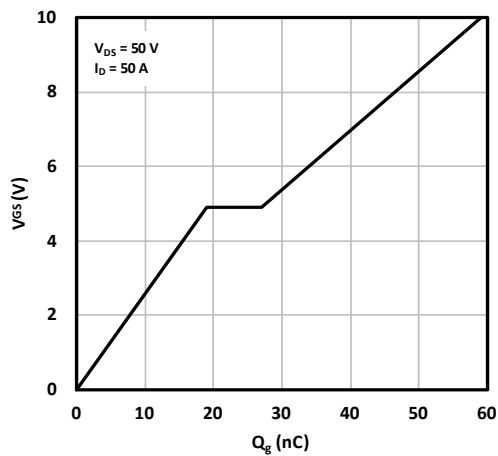


Figure 8. Maximum drain current vs. case temperature

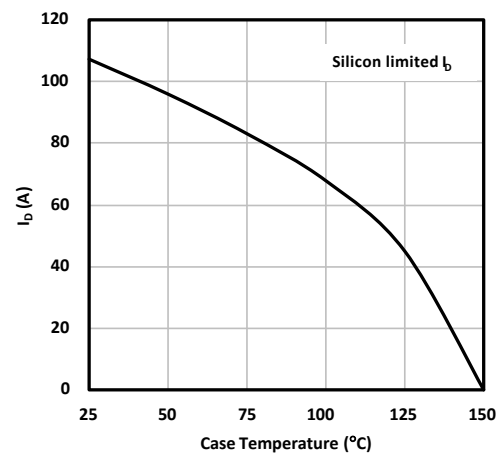


Figure 9. Resistive switching time test circuit & waveforms

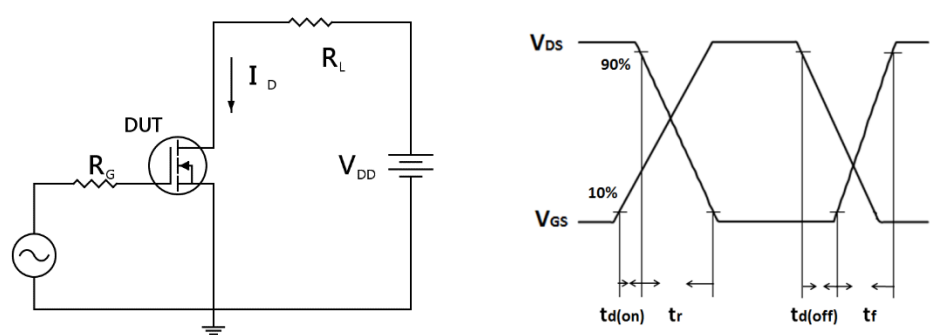


Figure 10. Gate charge test circuit & waveform

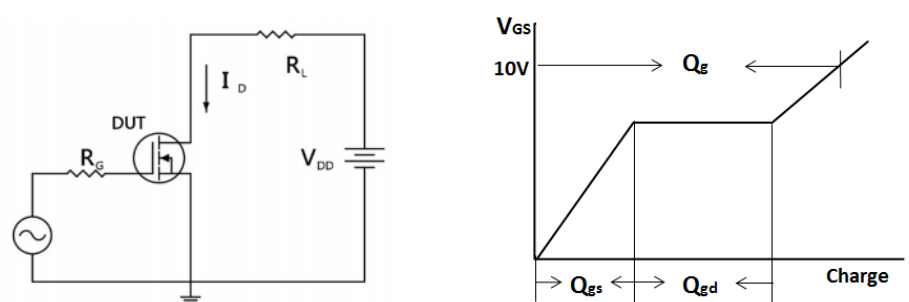


Figure 11. Peak diode recovery dv/dt test circuit & waveforms

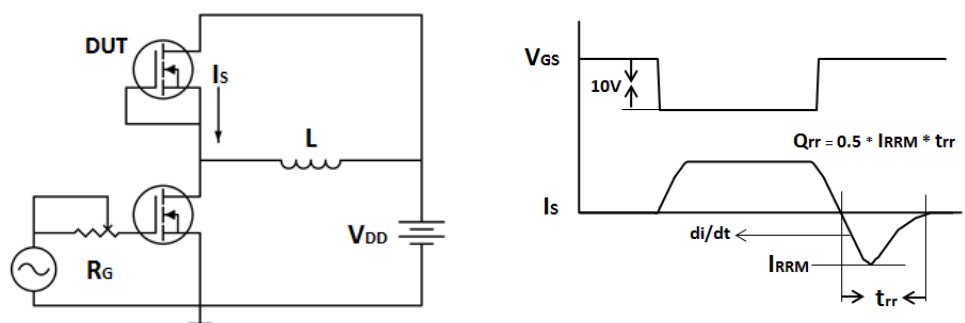
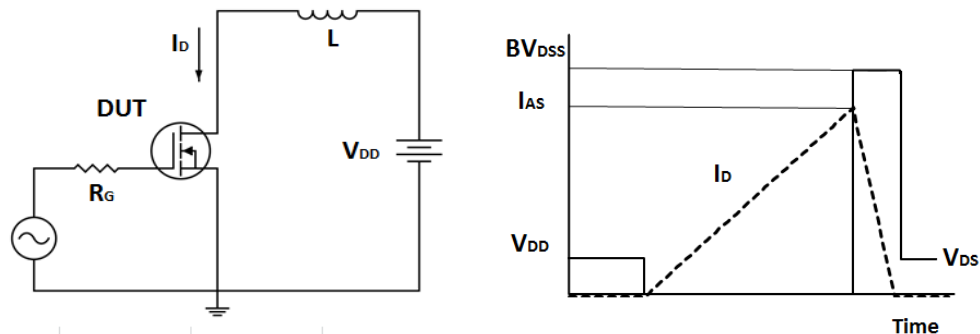
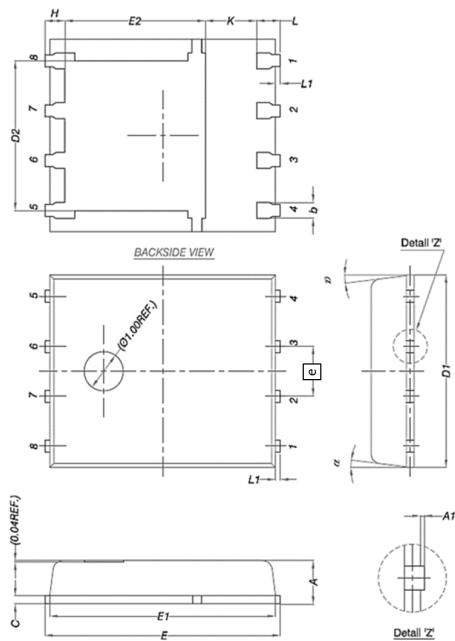


Figure 12. Unclamped inductive switching test circuit & waveforms



Package Outlines

DFN 5x6



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	-	0.05
b	0.30	0.40	0.50
c	0.15	0.25	0.35
D1	5.05	5.25	5.45
D2	3.80	4.10	4.25
E	5.95	6.15	6.35
E1	5.66	5.86	6.06
E2	3.52	3.72	3.92
e	1.27 BSC		
H	0.40	0.50	0.60
K	1.34	-	-
L	0.30	0.60	0.70
L1	0.05	0.15	0.25
α	0°	-	12°

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
BSS10N4R7SA1	BSS10N4R7SA1	DFN 5×6	Tape & Reel	5000 units

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