

BSD08NH078SK1

N-Channel Power MOSFET

80 V, 92 A, 7.8 mΩ

Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency. It has been optimized for low gate charge, low $R_{DS(on)}$, fast switching speed.

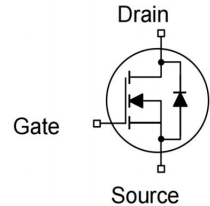
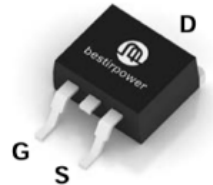
Features

BV_{DSS}	I_D	$R_{DS(on),max}$	$Q_{rr,typ}$
80 V	92 A	7.8 mΩ	86 nC

- $V_{DS}=80V$; $I_D=92A$ @ $V_{GS}=10V$;
 $R_{DS(ON)}<7.8m\Omega$ @ $V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Applications

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Absolute Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		80	V
V_{GSS}	Gate to Source Voltage		± 25	V
I_D	Continuous Drain Current, ($T_C = 25^\circ\text{C}$)		92	A
	Continuous Drain Current, ($T_C = 100^\circ\text{C}$)		64.4	
I_{DM}	Drain Current (1)	Pulsed	368	A
E_{AS}	Single Pulsed Avalanche Energy (2)		625	mJ
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	147	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.02	$^\circ\text{C/W}$

Notes 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. E_{AS} condition: $T_J=25^\circ\text{C}$, $V_{DD}=40V$, $V_G=10V$, $R_G=25\ \Omega$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$	-	6.5	7.8	mΩ

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$	-	5053	-	pF
C_{oss}	Output Capacitance		-	442	-	pF
C_{rss}	Reverse transfer capacitance		-	145	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{GS} = 10\text{ V}, V_{DD} = 50\text{ V}, I_D = 40\text{ A}$	-	115	-	nC
Q_{gs}	Gate to Source Charge		-	20	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	50	-	nC
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	20	-	-	S

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 40\text{ A}, R_L = 15\Omega$ $V_{GS} = 10\text{ V}, R_G = 2.5\Omega$	-	23	-	ns
t_r	Turn-On Rise Time		-	51	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	66	-	ns
t_f	Turn-Off Fall Time		-	23	-	ns

Source-Drain Diode Characteristics

I_S	Continuous Diode Forward Current		-	92	-	A
$I_{S\text{ pulse}}$	Diode Pulsed Current		-	368	-	
V_{SD}	Diode Forward Voltage ⁽¹⁾	$T_J = 25^\circ\text{C}, I_S = 40\text{ A}, V_{GS} = 0\text{ V}$	-	0.89	0.99	V
t_{rr}	Reverse Recovery Time ⁽¹⁾	$I_F = 75\text{ A}, diF/dt = 100\text{ A/us}$	-	41	-	ns
Q_{rr}	Reverse Recovery Charge ⁽¹⁾		-	86	-	nC

Notes

Notes 1. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1.5\%$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

Typical Performance Characteristics

Figure1. Output Characteristics

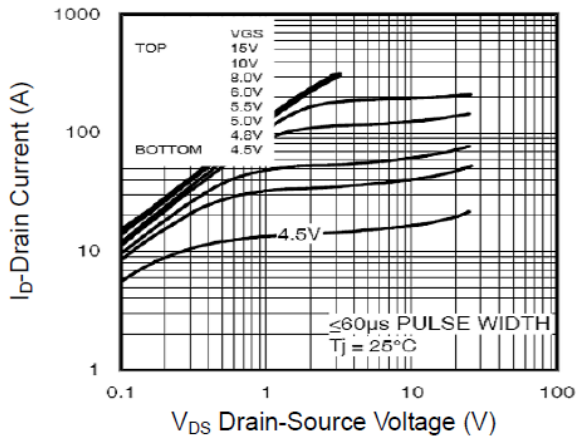


Figure2. Transfer Characteristics

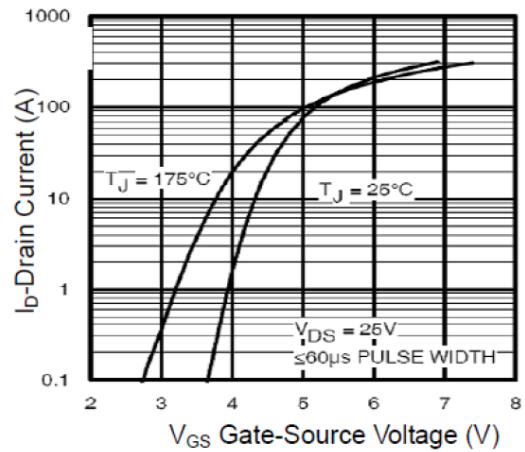


Figure3. BVDSS vs Junction Temperature

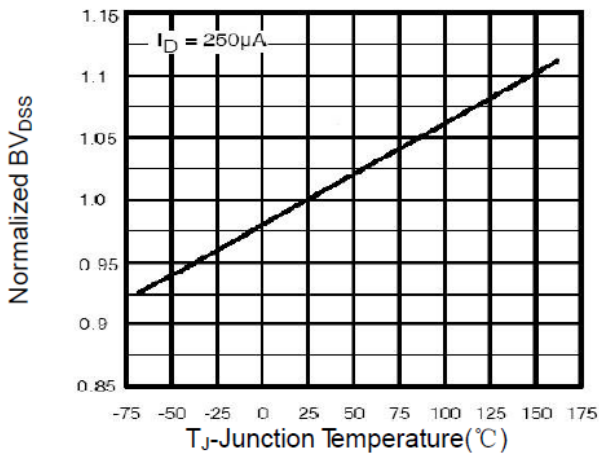


Figure4. ID vs Junction Temperature

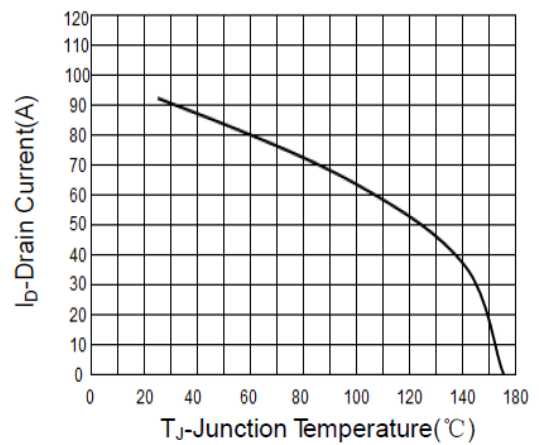


Figure5. VGS(th) vs Junction Temperature

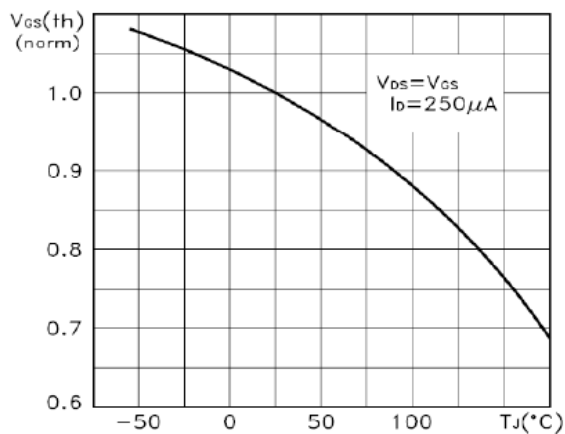
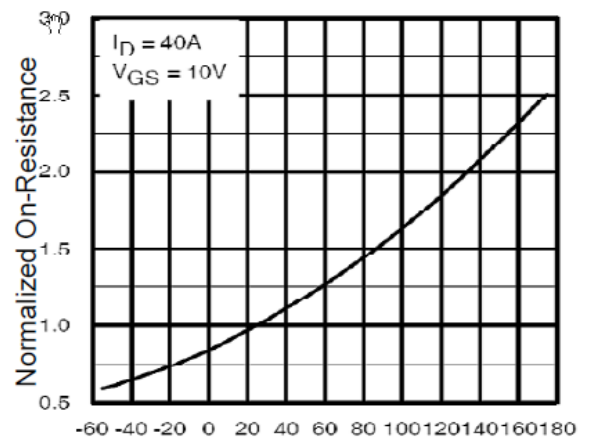


Figure6. Rds(on) Vs Junction Temperature



Typical Performance Characteristics

Figure7. Gate Charge

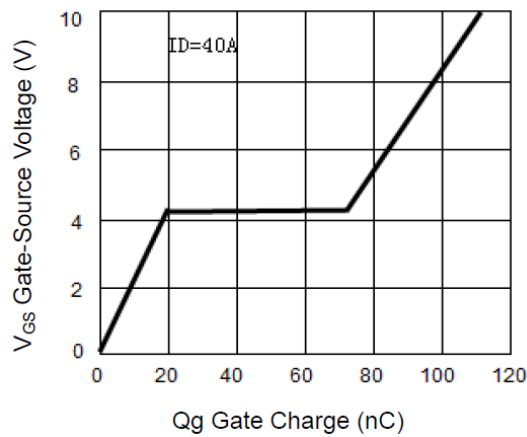


Figure8. Capacitance vs Vds

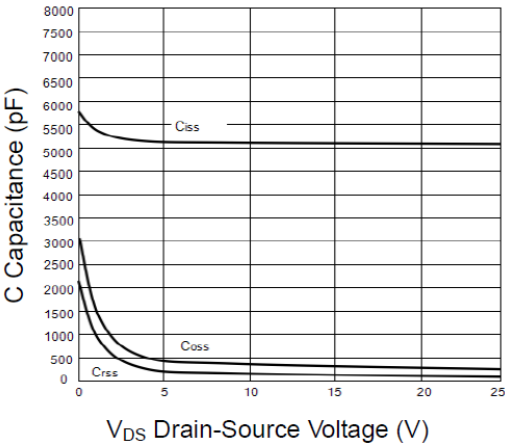


Figure9. Source- Drain Diode Forward

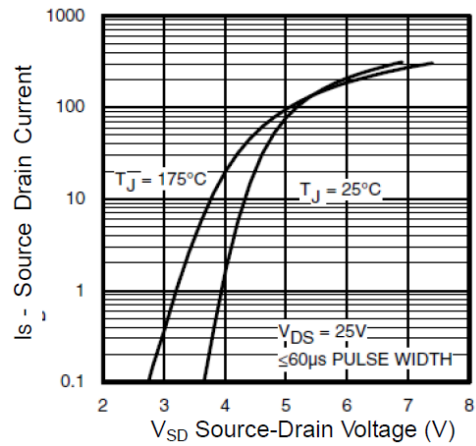


Figure10. Safe Operation Area

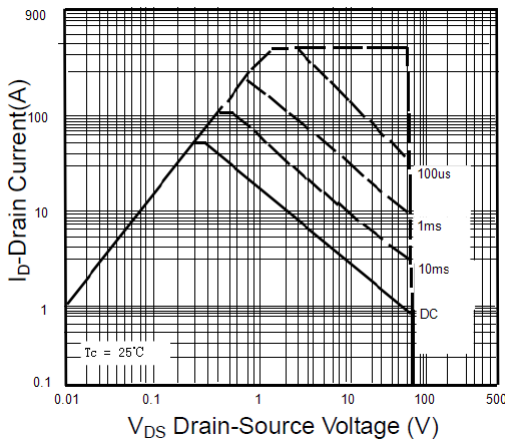
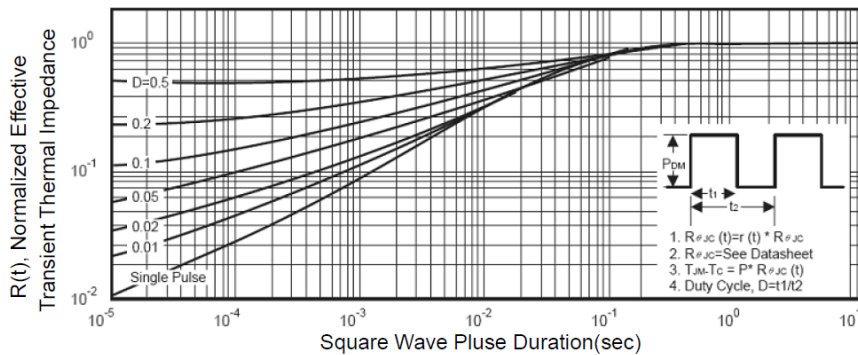


Figure11. Normalized Maximum Transient Thermal Impedance



Test Circuits

Figure 12: EAS Test Circuits

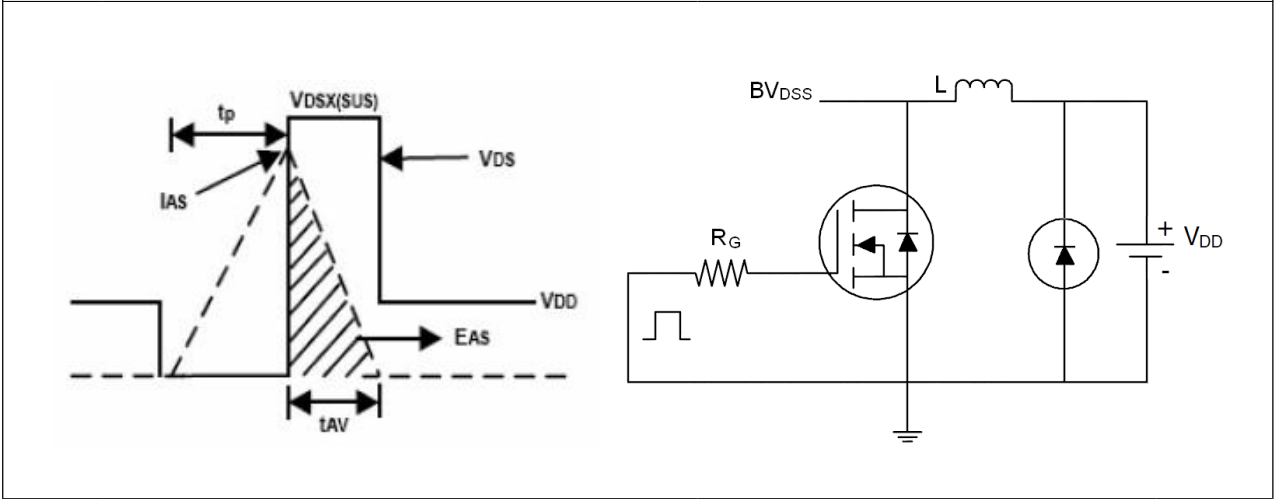


Figure 13: Gate Charge Test Circuit

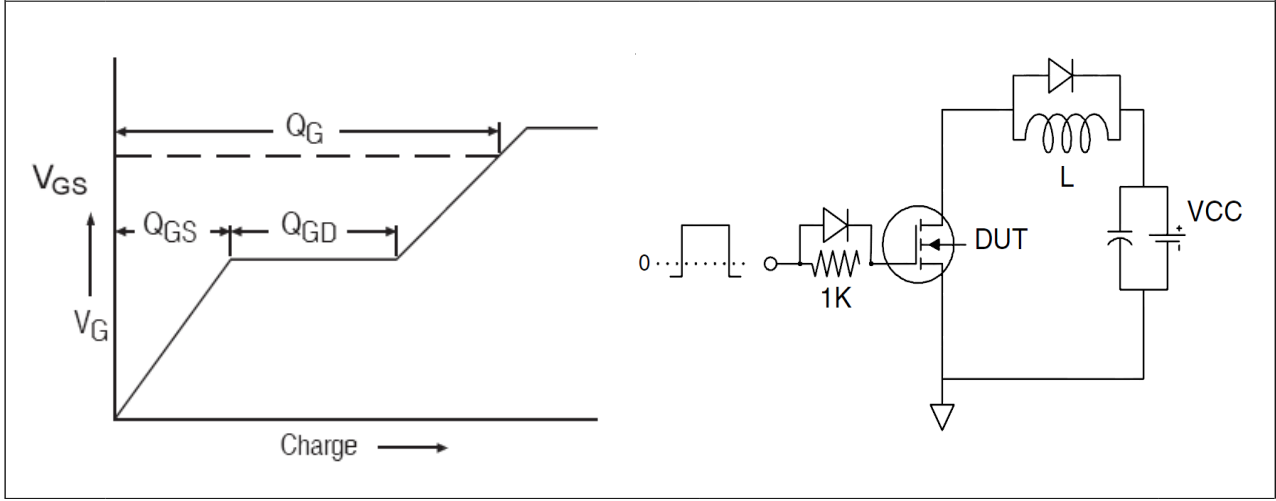
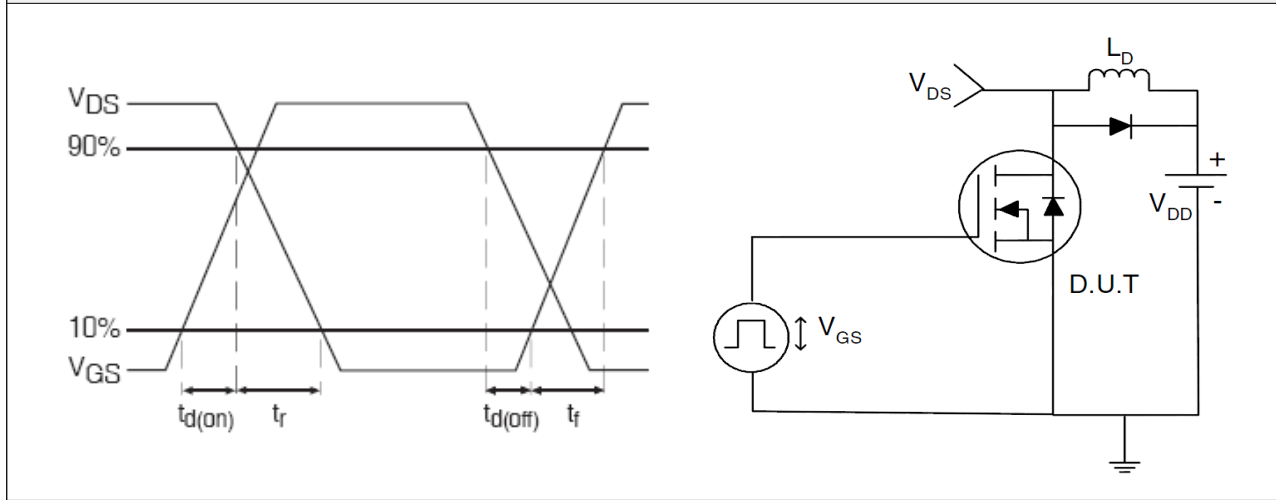
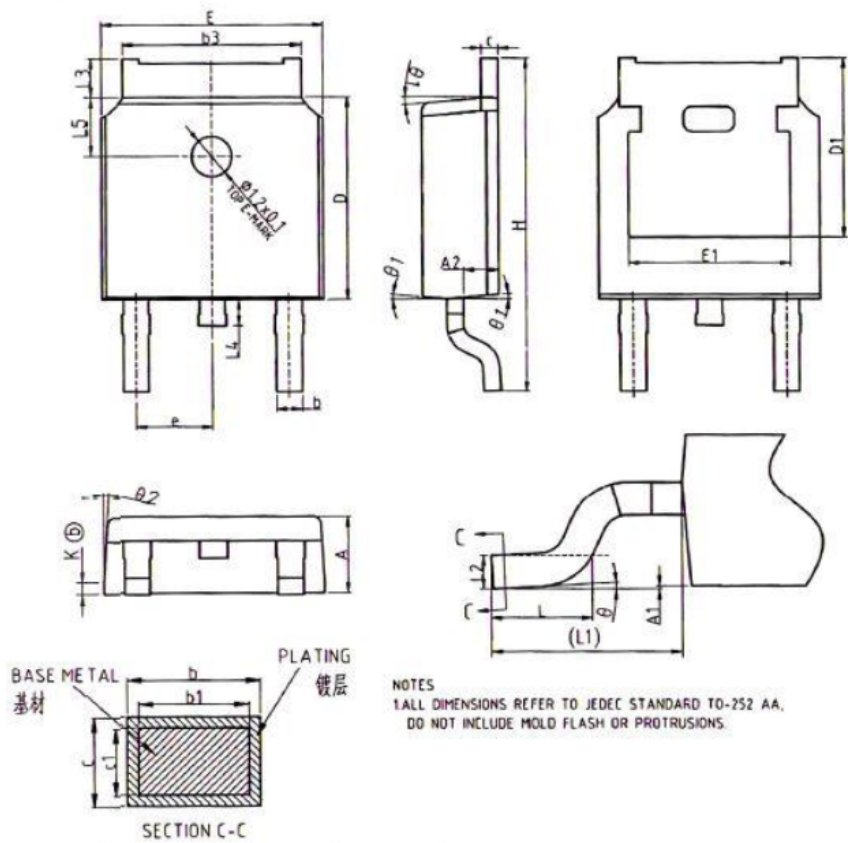


Figure 14: Switch Time Test Circuit



Package Outlines
DPAK



COMMON DIMENSIONS			
SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	-	8°
θ 1	5°	7°	9°
θ 2	5°	7°	9°
K	0.10REF		

* Dimensions in millimeters

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
BSD08NH078SK1	BSD08NH078SK1	DPAK	Tape & Reel	2500 units

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