

4-Bit Bidirectional Level Shifter for Open-Drain and Push-Pull Application

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Descriptions

The is a 4-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 4-bit input-output ports (An and Bn), one output enable (OE) and two supply pins (VCC(A) and VCC(B)). VCC(A) can be supplied at any voltage between 1.2 V and 5.5 V and VCC(B) can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to VCC(A) and pins Bn are referenced to VCC(B). A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features

- Wide supply voltage range: VCC(A): 1.2 V to 5.5 V and VCC(B): 1.65 V to 5.5 V
- Maximum data rates: Push-pull: 40 Mbps, Open-drain: 2 Mbps
- IOFF circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- No power-supply sequencing required – VCCA or VCCB can be ramped first

Applications

- PC, Tablet and Mobile phones

Functions and Pin Configuration

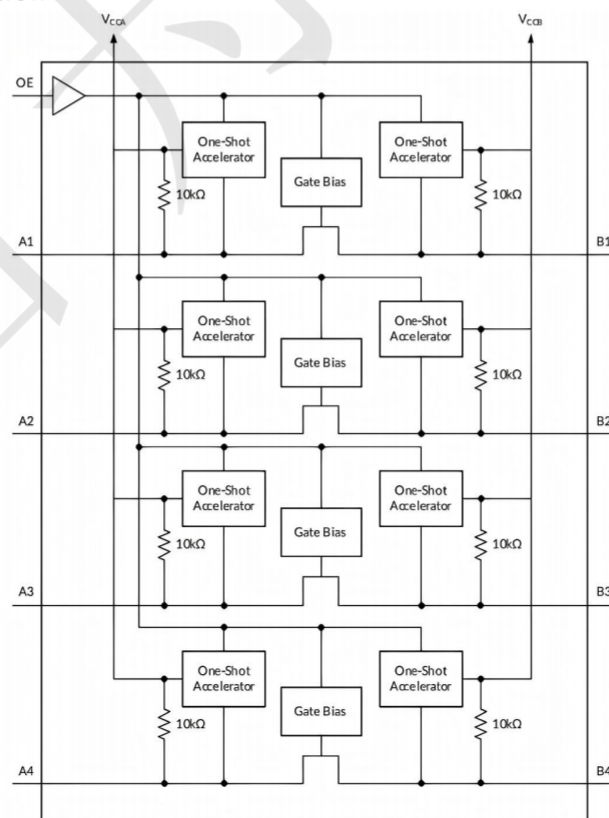


Fig.1 Functional Diagram

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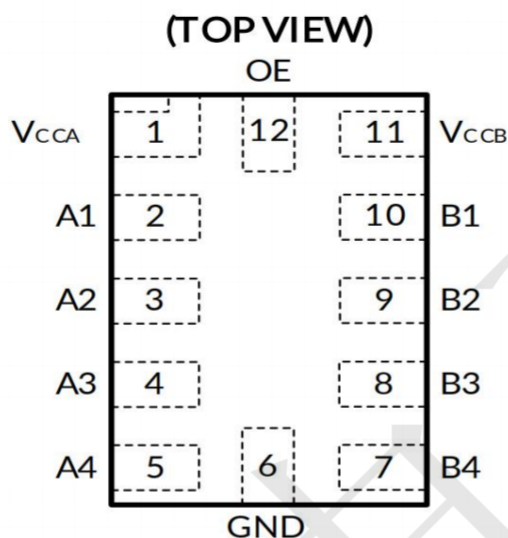


Fig.2 UQFN1.7×2-12

Pin Descriptions

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
UQFN1.7X2-12			
1	V _{CCA}	P	A Port Supply Voltage. $1.65V \leq V_{CCA} \leq 5.5V$ and $V_{CCA} \leq V_{CCB}$.
2	A1	I/O	Input/output A1. Reference to V _{CCA} .
3	A2	I/O	Input/output A2. Reference to V _{CCA} .
4	A3	I/O	Input/output A3. Reference to V _{CCA} .
5	A4	I/O	Input/output A4. Reference to V _{CCA} .
6	GND	—	Ground.
7	B4	I/O	Input/output B4. Reference to V _{CCB} .
8	B3	I/O	Input/output B3. Reference to V _{CCB} .
9	B2	I/O	Input/output B2. Reference to V _{CCB} .
10	B1	I/O	Input/output B1. Reference to V _{CCB} .
11	V _{CCB}	P	B Ports Supply Voltage
12	OE	I	Output Enable (Active High).

Function

V _{CCA}	V _{CCB}	OE	Status
1.2v ~ 5.5v	1.65v ~ 5.5v	L	Both Ax and Bx are High Z
1.2v ~ 5.5v	1.65v ~ 5.5v	H	Ax input (output) and Bx output(input)

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Absolute Maximum Ratings ⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	6.5	V
V_I	input voltage	OE [1]	-0.5	6.5	V
		An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [2] [3]	-0.5	$V_{CCI}+0.5$	V
V_O	output voltage	An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [3] [4]	-0.5	$V_{CCO}+0.5$	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
I_{OK}	output clamping current	$V_O < 0$ V	-50		mA
I_O	output current	$V_O = 0$ V to V_{CCO} [2]		± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	$T_{amb} = -40^\circ\text{C}$ to $+125^\circ\text{C}$		250	mW
T_{stg}	storage temperature		-65	150	$^\circ\text{C}$

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCI} is the supply voltage associated with the input.

[3] $V_{CCI} + 0.5$ V or $V_{CCO} + 0.5$ V should not exceed 6.5 V.

[4] V_{CCO} is the supply voltage associated with the output.

Recommend operating ratings ⁽²⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.3	5.5	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_I	input voltage	OE	0	5.5	V
		Power-down mode			
		An	0	5.5	V
		Bn	0	5.5	V
		Active mode			V

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		An, [3]	Bn	0	V_{CCI}	V
V_O	output voltage	Power-down mode				V
		An		0	5.5	V
		Bn		0	5.5	V
		Active mode				V
		An, [4]	Bn	0	V_{CCO}	V
T_{amb}	ambient temperature			-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving				
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			10	ns/V
		OE input				
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(B)}$ must be powered up prior to $V_{CC(A)}$, and $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[3] V_{CCI} is the supply voltage associated with the input.

[4] V_{CCO} is the supply voltage associated with the output.

Note:

1. "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.
2. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
3. $V_{CC(B)}$ must be powered up prior to $V_{CC(A)}$, and $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
4. The load resistance on I/O pins must not be less than 10 k Ω .

DC Electrical Characteristics ($T_a=25^\circ\text{C}$, $V_{VCCA}=1.2\text{V}\sim 1.8\text{V}$, $V_{VCCB}=1.62\text{V}\sim 3.6\text{V}$, unless otherwise specified)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25^\circ\text{C}$.

V _{CC(A)}	V _{CC(B)}								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	
1.3 V	0.03	0.001	0.08	0.01	0.15	0.07	0.26	0.35	μA
1.5 V	0.03	0.001	0.08	0.004	0.16	0.05	0.30	0.30	μA
1.8 V	0.03	0.001	0.08	0.001	0.16	0.03	0.33	0.25	μA
2.5 V			0.07	0.001	0.16	0.001	0.40	0.13	μA
3.3 V					0.16	0.001	0.42	0.05	μA
5.0 V							0.43	0.01	μA

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25^\circ\text{C}$. [1]

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port						
		$V_{CC(A)} = 1.3 \text{ V to } 1.95 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC(A)} - 0.2$		$V_{CC(A)}$	$V_{CC(A)} - 0.2$	$V_{CC(A)}$	V
		$V_{CC(A)} = 2.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	$V_{CC(A)} - 0.4$		$V_{CC(A)}$	$V_{CC(A)} - 0.4$	$V_{CC(A)}$	V

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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
		B port						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC(B)} - 0.4$		$V_{CC(B)}$	$V_{CC(B)} - 0.4$	$V_{CC(B)}$	V
		OE input						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$0.65V_{CC(A)}$		$V_{CC(A)}$	$0.65V_{CC(A)}$	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage	A or B port						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	0		0.15	0	0.15	V
		OE input						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	0		$0.35V_{CC(A)}$	0	$0.35V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	A port; $I_O = -20 \mu\text{A}; V_I \geq V_{CC(B)} - 0.4 \text{ V}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$0.67V_{CC(A)}$			$0.67V_{CC(A)}$		V
		B port; $I_O = -20 \mu\text{A}; V_I \geq V_{CC(A)} - 0.2 \text{ V}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$0.67V_{CC(B)}$			$0.67V_{CC(B)}$		V
V_{OL}	LOW-level output voltage	A or B port; $I_O = 1 \text{ mA}; V_I \leq 0.15 \text{ V}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			0.4		0.4	V
I_{OZ}	OFF-state output current	A or B port; $V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V}; V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			± 4		± 20	μA
I_I	input leakage current	OE input; $V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V}; V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			± 10		± 20	μA
I_{OFF}	power-off leakage current	A port; $V_I \text{ or } V_O = 0 \text{ V to } 5.5 \text{ V};$ $V_{CC(A)} = 0 \text{ V};$ $V_{CC(B)} = 0 \text{ V to } 5.5 \text{ V}$			± 15		± 20	μA
I_{CC}	supply current	OE = 0 V or $V_{CC(A)}$; An, Bn open						
		$I_{CC(A)}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			20		54	μA
		$V_{CC(A)} = 0 \text{ V};$ $V_{CC(B)} = 5.5 \text{ V}$			-1		-1	μA
		$I_{CC(B)}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			11		53	μA
		$V_{CC(A)} = 0 \text{ V};$ $V_{CC(B)} = 5.5 \text{ V}$			3.7		19	μA
		$I_{CC(A)} + I_{CC(B)}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$			21		105	μA

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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
		$V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$						
C_i	input capacitance	OE input; $V_{CC(A)} = 3.3 \text{ V};$ $V_{CC(B)} = 3.3 \text{ V}$		4				pF
$C_{i/o}$	input/output capacitance	A port; $V_{CC(A)} = 3.3 \text{ V}; V_{CC(B)} = 3.3 \text{ V}$						
		enabled		7				pF
		disabled		3.1				pF
		B port; $V_{CC(A)} = 3.3 \text{ V};$ $V_{CC(B)} = 3.3 \text{ V}$						
		enabled		7				pF
		disabled		3.1				pF

[1] $V_{CC(B)}$ must be powered up prior to $V_{CC(A)}$, and $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

AC Electrical Characteristics ($T_a=25^\circ\text{C}$, $V_{VCCA}=1.2\text{V}\sim 1.8\text{V}$, $V_{VCCB}=1.62\text{V}\sim 3.6\text{V}$, unless otherwise specified)

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	1.8±0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V	5.0 V ± 0.5 V	Unit
			Typ	Typ	Typ	Typ	
V _{CC(A)} = 1.3 V							
t _{PHL}	HIGH to LOW propagation delay	A to B	4.9	6.5	7.8	9.5	ns
t _{PLH}	LOW to HIGH propagation delay	A to B	8.6	6.9	6.2	6.0	ns
t _{PHL}	HIGH to LOW propagation delay	B to A	4.5	5.6	6.5	8.7	ns
t _{PLH}	LOW to HIGH propagation delay	B to A	5.8	5.1	4.9	4.8	ns
t _{en}	enable time	OE to A, B ; see Fig. 5 [1]	82	82	82	82	ns
t _{dis}	disable time	OE to A; see Fig.6 [1]	190	190	190	190	ns
		OE to B see Fig.6 [1]	174	137	182	131	ns
t _{TLH}	LOW to HIGH	A port	7.4	6.7	6.7	6.5	ns

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	output transition time	B port	10.2		8.2		6.6		6.5		ns
t _{THL}	HIGH to LOW output transition time	A port	7.3		7.3		7.6		7.6		ns
		B port	9.3		12.8		11.2		17.1		ns
t _{sk(O)}	output skew time	between channels [2]	0.7		0.7		0.7		0.7		ns
t _W	pulse width	data inputs	25		25		25		25		ns
f _{data}	data rate		10		40		40		40		Mbps
Symbol	Parameter	Conditions	V _{CC(B)}								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.5 V ± 0.1V											
t _{PHL}	HIGH to LOW propagation delay	A to B		6.0		7.0		8.6		10.5	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		12.6		10.0		8.5		8.0	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		5.1		5.5		5.9		6.5	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		8.5		8.0		5.8		5.5	ns
t _{en}	enable time	OE to A, B ; see Fig. 5 [1]		120		120		120		120	ns
t _{dis}	disable time	OE to A; see Fig.6 [1]		230		230		230		230	ns
		OE to B see Fig.6 [1]		200		150		180		115	ns
t _{TLH}	LOW to HIGH output transition time	A port	2.5	10.6	2.1	9.5	1.9	9.1	1.9	8.9	ns
		B port	4.1	15.2	3.2	10.6	2.8	8.7	0.4	7.5	ns
t _{THL}	HIGH to LOW output transition time	A port	3.0	9.7	3.1	10.8	3.1	10.1	3.1	10.2	ns
		B port	3.0	11.7	3.6	15.7	4.2	14.2	5.5	21.4	ns
t _{sk(O)}	output skew time	between channels [2]				0.7		0.7		0.7	ns
t _W	pulse width	data inputs			25		25		25		ns
f _{data}	data rate					40		40		40	Mbps
V _{CC(A)} = 1.8 V ± 0.15 V											
t _{PHL}	HIGH to LOW propagation	A to B		4.5		5.0		5.5		7.5	ns

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	delay										
t_{PLH}	LOW to HIGH propagation delay	A to B		11.3		8.4		6.4		6.1	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		3.5		4.1		4.5		5.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		6.5		6.0		5.0		4.6	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]		100		100		100		100	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]		200		200		200		200	ns
		OE to B see Fig.6 [1]		200		150		180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.3	8.7	1.8	7.6	1.6	7.4	1.5	7.1	ns
		B port	3.9	14.2	3.1	9.8	2.7	7.7	2.3	6.8	ns
t_{THL}	HIGH to LOW output transition time	A port	2.7	9.2	2.7	9.3	2.7	9.7	2.9	9.8	ns
		B port	2.6	9.6	2.9	12.0	3.3	9.8	4.3	15.0	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.7		0.7		0.7	ns
t_w	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					20		40		40	Mbps
$V_{CC(A)} = 2.5 V \pm 0.2 V$											
t_{PHL}	HIGH to LOW propagation delay	A to B				2.5		2.7		3.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B				5.7		5.0		5.2	ns
t_{PHL}	HIGH to LOW propagation delay	B to A				2.8		3.5		4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A				1.8		1.6		1.5	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]				80		80		80	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]				150		150		150	ns
		OE to B				150		180		115	ns

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		see Fig.6 [1]									
t_{TLH}	LOW to HIGH output transition time	A port			1.7	6.3	1.4	5.9	1.3	5.7	ns
		B port			2.7	9.1	2.4	7.1	2.1	6.0-	ns
t_{THL}	HIGH to LOW output transition time	A port			2.4	9.9	2.5	10.1	2.5	10.3	ns
		B port			2.3	9.8	2.5	7.4	3.0	10.5	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.7		0.7		0.7	ns
t_W	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					40		40		40	Mbps
$V_{CC(A)} = 3.3 V \pm 0.3 V$											
t_{PHL}	HIGH to LOW propagation delay	A to B						1.9		2.7	ns
t_{PLH}	LOW to HIGH propagation delay	A to B						3.0		3.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A						3.0		3.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A						1.9		1.7	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]						70		70	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]						180		180	ns
		OE to B see Fig.6 [1]						180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port						4.7	1.2	4.3	ns
		B port						6.6	2	5.8	ns
t_{THL}	HIGH to LOW output transition time	A port						7.3	2.3	7.9	ns
		B port						6.9	2.5	9.6	ns
$t_{sk(O)}$	output skew time	between channels [2]						0.7		0.7	ns
t_W	pulse width	data inputs							25		ns
f_{data}	data rate							40		40	Mbps
$V_{CC(A)} = 5.0 V \pm 0.5 V$											
t_{PHL}	HIGH to LOW propagation	A to B								1.8	ns

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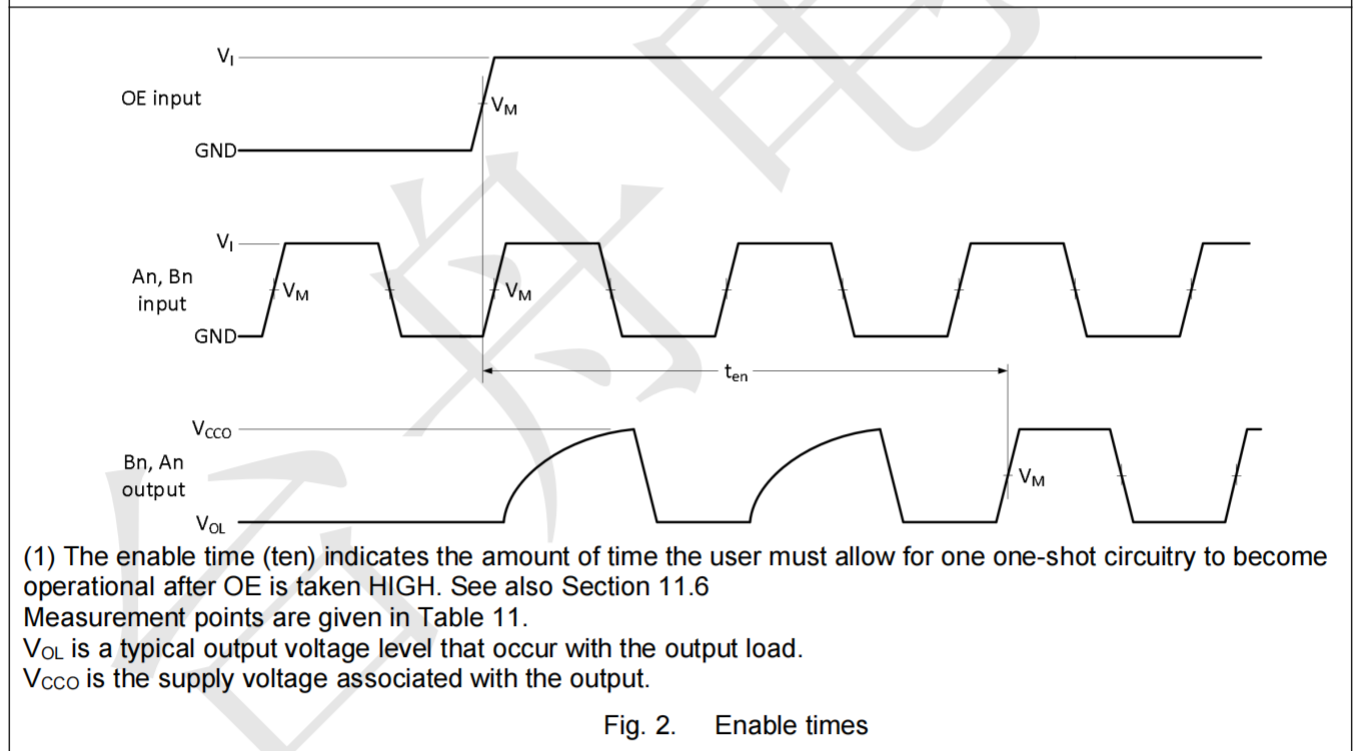
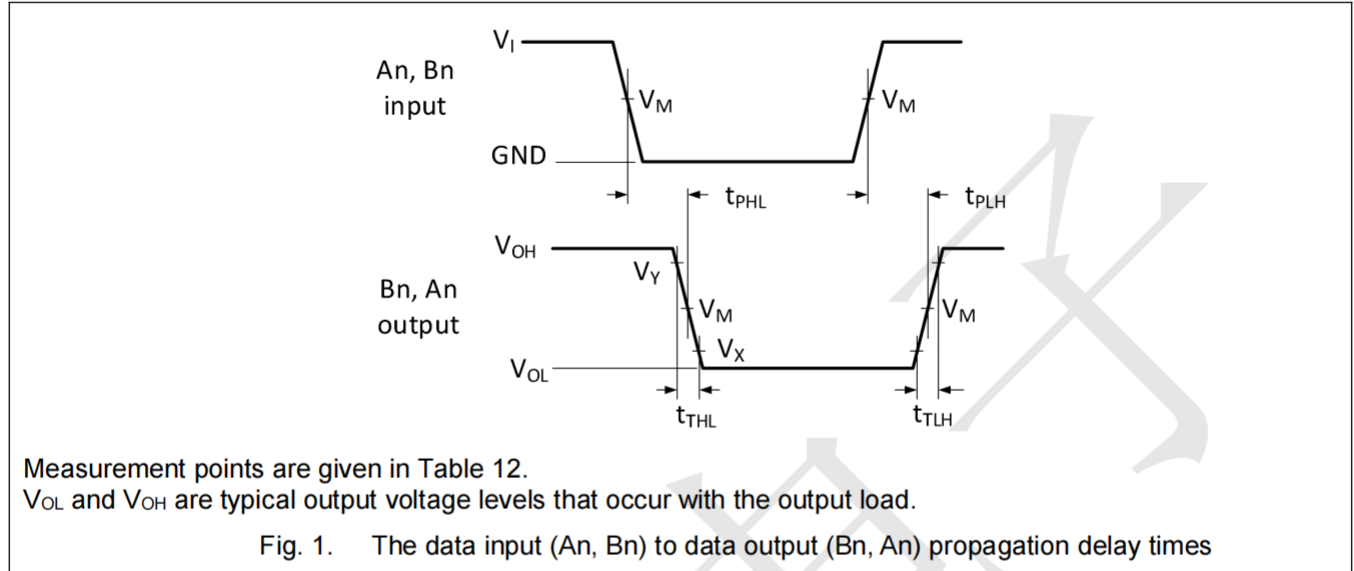
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	delay										
t_{PLH}	LOW to HIGH propagation delay	A to B								1.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A								2.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A								2.3	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]								60	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]								115	ns
		OE to B see Fig.6 [1]								115	ns
t_{TLH}	LOW to HIGH output transition time	A port								1.4	6.0
		B port								1.8	5.8
t_{THL}	HIGH to LOW output transition time	A port								2.2	9.4
		B port								2.2	9.2
$t_{sk(O)}$	output skew time	between channels [2]								0.7	ns
t_W	pulse width	data inputs								25	ns
f_{data}	data rate									40	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[2] Skew between any two outputs of the same package switching in the same direction.

Waveforms and test circuit



4-Bit Bidirectional Level Shifter for Open-Drian and Push-Pull Application

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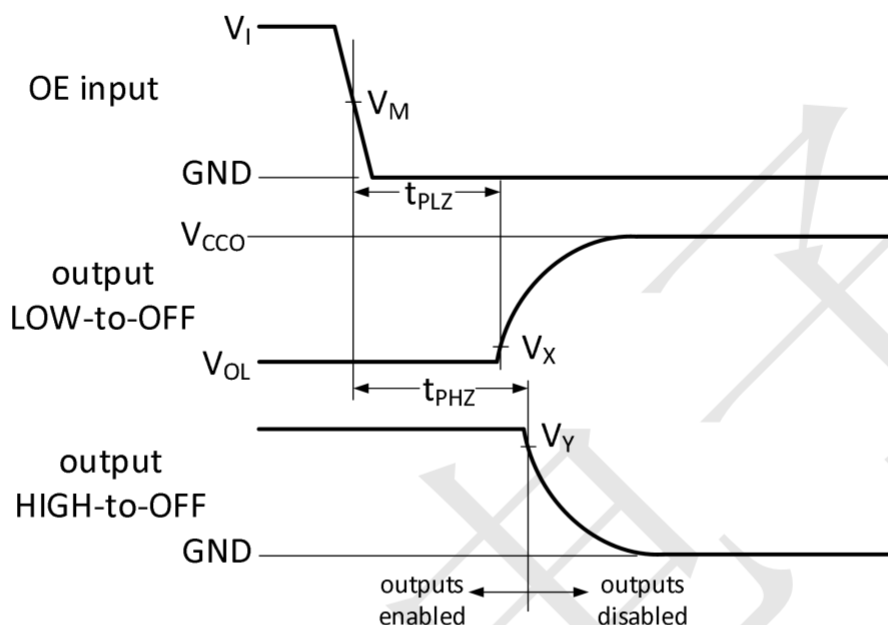


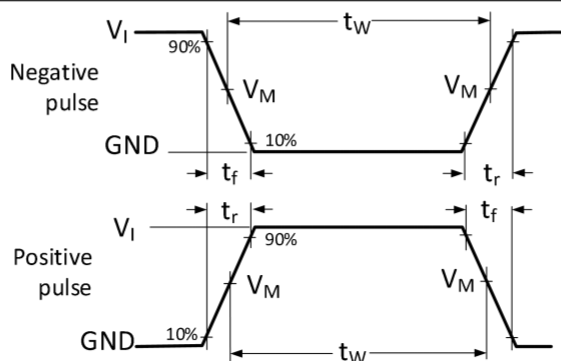
Fig. 3. Disable times

Measurement points

Supply Voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
$1.8\text{ V} \pm 0.15\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
$2.5\text{ V} \pm 0.2\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
$3.3\text{ V} \pm 0.3\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
$5.0\text{ V} \pm 0.5\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

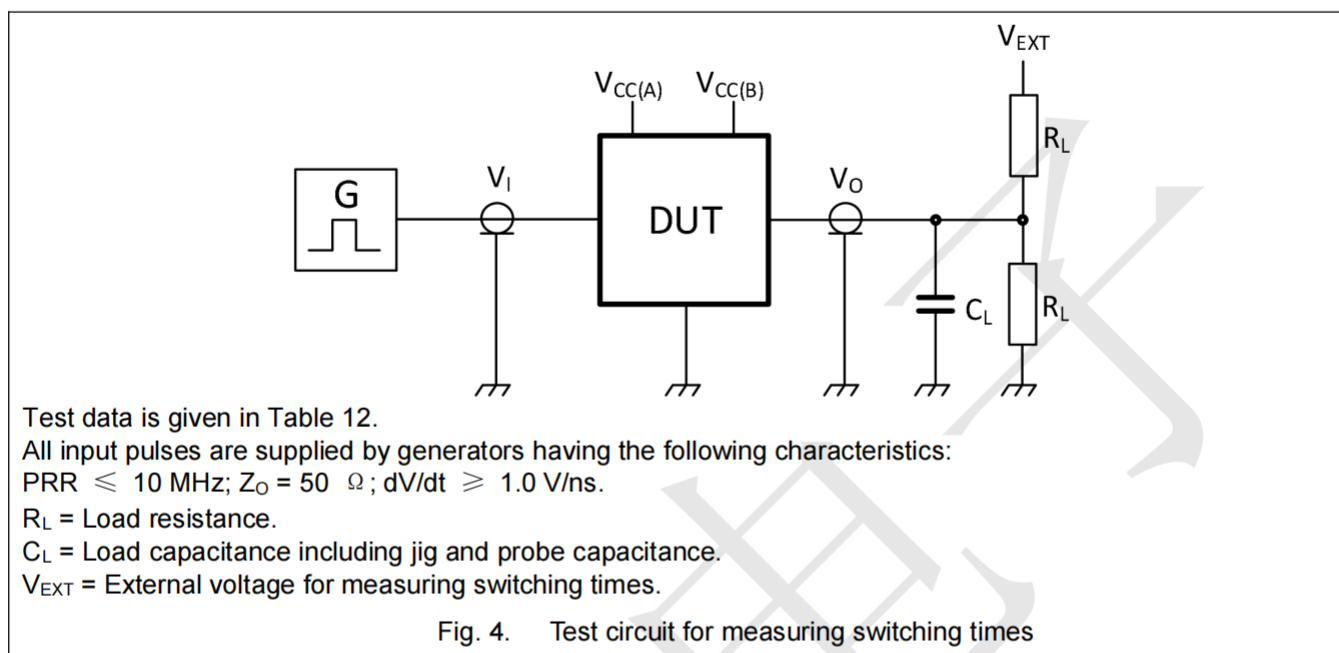
[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.



4-Bit Bidirectional Level Shifter for Open-Drian and Push-Pull Application

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Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	$\Delta t/\Delta V$	C_L	R_L [2]	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
1.3 V to 5.5 V	1.65 V to 5.5 V	V_{CCI}	$\leq 2.5 \text{ ns/V}$	15 pF	50 k Ω , 1M Ω	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, $R_L = 1 \text{ M}\Omega$. For measuring enable and disable times, $R_L = 50 \text{ k}\Omega$.

[3] V_{CCO} is the supply voltage associated with the outp

4-Bit Bidirectional Level Shifter for Open-Drian and Push-Pull Application

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Application information

Voltage level-translation applications. The can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I²C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports.

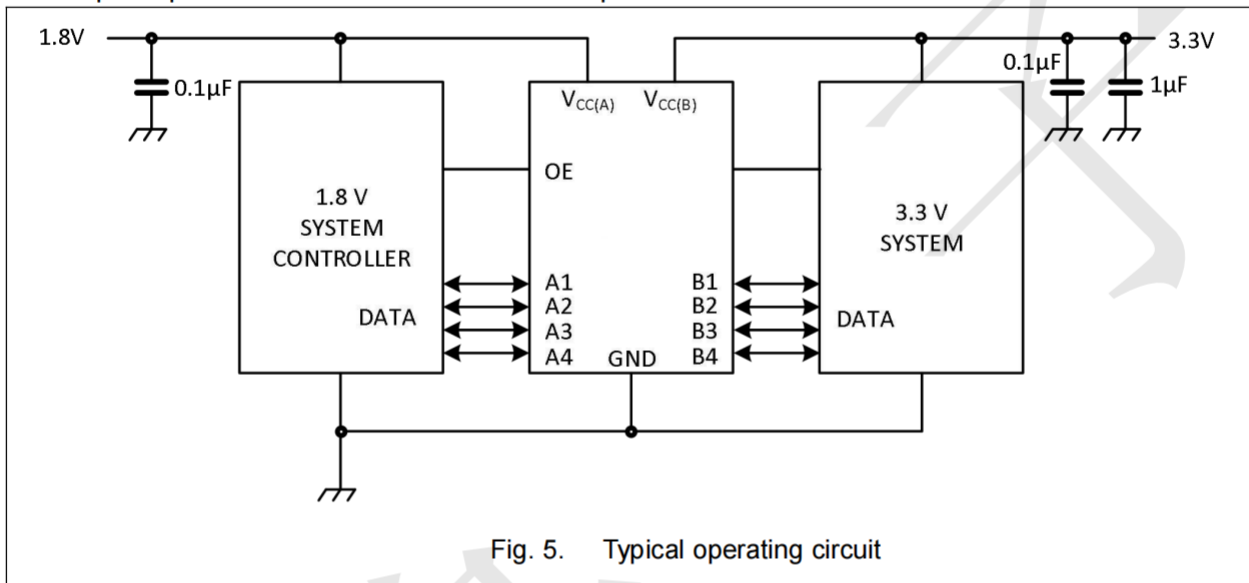


Fig. 5. Typical operating circuit

Architecture

The architecture of the is shown in Fig. 1. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

The is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10 k Ω pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $0.5V_{CC}$; it is de-activated approximately 50 ns after the output reaches $0.5V_{CC}$. During the acceleration time the driver output resistance is between approximately 50 Ω and 70 Ω .

To avoid signal contention and minimize dynamic I_{CC} , the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

Input driver requirements

As the is a switch type translator, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver.

4-Bit Bidirectional Level Shifter for Open-Drian and Push-Pull Application

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Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the around trip delay of any reflection is within the one-shot pulse duration.

Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, and $V_{CC(B)}$ must be ramped up first.

Enable and disable

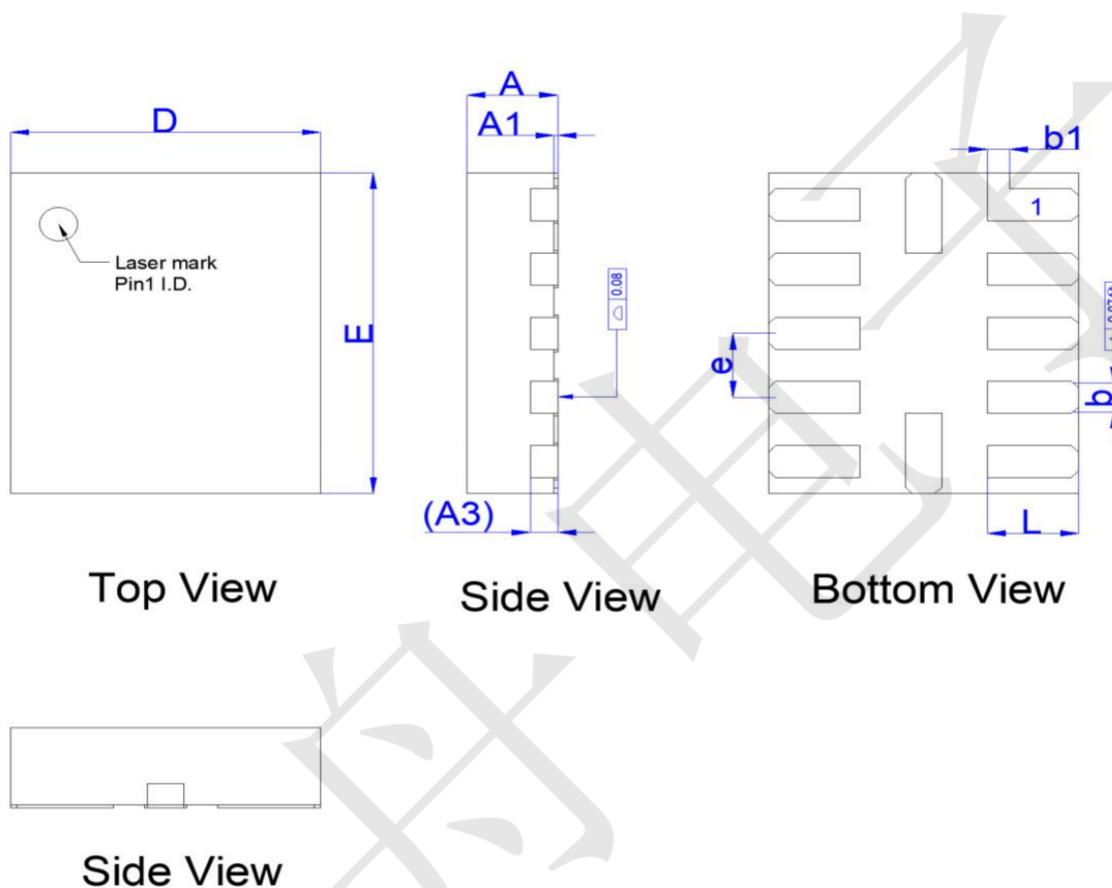
An output enable input (OE) is used to disable the device. Setting OE to LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Pull-up or pull-down resistors on I/O lines

Each A port I/O has an internal 10 k Ω pull-up resistor to $V_{CC(A)}$, and each B port I/O has an internal 10 k Ω pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 k Ω , this will affect the V_{OL} level. When OE goes LOW the internal pull-ups of the are disabled.

Package Outline Dimensions

UQFN 1.7x2 -12L



Symbol	Dimension in Millimeters		
	Min.	Typ.	Max.
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.152 Ref.		
b	0.15	0.20	0.25
b1	0.12 Ref.		
D	1.60	1.70	1.80
E	11.90	2.00	2.10
e	0.35	0.40	0.45
L	0.45	0.50	0.55