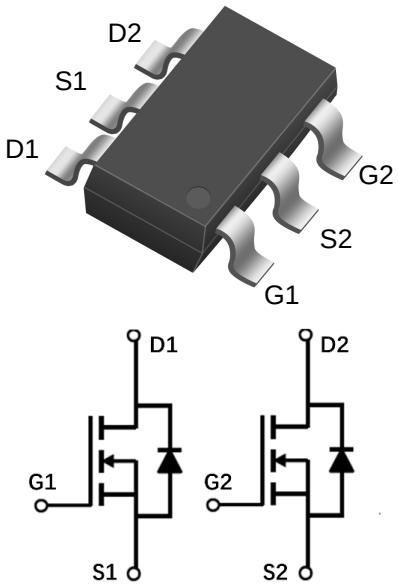
Description：

This Dual N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.



Features：

1) V_{DS}=30V,I_D=5A,$R_{DS(ON)}$<28mΩ @V_{GS}=10V（Typ：22mΩ）
2) Low gate charge.
3) Green device available.
4) Advanced high cell denity trench technology for ultra low $R_{DS(ON)}$.
5) Excellent package for good heat dissipation.
6) MSL3

Package Marking and Ordering Information：

Part NO.	Marking	Package	Packing
DO4842A	4842A	SOT-23-6D	3000pcs/Reel

Absolute Maximum Ratings：(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current-T_A=25℃[1]	5	A
	Continuous Drain Current-T_A=100℃[1]	3.5	
I_{DM}	Pulsed Drain Current[2]	20	
P_D	Power Dissipation	1.25	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55-+150	℃

Thermal Characteristics：

Symbol	Parameter	Max	Units
$R_{\theta JA}$	Thermal Resistance,Junction to Ambient	100	℃/W

Electrical Characteristics: (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=30V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[3]	V_{GS}=10V,I_D=4A	---	22	28	mΩ
		V_{GS}=4.5V,I_D=3A	---	32	42	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	---	400	---	pF
C_{oss}	Output Capacitance		---	59	---	
C_{rss}	Reverse Transfer Capacitance		---	47	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=10V,I_D=3A R_{ENG}=3Ω,V_{GS}=15V	---	2	---	ns
t_r	Rise Time		---	6	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	64	---	ns
t_f	Fall Time		---	35	---	ns
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=3A	---	8.5	---	nC
Q_{gs}	Gate-Source Charge		---	1.5	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	2	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_{SD}=5A	---	---	1.2	V
I_S	Continuous Drain Curren	V_D=V_G=0V	---	---	5	A
I_{SM}	Pulsed Drain Current		---	---	20	A
Trr	Reverse Recovery Time	I_F=3A,T_J=25℃ dI/dt=100A/us	---	6	---	ns
Qrr	Reverse Recovery Charge		---	2	---	nC

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics: (T_A=25℃ unless otherwise noted)

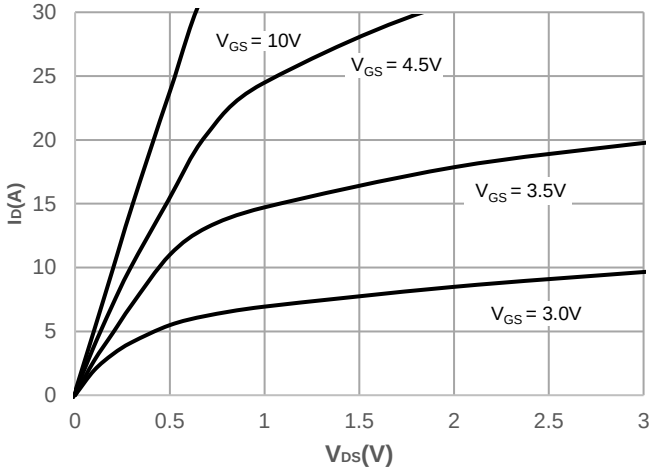


Figure 1: Output Characteristics

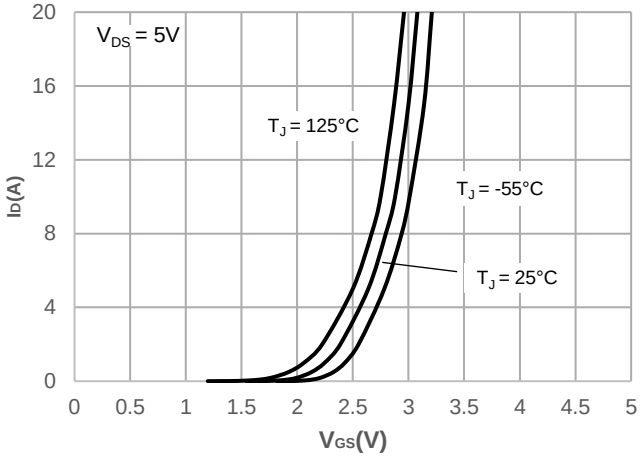


Figure 2: Typical Transfer Characteristics

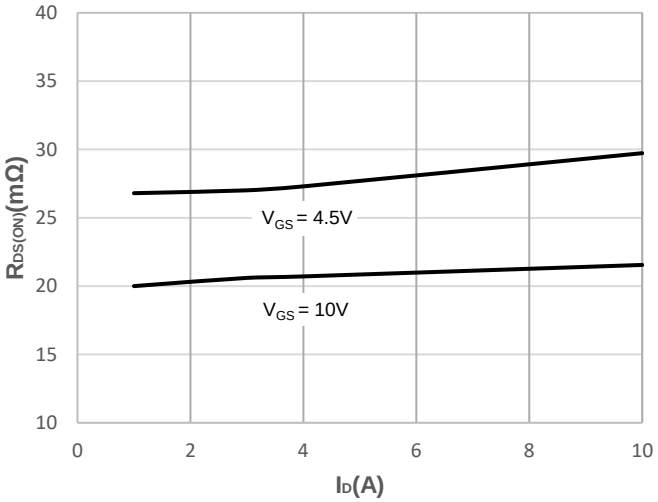


Figure 3: On-resistance vs. Drain Current

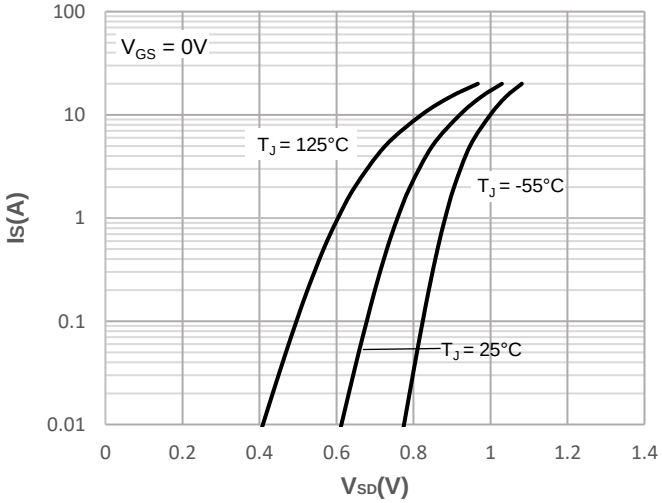


Figure 4: Body Diode Characteristics

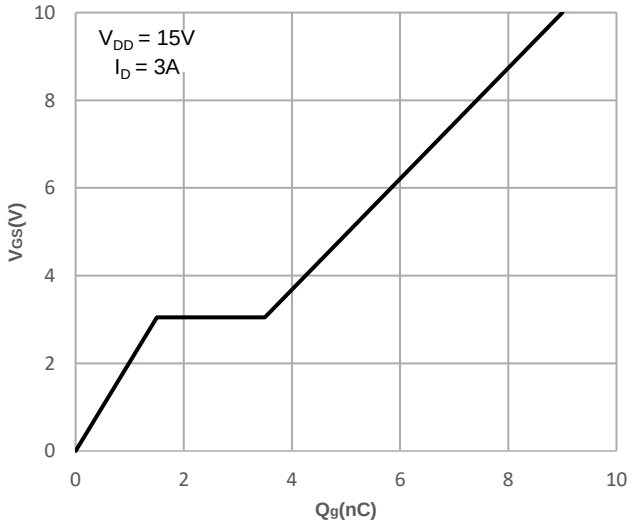


Figure 5: Gate Charge Characteristics

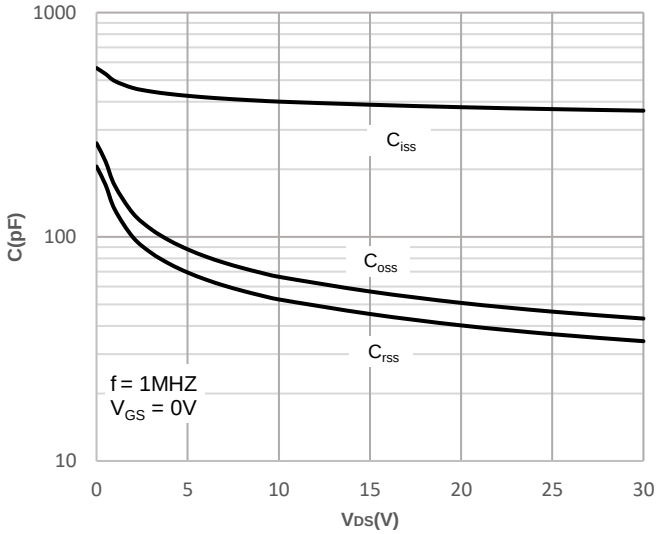


Figure 6: Capacitance Characteristics

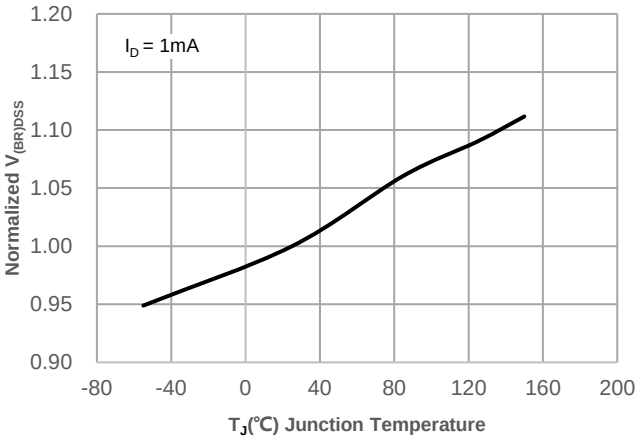


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

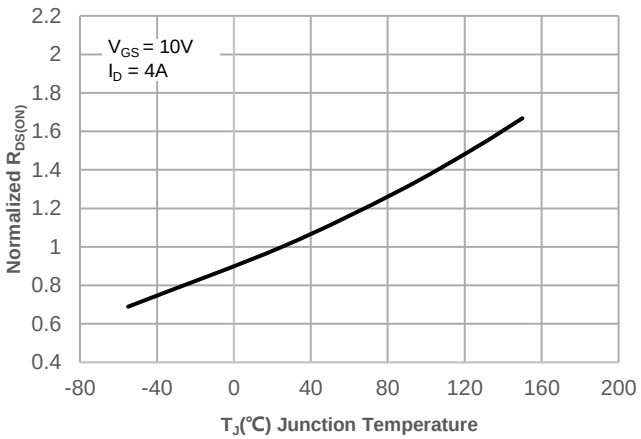


Figure 8: Normalized on Resistance vs. Junction Temperature

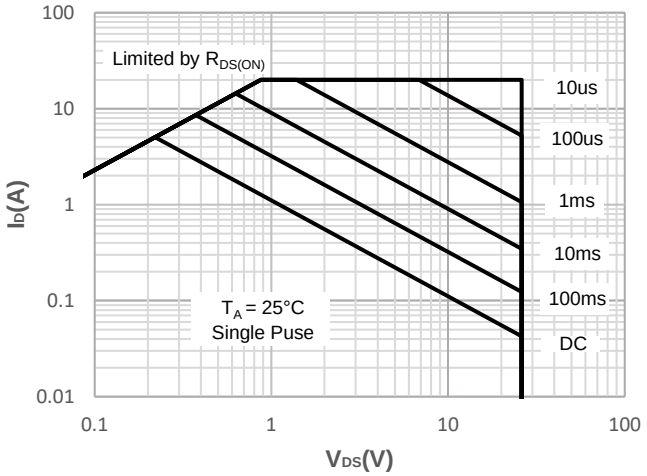


Figure 9: Maximum Safe Operating Area

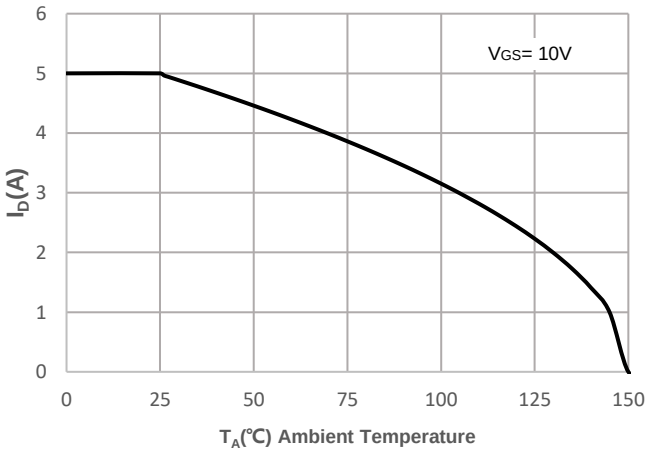


Figure 10: Maximum Continuous Drian Current vs. Ambient Temperature

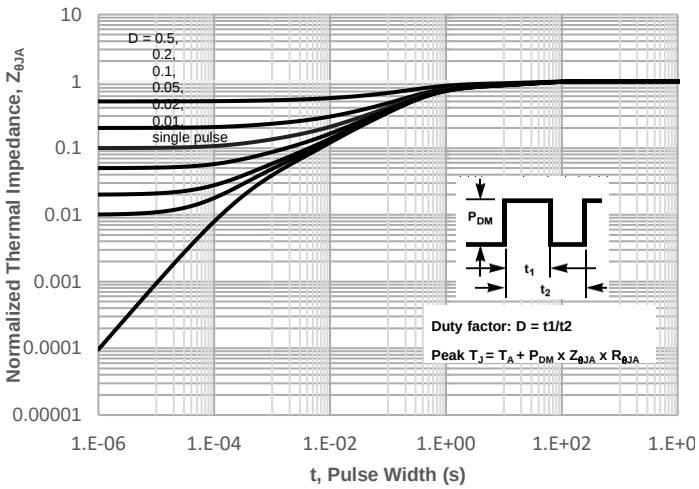


Figure 11: Normalized Maximum Transient Thermal Impedance

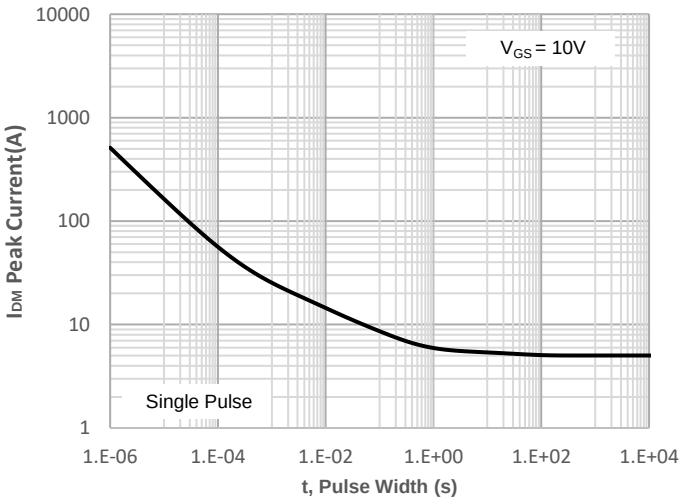
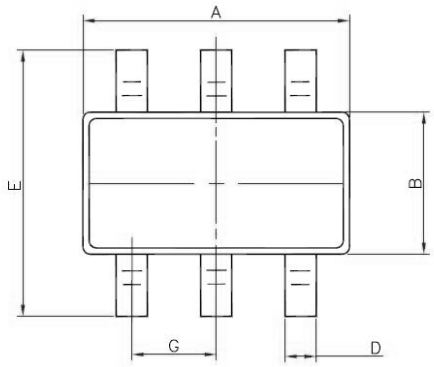
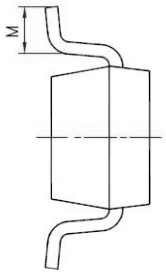
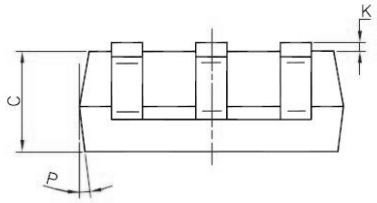


Figure 12: Peak Current Capacity

SOT-23-6D Package Outline Data





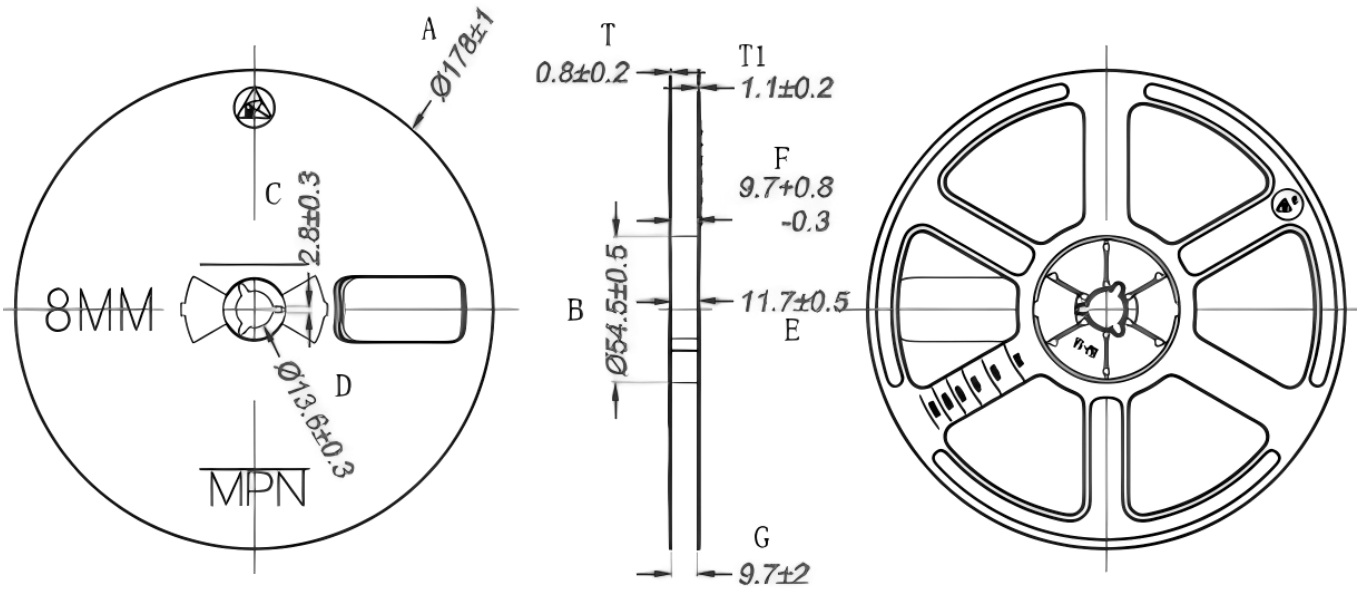


UNIT: mm

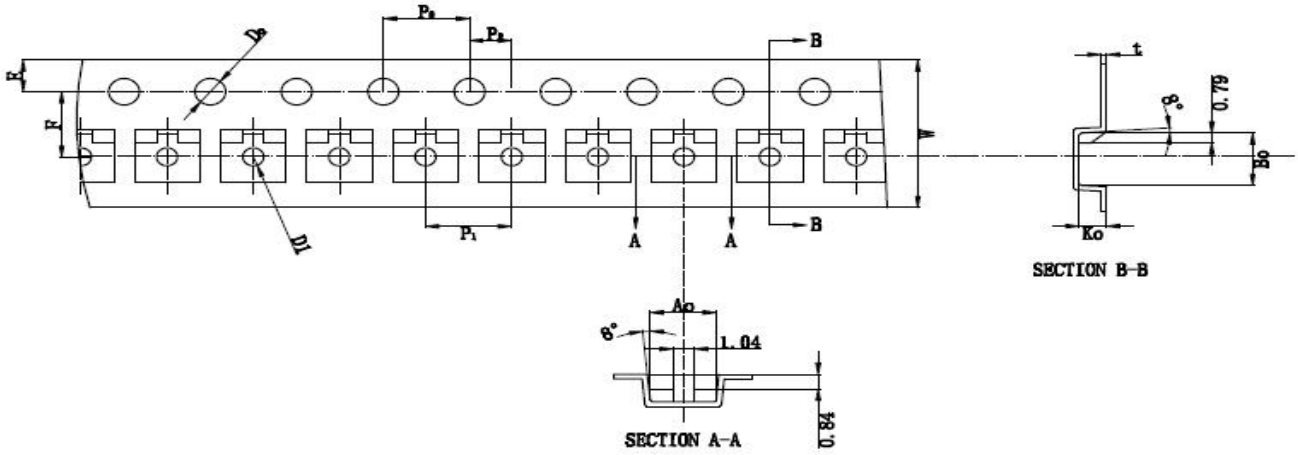
DIM	MILLIMETERS
A	2.82~3.02
B	1.60 ± 0.10
C	1.10 ± 0.05
D	0.40 ± 0.10
E	2.65~2.95
G	0.95typ
K	0.00~0.10
M	0.20MIN
P	9 ± 2°

Tape & Reel Information

Dimensions in mm

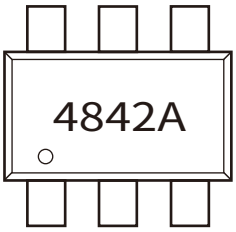


PKG TYPE	W	P	E	F	D	D1	Po	Po10	P2	A0	B0	K0	T
SOT23-6	8.00	4.00	1.75	3.50	1.50	1.00	4.00	40.00	2.00	3.13	3.22	1.30	0.20
Tolerance	±0.2	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.2	±0.1	±0.1	±0.1	±0.1	±0.03



Pulling direction

Marking Information：



Previous Version

Version	Date	Subjects (major changes since last revision)
1.1	2025-05-20	Release of final version

Attention :

- Information furnished in this document is believed to be accurate and reliable. However, Shenzhen Doingter Semiconductor Co.,Ltd. assumes noresponsibility for the consequences of use without consideration for such information nor use beyond it.
- Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Shenzhen Doingter complies with the agreement. Products and information provided in this document have no infringement of patents.
- Shenzhen Doingter assumes noresponsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied. Is a registered trademark of Shenzhen Doingter Semiconductor Co., Ltd. Copyright © 2013 Shenzhen DoingterSemiconductor Co.,Ltd. Printed All rights reserved.