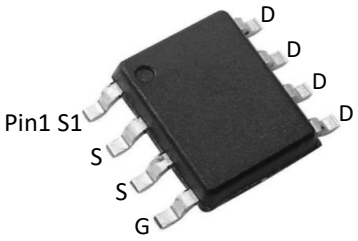
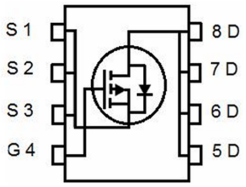
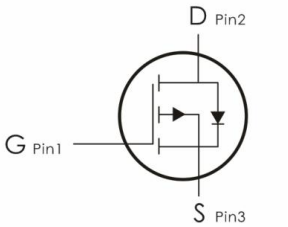
Description：

This P-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.







Features：

1) V_{DS}=-30V,I_D=-12A,$R_{DS(ON)}$<11mΩ @V_{GS}=-10V（Typ：8.5mΩ）
2) Low gate charge.
3) Green device available.
4) Advanced high cell denity trench technology for ultra low $R_{DS(ON)}$.
5) Excellent package for good heat dissipation.
6) MSL3

Package Marking and Ordering Information：

Part NO.	Marking	Package	Packing
SC014PG	C014P	SOP-8	3000 pcs/Reel

Absolute Maximum Ratings： (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current [1]	-12	A
	Continuous Drain Current-T_A=100℃ [1]	-8.4	
I_{DM}	Pulsed Drain Current [2]	-48	
P_D	Power Dissipation	3.3	W
E_{AS}	Single pulse avalanche energy [3]	133	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55-+150	℃

Thermal Characteristics：

Symbol	Parameter	Max	Units
$R_{\theta JA}$	Thermal Resistance,Junction to Ambient	38	℃/ W

Electrical Characteristics: (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	-30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=-30V	---	---	-1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	-1	-1.6	-3	V
$R_{DS(ON)}$	Drain-Source On Resistance[4]	V_{GS}=-10V,I_D=-10A	---	7	10	mΩ
		V_{GS}=-4.5V,I_D=-5A	---	11.5	14	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz	---	2350	---	pF
C_{oss}	Output Capacitance		---	341	--	
C_{rss}	Reverse Transfer Capacitance		---	315	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_G=2.5Ω, I_D=-6A,V_{GS}=-10V	---	14	---	ns
t_r	Rise Time		---	20	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	95	---	ns
t_f	Fall Time		---	65	---	ns
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-12A	---	30	---	nC
Q_{gs}	Gate-Source Charge		---	5.3	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	7.6	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_{SD}=-12A	---	---	-1.2	V
I_S	Continuous Drain Current	V_D=V_G=0V	---	---	-10	A
I_{SM}	Pulsed Drain Current		---	---	-40	A

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : TJ=25℃,VDD=-15V,V_G=-10V,L=0.5mH
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics: (T_A=25℃ unless otherwise noted)

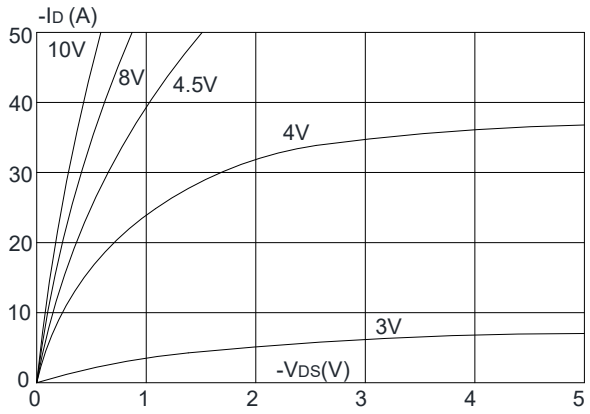


Figure1: Output Characteristics

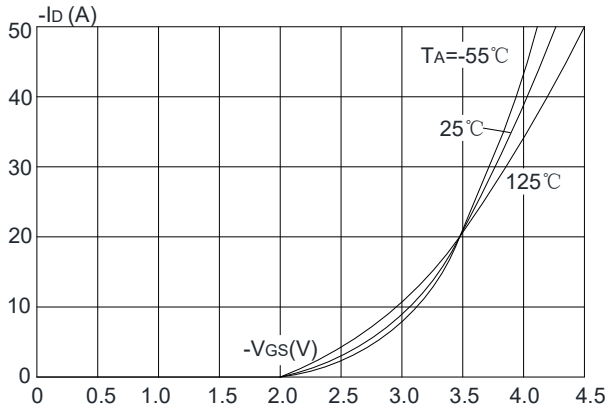


Figure 2: Typical Transfer Characteristics

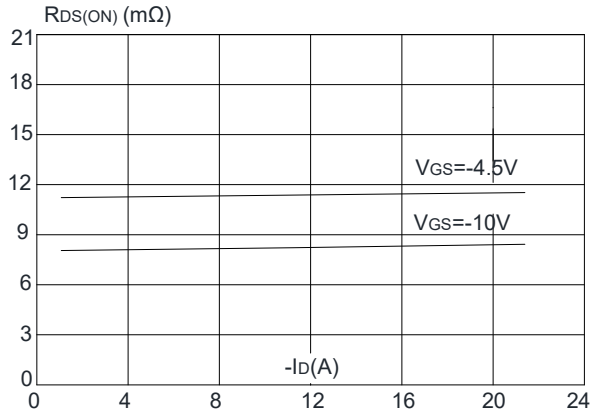


Figure 3: On-resistance vs. Drain Current

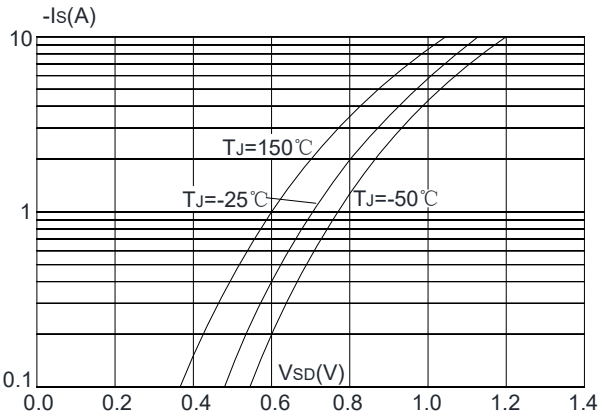


Figure 4: Body Diode Characteristics

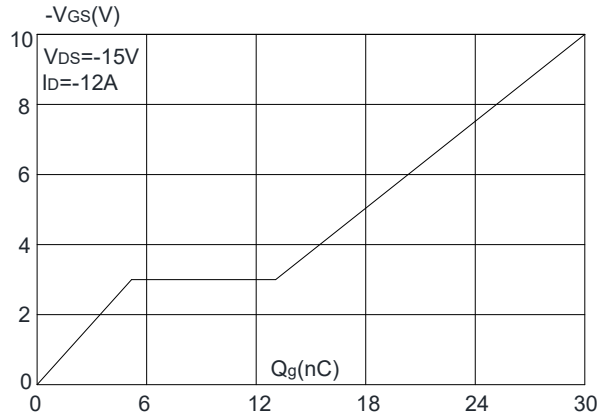


Figure 5: Gate Charge Characteristics

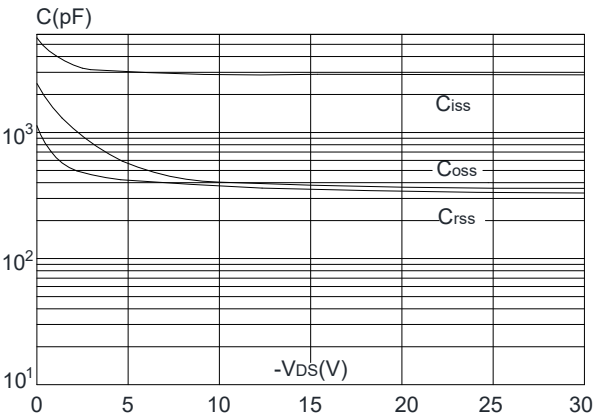


Figure 6: Capacitance Characteristics

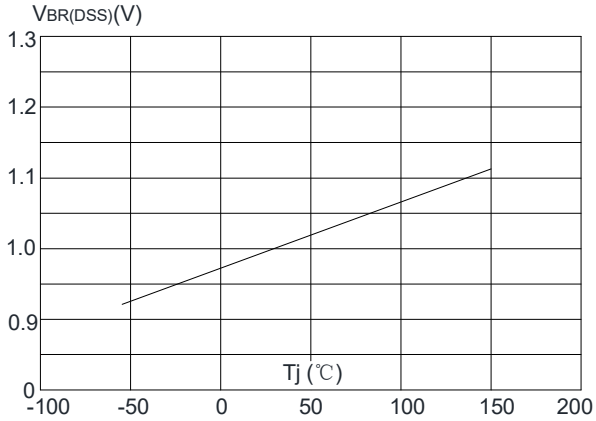


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

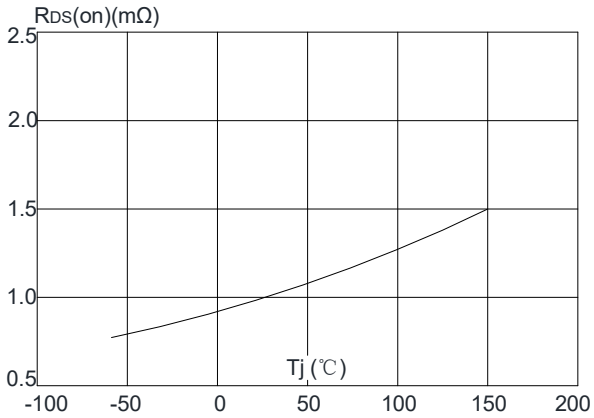


Figure 8: Normalized on Resistance vs. Junction Temperature

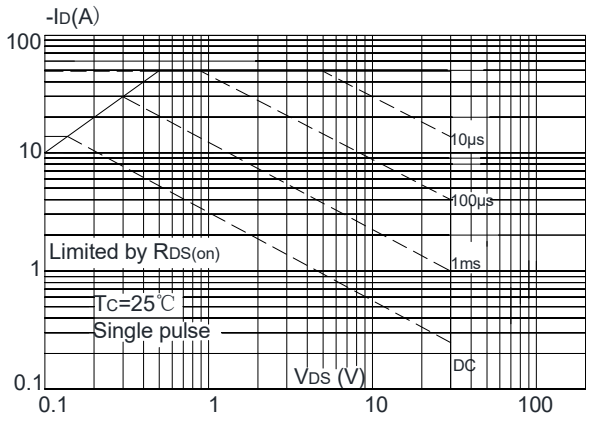


Figure 9: Maximum Safe Operating Area

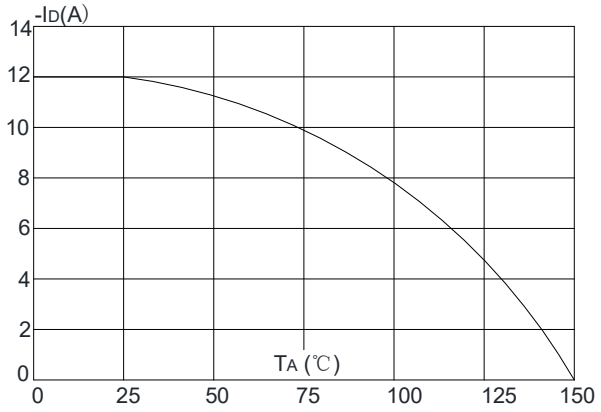


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

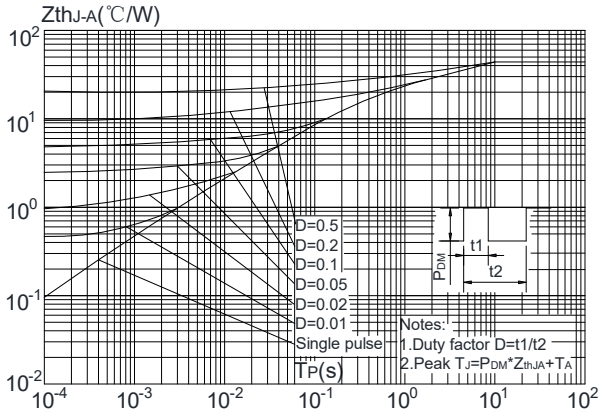
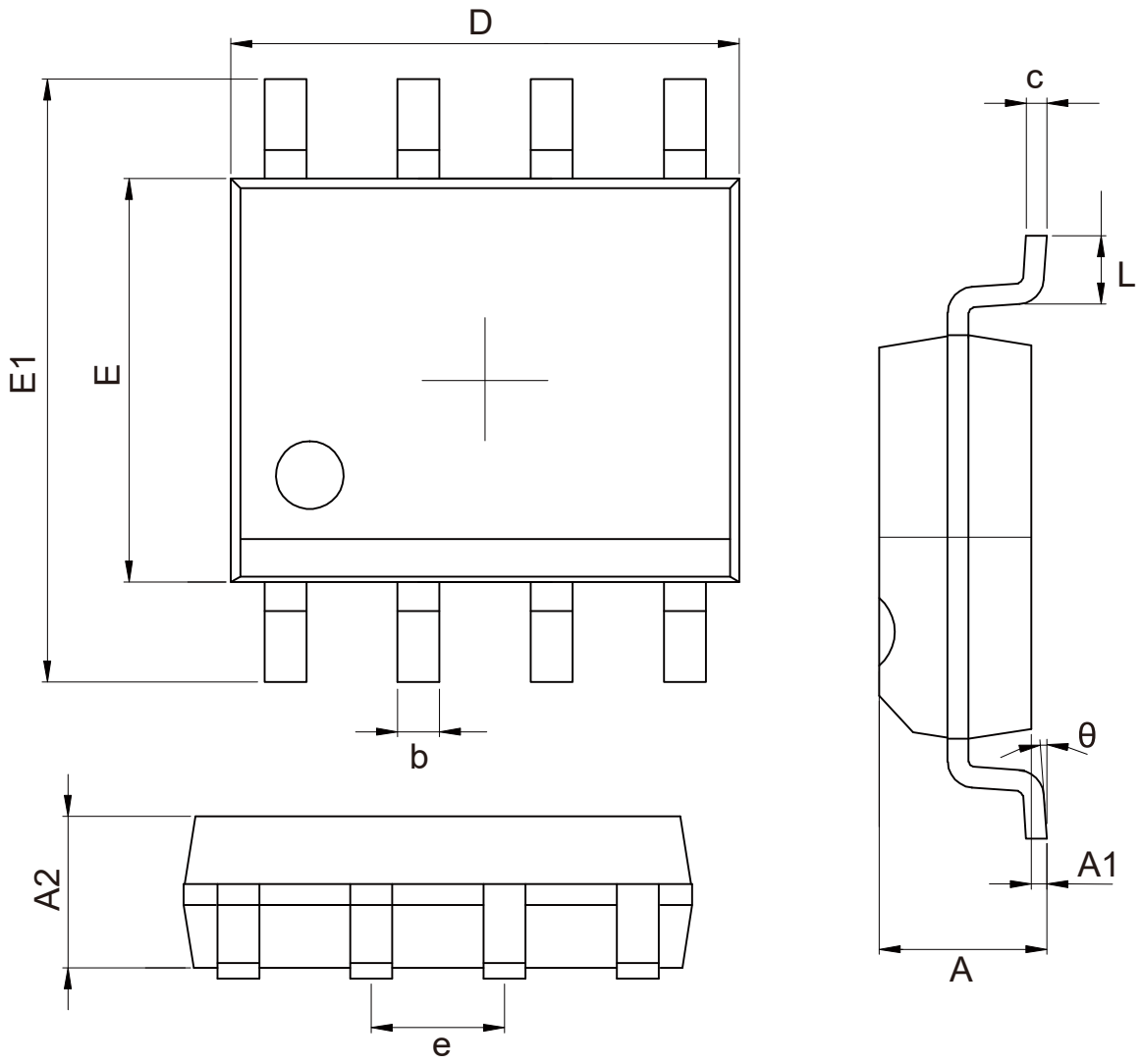


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SOP-8 Package Information：

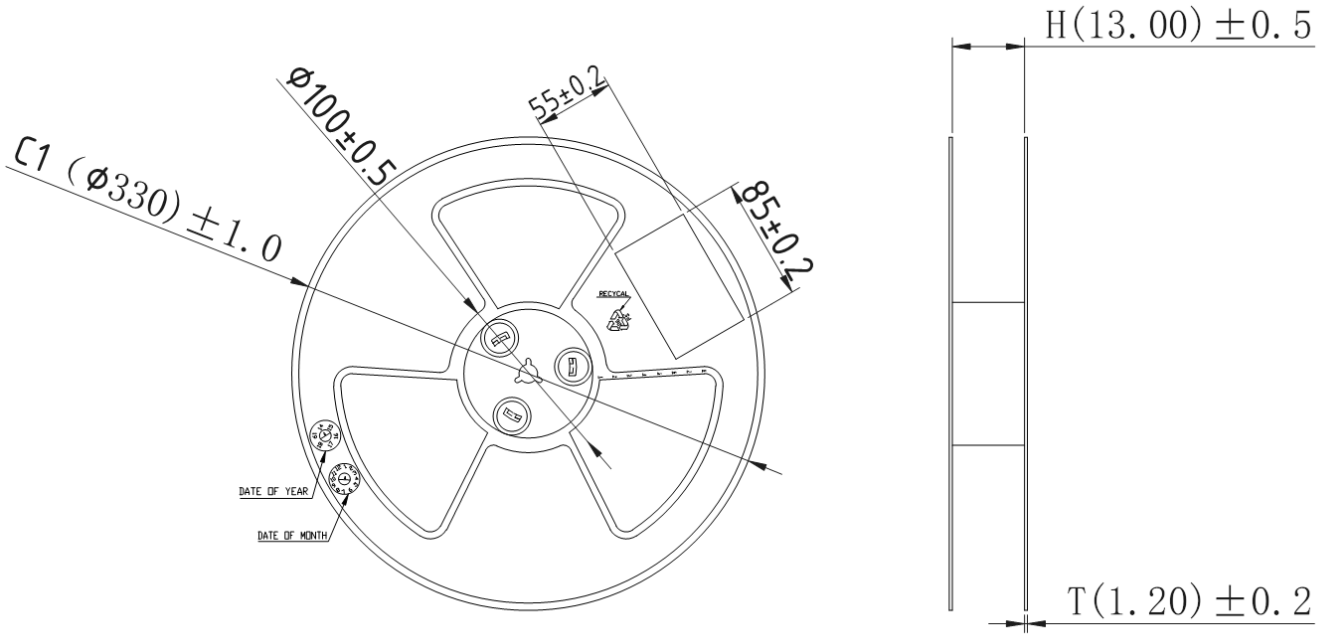


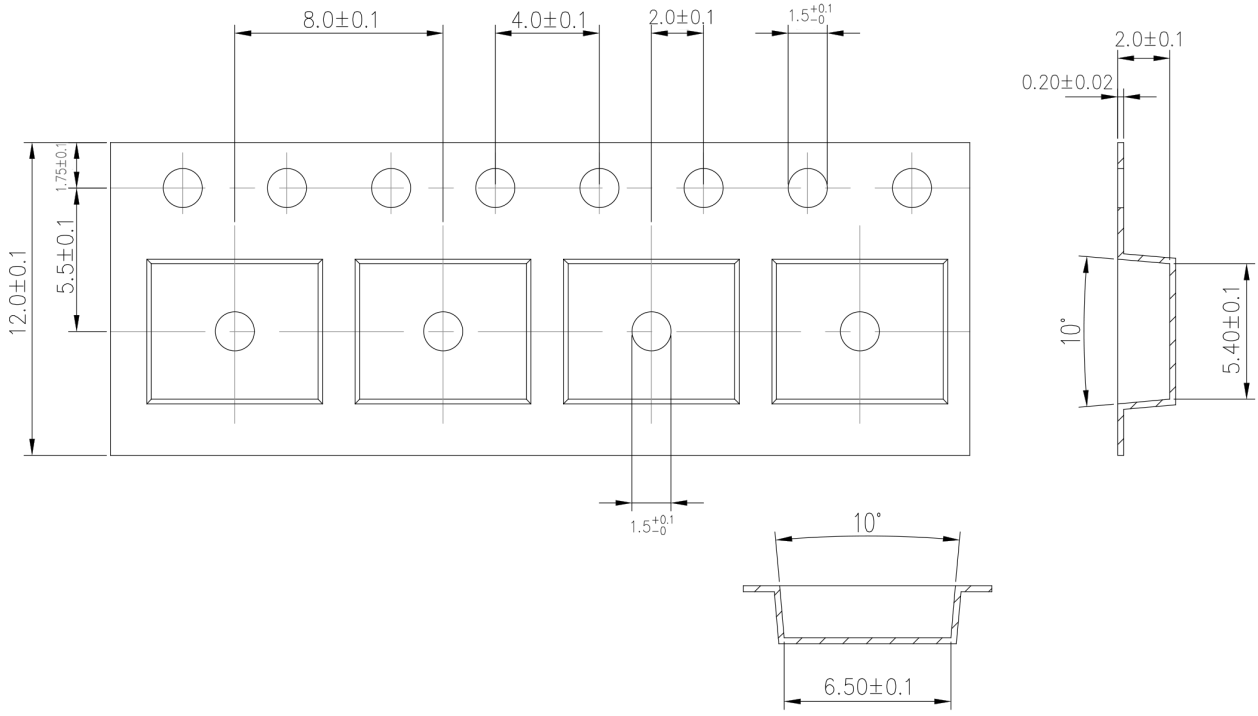
COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	1.350	——	1.750
A1	0.100	——	0.250
A2	1.350	——	1.550
b	0.330	——	0.510
c	0.170	——	0.250
D	4.700	——	5.100
E	3.800	3.900	4.000
E1	5.800	——	6.200
e	1.270BSC		
L	0.400	——	1.270
θ	0°	--	8°

Unit:mm

Tape & Reel Information

Dimensions in mm





Pulling direction →

Marking Information：

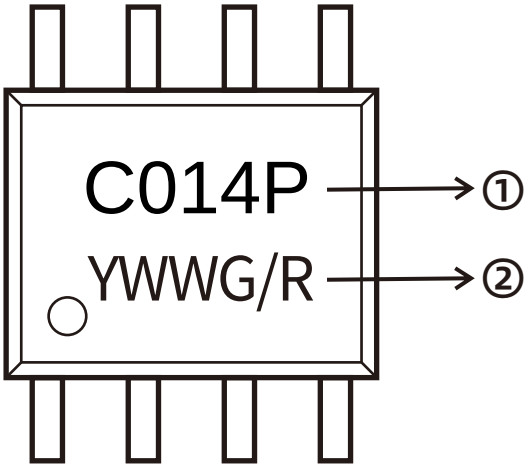
①. Part NO.

②. Date Code(YWWG / R)

Y : Year Code , last digit of the year

WW : Week Code(01-53)

G/R : G(Green) /R(Lead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.2	2026-05-15	Release of final version

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