

1. General Description

The HEF4013 is a dual D-type flip-flop that features independent set-direct input (SD), clear-direct input (CD), clock input (CP) and outputs (Q, $\overline{Q}$). Data is accepted when CP is LOW and is transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous CD and SD inputs are independent and override the D or CP inputs. The outputs are buffered for best system performance. The clock input's Schmitt-trigger action makes the circuit highly tolerant of slower clock rise and fall times.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and Benefits

- Wide supply voltage range from 3 V to 15 V
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Tolerant of slow clock rise and fall times
- Specified from -40 °C to +125 °C
- Packaging information: SOP14 / TSSOP14

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
HEF4013BT	SOP-14	plastic small outline package; 16 leads; body width 3.9 mm	2500
HEF4013BTT	TSSOP-14	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500

4. Function Diagram

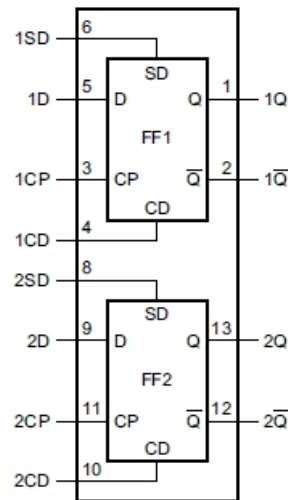


Fig. 1. Functional diagram

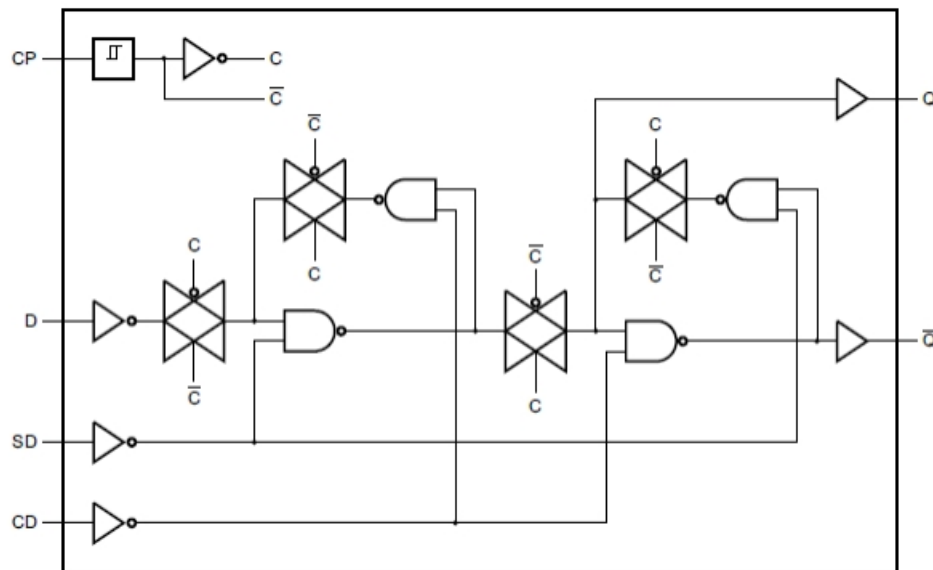
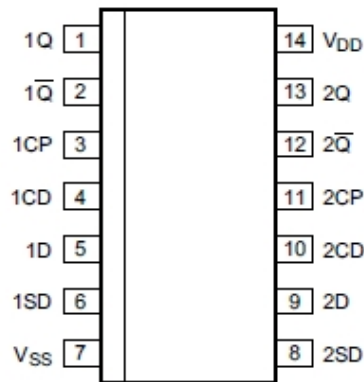


Fig. 2. Logic diagram (one flip-flop)

5. Pinning Information

Pinning



Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q	1	true output
1 $\overline{Q}$	2	complement output
1CP	3	clock input (LOW to HIGH edge-triggered)
1CD	4	asynchronous clear-direct input (active HIGH)
1D	5	data input
1SD	6	asynchronous set-direct input (active HIGH)
V _{SS}	7	ground (0V)
2SD	8	asynchronous set-direct input (active HIGH)
2D	9	data input
2CD	10	asynchronous clear-direct input (active HIGH)
2CP	11	clock input (LOW to HIGH edge-triggered)
2 $\overline{Q}$	12	complement output
2Q	13	true output
V _{DD}	14	supply voltage

6. Functional Description

Function table

Table 3. Function table

H = HIGH voltage level ; L = LOW voltage level ; X = don't care ; $\uparrow$ = LOW-to-HIGH transition

Input				Output	
nSD	nCD	nCP	nD	nQ	$\overline{nQ}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	$\uparrow$	L	L	H
L	L	$\uparrow$	H	H	L

7. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.)

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{DD}	supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	any one input		-	± 10	mA
V_I	input voltage	all inputs		-0.5	$V_{DD}+0.5$	V
T_{stg}	storage temperature	-		-65	+150	$^{\circ}\text{C}$
P_{tot}	total power dissipation	-		-	500	mW
P	device dissipation	per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	260		$^{\circ}\text{C}$

8. Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	supply voltage	-	3	-	15	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
t_{su}	set-up time	$V_{DD}=5V$	40	-	-	ns
		$V_{DD}=10V$	20	-	-	ns
		$V_{DD}=15V$	15	-	-	ns
t_{wCL}	clock pulse width	$V_{DD}=5V$	140	-	-	ns
		$V_{DD}=10V$	60	-	-	ns
		$V_{DD}=15V$	40	-	-	ns
f_{CL}	clock input frequency	$V_{DD}=5V$	3.5	7	-	MHz
		$V_{DD}=10V$	8	16	-	MHz
		$V_{DD}=15V$	12	24	-	MHz
t_{rCL}, t_{fCL}	clock rise and fall time	$V_{DD}=5V$	-	-	15	us
		$V_{DD}=10V$	-	-	10	us
		$V_{DD}=15V$	-	-	5	us
$t_{WS/R}$	Set or reset pulse width	$V_{DD}=5V$	180	-	-	ns
		$V_{DD}=10V$	80	-	-	ns
		$V_{DD}=15V$	50	-	-	ns

Note: If more than one unit is cascaded in a parallel clocked operation, t_{rCL} must be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transistion time of the output driving stage for the estimated capacitive load.

9. Static Characteristics

Table 8. DC Characteristics 1

$T_{amb} = 25\text{ }^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)			$T_{amb}=25\text{ }^{\circ}\text{C}$			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
I_{DD}	supply current	-	0, 5	5	-	-	1	μA
		-	0, 10	10	-	-	2	μA
		-	0, 15	15	-	-	4	μA
I_{OL}	LOW-level output current	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
I_{OH}	HIGH-level output current	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
V_{OL}	LOW-level output voltage	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
V_{OH}	HIGH-level output voltage	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
V_{IL}	LOW-level input voltage	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
V_{IH}	HIGH-level input voltage	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
I_I	input leakage current	-	15	15	-	-	± 1	μA

Table 9. DC Characteristics 2

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)			$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		$T_{amb}=+125^{\circ}\text{C}$		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.	
I_{DD}	supply current	-	0, 5	5	-	1	-	30	-	30	μA
		-	0, 10	10	-	2	-	60	-	60	μA
		-	0, 15	15	-	4	-	120	-	120	μA
I_{OL}	LOW-level output current	0.4	0, 5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0, 15	15	4	-	2.8	-	2.4	-	mA
I_{OH}	HIGH-level output current	4.6	0, 5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	-2.4	-	mA
V_{OL}	LOW-level output voltage	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5, 4.5	-	5	-	1.5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
I_I	input leakage current	-	0, 15	15	-	± 1	-	± 1	-	± 1	μA

10. Dynamic Characteristics

Table 10. AC Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$, $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 20\text{ k}\Omega$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
t_{PHL}	HIGH to LOW propagation delay	nCP to nQ, $\text{n}\overline{\text{Q}}$; see Figure 4	$V_{\text{DD}}=5\text{V}$	-	150	300	ns
			$V_{\text{DD}}=10\text{V}$	-	65	130	ns
			$V_{\text{DD}}=15\text{V}$	-	45	90	ns
		nSD to $\text{n}\overline{\text{Q}}$ or nCD to nQ	$V_{\text{DD}}=5\text{V}$	-	200	400	ns
			$V_{\text{DD}}=10\text{V}$	-	85	170	ns
			$V_{\text{DD}}=15\text{V}$	-	60	120	ns
t_{PLH}	LOW to HIGH propagation delay	nCP to nQ, $\text{n}\overline{\text{Q}}$; see Figure 4	$V_{\text{DD}}=5\text{V}$	-	150	300	ns
			$V_{\text{DD}}=10\text{V}$	-	65	130	ns
			$V_{\text{DD}}=15\text{V}$	-	45	90	ns
		nSD to nQ or nCD to $\text{n}\overline{\text{Q}}$	$V_{\text{DD}}=5\text{V}$	-	150	300	ns
			$V_{\text{DD}}=10\text{V}$	-	65	130	ns
			$V_{\text{DD}}=15\text{V}$	-	45	90	ns
t_{t}	transition time	see Figure 4	$V_{\text{DD}}=5\text{V}$	-	100	200	ns
			$V_{\text{DD}}=10\text{V}$	-	50	100	ns
			$V_{\text{DD}}=15\text{V}$	-	40	80	ns
$f_{\text{clk(max)}}$	maximum clock frequency	see Figure 4	$V_{\text{DD}}=5\text{V}$	3.5	7	-	MHz
			$V_{\text{DD}}=10\text{V}$	8	16	-	MHz
			$V_{\text{DD}}=15\text{V}$	12	24	-	MHz
t_{w}	pulse width	nCP input LOW; see Figure 4	$V_{\text{DD}}=5\text{V}$	-	70	140	ns
			$V_{\text{DD}}=10\text{V}$	-	30	60	ns
			$V_{\text{DD}}=15\text{V}$	-	20	40	ns
		nSD input HIGH or nCD input HIGH; see Figure 5	$V_{\text{DD}}=5\text{V}$	-	90	180	ns
			$V_{\text{DD}}=10\text{V}$	-	40	80	ns
			$V_{\text{DD}}=15\text{V}$	-	25	50	ns
t_{su}	set-up time	nD to nCP; see Figure 4	$V_{\text{DD}}=5\text{V}$	-	20	40	ns
			$V_{\text{DD}}=10\text{V}$	-	10	20	ns
			$V_{\text{DD}}=15\text{V}$	-	7	15	ns
t_{h}	hold time	nD to nCP; see Figure 4	$V_{\text{DD}}=5\text{V}$	-	2	5	ns
			$V_{\text{DD}}=10\text{V}$	-	2	5	ns
			$V_{\text{DD}}=15\text{V}$	-	2	5	ns

HEF4013



Dual D-type Flip-flop

Product datasheet, Rev. 1.0

Aug 08, 2024

t_{rCL} , t_{fCL}	clock input rise or fall time	-	$V_{DD}=5V$	-	-	15	us
			$V_{DD}=10V$	-	-	10	us
			$V_{DD}=15V$	-	-	5	us
C_i	input capacitance	any input		-	5	7.5	pF

Note: t_t is the same as t_{TLH} and t_{THL} .

11. Waveforms and test circuit

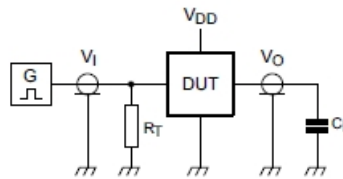


Fig. 3. Test circuit for measuring switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

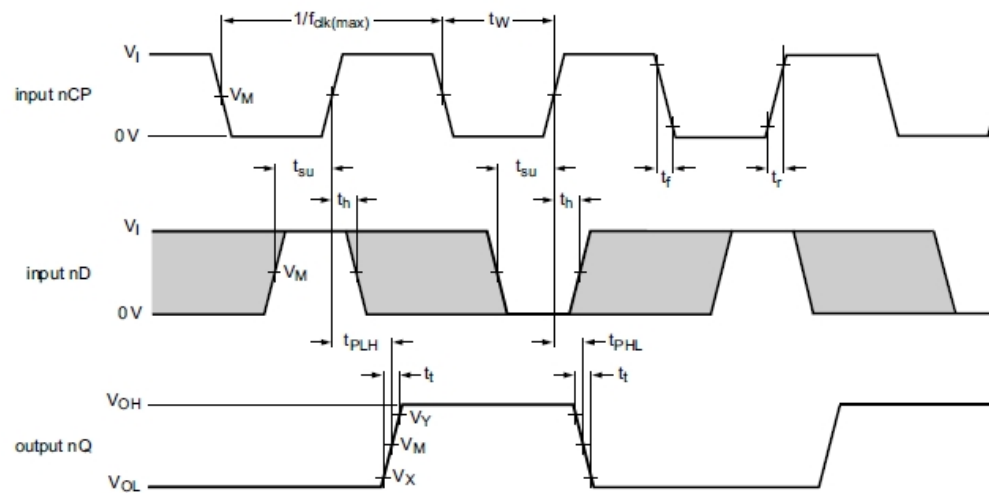


Fig. 4. Set-up time, hold time, minimum clock pulse width, propagation delay and transition times

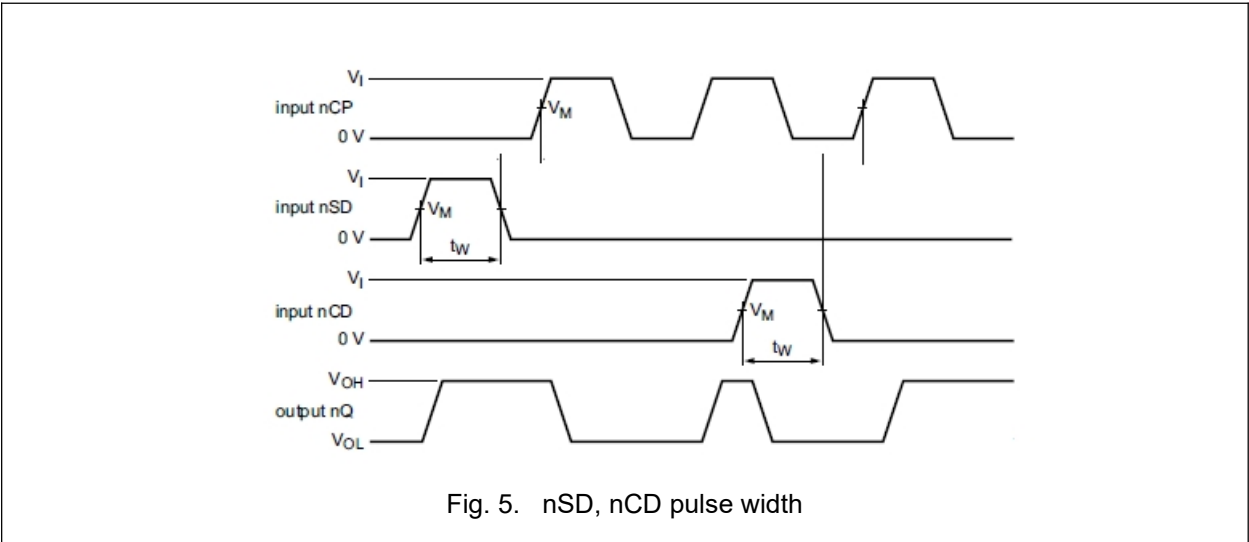


Table 11. Measurement points

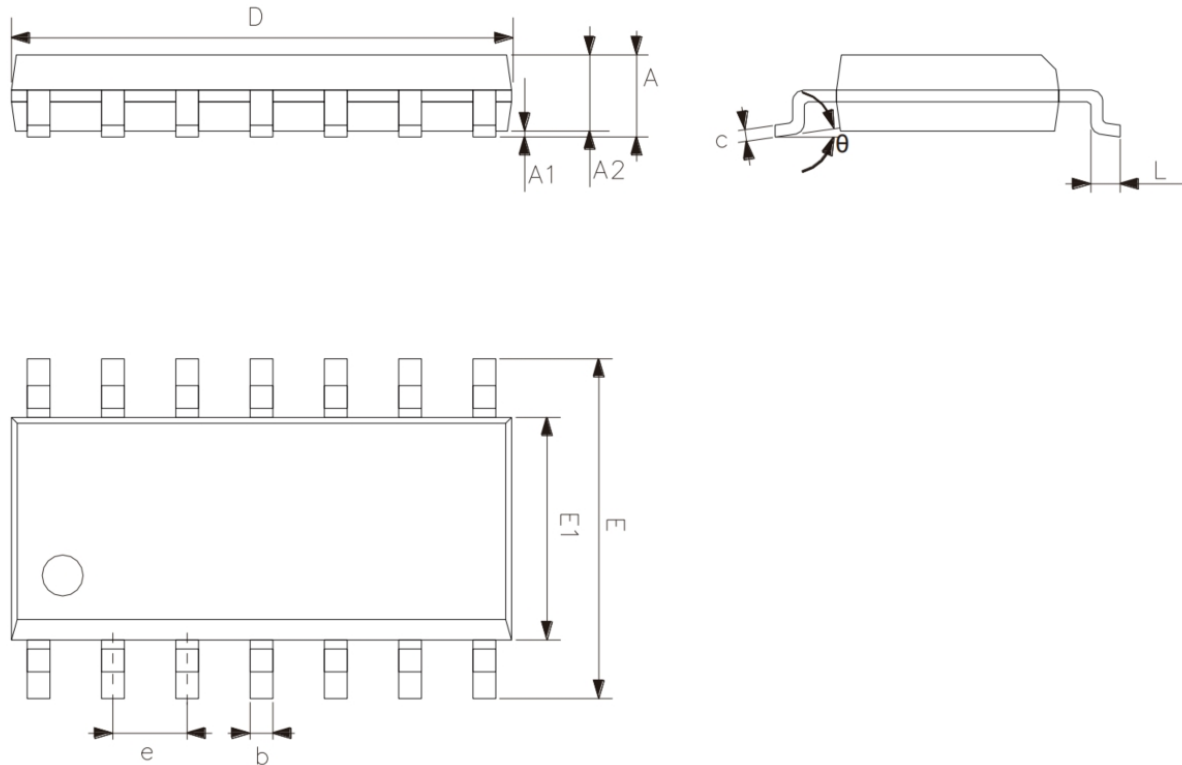
Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$

Table 12. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5V to 15V	V_{SS} or V_{DD}	$\leq 20\text{ns}$	50pF

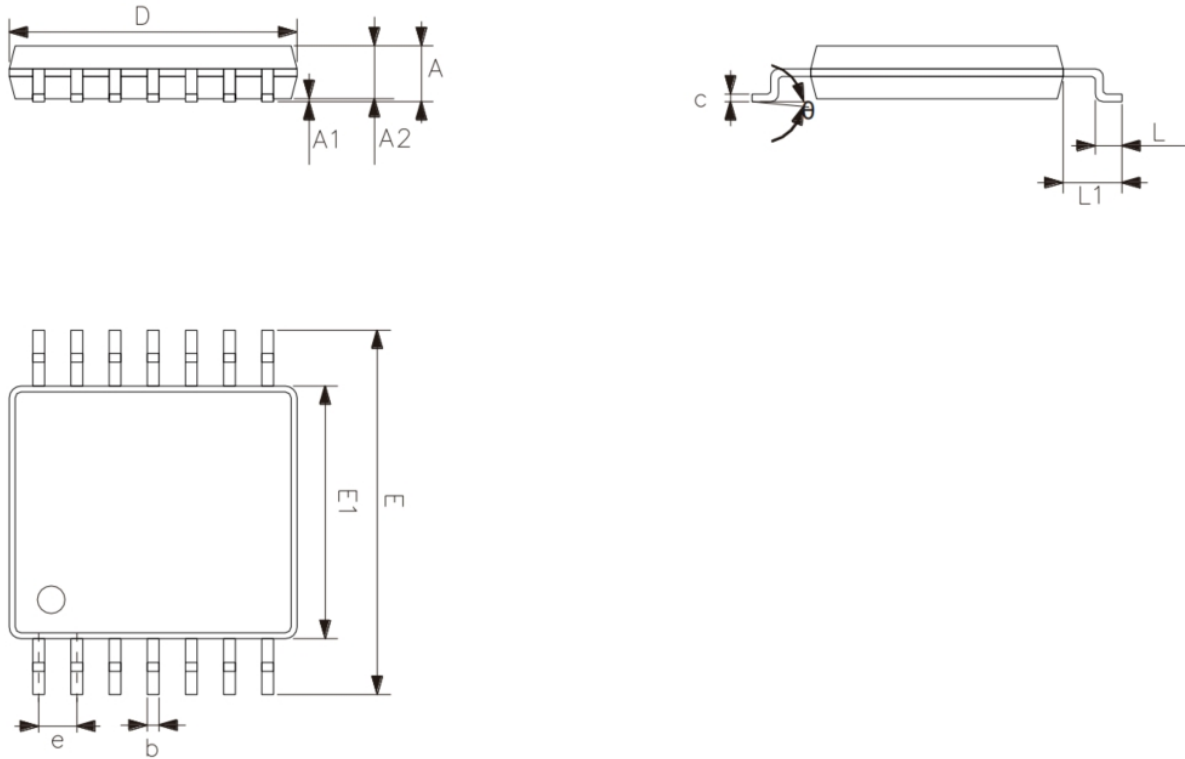
12. Package Outline

SOP-14



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.50	1.75
A1	0.05	0.25
A2	1.30	-
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0°	8°

TSSOP-14



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Document ID	Release Date	Data sheet status	Change notice	Supersedes
HEF4013 Rev. 1.0	Aug 08, 2024	Product datasheet		