

1. General Description

The HEF4052 is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logic includes two select inputs (S1 and S2) and an active LOW enable input ($\overline{E}$). Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY0 to nY3) and the other side connected to a common input/output (nZ). With $\overline{E}$ LOW, one of the four switches is selected (low-impedance ON-state) by S1 and S2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 and S2. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 and S2, and $\overline{E}$). The V_{DD} to V_{SS} range is 3V to 9V. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 9V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2. Features and Benefits

- Wide supply voltage range from 3 V to 9 V
- Fully static operation
- 5 V and 9 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to +125 °C
- Packaging information: SOP16 / TSSOP16

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
HEF4052BT	SOP-16	plastic small outline package; 16 leads; body width 3.9 mm	2500
HEF4052BTT	TSSOP-16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500

4. Function Diagram

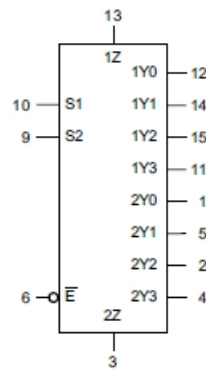


Fig. 1. Logic symbol

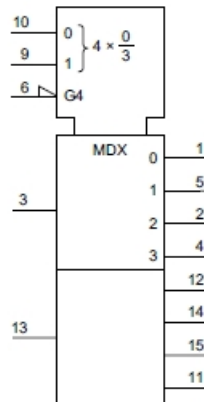


Fig. 2. IEC logic symbol

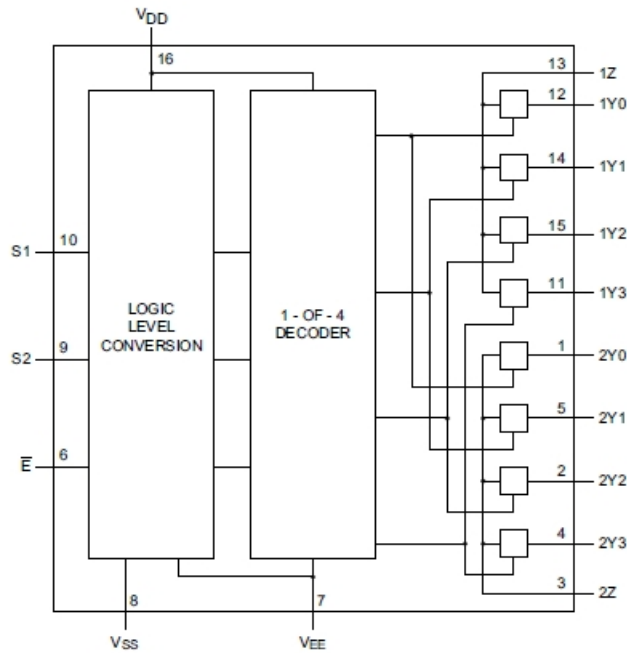


Fig. 3. Functional diagram

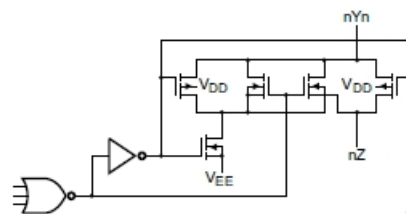


Fig. 4. Schematic diagram (one switch)

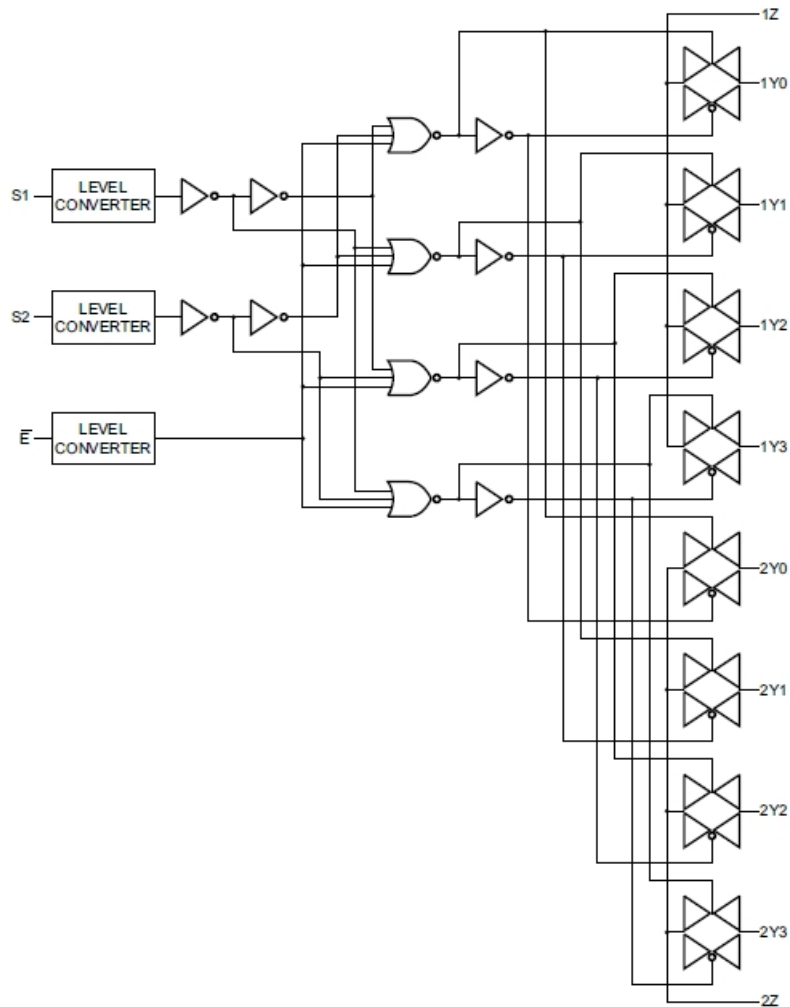
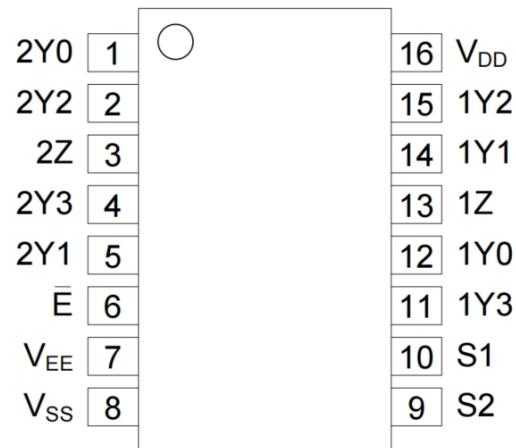


Fig. 5. Logic diagram

5. Pinning Information

Pinning



Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0	1	independent input or output
2Y2	2	independent input or output
2Z	3	common output or input
2Y3	4	independent input or output
2Y1	5	independent input or output
$\bar{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage
V_{SS}	8	ground (0V)
S2	9	select input
S1	10	select input
1Y3	11	independent input or output
1Y0	12	independent input or output
1Z	13	common output or input
1Y1	14	independent input or output
1Y2	15	independent input or output
V_{DD}	16	supply voltage

6. Functional Description

Function table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input			Channel ON
$\overline{E}$	S2	S1	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	switches off

7. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DD}	supply voltage	-	-0.5	+12	V
$V_{DD}-V_{EE}$	power supply range	-	-0.5	+12	V
I_Q	static current	$V_{DD}-V_{EE}=12V$	-	2	μA
V_I	input voltage	-	-0.5	$V_{DD}+0.5$	V
$ I_{IH} $	output high voltage current	$V_{DD}=5V, V_I=V_{DD}$	-	1	μA
$ I_{IL} $	output low voltage current	$V_{DD}=5V, V_I=0V$	-	1	μA
V_{IO}	input and output voltage range	-	$V_{EE}-0.5$	$V_{DD}+0.5$	V
I_{IK}	input clamping current	$V_I < -0.5V$ or $V_I > V_{DD}+0.5V$	-	± 20	mA
I_{IOK}	input and output clamp current	$V_{IO} < V_{EE}-0.5V$ or $V_{IO} > V_{DD}+0.5V$	-	± 20	mA
I_T	switch conduction current	$V_O = -0.5V$ to $V_{DD}+0.5V$	-	± 25	mA
I_{DD}, I_{GND}	V_{DD} or GND current	-	-	± 50	mA
T_{stg}	storage temperature	-	-65	+150	$^{\circ}C$
P_{tot}	total power dissipation	-	-	500	mW
T_L	Soldering temperature	10s	SOP/TSSOP		260 $^{\circ}C$

8. Recommended Operating Conditions

Table 5. Recommended Operating Conditions

 $T_{amb} = 25^{\circ}\text{C}$; $R_L = 10\text{k}\Omega$; $C_L = 50\text{pF}$; $\bar{E} = V_{DD}$; $V_{IS} = V_{DD} = 5\text{V}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	supply voltage	-	3	5	9	V
T_{amb}	ambient temperature	in free air	-40	-	+125	$^{\circ}\text{C}$
V_{EE}	supply voltage	-	-6.0	-	0	V
$V_{DD}-V_{EE}$	supply voltage	-	3.0	-	9.0	V
V_I	input voltage	-	0	-	V_{DD}	V
V_{IO}	input and output voltage	-	V_{EE}	-	V_{DD}	V
t_r, t_f	Input rise and fall time	-	-	-	1000	ns
		-	-	-	500	ns
		-	-	-	400	ns
C_i	input capacitance	-	-	-	7.5	pF

9. Static Characteristics

Table 8. DC Characteristics 1

 $T_{amb} = 25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)		T _{amb} =25℃			Unit
				Min.	Typ.	Max.	
I _{DD}	supply current	V _I =V _{DD} or V _{SS} , I _O =0A	V _{DD} =5V	-	-	20	uA
			V _{DD} =9V	-	-	40	uA
V _{IH}	HIGH-level input voltage	I _O <1uA	V _{DD} =5V	3.5	-	-	V
			V _{DD} =9V	7.0	-	-	V
V _{IL}	LOW-level input voltage	I _O <1uA	V _{DD} =5V	-	-	1.5	V
			V _{DD} =9V	-	-	3.0	V

I _I	input leakage current	V _I =0V or 9V, V _{DD} =9V		-	-	1.0	uA
I _{OZ}	3 state output leakage current	V _{DD} =9V	output to V _{DD}	-	-	1.6	uA
			output to V _{SS}	-	-	-1.6	uA
R _{ON}	ON resistance (rail)	V _I =0V to V _{DD} -V _{EE}	V _{DD} -V _{EE} =5V	-	350	2500	Ω
			V _{DD} -V _{EE} =9V	-	80	245	Ω
		V _I =0V	V _{DD} -V _{EE} =5V	-	115	340	Ω
			V _{DD} -V _{EE} =9V	-	50	160	Ω
		V _I =V _{DD} -V _{EE}	V _{DD} -V _{EE} =5V	-	120	365	Ω
			V _{DD} -V _{EE} =9V	-	65	200	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I =0V to V _{DD} -V _{EE}	V _{DD} -V _{EE} =5V	-	25	-	Ω
			V _{DD} -V _{EE} =9V	-	10	-	Ω
I _{S(OFF)}	OFF-state leakage current	V _{SS} =V _{EE} , V _{DD} -V _{EE} =9V	all channel off; E=V _{DD}	-	-	1.0	uA
			any channel; E=V _{SS}	-	-	1.0	uA

Note: On resistance waveform and test circuit see Figure 13 and Figure 14

Table 9. DC Characteristics 2

$T_{amb} = -40^\circ C$ to $+125^\circ C$, voltages are referenced to $V=$ (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)		T _{amb} =-40℃		T _{amb} =+85℃		T _{amb} =+125℃		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{DD}	supply current	V _I =V _{DD} or V _{SS} , I _O =0A	V _{DD} =5V	-	20	-	150	-	150	μA
			V _{DD} =9V	-	40	-	300	-	300	μA
V _{IH}	HIGH-level input voltage	I _O <1μA	V _{DD} =5V	3.5	-	3.5	-	3.5	-	V
			V _{DD} =9V	7.0	-	7.0	-	7.0	-	V
V _{IL}	LOW-level input voltage	I _O <1μA	V _{DD} =5V	-	1.5	-	1.5	-	1.5	V
			V _{DD} =9V	-	3.0	-	3.0	-	3.0	V
I _I	input leakage current	V _I =0V or 9V, V _{DD} =9V		-	1.0	-	1.0	-	1.0	μA
I _{OZ}	3 state output leakage current	V _{DD} =9V	output to V _{DD}	-	1.6	-	12.0	-	12.0	μA
			output to V _{SS}	-	-1.6	-	-12.0	-	-12.0	μA

10. Dynamic Characteristics

Table 10. AC Characteristics 1

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{EE}=V_{SS} = 0\text{ V}$, $t_r, t_f \leq 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
t _{PHL}	HIGH to LOW propagation delay time	Yn to Z; Z to Yn; see Figure 7	V _{DD} =5V	-	10	20	ns
			V _{DD} =9V	-	5	10	ns
		Sn to Yn, Z; see Figure 8	V _{DD} =5V	-	150	305	ns
			V _{DD} =9V	-	65	135	ns
t _{PLH}	LOW to HIGH propagation delay	Yn to Z; Z to Yn; see Figure 7	V _{DD} =5V	-	10	20	ns
			V _{DD} =9V	-	5	10	ns
		Sn to Yn, Z; see Figure 8	V _{DD} =5V	-	150	300	ns
			V _{DD} =9V	-	75	150	ns
t _{PHZ}	HIGH to OFF-state propagation delay	$\overline{E}$ to Yn, Z; see Figure 9	V _{DD} =5V	-	95	190	ns
			V _{DD} =9V	-	90	180	ns
t _{PLZ}	LOW to OFF-state propagation delay	$\overline{E}$ to Yn, Z; see Figure 9	V _{DD} =5V	-	100	205	ns
			V _{DD} =9V	-	90	180	ns
t _{PZH}	OFF-state to HIGH propagation delay	$\overline{E}$ to Yn, Z; see Figure 9	V _{DD} =5V	-	130	260	ns
			V _{DD} =9V	-	55	115	ns
t _{PZL}	OFF-state to LOW propagation delay	$\overline{E}$ to Yn, Z; see Figure 9	V _{DD} =5V	-	120	240	ns
			V _{DD} =9V	-	50	100	ns

Table 11. AC Characteristics11

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{EE}=V_{SS} = 0\text{ V}$, $V_I = 0.5V_{DD}$ (p-p) unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
d _{sin}	Square wave distortion	see Figure 10; R _L =10kΩ; C _L =15pF; channel ON; f _i =1kHz	V _{DD} =5V	0.25	-	-	%
			V _{DD} =9V	0.04	-	-	%
f _{ct}	any two channel crosstalk	V _{DD} =9V, see note2		1	-	-	MHz
V _{ct}	crosstalk voltage ($\overline{E}$ to Sn or Yn to Z)	see Figure 11; R _L =10kΩ; C _L =15pF; $\overline{E}$ or Sn=V _{DD} (square-wave)		50	-	-	mV
f _{OFF}	OFF frequency	V _{DD} =9V, see note3		1	-	-	MHz
f _{ON}	conduction frequency	V _{DD} =5V, see note4		13	-	-	MHz
		V _{DD} =9V, see note4		40	-	-	MHz

[1] f_i is biased at $0.5V_{DD}$; $V_I=0.5V_{DD}$ (p-p).

[2] $R_L=1\text{ k}\Omega$; $20\log V_{os}/V_{is} = -50\text{ dB}$, see Figure 12.

[3] $R_L=1\text{ k}\Omega$; $C_L = 5\text{ pF}$, channel off, $20\log V_{os}/V_{is} = -50\text{ dB}$, see Figure 10.

[4] $R_L=1\text{ k}\Omega$; $C_L = 5\text{ pF}$, channel on, $20\log V_{os}/V_{is} = -3\text{ dB}$, see Figure 10.

11. Waveforms and test circuit

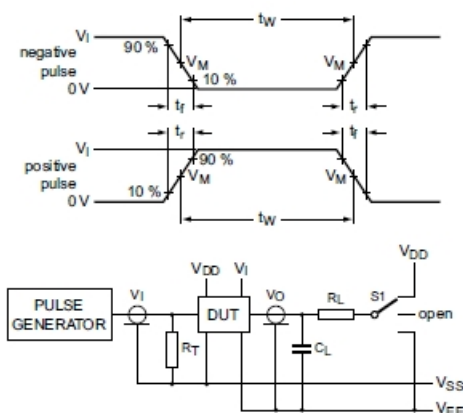


Fig. 6. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

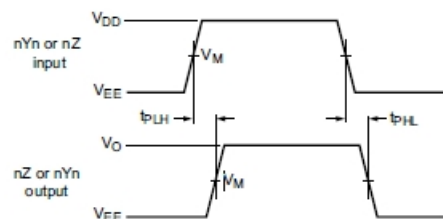
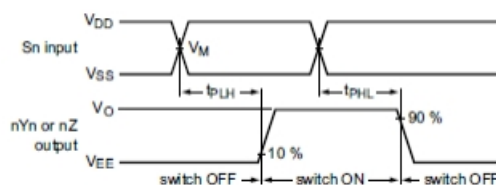


Fig. 7. nYn, nZ to nZ, nYn propagation delays

Fig. 8. S_n to nYn, nZ propagation delays

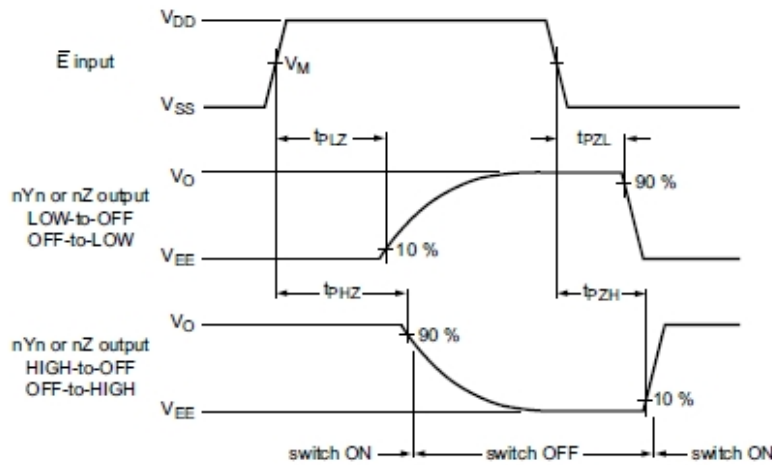


Fig. 9. Enable and disable times

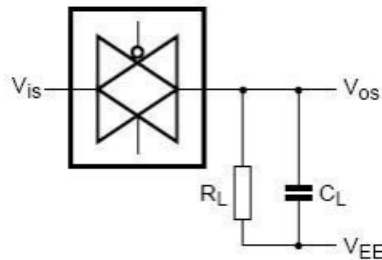


Fig. 10. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

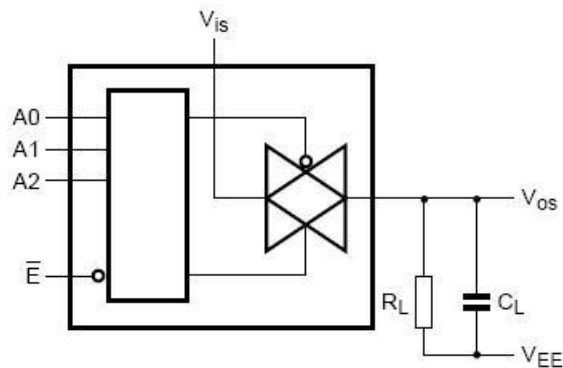


Fig. 11. Crosstalk logical input/output test

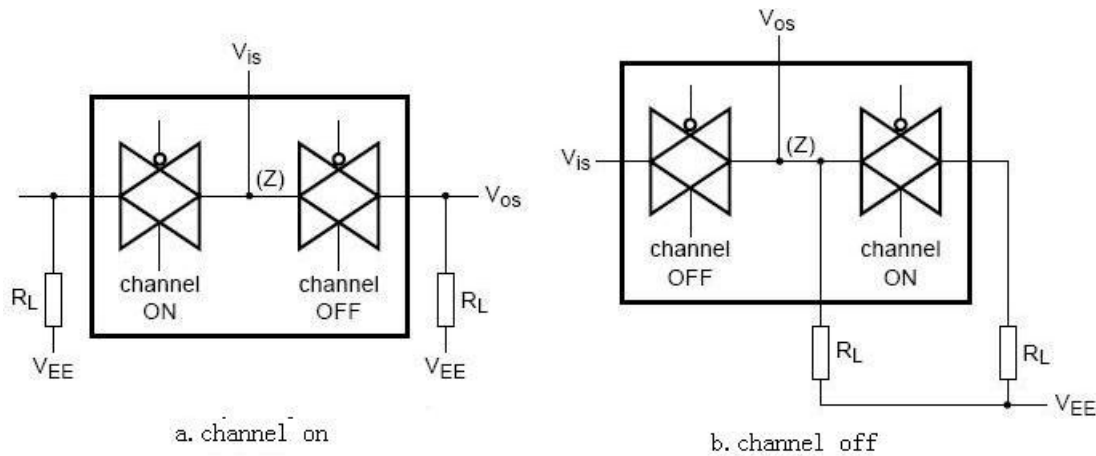


Fig. 12. Inter channel Crosstalk

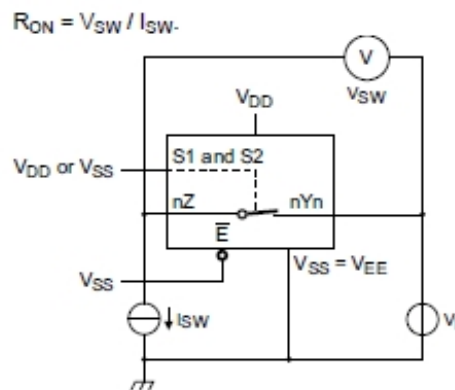


Fig. 13. Test circuit for measuring R_{ON}

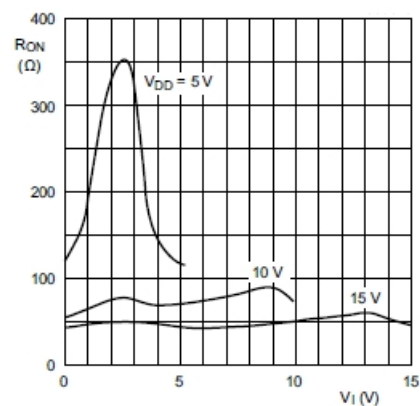


Fig. 14. Typical R_{ON} as a function of input voltage

Table 12. Measurement points

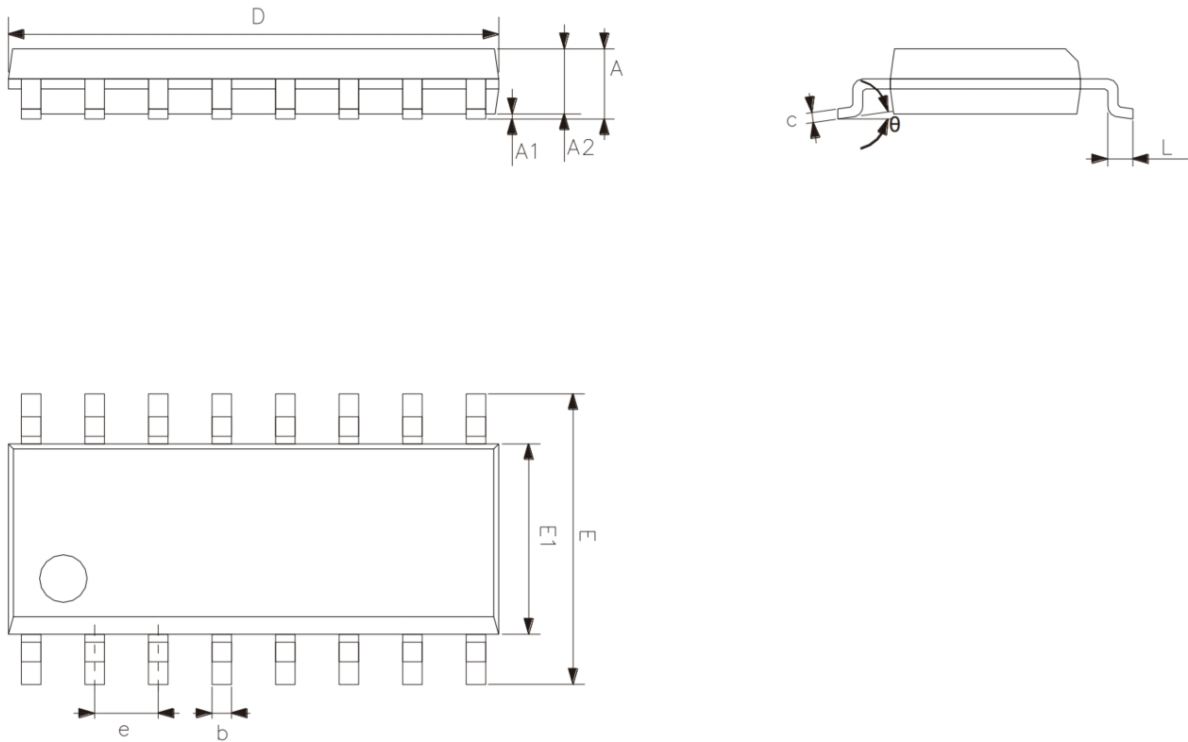
Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 9V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

Table 13. Test data

Test	Input		Load		Switch
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10k Ω	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10k Ω	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20ns	50pF	10k Ω	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20ns	50pF	10k Ω	V_{DD}
others	pulse	20ns	50pF	10k Ω	open

12. Package Outline

SOP-16



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

HEF4052

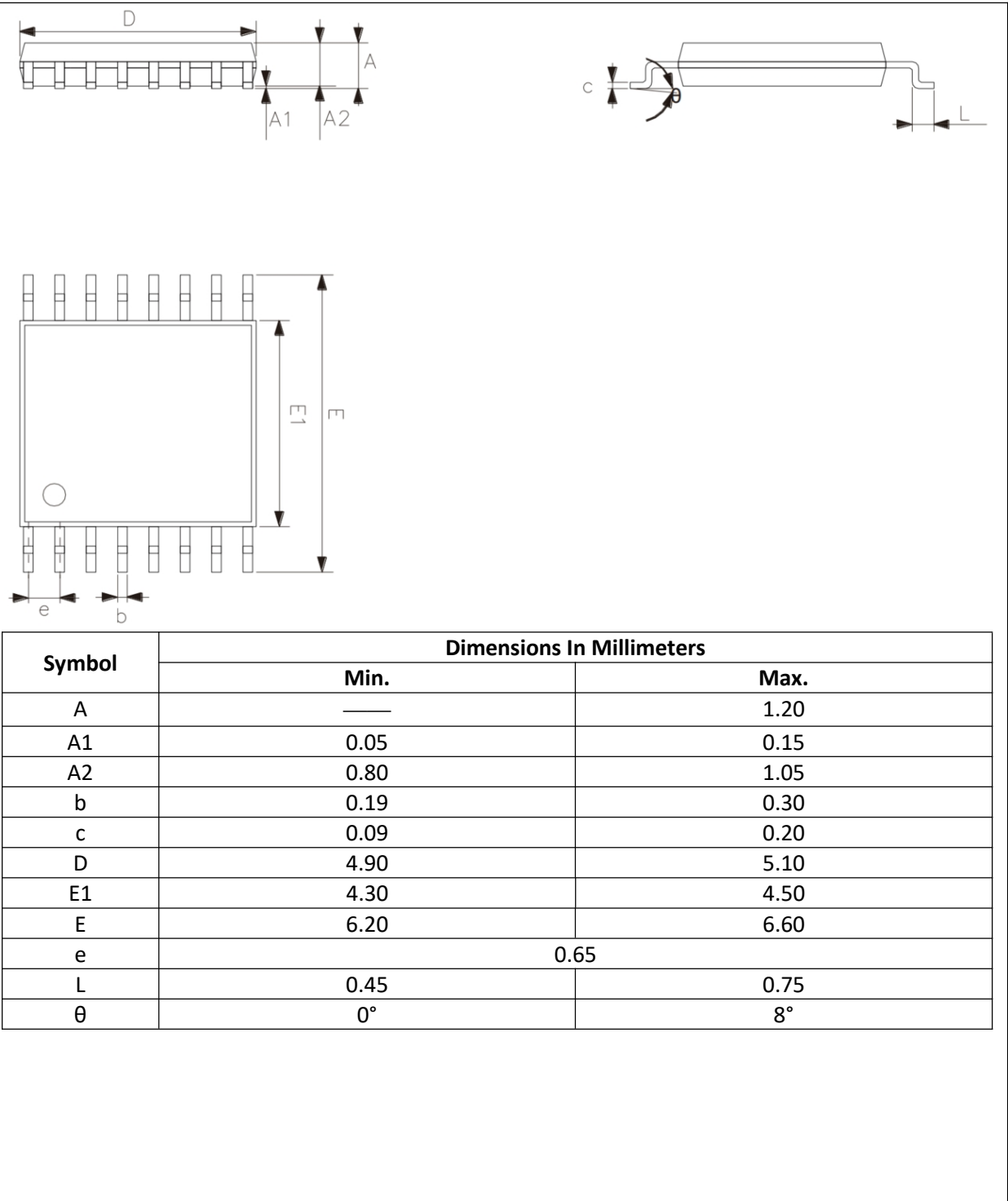


Dual 4-channel Analog Multiplexer/Demultiplexer

Product datasheet, Rev. 1.0

Aug 08, 2024

TSSOP-16



13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Document ID	Release Date	Data sheet status	Change notice	Supersedes
HEF4052 Rev. 1.0	Aug 08, 2024	Product datasheet		