

1. General Description

The 74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\bar{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period ($nQ=HIGH$, $n\bar{Q}=LOW$) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\bar{RD}$, which also inhibits the triggering.
3. An internal connection from nRD to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input nRD .

2. Features and Benefits

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Specified from $-40^{\circ}C$ to $+125^{\circ}C$
- Packaging information: SOP16/TSSOP16

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC123D	SOP-16	plastic small outline package; 16 leads; body width 3.9 mm	2500
74HCT123D			
74HC123PW	TSSOP-16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500
74HCT123PW			

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

4. Function Diagram

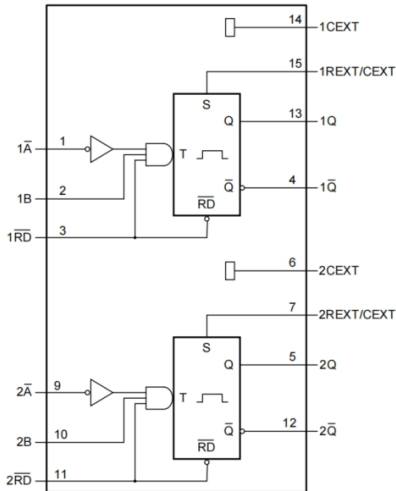


Fig. 1. Logic symbol

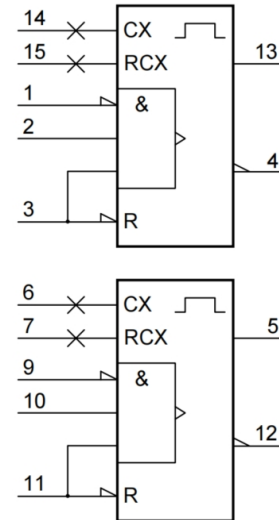


Fig. 2. IEC logic symbol

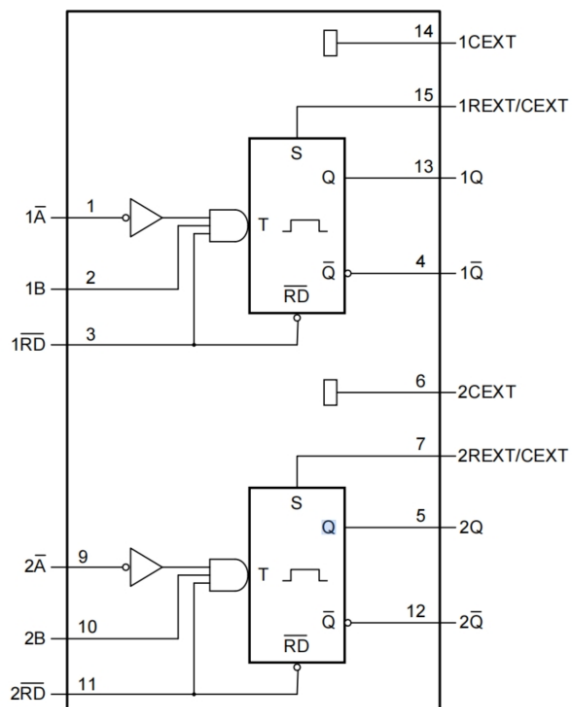
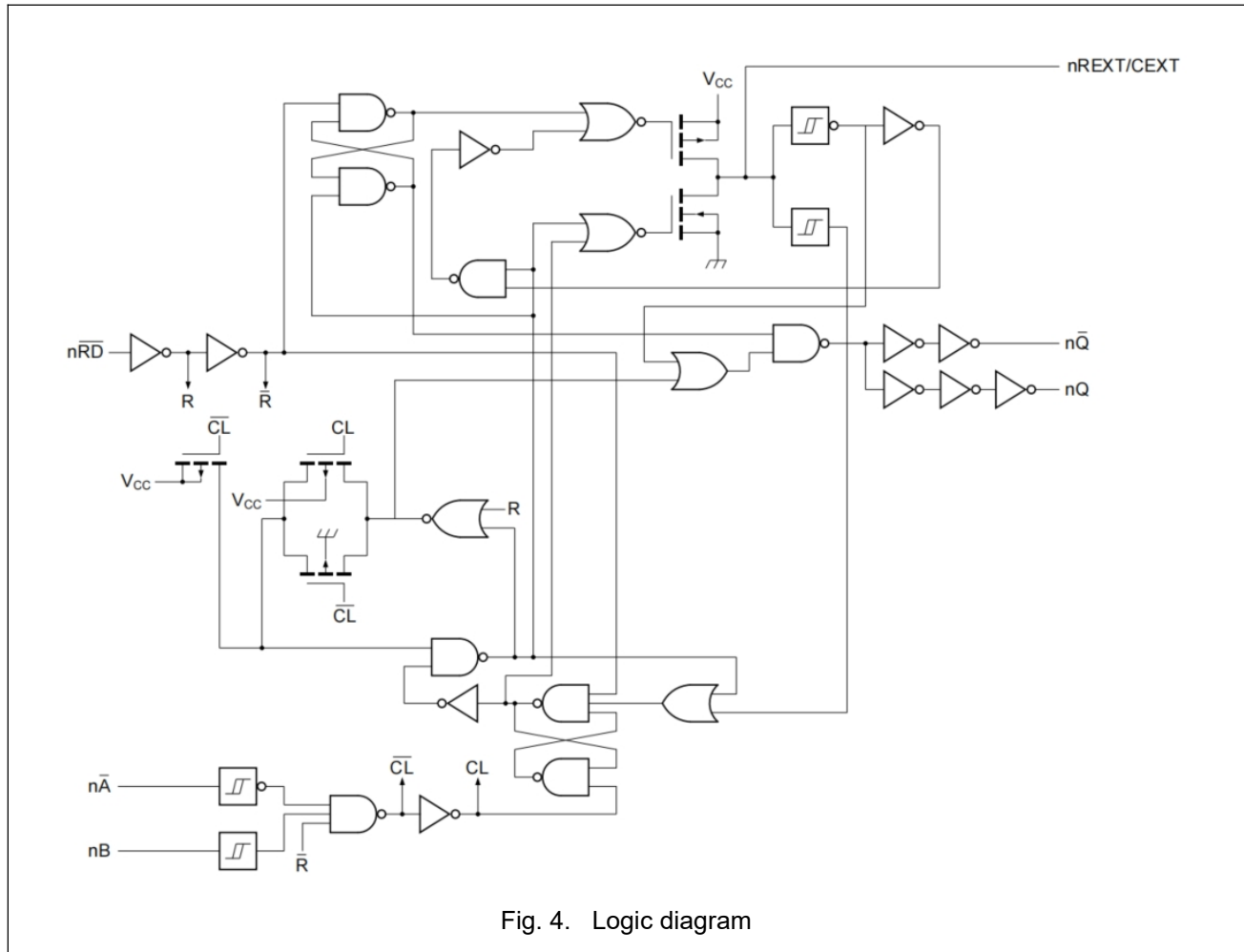


Fig. 3. Functional diagram

74HC123;74HCT123

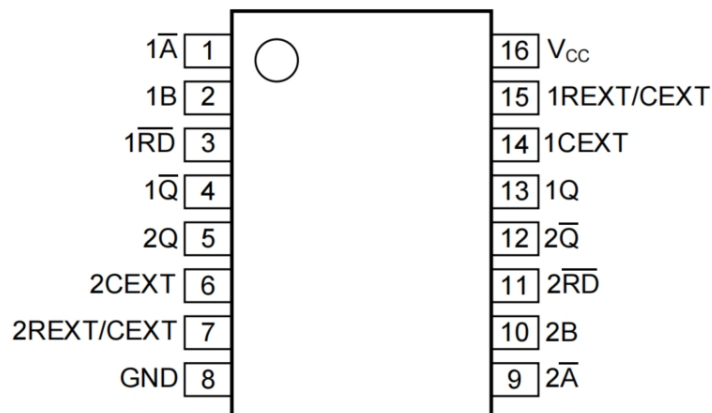
High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets



74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

5. Pinning Information



5.1. Pinning

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\bar{A}$	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
$1\overline{RD}$	3	direct reset LOW and positive-edge triggered input 1
$1\bar{Q}$	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0V)
$2\bar{A}$	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
$2\overline{RD}$	11	direct reset LOW and positive-edge triggered input 2
$2\bar{Q}$	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V_{CC}	16	supply voltage

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; $\uparrow$ = LOW-to-HIGH transition; $\downarrow$ = HIGH-to-LOW transition; X = don't care;  = one HIGH level output pulse;  = one LOW level output pulse;

Input			Output	
$\overline{nRD}$	$\overline{nA}$	nB	nQ	$\overline{nQ}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	$\uparrow$		
H	$\downarrow$	H		
$\uparrow$	L	H		

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$		± 20	mA
I_O	output current	except for pins nREXT/CEXT; $V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$		± 25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current			-50	mA
P_{tot}	total power dissipation			500	mW
T_{stg}	storage temperature		-65	150	$^{\circ}\text{C}$
T_L	soldering temperature	SOP/TSSOP	260		$^{\circ}\text{C}$

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC123			74HCT123			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0		V _{CC}	0		V _{CC}	V
V _O	output voltage		0		V _{CC}	0		V _{CC}	V
T _{amb}	ambient temperature		-40		+125	-40		+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$\overline{nRD}$ Input	V _{CC} = 2.0 V		625				ns/V
			V _{CC} = 4.5 V	1.67	139		1.67	139	ns/V
			V _{CC} = 6.0 V		83				ns/V

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

9. Electrical Characteristics

Table 6. DC Characteristics 1

Tamb=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HC123							
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V		1.5	1.2		V
		V _{CC} = 4.5 V		3.15	2.4		V
		V _{CC} = 6.0 V		4.2	3.2		V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V			0.8	0.5	V
		V _{CC} = 4.5 V			2.1	1.35	V
		V _{CC} = 6.0 V			2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	I _O = -20uA ; V _{CC} = 2.0V	1.9	2.0		V
			I _O = -20uA; V _{CC} = 4.5V	4.4	4.5		V
			I _O = -20uA; V _{CC} = 6.0V	5.9	6.0		V
			I _O = -4mA; V _{CC} = 4.5V	3.98	4.32		V
			I _O = -5.2mA; V _{CC} = 6.0V	5.48	5.81		V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O = 20uA ; V _{CC} = 2.0V		0	0.1	V
			I _O = 20uA ; V _{CC} = 4.5V		0	0.1	V
			I _O = 20uA ; V _{CC} = 6.0V		0	0.1	V
			I _O = 4mA; V _{CC} = 4.5V		0.15	0.26	V
			I _O = 5.2mA; V _{CC} = 6.0V		0.16	0.26	V
I _I	input leakage current	V _I = V _{CC} or GND ; V _{CC} = 6.0V				±1.0	uA
I _{CC}	supply current	V _I = V _{CC} or GND ; I _O = 0A ; V _{CC} = 6.0V				8.0	uA
C _I	Input capacitance				3.5		pF
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HCT123							
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5V to 5.5V		2.0	1.6		V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5V to 5.5V			1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} V _{CC} = 4.5V	I _O = -20uA	4.4	4.5		V
			I _O = -4mA	3.98	4.32		V

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$ $V_{CC} = 4.5V$	$I_O = 20\mu A$		0	0.1	V
			$I_O = 4mA$		0.15	0.26	V
ΔI_{CC}	additional supply current	per input pin ; $V_I = V_{CC} - 2.1V$; other inputs at V_{CC} or GND; $V_{CC} = 4.5V$ to $5.5V$; $I_O = 0A$	pins $n\overline{A}$, nB		35	125	μA
			pin $n\overline{RD}$		50	180	μA
I_I	input leakage current	$V_I = V_{CC}$ or GND ; $V_{CC} = 5.5V$				± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND ; $I_O = 0A$; $V_{CC} = 5.5V$				8.0	μA
C_I	Input capacitance				3.5		pF

Table 7. DC Characteristics 2

Tamb=-40°C to +85°C, voltages are referenced to GND (ground=0V) , unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HC123							
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V		1.5			V
		V _{CC} = 4.5 V		3.15			V
		V _{CC} = 6.0 V		4.2			V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V				0.5	V
		V _{CC} = 4.5 V				1.35	V
		V _{CC} = 6.0 V				1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	I _O = -20uA ; V _{CC} = 2.0V	1.9			V
			I _O = -20uA; V _{CC} = 4.5V	4.4			V
			I _O = -20uA; V _{CC} = 6.0V	5.9			V
			I _O = -4mA; V _{CC} = 4.5V	3.98			V
			I _O = -5.2mA; V _{CC} = 6.0V	5.48			V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O = 20uA ; V _{CC} = 2.0V		0	0.1	V
			I _O = 20uA ; V _{CC} = 4.5V		0	0.1	V
			I _O = 20uA ; V _{CC} = 6.0V		0	0.1	V
			I _O = 4mA; V _{CC} = 4.5V			0.33	V
			I _O = 5.2mA; V _{CC} = 6.0V			0.33	V

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

I_I	input leakage current	$V_I = V_{CC}$ or GND ; $V_{CC} = 6.0V$			± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND ; $I_O = 0A$; $V_{CC} = 6.0V$			8.0	μA
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HCT123						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5V$ to $5.5V$	2.0			V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5V$ to $5.5V$			0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} $V_{CC} = 4.5V$	$I_O = -20\mu A$	4.4		V
			$I_O = -4mA$	3.98		V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} $V_{CC} = 4.5V$	$I_O = 20\mu A$		0.1	V
			$I_O = 4mA$		0.33	V
ΔI_{CC}	additional supply current	per input pin ; $V_I = V_{CC} - 2.1V$; other inputs at V_{CC} or GND; $V_{CC} = 4.5V$ to $5.5V$; $I_O = 0A$	pins $n\overline{A}$, nB		160	μA
			pin $n\overline{RD}$		225	μA
I_I	input leakage current	$V_I = V_{CC}$ or GND ; $V_{CC} = 5.5V$			± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND ; $I_O = 0A$; $V_{CC} = 5.5V$			8.0	μA

Table 8. DC Characteristics 3

$T_{amb} = -40^\circ C$ to $+125^\circ C$, voltages are referenced to GND (ground=0V), unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC123						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0 V$	1.5			V
		$V_{CC} = 4.5 V$	3.15			V
		$V_{CC} = 6.0 V$	4.2			V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0 V$			0.5	V
		$V_{CC} = 4.5 V$			1.35	V
		$V_{CC} = 6.0 V$			1.8	V

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	I _O = -20uA ; V _{CC} = 2.0V	1.9			V
			I _O = -20uA; V _{CC} = 4.5V	4.4			V
			I _O = -20uA; V _{CC} = 6.0V	5.9			V
			I _O = -4mA; V _{CC} = 4.5V	3.7			V
			I _O = -5.2mA; V _{CC} = 6.0V	5.2			V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O = 20uA ; V _{CC} = 2.0V			0.1	V
			I _O = 20uA ; V _{CC} = 4.5V			0.1	V
			I _O = 20uA ; V _{CC} = 6.0V			0.1	V
			I _O = 4mA; V _{CC} = 4.5V			0.4	V
			I _O = 5.2mA; V _{CC} = 6.0V			0.4	V
I _I	input leakage current	V _I = V _{CC} or GND ; V _{CC} = 6.0V				±1.0	uA
I _{CC}	supply current	V _I = V _{CC} or GND ; I _O = 0A ; V _{CC} = 6.0V				160	uA
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HCT123							
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5V to 5.5V		2.0			V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5V to 5.5V				0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} V _{CC} = 4.5V	I _O = -20uA	4.4			V
			I _O = -4mA	3.7			V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} V _{CC} = 4.5V	I _O = 20uA			0.1	V
			I _O = 4mA			0.4	V
ΔI _{CC}	additional supply current	per input pin ; V _I = V _{CC} - 2.1V; other inputs at V _{CC} or GND; V _{CC} = 4.5V to 5.5V ; I _O = 0A	pins n $\overline{A}$, nB			170	uA
			pin n $\overline{RD}$			245	uA
I _I	input leakage current	V _I = V _{CC} or GND ; V _{CC} = 5.5V				±1.0	uA
I _{CC}	supply current	V _I = V _{CC} or GND ; I _O = 0A ; V _{CC} = 5.5V				160	uA

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

Table 9. AC Characteristics 1

Tamb=25°C, voltages are referenced to GND (ground=0V); CL=50pF, unless otherwise specified.

	Parameter	Conditions	Min	Typ	Max	Unit
74HC123						
t_{pd}	propagation delay	$\overline{nRD}, \overline{nA}, nB$ to nQ or $\overline{nQ}$; $C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$; see Figure 6 ^[1]	$V_{CC} = 2.0V$	83	255	ns
			$V_{CC} = 4.5V$	30	51	ns
			$V_{CC} = 5.0V$; $C_L = 15pF$	26		ns
			$V_{CC} = 6.0V$	24	43	ns
		$\overline{nRD}(\text{reset})$ to nQ or $\overline{nQ}$; $C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$; see Figure 6	$V_{CC} = 2.0V$	66	215	ns
			$V_{CC} = 4.5V$	25	43	ns
			$V_{CC} = 5.0V$; $C_L = 15pF$	20		ns
			$V_{CC} = 6.0V$	19	37	ns
t_t	transition time	see Figure 6 ^[1]	$V_{CC} = 2.0V$	19	75	ns
			$V_{CC} = 4.5V$	7	15	ns
			$V_{CC} = 6.0V$	6	13	ns
t_w	pulse width	$\overline{nA}$ LOW; see Figure 7	$V_{CC} = 2.0V$	100	8	ns
			$V_{CC} = 4.5V$	20	3	ns
			$V_{CC} = 6.0V$	17	2	ns
		nB HIGH; see Figure 7	$V_{CC} = 2.0V$	100	17	ns
			$V_{CC} = 4.5V$	20	6	ns
			$V_{CC} = 6.0V$	17	5	ns
		$\overline{nRD}$ LOW; see Figure 8	$V_{CC} = 2.0V$	100	14	ns
			$V_{CC} = 4.5V$	20	5	ns
			$V_{CC} = 6.0V$	17	4	ns
		nQ HIGH and $\overline{nQ}$ LOW; $V_{CC}=5.0V$; see Figure 7, 8 ^[2]	$C_{EXT} = 100nF$; $R_{EXT} = 10k\Omega$	450		us
			$C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$	75		ns
t_{rtrig}	retrigger time	$\overline{nA}$, nB ; $C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$; $V_{CC} = 5.0V$; see Figure 7 ^{[3][4]}		110		ns
R_{EXT}	external timing resistor	see Figure 7	$V_{CC} = 2.0V$	10	1000	k Ω
			$V_{CC} = 5.0V$	2	1000	k Ω
C_{EXT}	external timing capacitor	$V_{CC} = 5.0V$; see Figure 9 ^[4]				pF

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

C_{PD}	power dissipation capacitance	per monostable ; $V_I = \text{GND to } V_{CC}^{[5]}$		54		pF
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HCT123						
t_{PHL}	HIGH to LOW propagation delay	$n\overline{RD}, n\overline{A}, nB$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6	$V_{CC} = 4.5\text{V}$	30	51	ns
			$V_{CC} = 5.0\text{V} ; C_L = 15\text{pF}$	26		ns
		$n\overline{RD}(\text{reset})$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6	$V_{CC} = 4.5\text{V}$	27	46	ns
			$V_{CC} = 5.0\text{V} ; C_L = 15\text{pF}$	23		ns
t_{PLH}	LOW to HIGH propagation delay	$n\overline{RD}, n\overline{A}, nB$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6	$V_{CC} = 4.5\text{V}$	28	51	ns
			$V_{CC} = 5.0\text{V} ; C_L = 15\text{pF}$	26		ns
		$n\overline{RD}(\text{reset})$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6	$V_{CC} = 4.5\text{V}$	23	46	ns
			$V_{CC} = 5.0\text{V} ; C_L = 15\text{pF}$	23		ns
t_t	transition time	$V_{CC} = 4.5\text{V}$; see Figure 6 ^[1]		7	15	ns
t_w	pulse width	$V_{CC} = 4.5\text{V}$	$n\overline{A}$ LOW; see Figure 7	20	3	ns
			nB HIGH; see Figure 7	20	5	ns
			$n\overline{RD}$ LOW; see Figure 8	20	7	ns
		nQ HIGH and $n\overline{Q}$ LOW; $V_{CC}=5.0\text{V}$; see Figure 7, 8 ^[2]	$C_{EXT} = 100\text{nF}$; $R_{EXT} = 10\text{k}\Omega$		450	us
			$C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$		75	ns
t_{rtrig}	retrigger time	$n\overline{A}$, nB ; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; $V_{CC} = 5.0\text{V}$; see Figure 7 ^{[3][4]}		110		ns
R_{EXT}	external timing resistor	$V_{CC} = 5.0\text{V}$; see Figure 9	2		1000	k Ω
C_{EXT}	external timing capacitor	$V_{CC} = 5.0\text{V}$; see Figure 9 ^[4]				pF
C_{PD}	power dissipation capacitance	per monostable ; $V_I = \text{GND to } V_{CC} - 1.5\text{V}^{[5]}$		56		pF

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_t is the same as t_{THL} and t_{TLH} .
- [2] For other R_{EXT} and C_{EXT} combinations see Figure 9. If $C_{EXT} > 10nF$, the next formula is valid.
 $t_W = K \times R_{EXT} \times C_{EXT}$, where:
 t_W = typical output pulse width in ns;
 R_{EXT} = external resistor in $k\Omega$; C_{EXT} = external capacitor in pF;
 K = constant = 0.45 for $V_{CC} = 5.0V$ and 0.55 for $V_{CC} = 2.0V$.
The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7pF.
- [3] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT} . The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If $C_{EXT} > 10pF$, the next formula (at $V_{CC}=5.0V$) for the setup time of a retrigger pulse is valid:
 $T_{rtrig} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:
 T_{rtrig} = retrigger time in ns;
 C_{EXT} = external capacitor in pF; R_{EXT} = external resistor in $k\Omega$.
The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is 7pF.
- [4] When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50pF$.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 10. AC Characteristics 2

$T_{amb} = -40^\circ C$ to $+85^\circ C$, GND = 0V; $C_L = 50pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC123						
t_{pd}	propagation delay	$n\overline{RD}, n\overline{A}, nB$ to nQ or $n\overline{Q}$; $C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$; see Figure 6 ^[1]	$V_{CC} = 2.0V$		320	ns
			$V_{CC} = 4.5V$		64	ns
			$V_{CC} = 6.0V$		54	ns
		$n\overline{RD}(\text{reset})$ to nQ or $n\overline{Q}$; $C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$; see Figure 6	$V_{CC} = 2.0V$		270	ns
			$V_{CC} = 4.5V$		54	ns
			$V_{CC} = 6.0V$		46	ns
t_t	transition time	see Figure 6 ^[1]	$V_{CC} = 2.0V$		95	ns
			$V_{CC} = 4.5V$		19	ns
			$V_{CC} = 6.0V$		16	ns

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

t _w	pulse width	n $\overline{A}$ LOW; see Figure 7	V _{CC} = 2.0V	125			ns
			V _{CC} = 4.5V	25			ns
			V _{CC} = 6.0V	21			ns
		nB HIGH; see Figure 7	V _{CC} = 2.0V	125			ns
			V _{CC} = 4.5V	25			ns
			V _{CC} = 6.0V	21			ns
		n $\overline{RD}$ LOW; see Figure 8	V _{CC} = 2.0V	125			ns
			V _{CC} = 4.5V	25			ns
			V _{CC} = 6.0V	21			ns
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HCT123							
t _{PHL}	HIGH to LOW propagation delay	n $\overline{RD}$, n $\overline{A}$, nB to nQ or n $\overline{Q}$; C _{EXT} = 0pF; R _{EXT} = 5k Ω ; see Figure 6	V _{CC} = 4.5V			64	ns
		n $\overline{RD}$ (reset) to nQ or n $\overline{Q}$; C _{EXT} = 0pF; R _{EXT} = 5k Ω ; see Figure 6	V _{CC} = 4.5V			58	ns
t _{PLH}	LOW to HIGH propagation delay	n $\overline{RD}$, n $\overline{A}$, nB to nQ or n $\overline{Q}$; C _{EXT} = 0pF; R _{EXT} = 5k Ω ; see Figure 6	V _{CC} = 4.5V			64	ns
		n $\overline{RD}$ (reset) to nQ or n $\overline{Q}$; C _{EXT} = 0pF; R _{EXT} = 5k Ω ; see Figure 6	V _{CC} = 4.5V			58	ns
t _t	transition time	V _{CC} = 4.5V ; see Figure 6 ^[1]				19	ns
t _w	pulse width	V _{CC} = 4.5V	n $\overline{A}$ LOW; see Figure 7	25			ns
			nB HIGH; see Figure 7	25			ns
			n $\overline{RD}$ LOW; see Figure 8	25			ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_t is the same as t_{THL} and t_{TLH} .

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

Table 11. AC Characteristics 3

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, GND = 0V ; $C_L = 50\text{pF}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC123						
t_{pd}	propagation delay	$\overline{nRD}, \overline{nA}, nB$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6 ^[1]	$V_{CC} = 2.0\text{V}$		385	ns
			$V_{CC} = 4.5\text{V}$		77	ns
			$V_{CC} = 6.0\text{V}$		65	ns
		$\overline{nRD}(\text{reset})$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6	$V_{CC} = 2.0\text{V}$		325	ns
			$V_{CC} = 4.5\text{V}$		65	ns
			$V_{CC} = 6.0\text{V}$		55	ns
t_t	transition time	see Figure 6 ^[1]	$V_{CC} = 2.0\text{V}$		110	ns
			$V_{CC} = 4.5\text{V}$		22	ns
			$V_{CC} = 6.0\text{V}$		19	ns
t_w	pulse width	$\overline{nA}$ LOW; see Figure 7	$V_{CC} = 2.0\text{V}$	150		ns
			$V_{CC} = 4.5\text{V}$	30		ns
			$V_{CC} = 6.0\text{V}$	26		ns
		nB HIGH; see Figure 7	$V_{CC} = 2.0\text{V}$	150		ns
			$V_{CC} = 4.5\text{V}$	30		ns
			$V_{CC} = 6.0\text{V}$	26		ns
		$\overline{nRD}$ LOW; see Figure 8	$V_{CC} = 2.0\text{V}$	150		ns
			$V_{CC} = 4.5\text{V}$	30		ns
			$V_{CC} = 6.0\text{V}$	26		ns
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HCT123						
t_{PHL}	HIGH to LOW propagation delay	$\overline{nRD}, \overline{nA}, nB$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6	$V_{CC} = 4.5\text{V}$		77	ns
		$\overline{nRD}(\text{reset})$ to nQ or $n\overline{Q}$; $C_{EXT} = 0\text{pF}$; $R_{EXT} = 5\text{k}\Omega$; see Figure 6	$V_{CC} = 4.5\text{V}$		69	ns

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

t_{PLH}	LOW to HIGH propagation delay	$\overline{nRD}, \overline{nA}, nB$ to nQ or $\overline{nQ}$; $C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$; see Figure 6	$V_{CC} = 4.5V$			77	ns
		$\overline{nRD}(\text{reset})$ to nQ or $\overline{nQ}$; $C_{EXT} = 0pF$; $R_{EXT} = 5k\Omega$; see Figure 6	$V_{CC} = 4.5V$			69	ns
t_t	transition time	$V_{CC} = 4.5V$; see Figure 6 ^[1]				22	ns
t_w	pulse width	$V_{CC} = 4.5V$	$\overline{nA}$ LOW; see Figure 7	30			ns
			nB HIGH; see Figure 7	30			ns
			$\overline{nRD}$ LOW; see Figure 8	30			ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_t is the same as t_{THL} and t_{TLH} .

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

9.1. Waveforms and test circuit

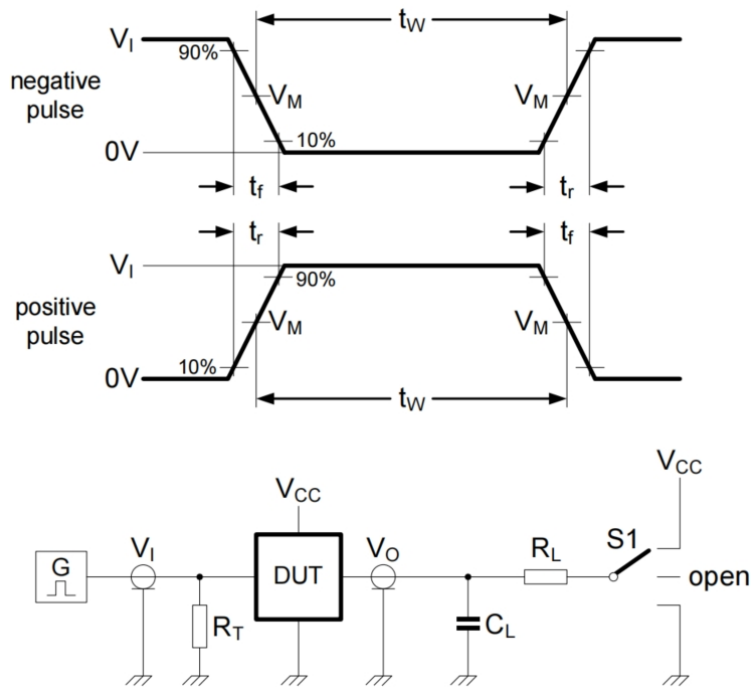


Fig. 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

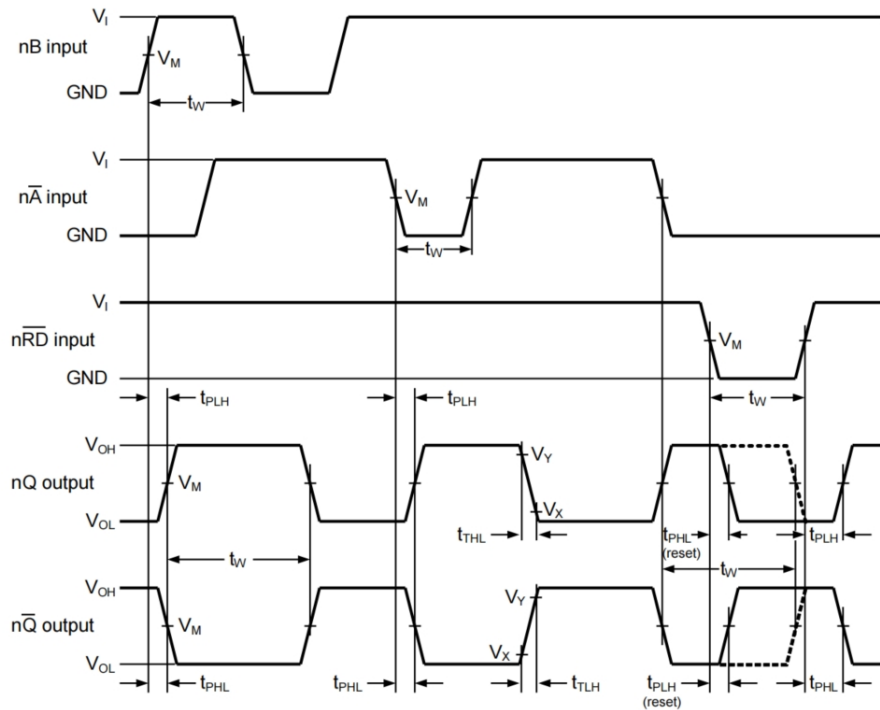


Fig. 6. Propagation delays from inputs ($n\bar{A}$, nB , $n\bar{RD}$) to outputs (nQ , $n\bar{Q}$ and output transition times)

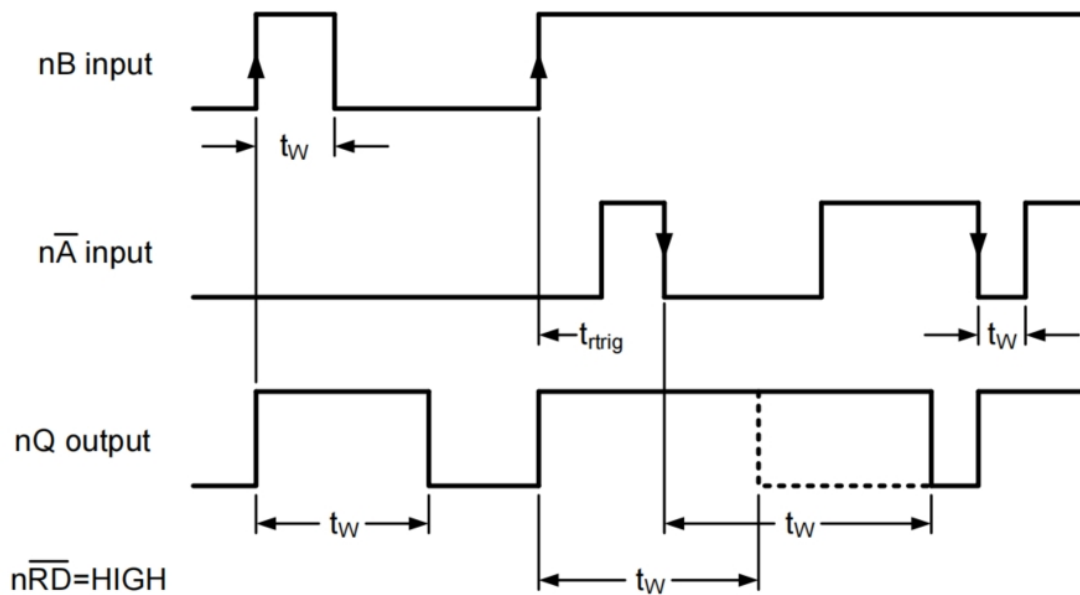


Fig. 7. Output pulse control using retrigger pulse

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

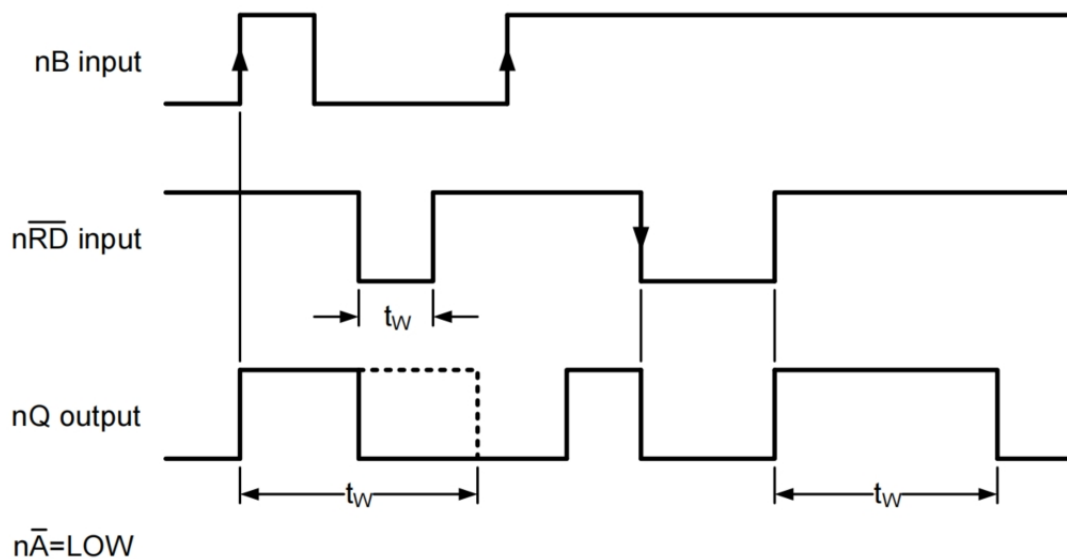


Fig. 8. Output pulse control using reset input $\overline{nRD}$

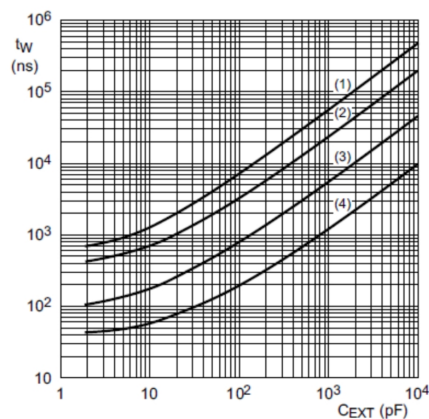


Fig. 9. Typical output pulse width as a function of the external capacitor value

$V_{CC} = 5.0V$; $T_{amb} = 25^\circ C$.

- (1) $R_{EXT} = 100k\Omega$
- (2) $R_{EXT} = 50k\Omega$
- (3) $R_{EXT} = 10k\Omega$
- (4) $R_{EXT} = 2k\Omega$

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

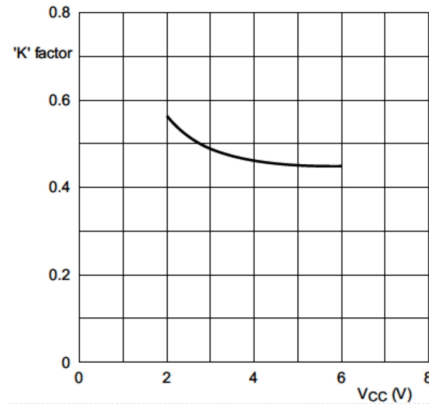


Fig. 10. AiP74HC123 typical 'K' factor as function of V_{CC}

C_{EXT} = 10nF ; R_{EXT} = 10kΩ to 100kΩ. T_{amb} = 25°C.

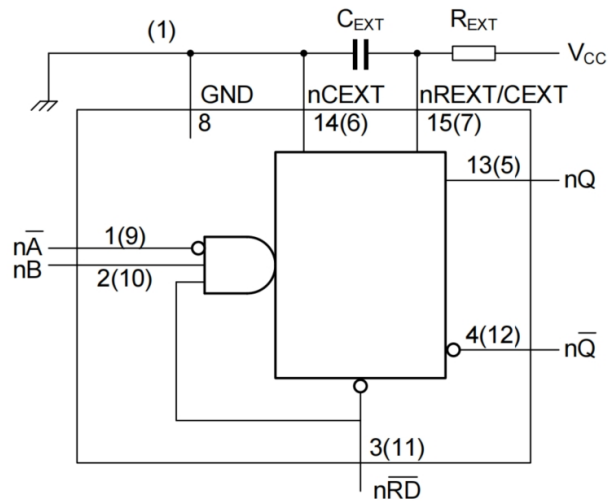


Fig. 11. Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.

For minimum noise generation it is recommended to ground pins 6 (2C_{EXT}) and 14 (1C_{EXT}) externally to pin 8 (GND)

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

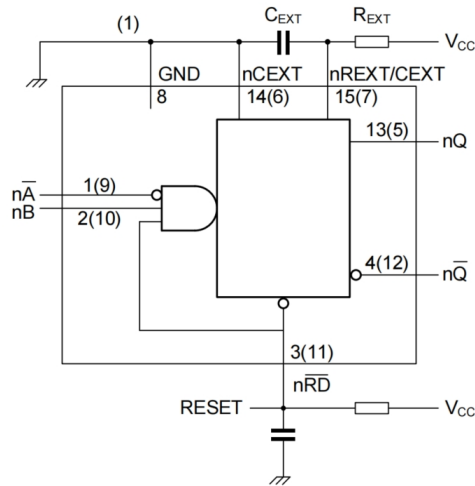


Fig. 12. Power-up output pulse elimination circuit

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT} . This output pulse can be eliminated using the circuit shown in Figure 12.

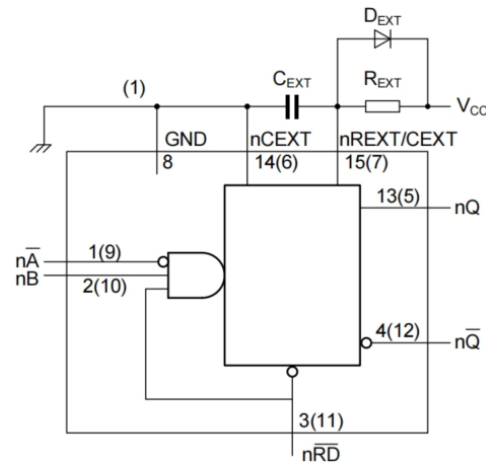


Fig. 13. Power-down protection circuit

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 13.

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

Table 12. Measurement points

Type	Input	Output
	V_M	V_M
74HC123	$0.5V_{CC}$	$0.5V_{CC}$
74HCT123	1.3 V	1.3 V

Table 13. Test data

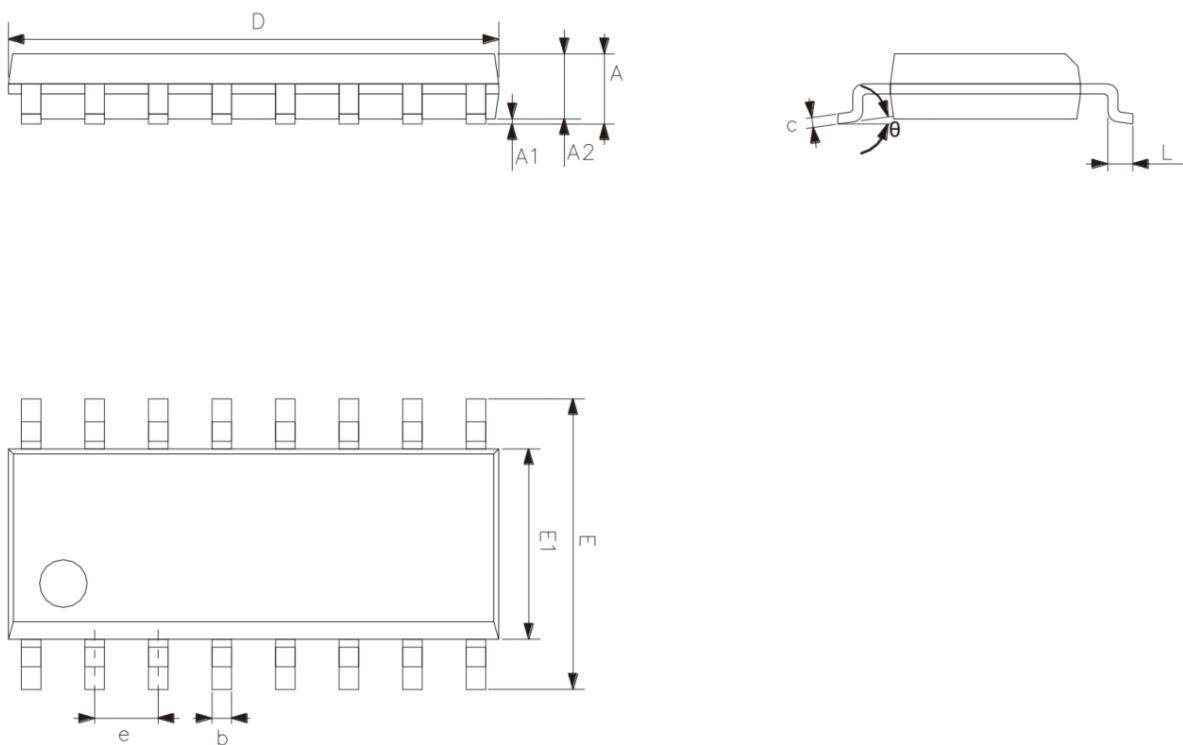
Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC123	V_{CC}	6 ns	15 pF, 50 pF	1k Ω	Open
74HCT123	3 V	6 ns	15pF, 50 pF	1k Ω	Open

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

10. Package Outline

SOP-16

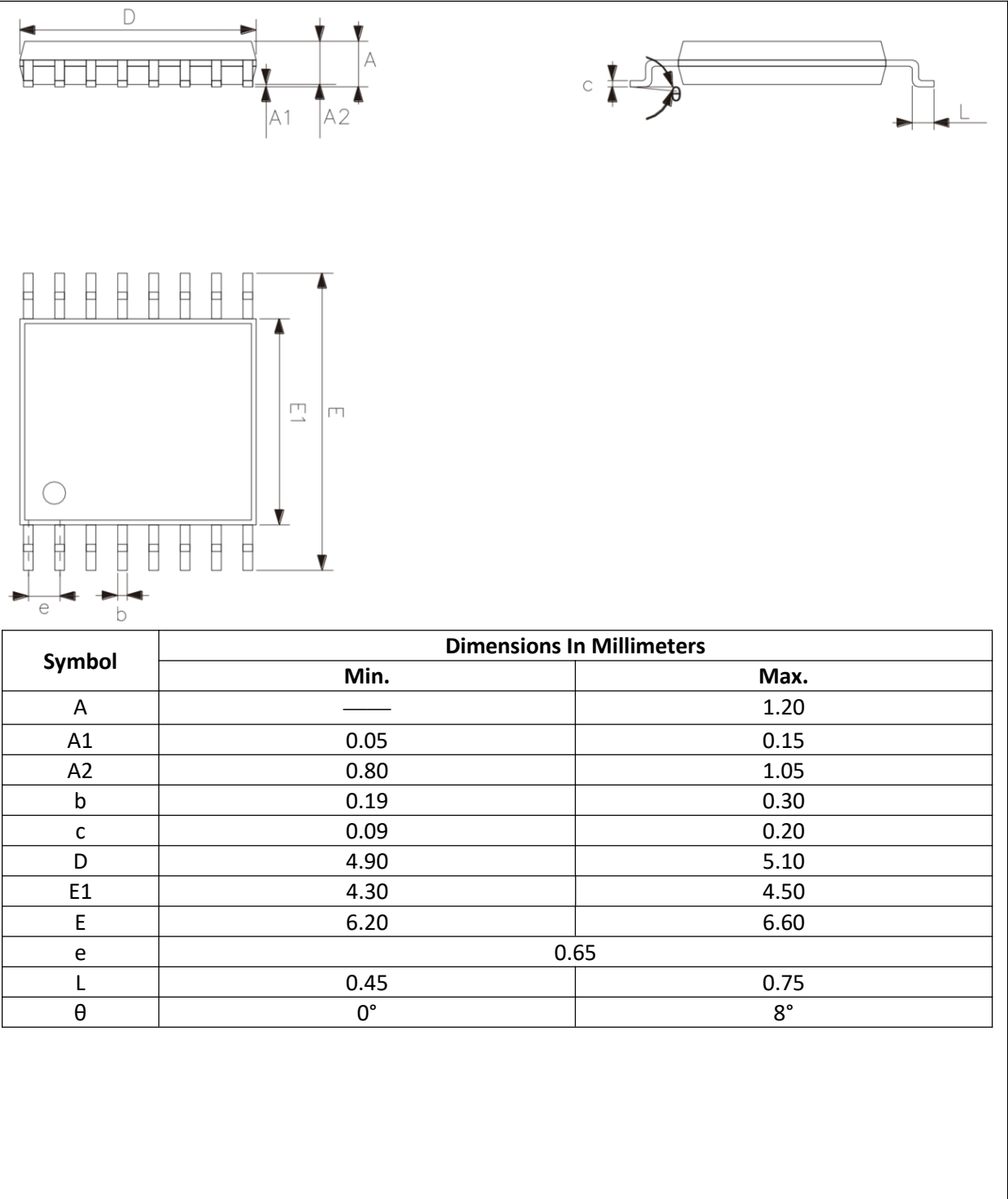


Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

74HC123;74HCT123

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

TSSOP-16



74HC123;74HCT123**High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets**

11. Abbreviations

Table 14. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

12. Revision History

Table 15. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT123 Rev. 1.0	Aug 08, 2024	Product datasheet		