

1. General Description

The HEF4094 is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs QP0 to QP7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (OE) signal is HIGH. Two serial outputs (QS1 and QS2) are available for cascading a number of HEF4094 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading HEF4094 devices when the clock has a slow rise time. It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and Benefits

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: SOP16 / TSSOP16

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
HEF4094BT	SOP-16	plastic small outline package; 16 leads; body width 3.9 mm	2500
HEF4094BTT	TSSOP-16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500

4. Function Diagram

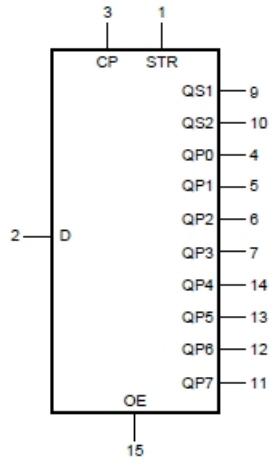


Fig. 1. Logic symbol

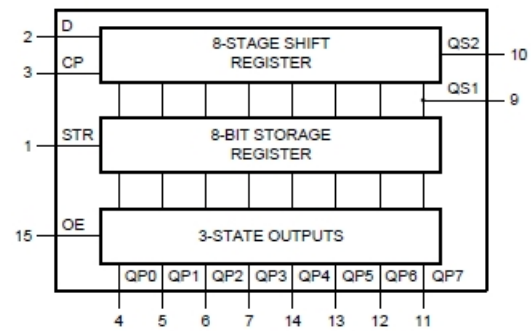


Fig. 2. Functional diagram

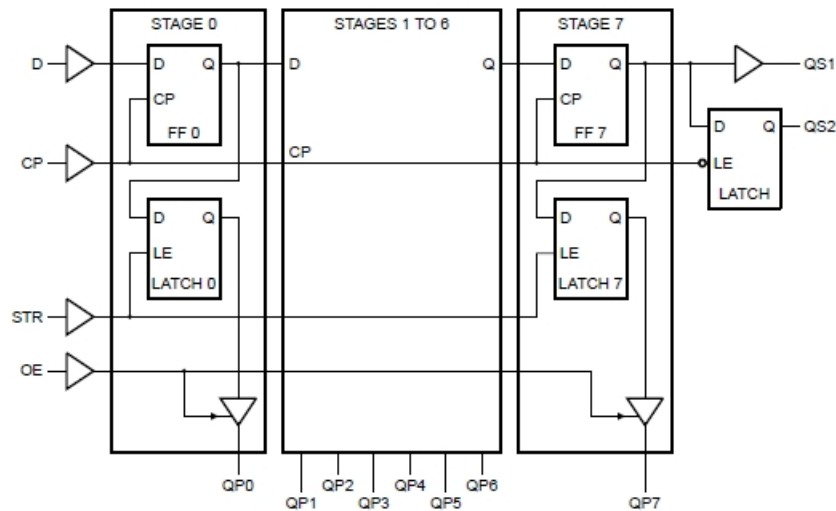


Fig. 3. Functional diagram

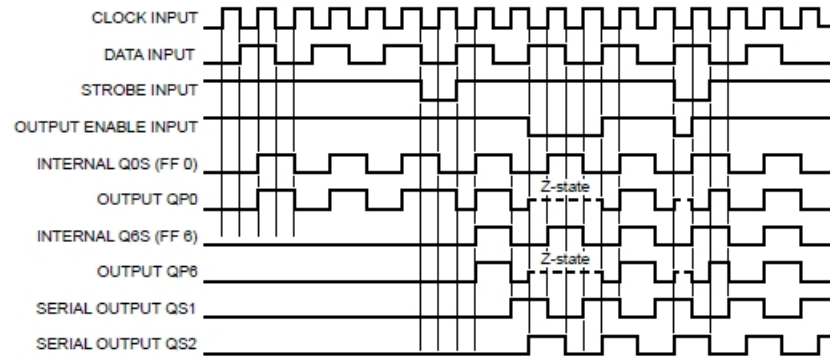
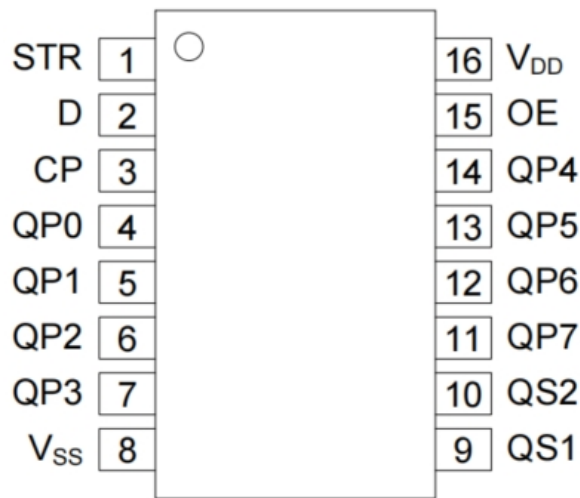


Fig. 4. Timing diagram

5. Pinning Information

Pinning



Pin description

Table 2. Pin description

Symbol	Pin	Description
STR	1	strobe input
D	2	data input
CP	3	clock input
QP0	4	parallel output
QP1	5	parallel output
QP2	6	parallel output
QP3	7	parallel output
V _{SS}	8	ground (0V)
QS1	9	serial output
QS2	10	serial output
QP7	11	parallel output
QP6	12	parallel output
QP5	13	parallel output
QP4	14	parallel output
OE	15	output enable input
V _{DD}	16	supply voltage

6. Functional Description

Function table

Table 3. Function table

Input				Output			
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn-1	Q6S	NC
↑	H	H	H	H	QPn-1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=HIGH-impedance OFF-state;

[2] NC=no change; ↑=positive-going transition; ↓=negative-going transition;

[3] Q6S=the data in register stage 6 before the LOW to HIGH clock transition;

[4] Q7S=the data in register stage 7 before the HIGH to LOW clock transition.

7. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{DD}	supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	any one input		-	±10	mA
V_I	input voltage	all inputs		-0.5	$V_{DD}+0.5$	V
T_{stg}	storage temperature	-		-65	+150	°C
P_{tot}	total power dissipation	-		-	500	mW
P	device dissipation	per output transistor		-	100	mW
T_L	soldering temperature	10s	SOP/TSSOP	260		°C

8. Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	supply voltage	-	3	-	15	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
t _{su}	data setup time	V _{DD} =5V	125	-	-	ns
		V _{DD} =10V	55	-	-	ns
		V _{DD} =15V	35	-	-	ns
t _w	clock pulse width	V _{DD} =5V	200	-	-	ns
		V _{DD} =10V	100	-	-	ns
		V _{DD} =15V	83	-	-	ns
f _{max}	clock input frequency	V _{DD} =5V	dc	-	1.25	MHz
		V _{DD} =10V		-	2.5	MHz
		V _{DD} =15V		-	3	MHz
t _{rCL} , t _{fCL}	clock rise and fall time	V _{DD} =5V	-	-	15	us
		V _{DD} =10V	-	-	5	us
		V _{DD} =15V	-	-	5	us
t _w	strobe setup time	V _{DD} =5V	200	-	-	ns
		V _{DD} =10V	80	-	-	ns
		V _{DD} =15V	70	-	-	ns

9. Static Characteristics

Table 8. DC Characteristics 1

T_{amb} = 25 °C, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)			T _{amb} =25 °C			Unit
		V _O	V _{IN}	V _{DD}	Min.	Typ.	Max.	
I _{DD}	supply current	-	0, 5	5	-	-	5	uA
		-	0, 10	10	-	-	10	uA
		-	0, 15	15	-	-	20	uA
I _{OL}	LOW-level output current	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA

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I_{OH}	HIGH-level output current	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
V_{OL}	LOW-level output voltage	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
V_{OH}	HIGH-level output voltage	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
V_{IL}	LOW-level input voltage	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
V_{IH}	HIGH-level input voltage	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
I_I	input leakage current	-	0, 15	15	-	-	± 1	μA
I_{OZ}	OFF-state output current	0, 15	0, 15	15	-	-	± 1	μA

Table 9. DC Characteristics 2

 $T_{amb} = -40^\circ C$ to $+85^\circ C$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)			$T_{amb} = -40^\circ C$		$T_{amb} = +85^\circ C$		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	
I_{DD}	supply current	-	0, 5	5	-	5	-	150	μA
		-	0, 10	10	-	10	-	300	μA
		-	0, 15	15	-	20	-	600	μA
I_{OL}	LOW-level output current	0.4	0, 5	5	0.61	-	0.42	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	mA
		1.5	0, 15	15	4	-	2.8	-	mA
I_{OH}	HIGH-level output current	4.6	0, 5	5	-0.61	-	-0.42	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	mA

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V_{OL}	LOW-level output voltage	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
I_I	input leakage current	-	0, 15	15	-	± 1	-	± 1	μA
I_{OZ}	OFF-state output current	0, 15	0, 15	15	-	± 1	-	± 12	μA

Table 10. DC Characteristics 3

 $T_{amb} = -40^\circ C$ to $+125^\circ C$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)			$T_{amb} = -40^\circ C$		$T_{amb} = +125^\circ C$		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	
I_{DD}	supply current	-	0, 5	5	-	5	-	150	μA
		-	0, 10	10	-	10	-	300	μA
		-	0, 15	15	-	20	-	600	μA
I_{OL}	LOW-level output current	0.4	0, 5	5	0.61	-	0.36	-	mA
		0.5	0, 10	10	1.5	-	0.9	-	mA
		1.5	0, 15	15	4	-	2.4	-	mA
I_{OH}	HIGH-level output current	4.6	0, 5	5	-0.61	-	-0.36	-	mA
		2.5	0, 5	5	-1.8	-	-1.15	-	mA
		9.5	0, 10	10	-1.5	-	-0.9	-	mA
		13.5	0, 15	15	-4	-	-2.4	-	mA
V_{OL}	LOW-level output voltage	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V

V_{OH}	HIGH-level output voltage	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
I_I	input leakage current	-	0, 15	15	-	± 1	-	± 1	μA
I_{OZ}	OFF-state output current	0, 15	0, 15	15	-	± 1	-	± 12	μA

10. Dynamic Characteristics

Table 11. AC Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$, $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PHL}, t_{PLH}	propagation delay time	CP to QS1; see Figure 6	$V_{DD}=5V$	-	300	600 ns
			$V_{DD}=10V$	-	125	250 ns
			$V_{DD}=15V$	-	95	190 ns
		CP to QS2; see Figure 6	$V_{DD}=5V$	-	230	460 ns
			$V_{DD}=10V$	-	110	220 ns
			$V_{DD}=15V$	-	75	150 ns
		CP to QPn; see Figure 6	$V_{DD}=5V$	-	420	840 ns
			$V_{DD}=10V$	-	195	390 ns
			$V_{DD}=15V$	-	135	270 ns
		STR to QPn; see Figure 7	$V_{DD}=5V$	-	290	580 ns
			$V_{DD}=10V$	-	145	290 ns
			$V_{DD}=15V$	-	100	200 ns
t_{PHZ}, t_{PZH}	HIGH to OFF-state/OFF-state to HIGH propagation delay	OE to QPn; see Figure 8	$V_{DD}=5V$	-	140	280 ns
			$V_{DD}=10V$	-	60	120 ns
			$V_{DD}=15V$	-	45	90 ns

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t_{PLZ}, t_{PZL}	LOW to OFF-state/OFF-state to LOW propagation delay	OE to QPn; see Figure 8	$V_{DD}=5V$	-	100	200	ns
			$V_{DD}=10V$	-	50	100	ns
			$V_{DD}=15V$	-	40	80	ns
t_w	pulse width	minimum HIGH strobe pulse; see Figure 7	$V_{DD}=5V$	-	100	200	ns
			$V_{DD}=10V$	-	40	80	ns
			$V_{DD}=15V$	-	35	70	ns
		minimum LOW clock pulse; see Figure 6	$V_{DD}=5V$	-	100	200	ns
			$V_{DD}=10V$	-	50	100	ns
			$V_{DD}=15V$	-	40	83	ns
t_{su}	data setup time	D to CP; see Figure 9	$V_{DD}=5V$	-	60	125	ns
			$V_{DD}=10V$	-	30	55	ns
			$V_{DD}=15V$	-	20	35	ns
t_t	transition time	-	$V_{DD}=5V$	-	100	200	ns
			$V_{DD}=10V$	-	50	100	ns
			$V_{DD}=15V$	-	40	80	ns
t_{rCL}, t_{fCL}	clock input rise and fall time	-	$V_{DD}=5V$	15	-	-	us
			$V_{DD}=10V$	5	-	-	us
			$V_{DD}=15V$	5	-	-	us
f_{max}	maximum clock frequency	see Figure 6	$V_{DD}=5V$	1.25	2.5	-	MHz
			$V_{DD}=10V$	2.5	5	-	MHz
			$V_{DD}=15V$	3	6	-	MHz
C_i	input capacitance	any input		-	5	7.5	pF

11. Waveforms and test circuit

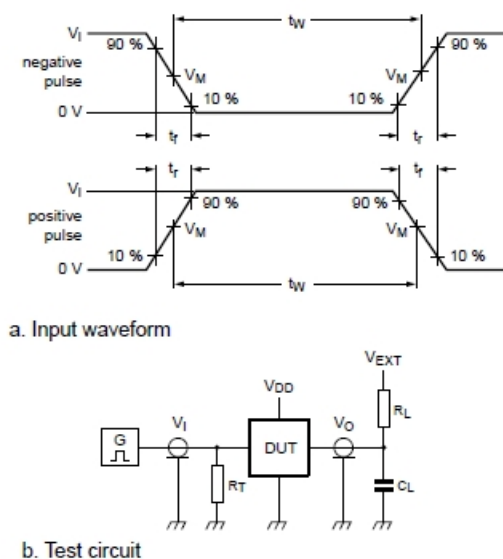


Fig. 5. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

V_{EXT} =External voltage for measuring switching times.

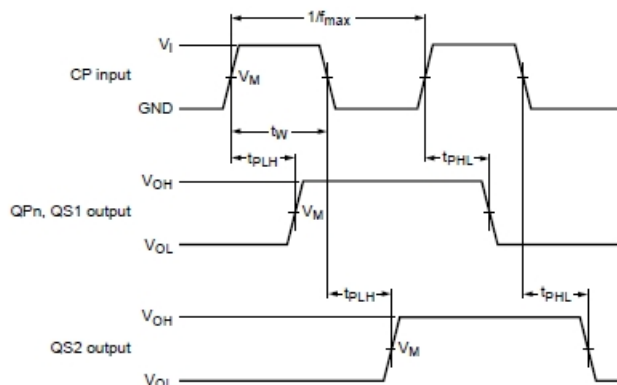


Fig. 6. Clock to outputs propagation delays, and clock pulse width and maximum frequency

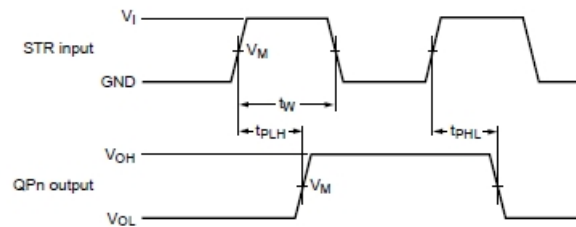


Fig. 7. Strobe to output propagation delays, and strobe pulse width, set up and hold times

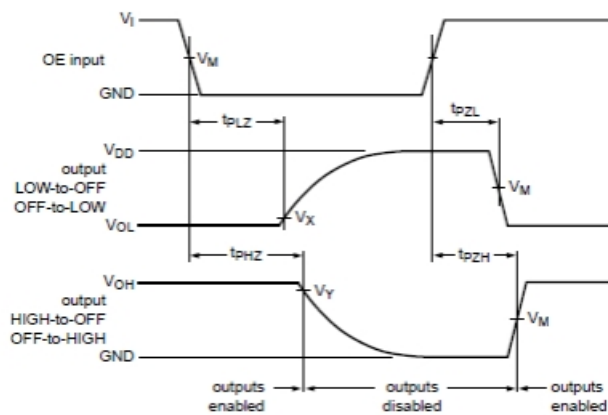


Fig. 8. 3-state output enable and disable times for OE input

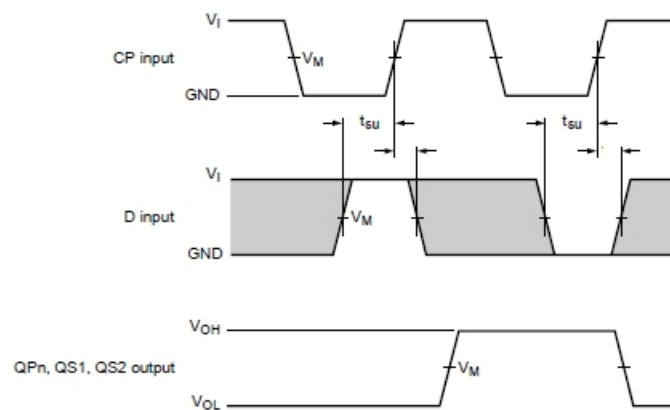


Fig. 9. Data input data set up and hold times

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Table 12. Measurement points

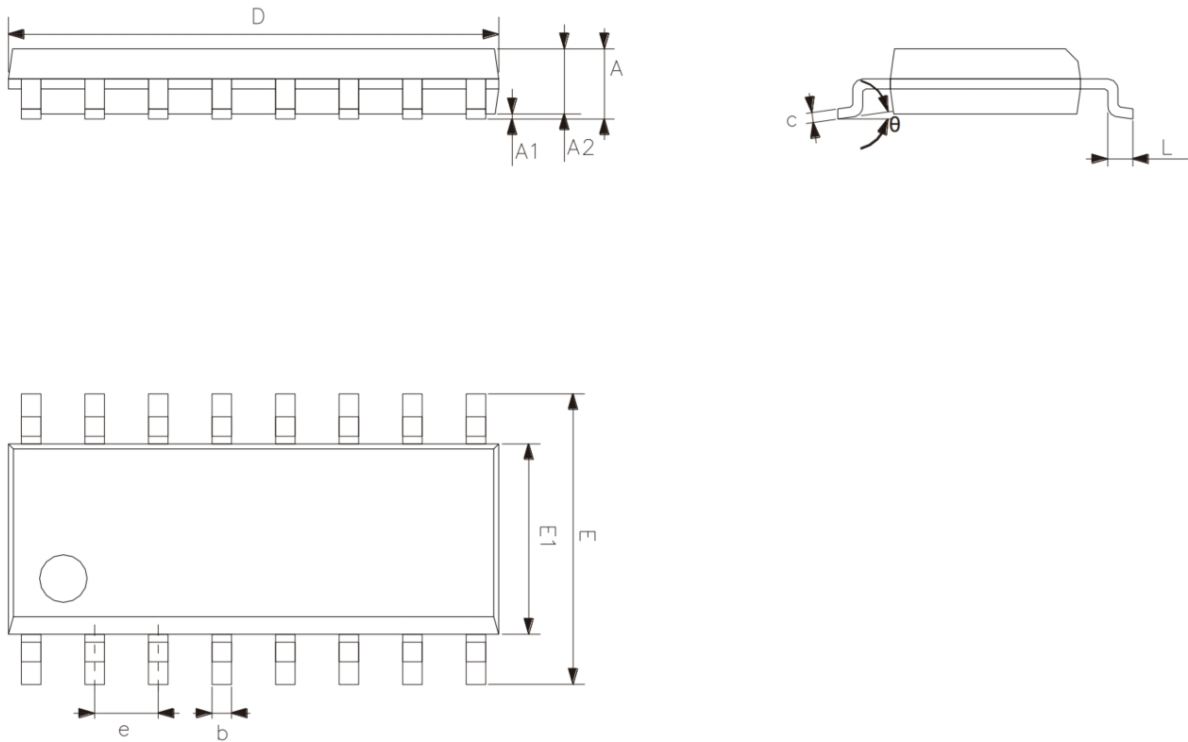
Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$

Table 13. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{DD}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}
5V to 15V	V_{SS} or V_{DD}	$\leq 20\text{ns}$	50pF	1k Ω	open	V_{SS}	V_{DD}

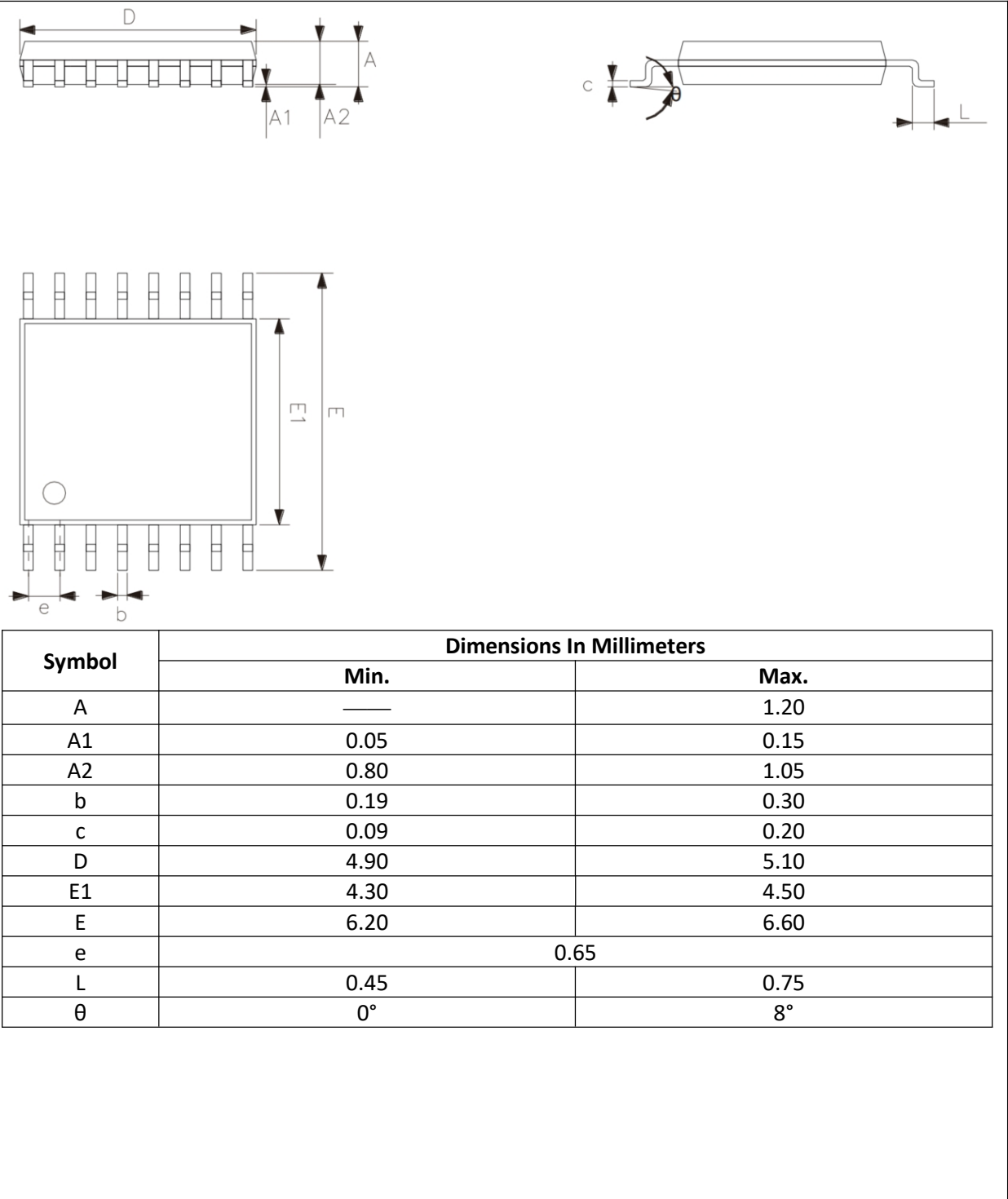
12. Package Outline

SOP-16



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

TSSOP-16



13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Document ID	Release Date	Data sheet status	Change notice	Supersedes
HEF4094 Rev. 1.0	Aug 08, 2024	Product datasheet		