

1. General Description

The HEF4066 provides four single-pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

The HEF4066 is pin compatible with the HEF4016 but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.

2. Features and Benefits

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40°C to +125°C
- Packaging information: SOP14 / TSSOP14

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
HEF4066BT	SOP-14	plastic small outline package; 16 leads; body width 3.9 mm	2500
HEF4066BTT	TSSOP-14	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500

4. Function Diagram

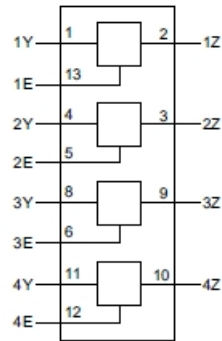


Fig. 1. Functional diagram

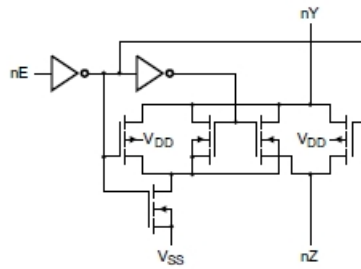
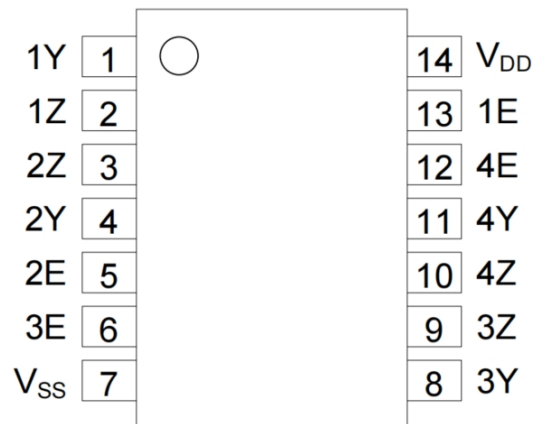


Fig. 2. Logic diagram (one switch)

5. Pinning Information

Pinning



Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y	1	independent input or output
1Z	2	independent input or output
2Z	3	independent input or output
2Y	4	independent input or output
2E	5	enable input (active HIGH)
3E	6	enable input (active HIGH)
V _{SS}	7	ground (0V)
3Y	8	independent input or output
3Z	9	independent input or output
4Z	10	independent input or output
4Y	11	independent input or output
4E	12	enable input (active HIGH)
1E	13	enable input (active HIGH)
V _{DD}	14	supply voltage

6. Functional Description

Function table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Switch
nE	
H	ON
L	OFF

7. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.)

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{DD}	supply voltage	-		-0.5	+12	V
V_I	input voltage	-		-0.5	$V_{DD}+0.5$	V
I_{IK}	input clamping current	$V_I < 0.5V$ or $V_I > V_{DD}+0.5V$		-	± 10	mA
$I_{I/O}$	input/output current	-		-	± 10	mA
T_{stg}	storage temperature	-		-65	+150	°C
P_{tot}	total power dissipation	-		-	500	mW
P	device dissipation	per output transistor		-	100	mW
T_L	soldering temperature	10s	SOP/TSSOP	260		°C

8. Recommended Operating Conditions

Table 5. Recommended Operating Conditions

 $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$; $nE = V_{DD}$; $V_{IS} = V_{DD} = 5\text{ V}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	supply voltage	-	3	5	9	V
T_{amb}	ambient temperature	in free air	-40	-	+125	$^{\circ}\text{C}$
V_I	input voltage	-	0	-	V_{DD}	V
t_{PHZ}	Disable output time (High level→turn off)	nE to nZ or nE to nY	-	80	160	ns
t_{PLZ}	Disable output time (Low level→turn off)	nE to nZ or nE to nY	-	80	160	ns
$t_{\text{PZH}}, t_{\text{PZL}}$	Enable output time (turn off→high/low level)	-	-	45	90	ns
C_i	input capacitance	-	-	-	7.5	pF

9. Static Characteristics

Table 8. DC Characteristics 1

 $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)		T _{amb} =25 °C			Unit
				Min.	Typ.	Max.	
I _{DD}	supply current	V _I =V _{DD} or V _{SS} , I _O =0A	V _{DD} =5V	-	-	1.0	uA
			V _{DD} =9V	-	-	2.0	uA
V _{IH}	HIGH-level input voltage	I _o <1uA	V _{DD} =5V, V _O =0.5V or 4.5V	3.5	-	-	V
			V _{DD} =9V, V _O =0.5V or 8V	7.0	-	-	V
V _{IL}	LOW-level input voltage	I _o <1uA	V _{DD} =5V, V _O =0.5V or 4.5V	-	-	1.5	V
			V _{DD} =9V, V _O =0.5V or 8V	-	-	3.0	V

I_I	input leakage current	$V_I=0V$ or $9V$, $V_{DD}=9V$		-	-	1.0	μA
R_{ON}	ON resistance (rail)	$V_I=0V$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5V$	-	350	2500	Ω
			$V_{DD}-V_{EE}=9V$	-	80	245	Ω
		$V_I=0V$	$V_{DD}-V_{EE}=5V$	-	115	340	Ω
			$V_{DD}-V_{EE}=9V$	-	50	160	Ω
		$V_I=V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5V$	-	120	365	Ω
			$V_{DD}-V_{EE}=9V$	-	65	200	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I=0V$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5V$	-	25	-	Ω
			$V_{DD}-V_{EE}=9V$	-	10	-	Ω

Note: On resistance waveform and test circuit see Figure 9 and Figure 10.

Table 9. DC Characteristics 2

$T_{amb} = -40^\circ C$ to $+85^\circ C$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)		$T_{amb}=-40^\circ C$		$T_{amb}=+85^\circ C$		Unit
				Min.	Max.	Min.	Max.	
I_{DD}	supply current	$V_I=V_{DD}$ or V_{SS} , $I_O=0A$	$V_{DD}=5V$	-	1.0	-	7.5	μA
			$V_{DD}=9V$	-	2.0	-	15.0	μA
V_{IH}	HIGH-level input voltage	$ I_O <1\mu A$	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5	-	3.5	-	V
			$V_{DD}=9V$, $V_O=0.5V$ or $8V$	7.0	-	7.0	-	V
V_{IL}	LOW-level input voltage	$ I_O <1\mu A$	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	-	1.5	-	1.5	V
			$V_{DD}=9V$, $V_O=0.5V$ or $8V$	-	3.0	-	3.0	V
I_I	input leakage current	$V_I=0V$ or $9V$, $V_{DD}=9V$		-	-	-	1.0	μA

Table 10. DC Characteristics 3

$T_{amb} = -40^\circ C$ to $+125^\circ C$, voltages are referenced to V_{SS} (ground = 0 V), unless otherwise specified.

Symbol	Parameter	Conditions (V)		$T_{amb}=-40^\circ C$		$T_{amb}=+125^\circ C$		Unit
				Min.	Max.	Min.	Max.	
I_{DD}	supply current	$V_I=V_{DD}$ or V_{SS} , $I_O=0A$	$V_{DD}=5V$	-	1.0	-	7.5	μA
			$V_{DD}=9V$	-	2.0	-	15.0	μA
V_{IH}	HIGH-level input voltage	$ I_O <1\mu A$	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5	-	3.5	-	V
			$V_{DD}=9V$, $V_O=0.5V$ or $8V$	7.0	-	7.0	-	V

V_{IL}	LOW-level input voltage	$ I_O < 1\mu A$	$V_{DD}=5V, V_O=0.5V$ or 4.5V	-	1.5	-	1.5	V
			$V_{DD}=9V, V_O=0.5V$ or 8V	-	3.0	-	3.0	V
I_i	input leakage current	$V_i=0V$ or 9V, $V_{DD}=9V$		-	-	-	1.0	μA

10. Dynamic Characteristics

Table 11. AC Characteristics1

$T_{amb} = 25\text{ }^{\circ}C$, $V_{EE} = V_{SS} = 0\text{ V}$, $t_r, t_f \leq 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
t_{PHL}	HIGH to LOW propagation delay time	nY to nZ; nZ to nY; see Figure 4	$V_{DD}=5V$	-	10	20	ns
			$V_{DD}=9V$	-	5	10	ns
t_{PLH}	LOW to HIGH propagation delay	nY to nZ; nZ to nY; see Figure 4	$V_{DD}=5V$	-	10	20	ns
			$V_{DD}=9V$	-	5	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	80	160	ns
			$V_{DD}=9V$	-	65	130	ns
t_{PLZ}	LOW to OFF-state propagation delay	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	80	160	ns
			$V_{DD}=9V$	-	70	140	ns
t_{PZH}	OFF-state to HIGH propagation delay	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	40	80	ns
			$V_{DD}=9V$	-	20	40	ns
t_{PZL}	OFF-state to LOW propagation delay	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	45	90	ns
			$V_{DD}=9V$	-	20	40	ns

Table 12. AC Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{EE} = V_{SS} = 0\text{ V}$, $V_i = 0.5V_{DD}$ (p-p), unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
d_{sin}	Square wave distortion	see Figure 6; $R_L=10\text{k}\Omega$; $V_{DD}=5\text{V}$ $C_L=15\text{pF}$; channel ON; $f_i=1\text{kHz}$	0.25	-	-	%
		$V_{DD}=9\text{V}$	0.04	-	-	%
f_{ct}	any two channel crosstalk	$V_{DD}=9\text{V}$, see note2	1	-	-	MHz
V_{ct}	crosstalk voltage (nE to nY to nZ)	see Figure 7; $R_L=10\text{k}\Omega$; $C_L=15\text{pF}$; E or Sn= V_{DD} (square-wave)	50	-	-	mV
f_{OFF}	OFF frequency	$V_{DD}=9\text{V}$, see note3	1	-	-	MHz
f_{ON}	conduction frequency	$V_{DD}=5\text{V}$, see note4	-	-	-	MHz
		$V_{DD}=9\text{V}$, see note4	90	-	-	MHz

[1] f_i is biased at $0.5V_{DD}$; $V_i=0.5V_{DD}$ (p-p).

[3] $R_L=1\text{k}\Omega$; $C_L=5\text{pF}$, channel off, $20\log V_{os}/V_{is} = -50\text{dB}$, see Figure 6.

[2] $R_L=1\text{k}\Omega$; $20\log V_{os}/V_{is} = -50\text{dB}$, see Figure 8.

[4] $R_L=1\text{k}\Omega$; $C_L=5\text{pF}$, channel on, $20\log V_{os}/V_{is} = -3\text{dB}$, see Figure 6.

11. Waveforms and test circuit

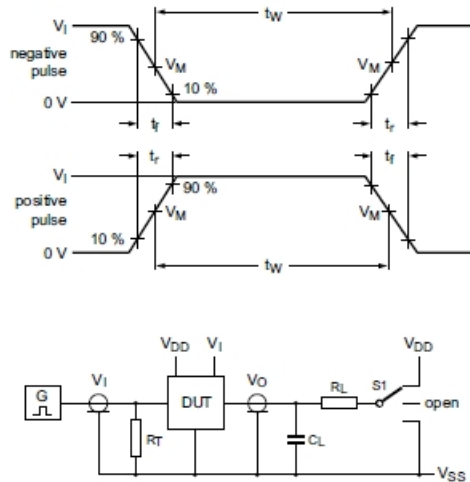


Fig. 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

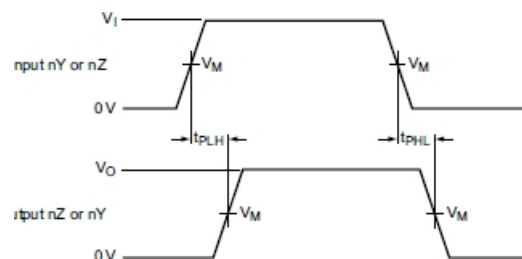


Fig. 4. nY or nZ to nZ or nY propagation delays

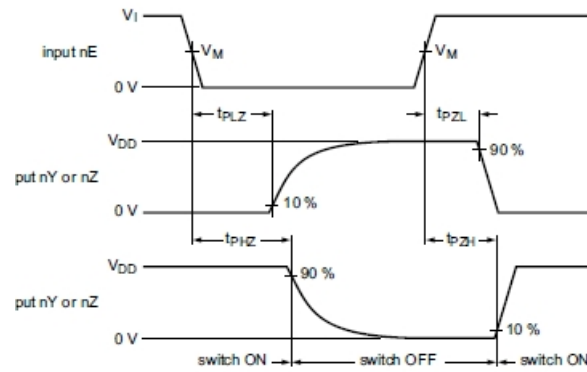


Fig. 5. Enable and disable times

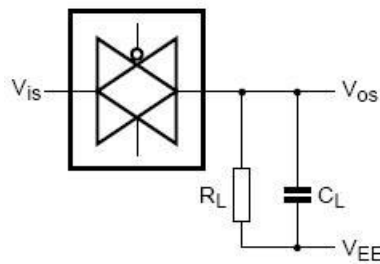


Fig. 6. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

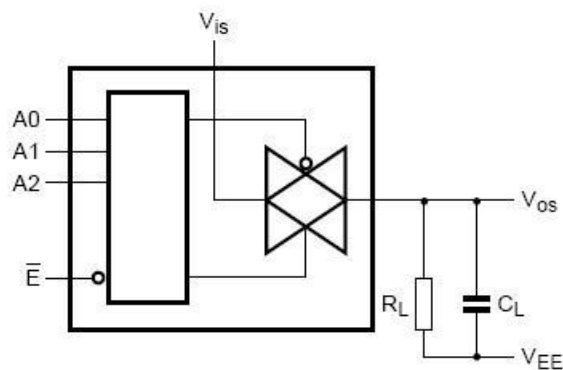


Fig. 7. Crosstalk logical input/output test

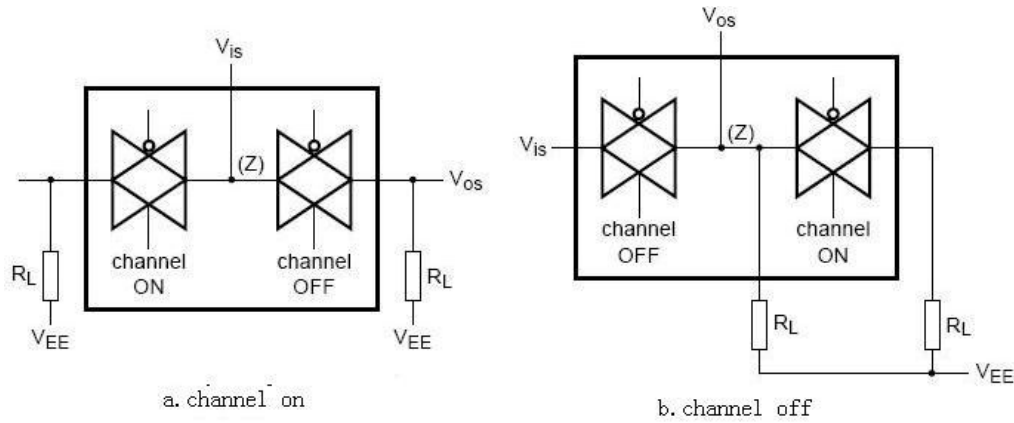


Fig. 8. Inter channel Crosstalk

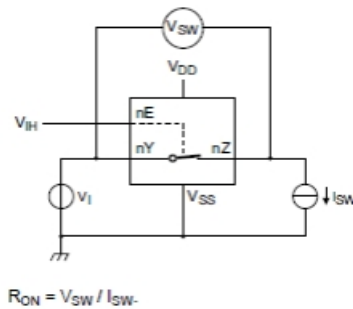


Fig. 9. Test circuit for measuring R_{ON}

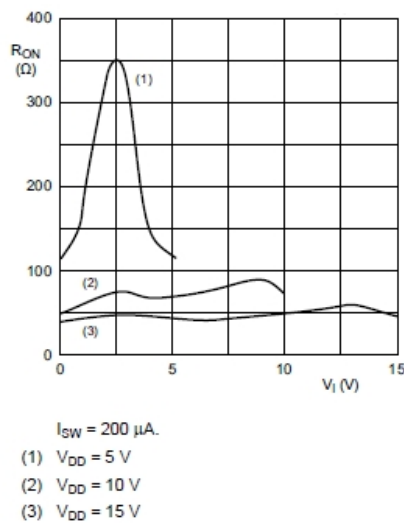


Fig. 10. Typical R_{ON} as a function of input voltage

Table 13. Measurement points

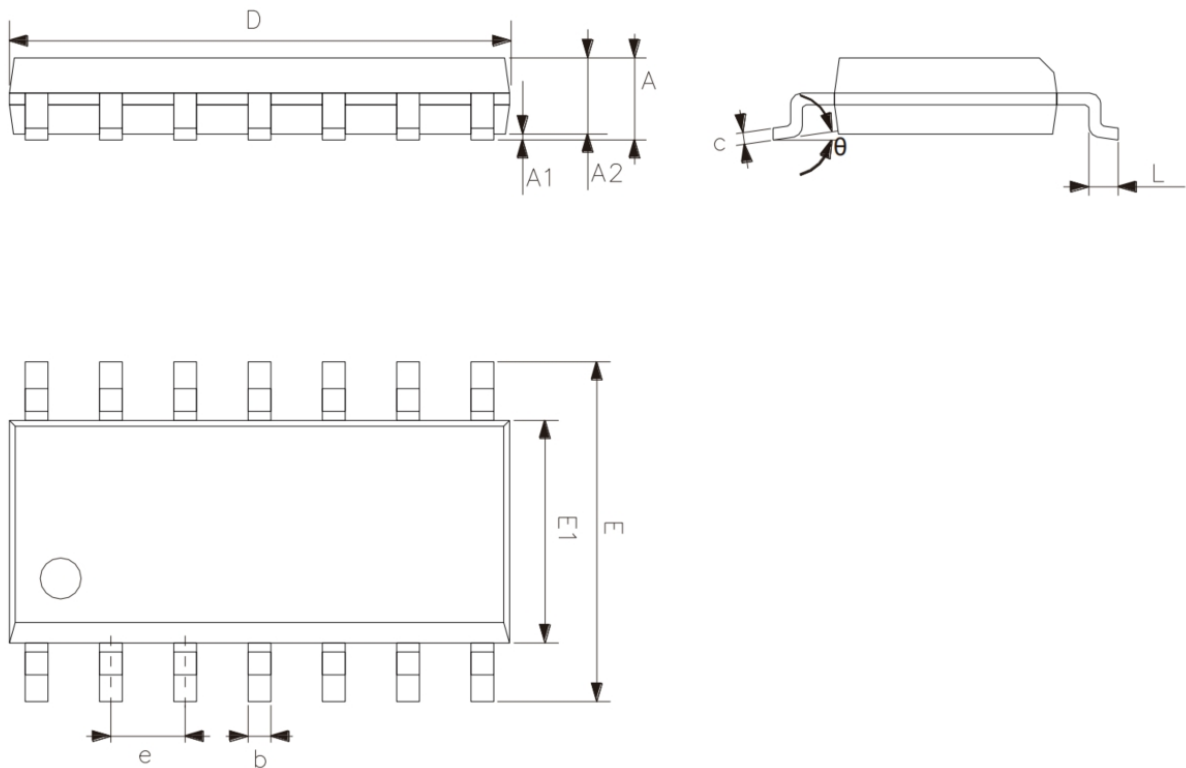
Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 9V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

Table 14. Test data

Test	Input		Load		Switch
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10k Ω	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10k Ω	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20ns	50pF	10k Ω	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20ns	50pF	10k Ω	V_{DD}
others	pulse	20ns	50pF	10k Ω	open

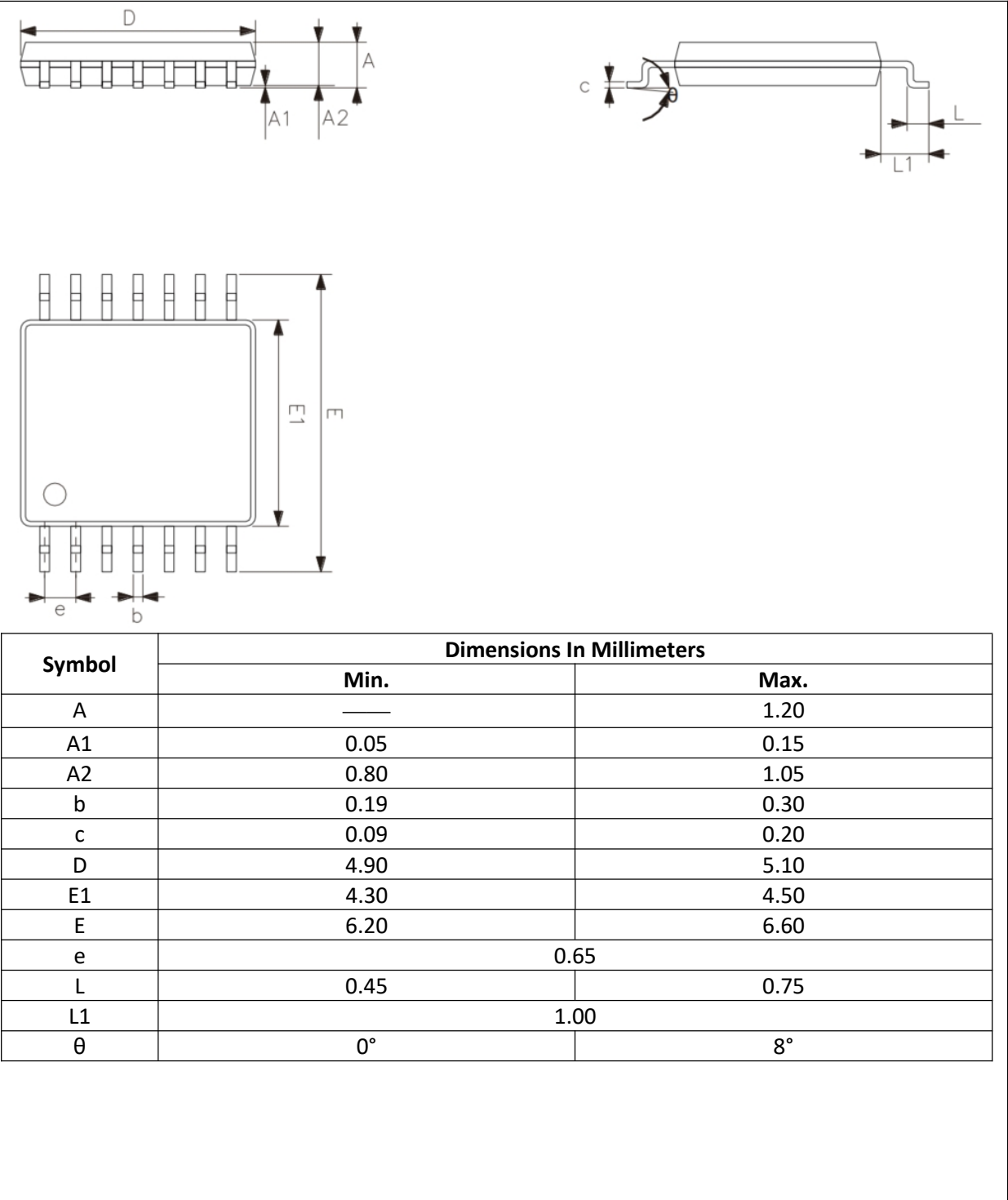
12. Package Outline

SOP-14



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.50	1.75
A1	0.05	0.25
A2	1.30	-
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0°	8°

TSSOP-14



13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Document ID	Release Date	Data sheet status	Change notice	Supersedes
HEF4066 Rev. 1.0	Aug 08, 2024	Product datasheet		