

PRODUCT SPECIFICATION

C u s t o m e r : _____
P r o d u c t N a m e : 1-Wire-to-I²C Master Communication Bridge
P a r t N O : _____ FW28E17Q
I s s u e D a t e : _____

Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- Extending I²C Communication Distance via 1-Wire Protocol (Typically 100 meters)
- Pre-programmed unique 64-bit 1-Wire ROM ID at the factory
- 1-Wire interface supports communication speeds of 15kbps and 77kbps
- I²C interface supports communication speeds of 100kHz, 400kHz, and 1MHz
- I²C interface supports clock stretching function
- Chip package: 16-Pin TQFN
- Temperature range: -40° C to +125° C
- Power supply range: 2.4V to 5.5V
- Low static current
 - Normal operation: 250 μ A (typ)
 - Sleep mode: 0.3 μ A (typ)

2 Applications

- Remote Peripheral Identification and Control
- I²C Sensors
- Display Controllers
- Digital-to-Analog, Analog-to-Digital Converters

3 Description

The FW28E17Q is a communication bridge that functions as a 1-Wire slave to I²C master interface. It serializes incoming data via the 1-Wire protocol and translates it into corresponding I²C output. The 1-Wire interface requires only a single signal line, which effectively conserves GPIO resources.

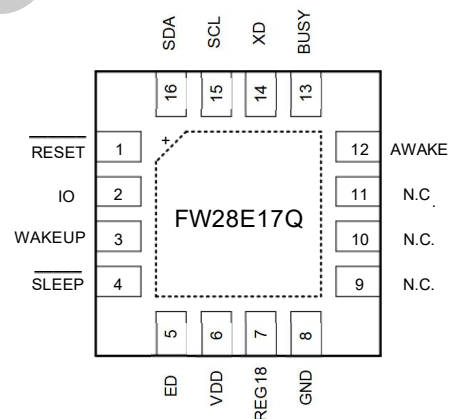
Within the 1-Wire bus, the FW28E17Q is assigned a unique ROM ID that serves as its node address. This ensures that the chip can coexist with other devices

on the same bus and can be individually accessed without interfering with other nodes.

The FW28E17Q offers flexible configuration by supporting multiple 1-Wire and I²C speed modes, making it well-suited for a wide range of complex I²C slave applications, including display controllers, ADCs, DACs, I²C sensors, and more.

Designed for low-power operation, the FW28E17Q can enter sleep mode—reducing power consumption to 0.3 μ A—either by asserting the Sleep pin or by issuing a 1-Wire command. The independent Sleep, Wakeup, and Awake pins provide flexible control options to accommodate various user requirements, with the Awake pin also capable of controlling a remote power supply..

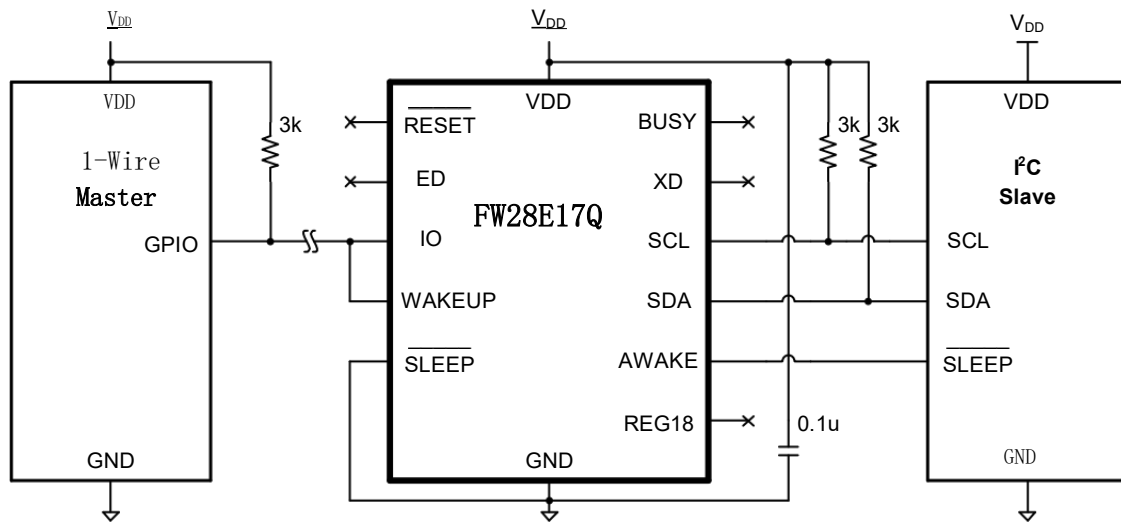
4 Pin Configurations



Device Information

TYPE	Package	Package Size
FW28E17Q	TQFN (16)	4.0mm ×4.0mm

5 Typical application circuit schematic



6 Pin Configurations

No.	Name	Type	description
1	RESET	Bi-directional	This pin is an active-low reset. It can function as an output to provide a reset source for other devices, or it can accept an external active-low reset input. An internal pull-up resistor is provided, allowing this pin to support wired-AND connections with internal reset sources.
2	IO	Open-drain output	1-Wire communication pin. Open-drain output, requiring a pull-up resistor.
3	WAKEUP	output	Wake-up pin: When detecting a rising edge, FW28E17Q will enter the wake-up state.
4	SLEEP	output	Sleep pin: When detecting a falling edge, FW28E17Q will enter the sleep state.
5	ED	Push-pull output	Error Flag: When the FW28E17Q detects a communication error, this pin is driven low and remains in that state until a 1-Wire reset command is received. Communication errors that trigger this condition include invalid function commands, CRC-16 checksum mismatches, and I ² C bus communication failures.
6	VDD	-	Power supply pin: Voltage range is 2.4V to 5.5V. This pin requires a 0.1uF bypass capacitor.
7	REG18	-	Voltage Regulator Output Pin: The typical output voltage is 1.8V. This pin can drive a maximum load current of 200μA.

8	GND	–	Ground Pin
9, 10, 11	N.C.	–	NA
12	AWAKE	Push-pull output	Wake-up indicator: When FW28E17Q is in the wake-up state, this pin outputs high; otherwise, it outputs low. This pin can be used to wake up or put other devices to sleep (based on the wake-up state of FW28E17Q).
13	BUSY	Push-pull output	Busy indicator: After FW28E17Q receives a complete 1-Wire data packet, this pin outputs low until the I ² C communication is completed. When this indicator is low, FW28E17Q will ignore all 1-Wire communications.
14	XD	Push-pull output	Wait-for-data indicator: After FW28E17Q receives a function command, this pin outputs low until a complete 1-Wire data packet is received. Note: For function commands that do not require a complete 1-Wire data packet, this pin will not output low.
15	SCL	Open-drain output	I ² C Serial Clock Pin. Requires a pull-up resistor.
16	SDA	Open-drain output	I ² C Serial data Pin. Requires a pull-up resistor.

7 Specifications

7.1 Absolute Maximum Ratings

	Min	Max	Units
Supply VDD	–0.5	6	V
Voltage on any pin	–0.5	(VDD+0.5) and ≤ 6	V
Operating temperature range	–55	150	° C
Junction temperature		150	° C
Storage temperature	–60	150	° C

7.2 ESD Ratings

		Value	Units
Electrostatic discharge voltage V _{ESD}	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±5000	V
	Machine Mode (MM), per JEDEC-STD Classification	300	V

7.3 Suggested operating range

	Min	Typ	Max	Units
Supply VDD	2.4	3.3	5.5	V
Operating temperature T _A	- 40	25	125	° C

7.4 Electrical characteristics

If not otherwise specified, the following data represent the characteristics of the chip within the T_A = - 40~125°C , VDD=2.4V~5.5V

range. (Typical operating conditions are +25°C and 3.3V).

Parameters	Test conditions	Min	Typ	Max	Units
Supply current	Wake-up state		250	500	uA
	Sleep state		0.3	16	uA
Wake-up time			2		us
Regulated output		1.62	1.8	1.98	V

8 Detailed Description

The FW28E17Q comprises a 1-Wire communication front-end (operating as a slave), an I²C bus controller (operating as a master), and master control logic that bridges the two protocol domains. Serial data exchange between the host and the FW28E17Q takes place over the 1-Wire bus. The host controls the I²C bus by transmitting and receiving 1-Wire data packets, which contain function commands, I²C slave addresses, data length fields, and I²C payload data. Note that both read and write operations on the 1-Wire bus transmit data with the least significant bit (LSB) first.

The 1-Wire bus is a single-master, multi-slave communication system implemented over a single signal line. All devices on the bus must drive the line at appropriate times; therefore, they are required to be connected with open-drain outputs. The 1-Wire protocol is command-based, and the command hierarchy of the FW28E17Q is illustrated in Figure 1.

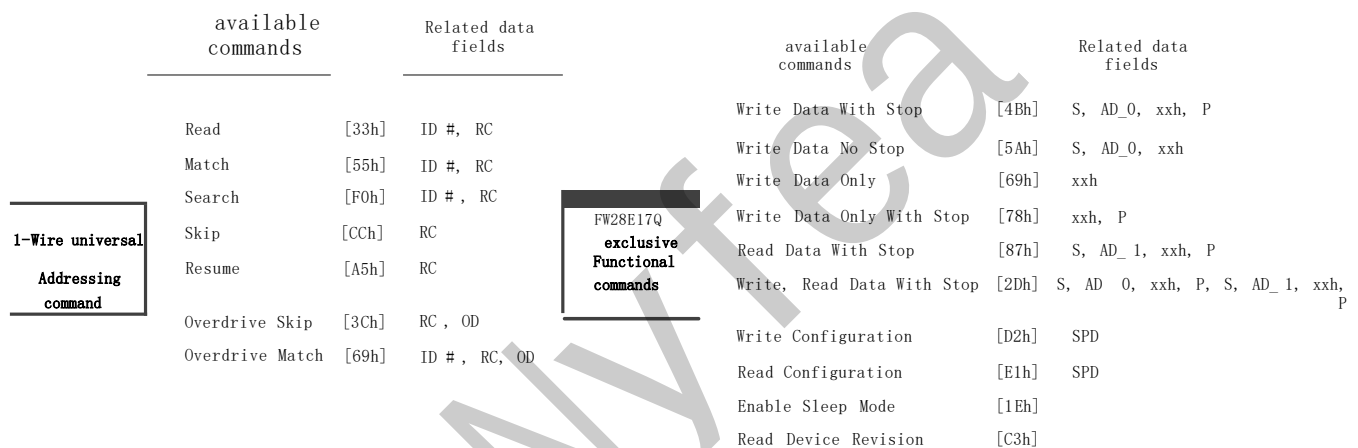


Figure 1: Command Hierarchy Architecture of FW28E17Q

The FW28E17Q supports Standard Mode and Overdrive Mode on the 1-Wire bus, corresponding to maximum data rates of 15 kbps and 77 kbps, respectively. The pull-up resistor value on the 1-Wire bus is primarily determined by the network size and the total bus capacitance. In general, larger networks or higher capacitive loads require smaller pull-up resistors to meet the timing specifications of the 1-Wire protocol.

Each FW28E17Q device is assigned a unique 64-bit ROM ID that serves as its node address on the 1-Wire bus. This ensures that the chip can coexist with other devices and be individually accessed without affecting other nodes. The ROM ID consists of an 8-bit family code, a 48-bit unique serial number, and an 8-bit CRC, as illustrated in Figure 2. The CRC is calculated using the polynomial $x^8 + x^5 + x^4 + 1$ over the family code and serial number.

The CRC generator comprises a shift register and XOR gates, as shown in Figure 3. The shift register is initially cleared to all zeros, after which data bits are shifted in sequentially—starting from the least significant bit of the family code through to the most significant bit of the serial number. Once all data bits have been processed, the value remaining in the shift register constitutes the CRC. If the CRC bits are then shifted in again in the same order, the shift register returns to the all-zero state..

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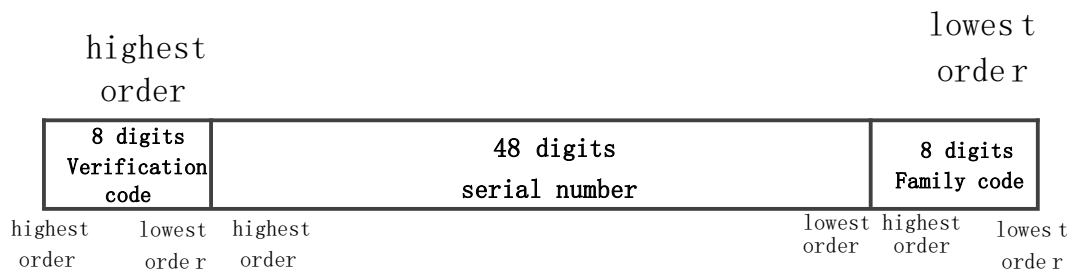


Figure 2: 64-bit ROM ID

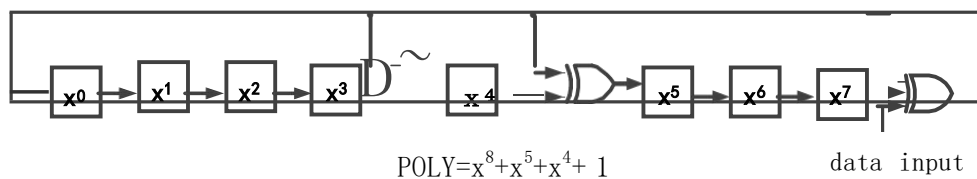


Figure 3: CRC-8 Generator

8.1 1-Wire Signal Timing

The FW28E17Q requires a well-defined protocol to ensure data integrity during communication. The 1-Wire protocol defines six basic signal types on the single data line: Reset Pulse, Presence Pulse, Write 0, Write 1, Read 0, and Read 1. With the exception of the Presence Pulse, all signals are initiated by the bus master and are timed from the falling edge of the bus. The FW28E17Q supports two 1-Wire speed modes: Standard Mode and Overdrive Mode. Overdrive Mode is entered via a specific command and is exited upon receipt of a Standard Mode reset pulse (bus held low for more than 480 μ s). Faster timing parameters are applied when operating in Overdrive Mode.

The initialization sequence—consisting of a Reset Pulse followed by a Presence Pulse, as shown in Figure 4—is a mandatory starting step for all 1-Wire communication. The master generates a Reset Pulse by pulling the bus low for more than 480 μ s in Standard Mode, or more than 48 μ s in Overdrive Mode. The FW28E17Q detects the Reset Pulse, resets its communication state, and then—after a specified delay following the end of the Reset Pulse (when the master releases the bus)—responds with a Presence Pulse by pulling the bus low for 60 - 240 μ s (Standard) or 8 - 24 μ s (Overdrive). To detect the Presence Pulse, the master must sample the bus within a specific time window. If the bus is sampled low, it indicates that the Presence Pulse has been received, confirming that the FW28E17Q is ready to begin communication. If the bus is sampled high, it indicates the absence of a Presence Pulse, meaning either the Reset Pulse was not recognized by the FW28E17Q or no device is connected to the bus.

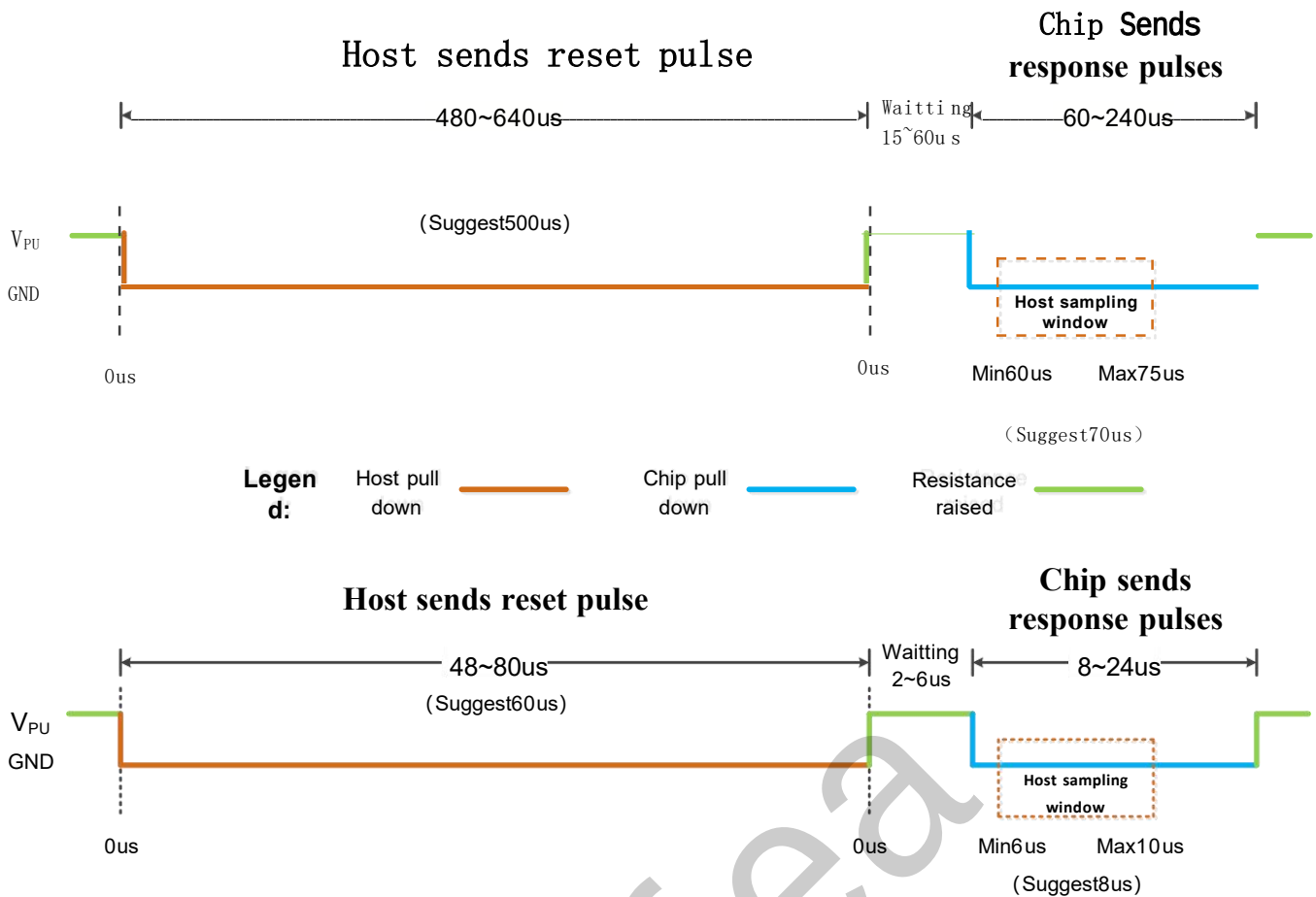


Figure 4: Initialization Sequence (Above: Standard Mode; Below: Overdrive Mode)

1-Wire data transmission is organized into time slots, each carrying a single bit of data. Write slots transfer data from the master to the FW28E17Q, while read slots transfer data from the FW28E17Q to the master. Both types of slots begin with the master pulling the bus low. The slot duration must be at least 65 μ s in Standard Mode and 13 μ s in Overdrive Mode. A recovery time of at least 1 μ s is required between adjacent slots. These timing parameters determine the maximum achievable communication rate.

At the start of a write slot, the FW28E17Q samples the bus within a specific time window, as shown in Figure 5. The sampled value represents one bit of data received by the device. Write slots are further divided into two signal types:

Write 1 slot: After pulling the bus low, the master must release it within 15 μ s (or 2 μ s in Overdrive Mode).

Write 0 slot: After pulling the bus low, the master must hold it low for at least 60 μ s (or 6 μ s in Overdrive Mode) before releasing it..

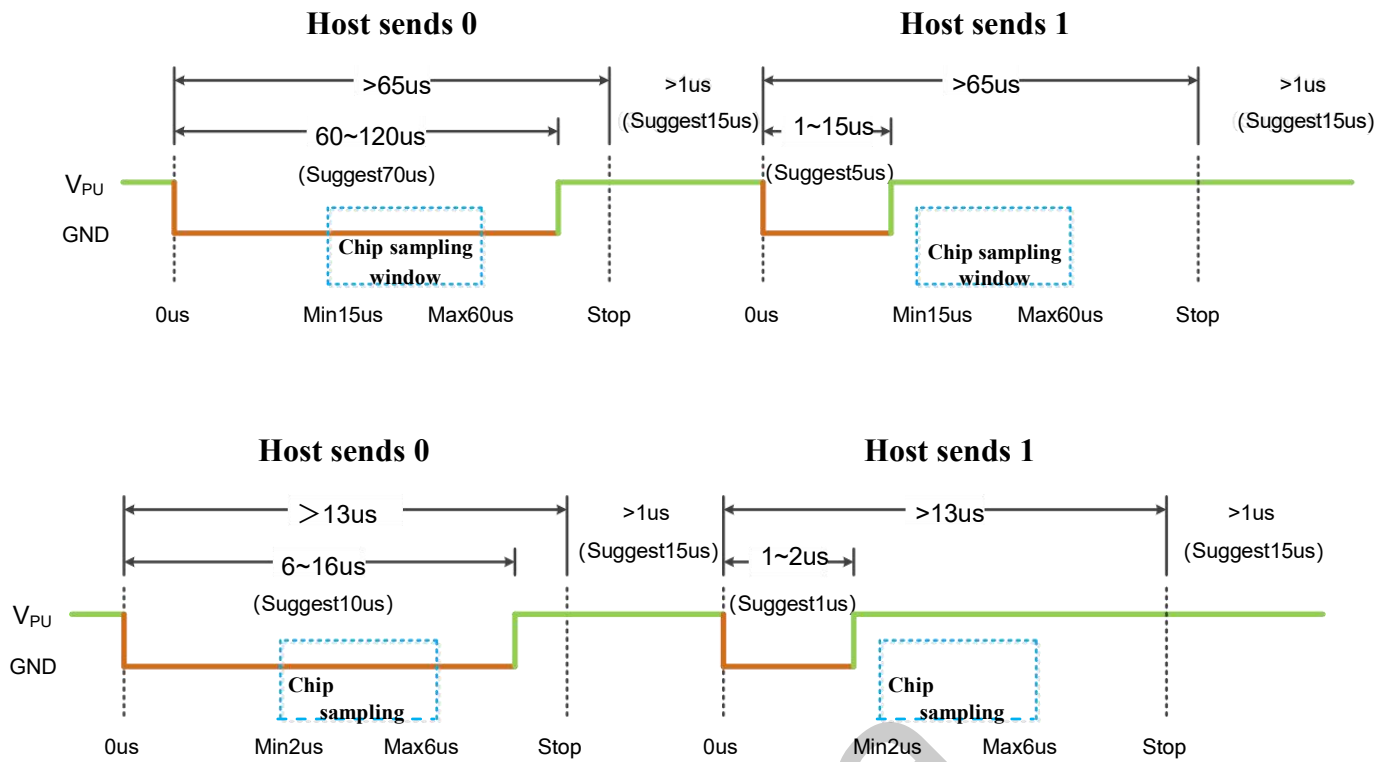
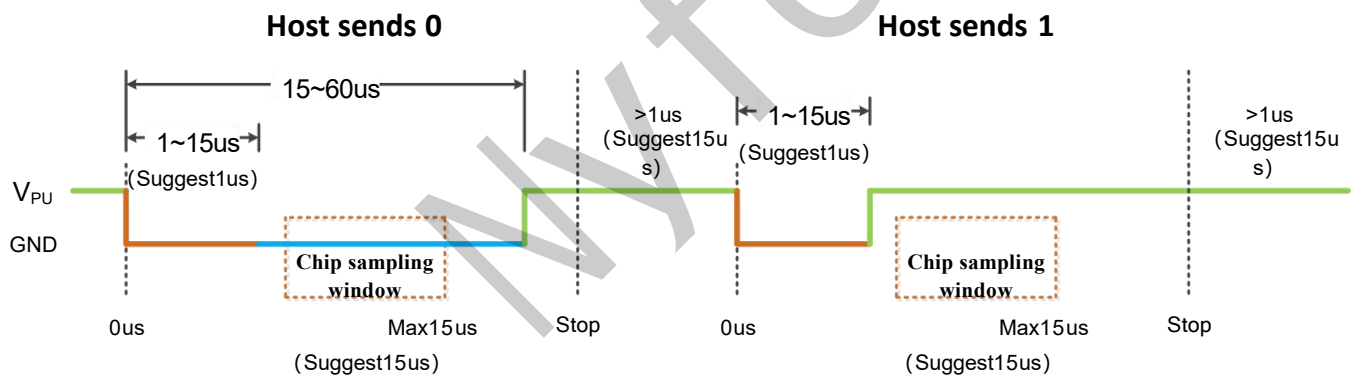


Figure 5: Write Slot (Above: Standard Mode; Below: Overdrive Mode)



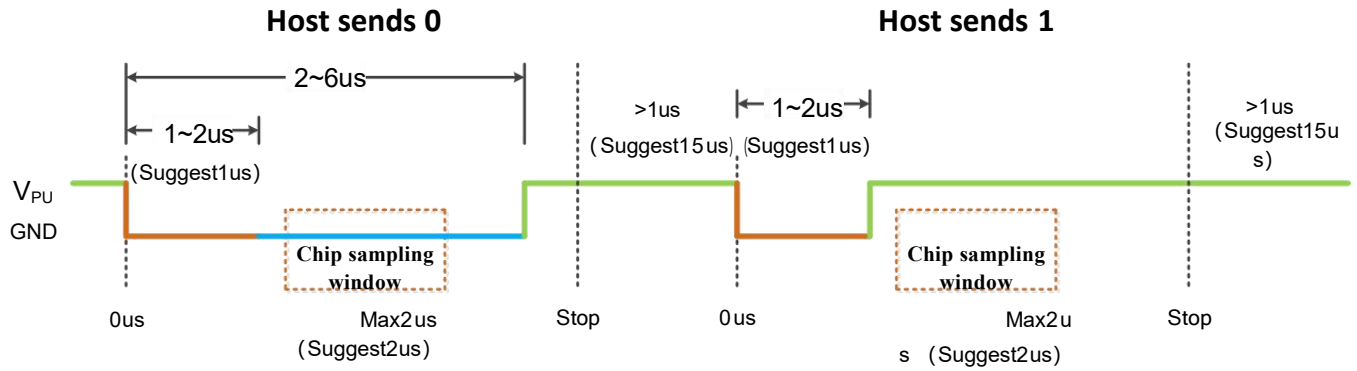


Figure 5: Read Slot (Above: Standard Mode; Below: Overdrive Mode)

The FW28E17Q can transmit data to the master only when the master initiates a read slot. As illustrated in Figure 6, the master begins a read slot by pulling the bus low. It must then hold the bus low for $1 - 15 \mu s$ to ensure that the falling edge is properly detected by the FW28E17Q. Once the FW28E17Q has successfully recognized this condition, it determines the subsequent bus behavior based on the data bit it intends to send. Read slots are therefore divided into two types:

- 1) Read 1 slot: The bus is released directly after the falling edge (i.e., no additional low period is inserted).
- 2) Read 0 slot: Starting from the falling edge, the FW28E17Q holds the bus low for $15 - 60 \mu s$ (or $2 - 6 \mu s$ in Overdrive Mode) before releasing it.

To receive data from the FW28E17Q, the master must sample the bus within a specific time window. The sampled value represents the received data bit. Note that the effective data duration for a Read 0 slot is at least 15 μs (or 2 μs in Overdrive Mode); therefore, the sampling window must not exceed this effective duration. For maximum timing margin, it is recommended that the master release the bus as early as possible (1 μs in both Standard and Overdrive Modes) and delay the sampling point as late as possible (15 μs in Standard Mode and 2 μs in Overdrive Mode).

In a 1-Wire environment, noise interference and signal reflections may cause non-ideal bus transitions such as ringing or glitches, potentially causing the FW28E17Q to lose synchronization with the master. This can lead to issues such as the Search ROM command entering a loop or the forced termination of function commands. To improve performance in multi-slave 1-Wire networks, the FW28E17Q incorporates Schmitt trigger inputs and glitch filtering circuits to reduce sensitivity to bus noise. Figure 7 illustrates the device's noise suppression characteristics in three typical scenarios (note that the glitch filter is enabled only in Standard Mode and is disabled in Overdrive Mode):

Scenario 1: The bus voltage exceeds the high threshold (V_{TH}) but does not fall below the low threshold (V_{TL}). This glitch is filtered by the Schmitt trigger.

Scenario 2: The bus voltage rises above V_{TH} and returns below V_{TL} within 1 μs . This glitch is filtered by the filtering circuit.

Scenario 3: The bus voltage rises above V_{TH} and returns below V_{TL} after more than 1 μs . This glitch is not filtered and is interpreted as the start of a new slot..

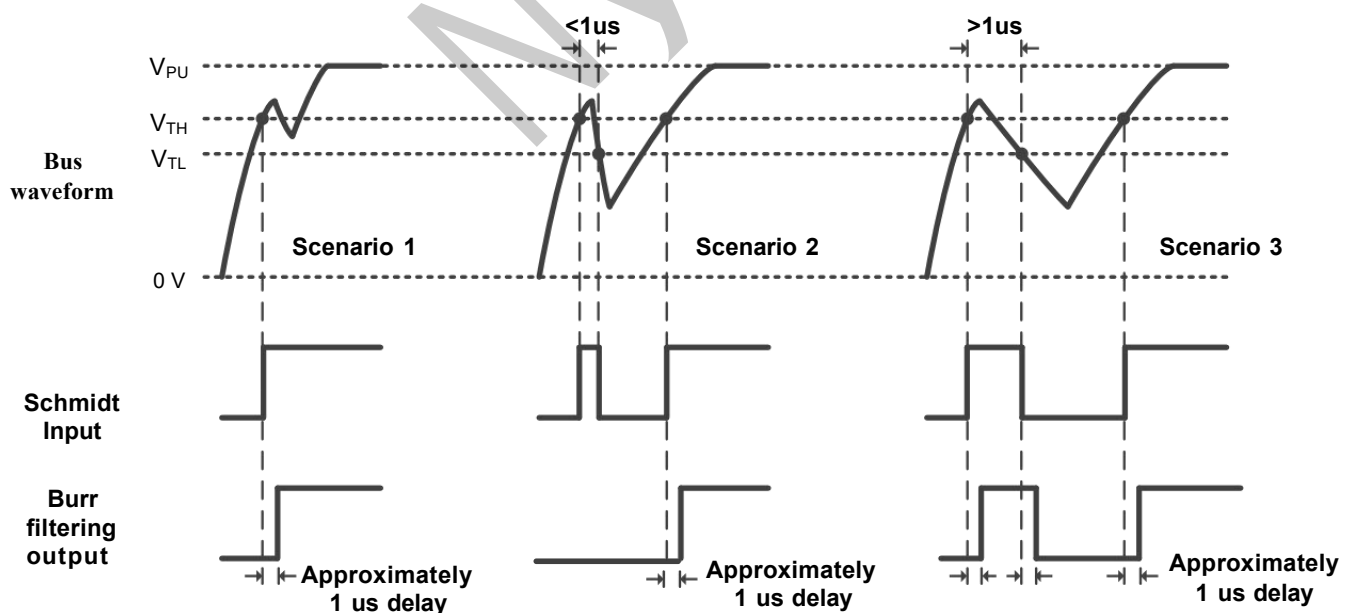


Figure 7: Noise Suppression Characteristics

The 1-Wire communication process of the FW28E17Q comprises four stages: Initialization Sequence, Addressing Commands, Function Commands, and I²C Data Transfer. Following initialization, the master may issue addressing commands to search for and select specific devices on the bus. The FW28E17Q supports seven addressing commands, the execution flow of which is illustrated in Figure 8.

Read ROM [33h]

This command reads the 64-bit ROM ID of the device. Note that if multiple devices are present on the bus, all will begin transmitting simultaneously, resulting in bus contention. Under open-drain connections, the bus behaves as a wired-AND output; consequently, the data read is the bitwise AND of all ROM IDs. In such cases, the CRC computed from the family code and serial number will not match the read checksum.

Match ROM [55h]

This command is followed by a 64-bit ROM ID and is used to address a specific device. Only the device whose ROM ID fully matches the transmitted ID will proceed to execute subsequent function commands. All other devices remain idle and wait for the next reset pulse.

Search ROM [F0h]

When the system starts, the master may be unaware of the number of connected devices or their ROM IDs. This command, combined with a binary tree search algorithm, is used to identify the ROM IDs of all devices on the bus. Starting from the least significant bit, for each bit of the ROM ID, the master initiates three time slots. In the first slot, all devices participating in the search transmit the true value of their ROM ID bit. In the second slot, they transmit the complement of that bit. In the third slot, the master sends the desired true value for that bit. Devices whose ROM IDs do not match the master's selection are excluded from the search and await the next reset pulse.

By exploiting the wired-AND behavior of the bus, the master can infer the ROM ID bit states of all devices from the results of the first two slots. If both the true value and its complement are 0, this indicates a discrepancy in the ROM ID bit among devices. By selecting the branch value in the third slot, the master navigates down one path of the search tree. After completing a full round of searches, the 64-bit selection value becomes the ROM ID of a specific device on the bus; all other devices are placed in an idle state. Repeated rounds of this process will eventually identify the ROM IDs of all devices on the bus.

1 Skip ROM [CCh]

This command directly addresses all devices on the bus. Note: If subsequent function commands are read-type commands, bus data conflicts will occur.

1 Resume ROM [A5h]

This command enables direct addressing of the previously selected device, thereby maximizing data throughput. The FW28E17Q maintains an internal RC flag. This flag is set to 1 only when the Search ROM, Match ROM, or Overdrive Match commands have been executed successfully. Prior to each execution of the Search ROM, Match ROM, Overdrive Match, Read ROM, Skip ROM, or Overdrive Skip commands, the RC flag is cleared to 0. Once the RC flag is set to 1, the master may use the Resume command to repeat addressing the device without re-sending the full ROM ID.

Overdrive Skip ROM [3Ch]

This command addresses all devices on the bus while simultaneously configuring all overdrive-capable devices to enter Overdrive Mode (OD=1). Subsequent communication must conform to the signal timing specifications of Overdrive Mode. The bus remains in Overdrive Mode until a Standard-Mode reset pulse (bus held low for more than 480 μ s) is issued, which returns all devices to Standard Mode (OD=0).

Overdrive Match ROM [69h]

This command is used in Overdrive Mode to address a specific device by following it with a 64-bit ROM ID, and it configures the targeted device to remain in Overdrive Mode (OD=1). If a device is already in Overdrive Mode prior to receiving this command, it will not exit Overdrive Mode regardless of whether the match is successful or not; it will only return to Standard Mode upon receiving a Standard-Mode reset pulse.

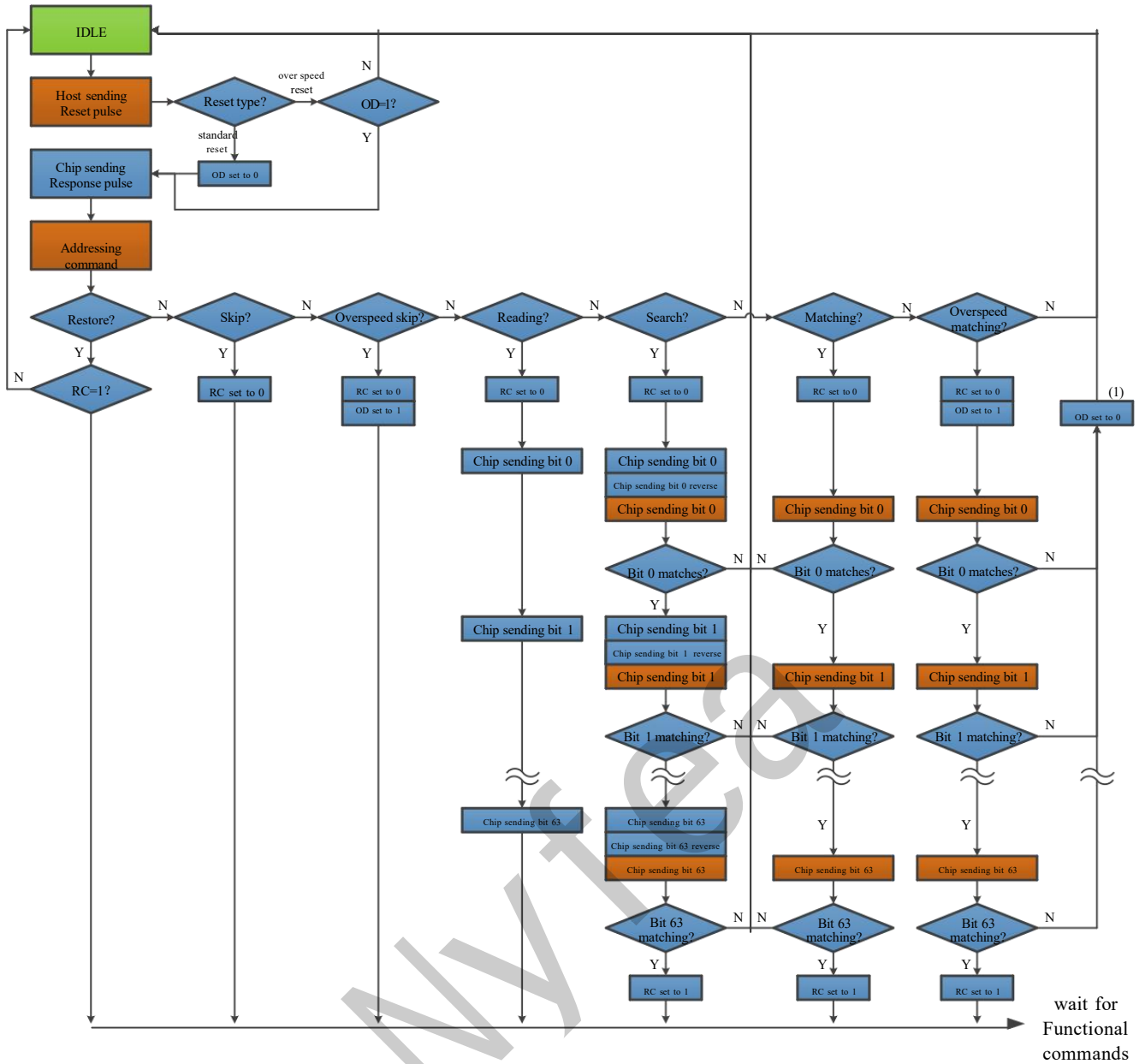


Figure 8 – Addressing Commands Flow

Note (1): If already in Overdrive Mode before receiving the [Overdrive-Match] command, the OD flag will remain at 1.

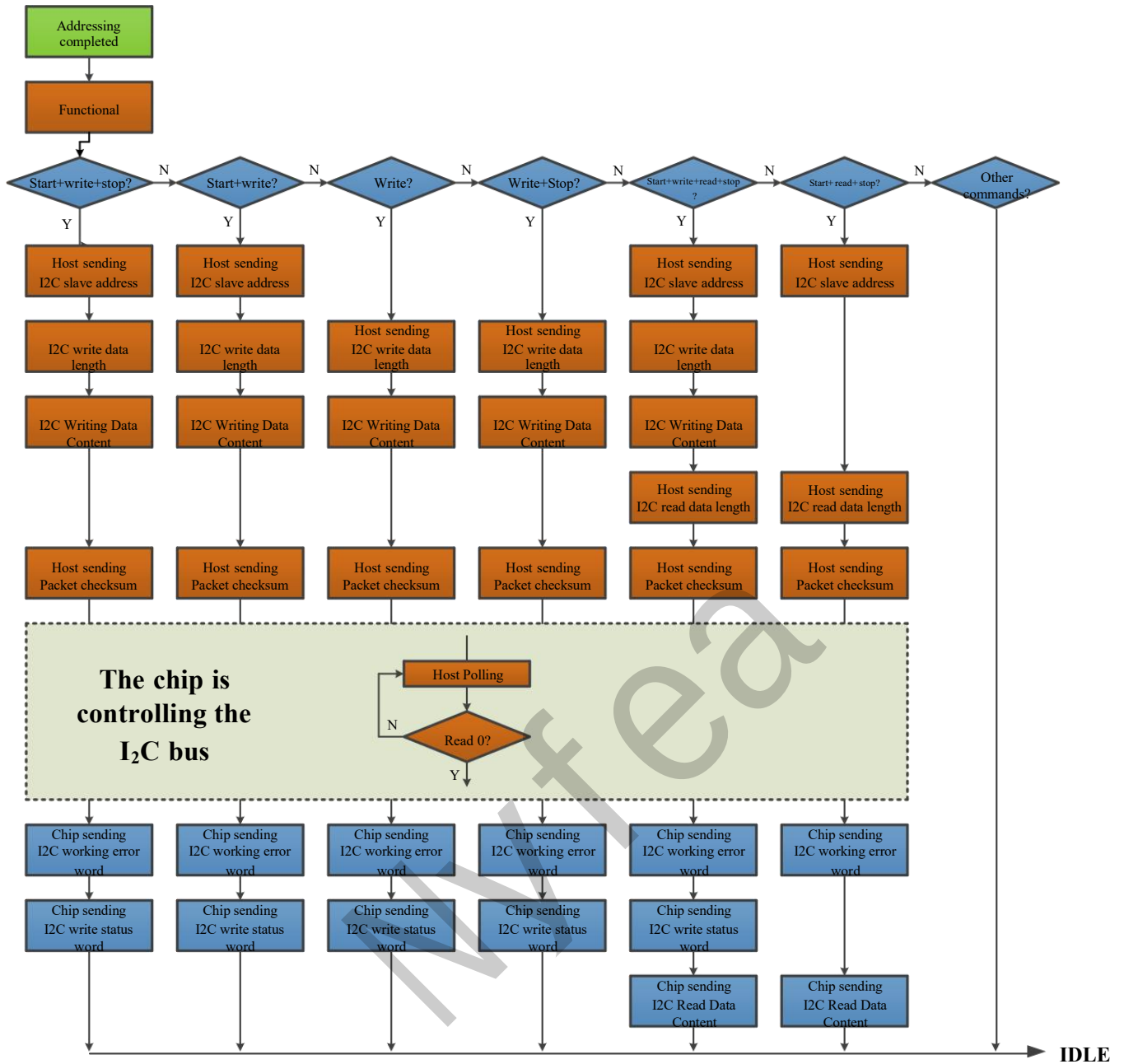


Figure 9 – Function Commands Flow

Once addressed, the FW28E17Q can receive and execute subsequent function commands. The device supports six types of I²C control commands, as shown in Figure 9. These commands, along with their associated parameters—including the I²C slave address, write data length, write data payload, read data length, and checksum—together form a 1-Wire data packet. The write/read data length field specifies the number of bytes to be written or read, and can range from 1 to 255. If this length is set to 0, the Error Detection (ED) pin is asserted and the FW28E17Q enters an idle state.

The 16-bit checksum serves as a cyclic redundancy check (CRC) for the 1-Wire data packet (excluding the checksum field itself), using the generating polynomial $x^{16} + x^{15} + x^2 + 1$. Unlike the CRC-8 used in the ROM ID, the CRC-16 is transmitted as the complement of the computed result. The FW28E17Q integrates a CRC-16 generator, as illustrated in Figure 10, which performs the CRC calculation concurrently with packet reception. If the calculated value does not match the received checksum, the Error Detection (ED) pin is asserted and the device enters an idle state..

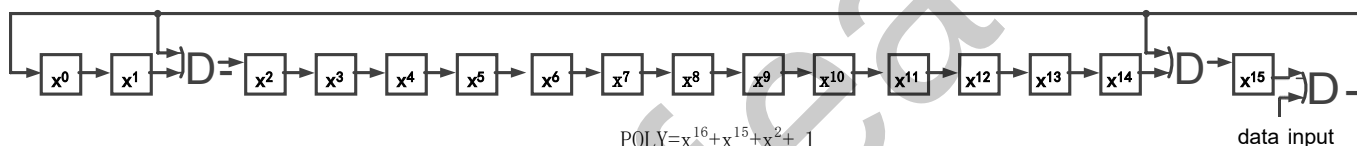


Figure 10 CRC-16 Generator

After the 1-Wire data packet has been transmitted, the FW28E17Q initiates control of the I²C bus based on the contents of the packet. At this point, the host may query the completion status using one of three methods: 1) waiting for a specific delay; 2) polling the Busy Flag pin (BUSY); or 3) polling the bus by continuously initiating read time slots—where a read 1 indicates that the task is still in progress, and a read 0 indicates completion. Regardless of the method chosen, the host must query the bus at least once. A read bit value of 0 represents task completion and must occur before any subsequent data bytes can be read. Upon completing the bus query, the host may read two bytes representing the I²C communication status: the error status byte and the write status byte.

Table 1 – Error Status Byte

7	6	5	4	3	2	1	0
0	0	0	0	Invalid Start	0	Invalid Address	Checksum Error

Table 2 – Description of Error Status Byte Contents

Flag Name	Description
Invalid Start	A value of 1 indicates: When FW28E17Q sends the start condition, the SCL line is pulled down by another device, preventing the correct generation of the start

	condition.
Invalid Adress	A value of 1 indicates: The I ² C address sent by FW28E17Q did not receive an ACK.
Checksum Error	A value of 1 indicates: The checksum calculated by FW28E17Q does not match the received checksum.

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Table 3 – Write Status Byte

7	6	5	4	3	2	1	0
WB[7]	WB[6]	WB[5]	WB[4]	WB[3]	WB[2]	WB[1]	WB[0]

Table 4 – Description of Write Status Byte Contents

Flag Name	Description
WB[7:0]	Indicates from which byte the write data is not acknowledged (NACK) by the slave N. A value of 0 represents all bytes acknowledged by the slave.

When the value of the error status byte is not 00h, the error flag pin (ED) will be set until a 1-Wire reset pulse is received, clearing it. Simultaneously, the value of the write status byte will be FFh because the I²C communication hasn't been initiated yet.

To visually describe the functional commands, consider the following schematic:

Table 5 – Legend for Color Representation

1-Wire	The host writing to FW28E17Q
	The host reading to FW28E17Q
	"The host polling FW28E17Q"
I ² C	FW28E17Q writing to the I ² C slave.
	"FW28E17Q reading to the I ² C slave."

Table 6 – I²C Identification Description

Flag Name	Description
S	Start Condition
Sr	Repeated Start Condition
AD, 0	Write Address
AD, 1	Read Address
xxh[#]	Write Data
(xxh)[#]	Read Data
P	Stop Condition
ACK	ACK
NACK	NACK

Table 7 – Generic 1-Wire Data Flow (Initialization and addressing details are omitted in the following text)

initialization		address	1-Wire packet		I ² C Controlling	Return results	
reset pulse	Response pulse	Addressing command	Functional commands	Command parameters	Polling	status word	Read data

Table 8 – Typical I²C Data Flow (Using a two-byte write as an example)

I ² C Controlling							
S	AD, 0	ACK	xxh _[1]	ACK	xxh _[2]	ACK	P

1 The command "Start, Write Data, Stop (Write Data with Stop) [4Bh]

This command addresses the I²C slave and writes 1 to 255 bytes in a single transaction. The number of bytes actually transmitted in the write data must exactly match the specified write data length. The FW28E17Q relies on this length field to determine when to stop receiving data. If a mismatch occurs, the device may misinterpret a portion of the data payload as the CRC-16 checksum, resulting in a command verification error.

command [4Bh]	slave address	write length	write data	data packet	polling	Error Status Word	Write Status Word
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expected I²C output

S	AD, 0	ACK	xxh _[1]	ACK	...	xxh _[255]	ACK	P
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1 Start, Write Data (no Stop) [5Ah]

The command "Start, Write Data (no Stop) [5Ah]" is used to address an I²C slave device, where data ranging from 1 to 255 bytes is written, but a Stop condition is not sent to conclude the ongoing I²C communication. 1-Wire data flow

command [5Ah]	slave address	write length	write data	data packet	polling	Error Status Word	Write Status Word
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expected I²C output

S	AD, 0	ACK	xxh _[1]	ACK	...	xxh _[255]	ACK
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1 Write Data Only[69h]

The command writes 1 to 255 bytes but does not send a stop condition to end the current I²C communication. 1-Wire data flow

command [69h]	slave address	write length	write data	data packet	polling	Error Status Word	Write Status Word
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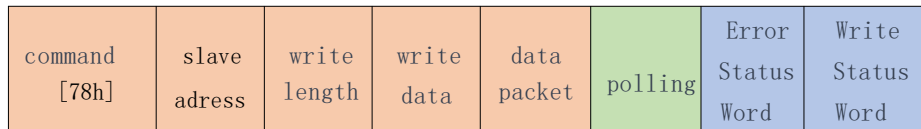
expected I²C output

xxh _[1]	ACK	...	xxh _[255]	ACK
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1 Write Data Only with Stop[78h]

This command writes 1 to 255 bytes and then issues a STOP condition to terminate the current communication session. It can be combined with the preceding two commands to enable the transmission of a large amount of data within a single I²C transaction—beginning with a START condition and ending with a STOP condition.

1-Wire data flow



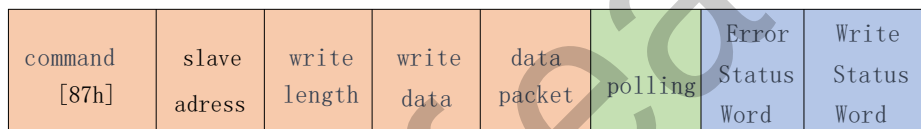
expected I²C output



1 Read Data with Stop[87h]

The command addresses an I²C slave and reads 1 to 255 bytes within a single communication, finally sending a stop condition to end the I²C communication.

1-Wire data flow



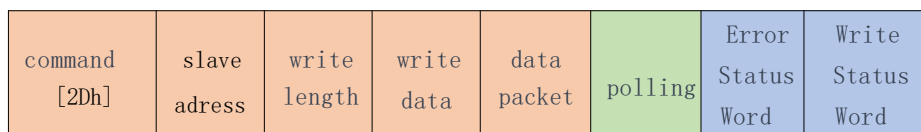
expected I²C output



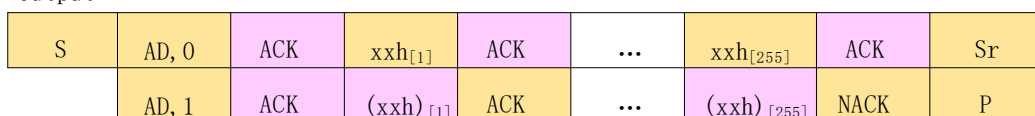
1 Write, Read Data with Stop[2Dh]

This command first addresses an I²C slave and writes 1 to 255 bytes. It then re-addresses the same slave, changes the bus direction to read, and reads 1 to 255 bytes. Finally, it issues a STOP condition to conclude the I²C transaction.

1-Wire data flow



expected I²C output



In addition to the six I²C control commands described above, the FW28E17Q also supports three configuration commands for adjusting the I²C communication rate and enabling sleep mode. Since these configuration commands do not involve I²C bus operations, they do not return error status words or write status words.

1 Write Configuration[D2h]

This command is used to write the configuration word for the I²C communication rate.

1-Wire data flow

Reset Pulse	Response Pulse	Addressing Command	Command [D2h]	Configuration Byte
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Table 9 Configuration Byte (Power-On Default Value is 01h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPD[1]	SPD[0]

Table 10 Explanation of Configuration Byte Content

Flag Name	Description
SPD[1:0]	00b=100kHz, 01b=400kHz, 10b=1MHz, 11b=Unused

1 Read Configuration[E1h]

The command is used to read the I²C communication rate configuration byte. 1-Wire data flow

Reset Pulse	Response Pulse	Addressing Command	Command [E1h]	Configuration Byte
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1 Enable Sleep Mode[1Eh]

This command configures the FW28E17Q to enter a sleep state. Its function is equivalent to that of the Sleep pin (SLEEP). When the device enters sleep mode, all internal modules are powered down, and all 1-Wire communication is effectively ignored. The FW28E17Q exits the sleep state upon detecting a rising edge on the Wakeup pin (WAKEUP).

Pulse	Response Pulse	Addressing Command	Command [1Eh]
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8.2 I²C Signal Timing

The I²C bus is a two-wire, half-duplex, multi-slave communication system comprising a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both SDA and SCL must be configured as open-drain outputs. Note that I²C data transfers begin with the most significant bit (MSB) of each data byte. For every data bit transmitted, SCL provides a corresponding clock pulse. To ensure data integrity, the I²C protocol requires that SDA remain stable while SCL is high; SDA may only change state when SCL is low. Any transition on SDA while SCL is high is interpreted as either a START or STOP condition, both of which—along with the SCL clock pulses—are generated exclusively by the master. Every slave device on the bus must have a unique address and can only be accessed when addressed by the master.

FW28E17Q, acting as an I²C bus controller (i.e., master), supports three communication speeds: 100kHz, 400kHz, and 1MHz, with the following critical timing parameters:

Table 11 the I²C bus controller timing parameters

Parameters	Symbol	100kHz	400kHz	1MHz
Repeat Start Condition Setup Time	t _{SU, STA}	5.25us	1.25us	0.50us
Start Condition Hold Time	t _{HD, STA}	5.25us	1.25us	0.50us
Data Setup Time	t _{SU, DAT}	5.00us	1.00us	0.25us
Data Hold Time	t _{HD, DAT}	0.25us	0.25us	0.25us
Clock High Pulse Width	t _{HI, SCL}	5.25us	1.25us	0.50us
Clock Low Pulse Width	t _{LO, SCL}	5.25us	1.25us	0.50us
Stop Condition Setup Time	t _{SU, STO}	5.25us	1.25us	0.50us
Bus Recovery Time	t _{BUF}	5.25us	1.25us	0.50us

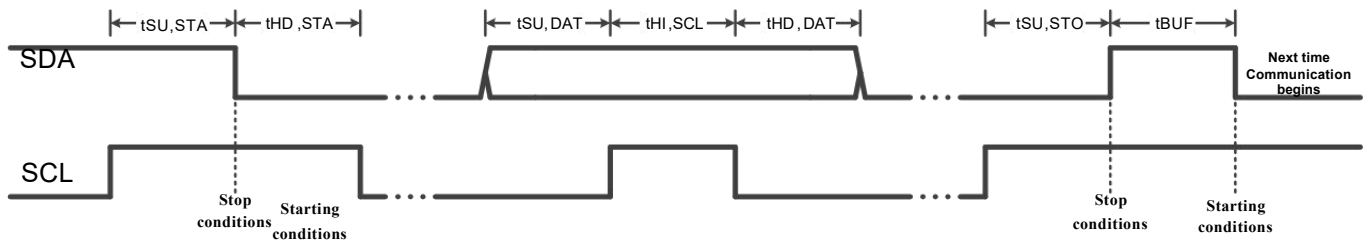


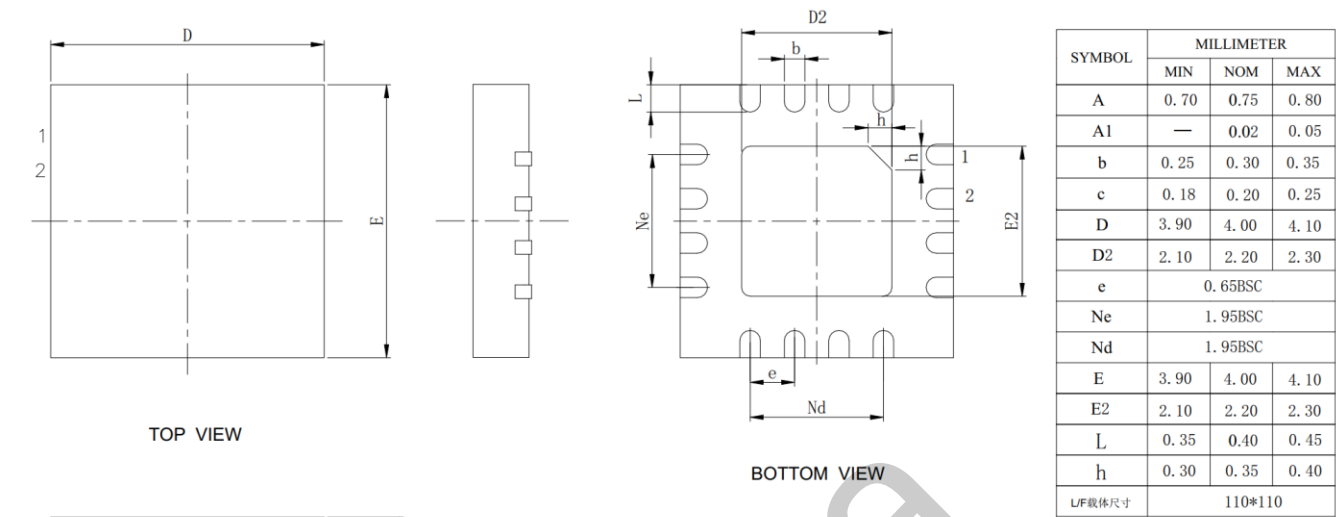
Figure 11 I²C Bus Controller Timing Diagram

The FW28E17Q supports clock stretching on the I²C bus. This allows a slave device to pause an ongoing I²C transaction by pulling the SCL line low, and to resume communication by releasing SCL high. This feature is primarily used in two scenarios:

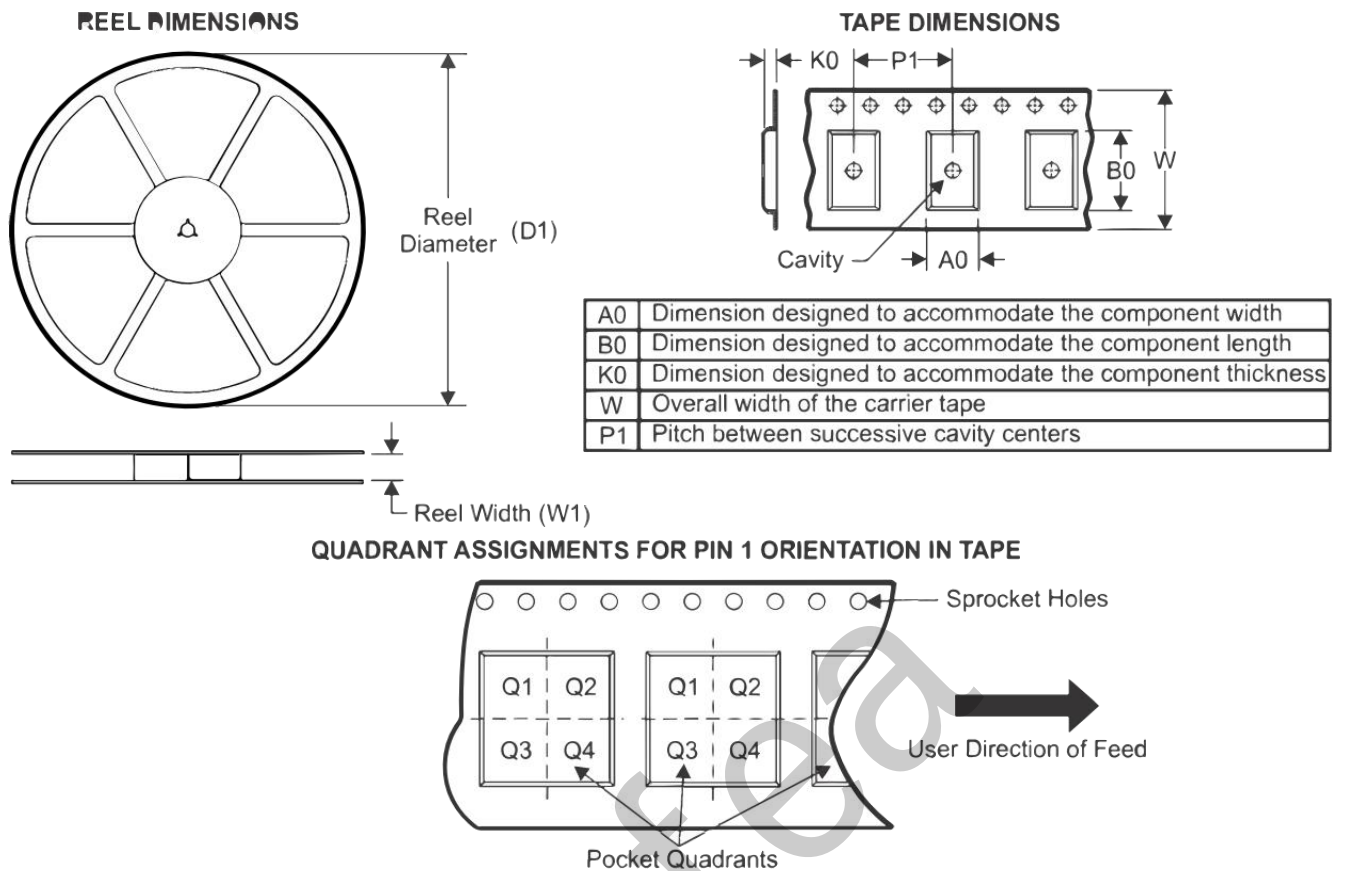
- 1) At the byte level, a slave device may need additional time to process received data or prepare data for transmission, even if it can accept data bytes at a relatively high rate. In this case, the slave can pull SCL low after sending an acknowledge (ACK), forcing the FW28E17Q (or other bus devices) to wait until the slave is ready before the next byte is transmitted.
- 2) At the bit level, some slave devices—such as hardware-constrained MCUs—may not be capable of handling data at faster bit rates. To accommodate this, the slave can lengthen the low period of each SCL clock pulse, effectively reducing the overall bus frequency. The FW28E17Q automatically adapts to the operational I²C rate of such slave devices.

9 Packaging Information

9.1 Package Outline (TQFN-16)



9.2 Tape and Reel Information



PACKAGE	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1
TQFN (16)	329	12.4	4.25	4.25	0.95	8.00	12.00	Q1

Note: All dimensions mentioned above are in millimeters.

10 Ordering Information

ORDER CODE	DEVICE	PACKAGE	QUANTITY	NOTES
FW28E17Q-T&R	FW28E17Q	TQFN (16)	4000	Tape&Reel