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MP2645A

5-Cell Battery Active Balancer with Stackable Interface

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP2645A is a 5-cell highly integrated, bidirectional buck-boost active balancer with a novel topology (MPS patented).

A single MP2645A can redistribute charge between 5 series cells, including Li-ion, Li-polymer, LiFePO4 batteries or super capacitors. The MP2645A operates with 2 to 5 cells and tolerates stack voltages up to 40V. The MP2645A can be configured for up to 3 Amps of charge redistribution.

As an alternative to dissipating energy with passive balancing, the MP2645A efficiently moves charge between cells with much faster balancing and minimal heat generation. The MP2645A can also compensate for cell capacity mismatch to extend battery runtime. By overlapping multiple MP2645A, active balancing can be achieved across long, high voltage battery stacks.

The MP2645A is easily controlled via a simple robust one-wire interface. A stacking feature allows up to 8 series devices, balancing up to 33 series cells, to be operated from a single control signal.

The MP2645A is available in a QFN-19 (4mmx4mm) package.

FEATURES

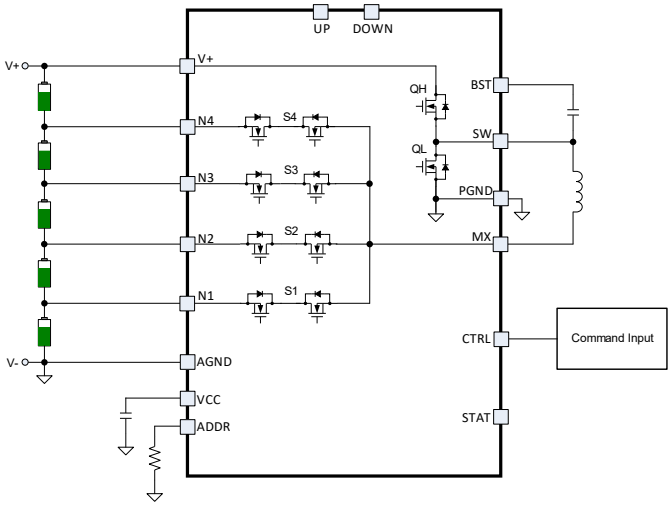
- 2 to 5 Cell Active Balancer
- Only 1 Inductor Required
- 40V Max Stack Voltage
- Up to 3A Balance Current
- One Wire Interface
- Stackable Operation and Communication
- Supports Parallel Operation for Higher Balancing Current
- Directly Powered from Battery Cells
- Includes Watchdog Timer
- Pack Over-voltage Protection
- Thermal Shutdown Protection

APPLICATIONS

- Industrial/Residential Energy Storage
- Battery Backup Systems
- Electric Fork Lifts
- Redeployed & 2nd Life Batteries
- Long-life Battery Systems

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MP2645AGRE-xxxx**	QFN-19 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP2645AGRE-xxxx-Z).

** "xxxx" is the configuration code identifier for the register settings. Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique configuration code. The factory default is "-0000." This setting can be viewed in the OTP register map.

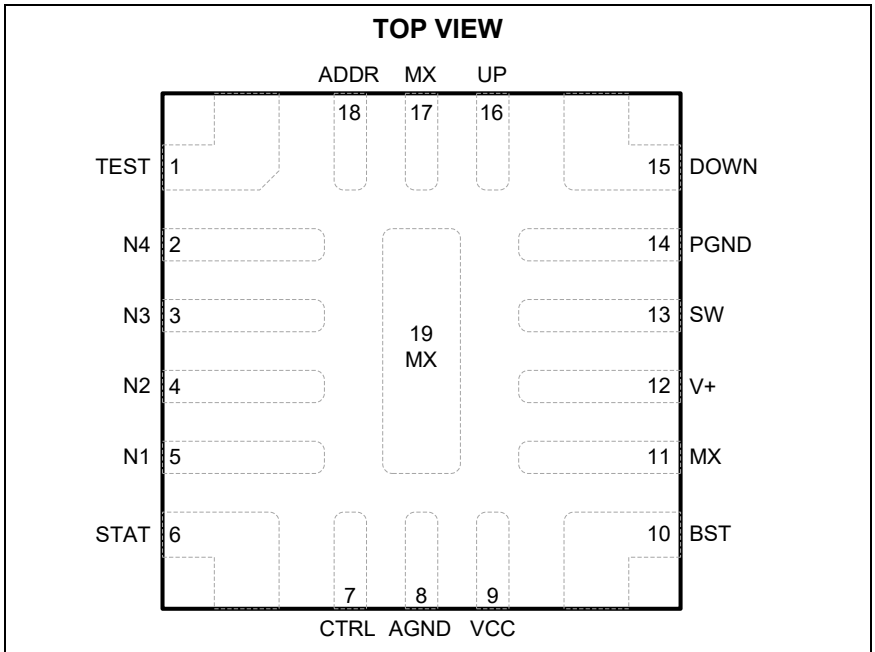
*** Moisture Sensitivity Level Rating

TOP MARKING

MPSYWW
MP2645
LLLLLL
$E

MPS: MPS prefix
Y: Year code
WW: Week code
MP2645: Part number
LLLLLL: Lot number
$: Wafer ID
E: Wettable flank

PACKAGE REFERENCE



QFN-19 (4mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Type(1)	Description
1	TEST	DI	**Test mode pin.** For IC manufacture use only, connect this pin to AGND on PCB.
2	N4	P	**4th cell connection.** Connect a capacitor across cell 4.
3	N3	P	**3rd cell connection.** Connect a capacitor across cell 3.
4	N2	P	**2nd cell connection.** Connect a capacitor across cell 2.
5	N1	P	**1st cell connection.** Connect a capacitor across cell 1.
6	STAT	DO	**Status report.** Open drain output active low. When a read command is received, the IC generates pulses to report IC status.
7	CTRL	DI	**One-wire control input.** Active Low.
8	AGND	P	**Analog ground.** Short AGND to PGND on PCB.
9	VCC	P	**Bias supply.** The VCC pin is a regulated 3.6V output from V+. VCC pin provides power for IC internal circuits and the switching FETs driver. Bypass VCC to AGND with a 1μF ceramic capacitor with shortest trace. DO NOT connect external load on VCC pin.
10	BST	P	**Bootstrap.** Connect a 100nF BST capacitor between BST and SW node.
11,17	MX	P	**Inductor connection.** Connect to power inductor with shortest/widest trace.
12	V+	P	**5th cell connection.** Connect to the top cell of battery stack. Bypass V+ pin with a ceramic capacitor from V+ to PGND. Place the capacitor as close to the IC as possible with shortest/widest trace. This pin is also the power input of the IC. If the cell number is less than 5, short top N# to V+. E.g. If the target batteries are 3 cells, short pin N3, N4 and V+ together.
13	SW	P	**Switching node.** Connect to power inductor with shortest/widest trace.
14	PGND	P	**Power ground.** Connect to PCB ground plane as much as possible.
15	DOWN	DI	**Downstream signal input.** A 1V difference lower than V+ will trigger STAT output active low.
16	UP	DO	**Upstream signal output.** Open drain output to transfer CTRL signal to upper stack.
18	ADDR	AI	**Device address setting pin.** A resistor is connected between this pin and AGND to set the device address.
19	MX	P	**Exposed Pad, inductor connection.** Short Pin 11, Pin 17 and Pin 19 with widest trace on PCB.

Note:

1) AI = Analog Input, AO = Analog Output, AIO = Analog Input Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input Output, P = Power

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ABSOLUTE MAXIMUM RATINGS (2)

V+, DOWN, UP to AGND ..... -0.3V to +40V
SW, N1, N2, N3, N4, MX, CTRL, STAT to AGND ..... -0.3V to +28V
V+ to SW .....-0.3V (-2V for 20ns) to +28V
SW to PGND .....-0.3V (-2V for 20ns) to +28V
N3, N2 to MX ..... -28V to +28V
N4 to MX..... -5V to +28V
N1 to MX..... -28V to +5V
V+ to DOWN..... -0.3V to +5V
BST to SW..... -0.3V to +4V
VCC to AGND..... -0.3V to +4V
All other pins.....-0.3V to VCC+0.3V
Continuous power dissipation (T_A = 25°C) (3) (6)
FCQFN-19 (4mmx4mm) 2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Discharge (ESD) Ratings

Human body model (HBM)……...
VCC - VIN.....Class 1C (4)
Other pins..... Class 2 (4)
Charged device model (CDM).....Class C2b (5)

Recommended Operating Conditions

V_{IN}..... 5V to 24V
$I_{BALANCE}$.....3A
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***
QFN-19 (4mmx4mm) JESD51-5/7 (6)	39.6	2.4	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)- T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per AEC-Q100-002.
5) Per AEC-Q100-011.
6) Measured on JESD51-5,7, 4-layer PCB, where a thermal via array under the exposed pad. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-5,7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.

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ELECTRICAL CHARACTERISTICS

Typical values are at V_{V+} = 20V, V_{CTRL} = 0V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{V+} = 20V, V_{CTRL} = 0V, T_J = -20°C to +125°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Currents						
V+ shutdown supply current	I_{SD_V+}	CTRL = 3V, all cells are 3.3V		2	3.9	µA
V+ quiescent supply current	I_{Q_V+}	CTRL = 0V, all cells are 3.3V, no switching		220	290	µA
N1 shutdown supply current	I_{SD_N4}	CTRL = 3V, all cells are 3.3V	-6	-3.5	-1	µA
N2 shutdown supply current	I_{SD_N3}	CTRL = 3V, all cells are 3.3V	-1	0	1	µA
N3 shutdown supply current	I_{SD_N2}	CTRL = 3V, all cells are 3.3V	-1	0	1	µA
N4 shutdown supply current	I_{SD_N1}	CTRL = 3V, all cells are 3.3V	1	3.5	6.5	µA
On Resistance						
S1 on resistance	R_{ON_S1}			30		mΩ
S2 on resistance	R_{ON_S2}			30		mΩ
S3 on resistance	R_{ON_S3}			30		mΩ
S4 on resistance	R_{ON_S4}			30		mΩ
QH on resistance	R_{ON_QH}			19		mΩ
QL on resistance	R_{ON_QL}			17		mΩ
PWM Converter						
Switching frequency	f_{SW}	ADDR = 0,2,4,6,	380	435	460	kHz
		ADDR = 1,3,5,7,	410	465	500	kHz
Current Regulation						
S1 buck output current regulation	I_{BUCK_S1}	$I_{BALANCE}$ = 1A, V_{N1} > 2.6V, T_J = -20°C to +85°C	0.935	1	1.055	A
		$I_{BALANCE}$ = 2A, V_{N1} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N1} > 2.6V T_J = -20°C to +85°C	2.83	3	3.145	
S2 buck output current regulation	I_{BUCK_S2}	$I_{BALANCE}$ = 1A, V_{N2} > 2.6V T_J = -20°C to +85°C	0.935	1	1.055	A
		$I_{BALANCE}$ = 2A, V_{N2} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N2} > 2.6V T_J = -20°C to +85°C	2.83	3	3.145	
S3 buck output current regulation	I_{BUCK_S3}	$I_{BALANCE}$ = 1A, V_{N3} > 2.6V T_J = -20°C to +85°C	0.935	1	1.055	A
		$I_{BALANCE}$ = 2A, V_{N3} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N3} > 2.6V T_J = -20°C to +85°C	2.83	3	3.145	

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{V+} = 20V, V_{CTRL} = 0V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{V+} = 20V, V_{CTRL} = 0V, T_J = -40°C to +125°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
S4 buck output current regulation	I_{BUCK_S4}	$I_{BALANCE}$ = 1A, V_{N4} > 2.6V T_J = -20°C to +85°C	0.875	1	1.045	A
		$I_{BALANCE}$ = 2A, V_{N4} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N4} > 2.6V T_J = -20°C to +85°C	2.86	3	3.175	
S1 boost input current regulation	I_{BOOST_S1}	$I_{BALANCE}$ = 1A, V_{N1} > 2.6V T_J = -20°C to +85°C	0.935	1	1.055	A
		$I_{BALANCE}$ = 2A, V_{N1} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N1} > 2.6V T_J = -20°C to +85°C	2.83	3	3.145	
S2 boost input current regulation	I_{BOOST_S2}	$I_{BALANCE}$ = 1A, V_{N2} > 2.6V T_J = -20°C to +85°C	0.935	1	1.055	A
		$I_{BALANCE}$ = 2A, V_{N2} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N2} > 2.6V T_J = -20°C to +85°C	2.83	3	3.145	
S3 boost input current regulation	I_{BOOST_S3}	$I_{BALANCE}$ = 1A, V_{N3} > 2.6V T_J = -20°C to +85°C	0.935	1	1.055	A
		$I_{BALANCE}$ = 2A, V_{N3} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N3} > 2.6V T_J = -20°C to +85°C	2.83	3	3.145	
S4 boost input current regulation	I_{BOOST_S4}	$I_{BALANCE}$ = 1A, V_{N4} > 2.6V T_J = -20°C to +85°C	0.935	1	1.055	A
		$I_{BALANCE}$ = 2A, V_{N4} > 2.6V T_J = -20°C to +85°C	1.885	2	2.095	
		$I_{BALANCE}$ = 3A, V_{N4} > 2.6V T_J = -20°C to +85°C	2.83	3	3.145	
CTRL Interface						
Logic high voltage	V_H		1.6			V
Logic low voltage	V_L				1	V
Initialization time (7)	t_{INIT}			250		µs
Shutdown time	t_{OFF}		1.5	2	2.5	ms
Pulse high period	t_{HIGH}		3		22	µs
Pulse low period	t_{LOW}		3		22	µs
Data storage time	t_{STORE}		50			µs

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{V+} = 20V, V_{CTRL} = 0V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{V+} = 20V, V_{CTRL} = 0V, T_J = -40°C to +125°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
STAT, UP, DOWN						
STAT sink current capability	V_{SINK_STAT}	Sink 5mA			0.3	V
STAT pulse frequency	f_{STAT}	10kHz option	9	10	11	kHz
		100kHz option	90	100	110	kHz
UP sink current capability	V_{SINK_UP}	Sink 5mA			0.3	V
DOWN input threshold low	V_{DOWN_L}	Lower than V+	-1.4			V
DOWN input threshold high	V_{DOWN_H}	Lower than V+			-0.7	V
ADDR						
ADDR pin resistance	R_{ADDR}	ADDR=0	0	0	27	kΩ
		ADDR=1	67	72	77	
		ADDR=2	117	122	127	
		ADDR=3	167	172	177	
		ADDR=4	217	222	227	
		ADDR=5	267	272	277	
		ADDR=6	317	322	327	
		ADDR=7	367	NC	NC	
Protection						
V+ over voltage protection	V_{OVP}		24.8	26	27.2	V
V+ over voltage protection hysteresis	V_{OVP_HYS}			1.5		V
Over-Temperature Protection						
Thermal shutdown (7)	T_{SD}	Junction temperature rising		150		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C

Note:

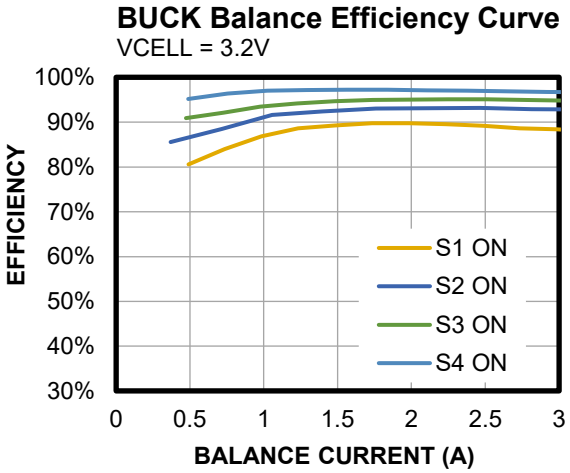
7) Guaranteed by design

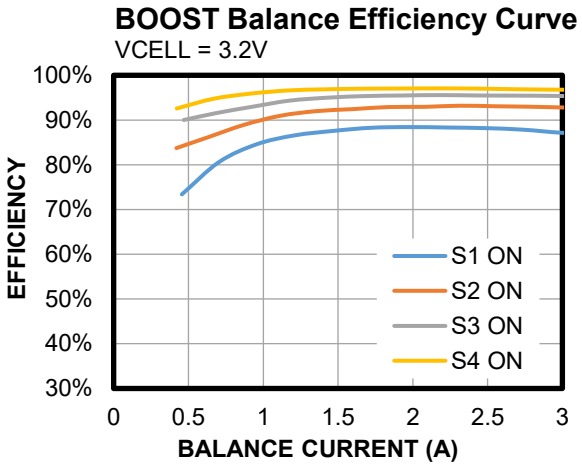
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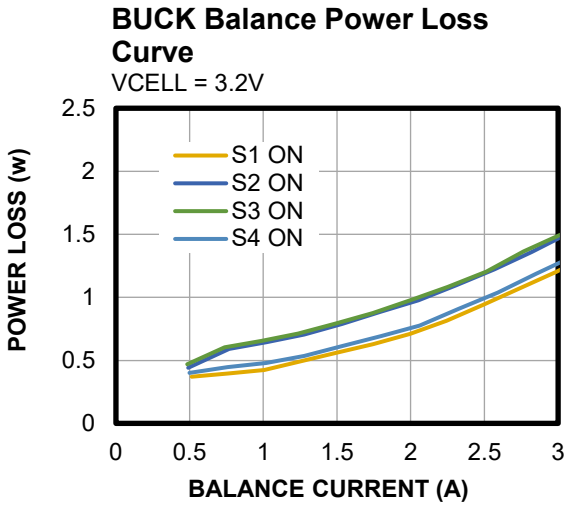
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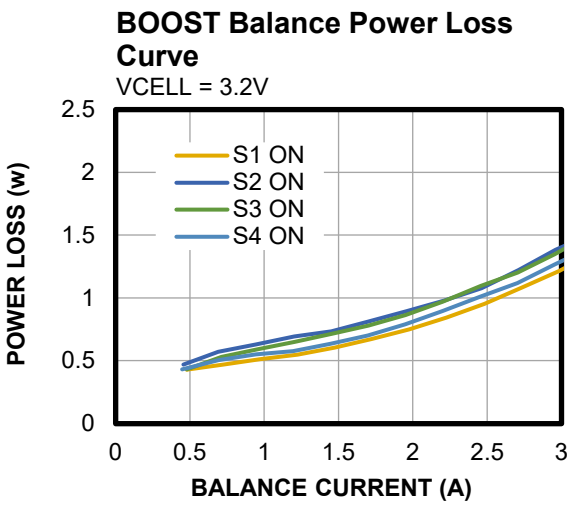
TYPICAL CHARACTERISTICS

T_A = 25°C, V_{CELL} = 3.2V, L = 4.7µH (DCR = 19.5mΩ), $I_{BALANCE}$ = 2A, unless otherwise noted.









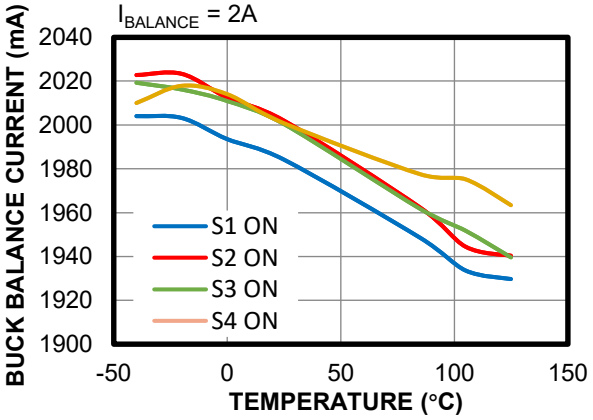
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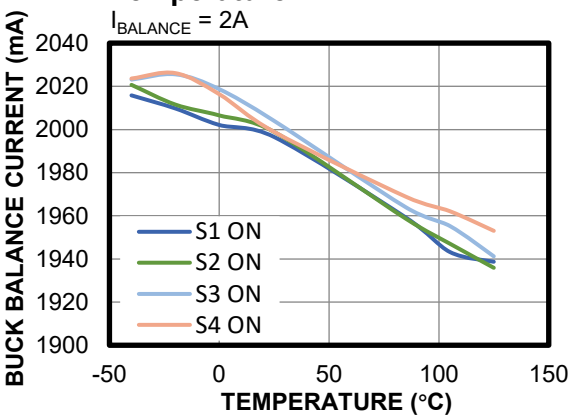
TYPICAL CHARACTERISTICS *(continued)*

V_{V+} = 20V, V_{CTRL} = 0V, T_A = -40°C to +125°C, all voltages with respect to ground, unless otherwise noted.

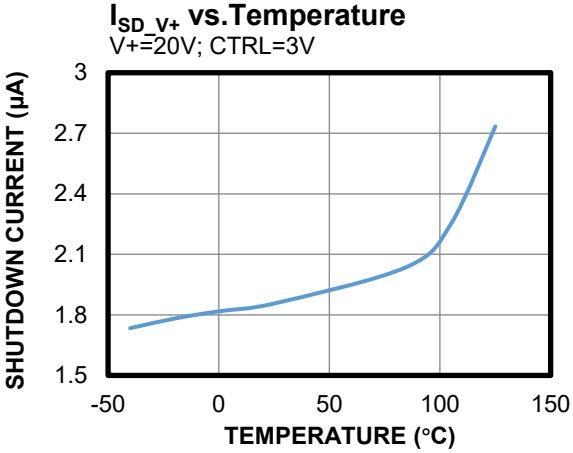
BUCK Balance Current vs. Temperature



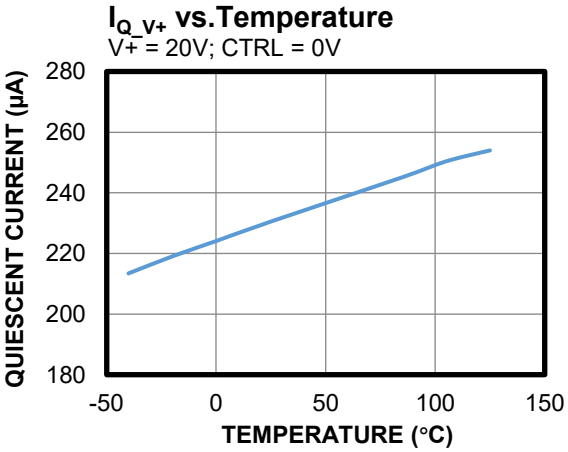
BOOST Balance Current vs. Temperature



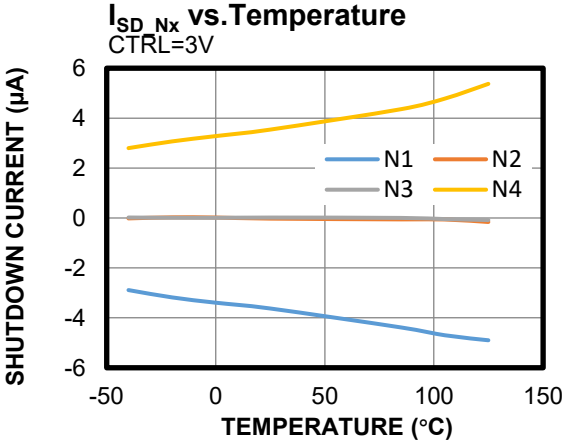
I_{SD_V+} vs.Temperature



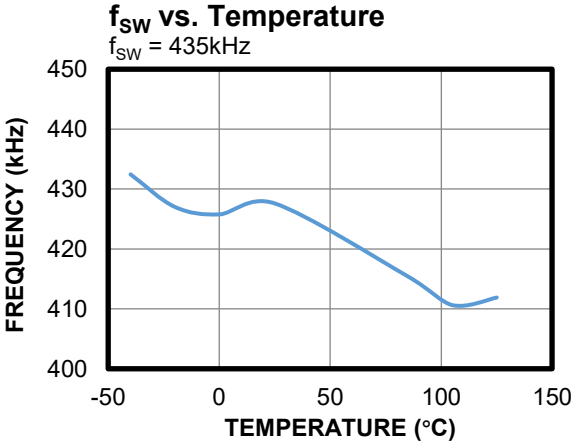
I_{Q_V+} vs.Temperature



I_{SD_Nx} vs.Temperature



f_{SW} vs. Temperature



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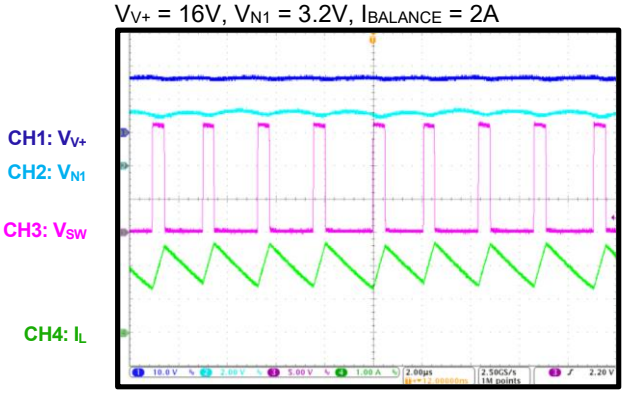
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TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CELL} = 3.2V, L = 4.7µH (DCR = 19.5mΩ), $I_{BALANCE}$ = 2A, unless otherwise noted.

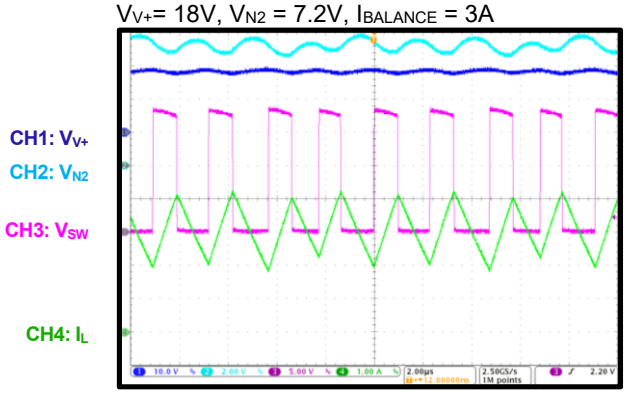
BUCK MODE Steady State when S1 ON

V_{V+} = 16V, V_{N1} = 3.2V, $I_{BALANCE}$ = 2A



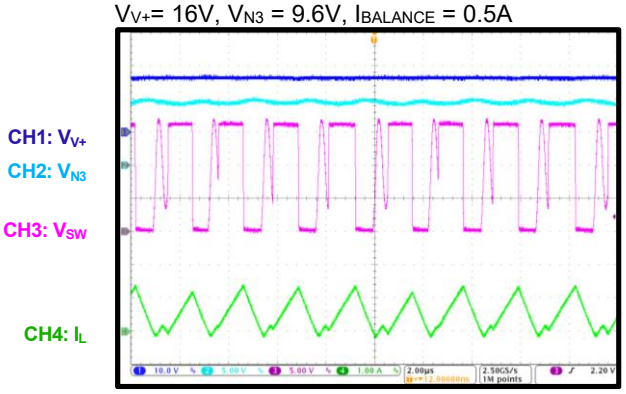
BUCK MODE Steady State when S2 ON

V_{V+}= 18V, V_{N2} = 7.2V, $I_{BALANCE}$ = 3A



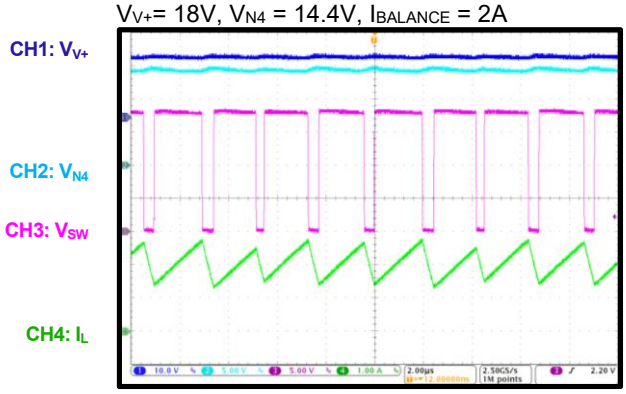
BUCK MODE Steady State when S3 ON

V_{V+}= 16V, V_{N3} = 9.6V, $I_{BALANCE}$ = 0.5A



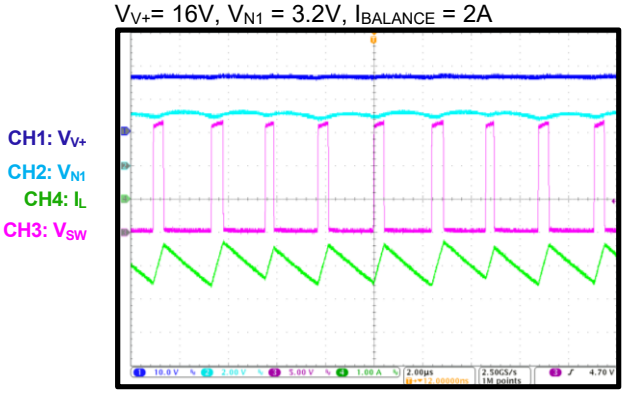
BUCK MODE Steady State when S4 ON

V_{V+}= 18V, V_{N4} = 14.4V, $I_{BALANCE}$ = 2A



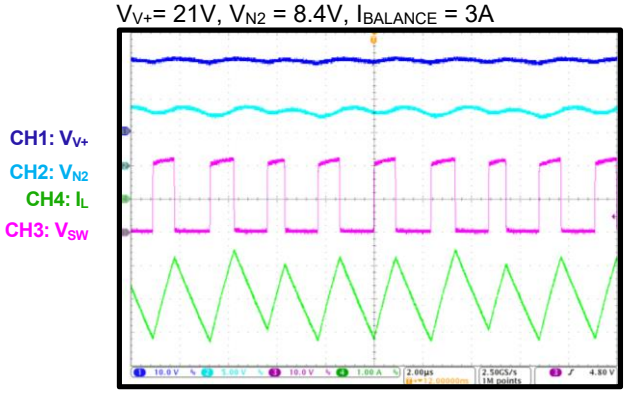
BOOST MODE Steady State when S1 ON

V_{V+}= 16V, V_{N1} = 3.2V, $I_{BALANCE}$ = 2A



BOOST MODE Steady State when S2 ON

V_{V+}= 21V, V_{N2} = 8.4V, $I_{BALANCE}$ = 3A



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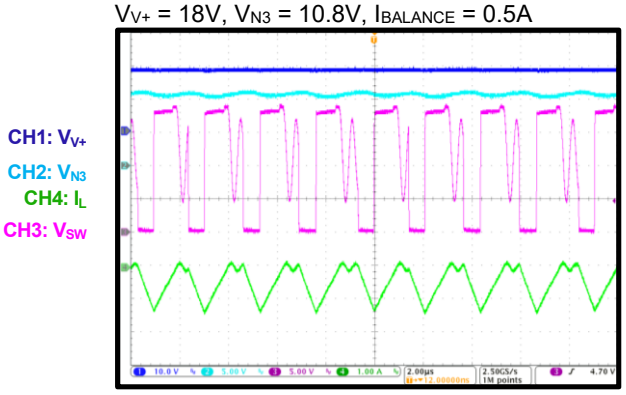
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T_A = 25°C, V_{CELL} = 3.2V, L = 4.7µH (DCR = 19.5mΩ), $I_{BALANCE}$ = 2A, unless otherwise noted.

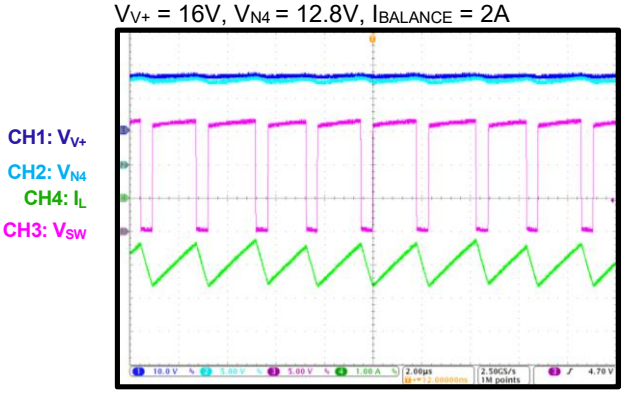
BOOST MODE Steady State when S3 ON

V_{V+} = 18V, V_{N3} = 10.8V, $I_{BALANCE}$ = 0.5A



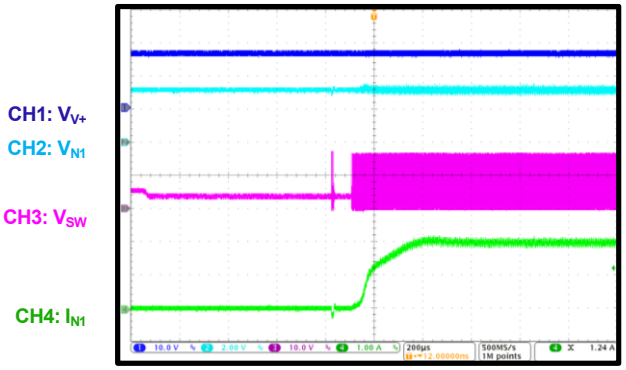
BOOST MODE Steady State when S4 ON

V_{V+} = 16V, V_{N4} = 12.8V, $I_{BALANCE}$ = 2A



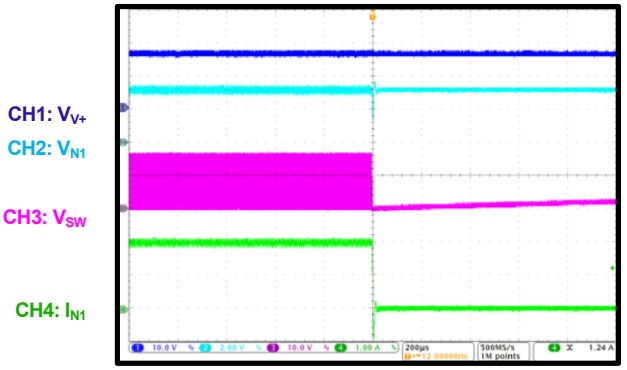
BUCK MODE ON when S1 ON

V_{V+} = 16V, V_{N1} = 3.2V, $I_{BALANCE}$ = 2A



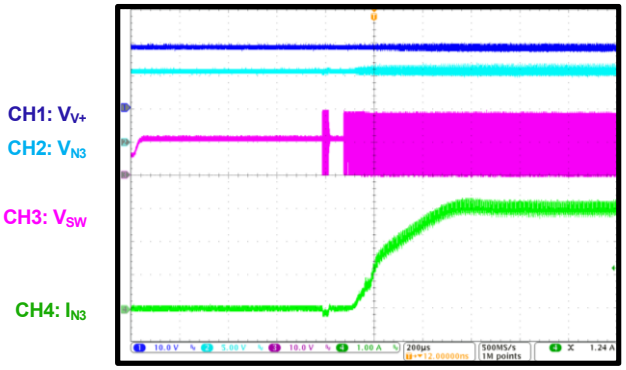
BUCK MODE OFF when S1 ON

V_{V+} = 16V, V_{N1} = 3.2V, $I_{BALANCE}$ = 2A



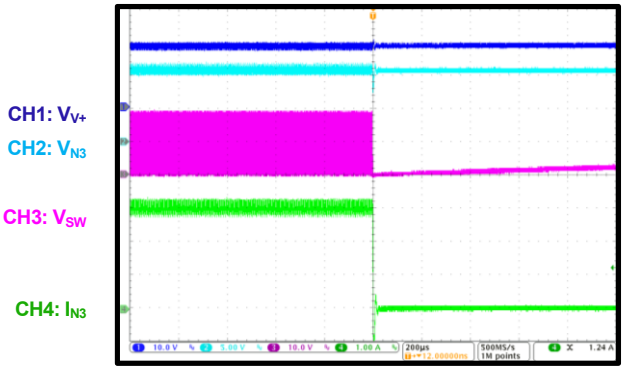
BUCK MODE ON when S3 ON

V_{V+} = 18V, V_{N3} = 10.8V, $I_{BALANCE}$ = 3A



BUCK MODE OFF when S3 ON

V_{V+} = 18V, V_{N3} = 10.8V, $I_{BALANCE}$ = 3A



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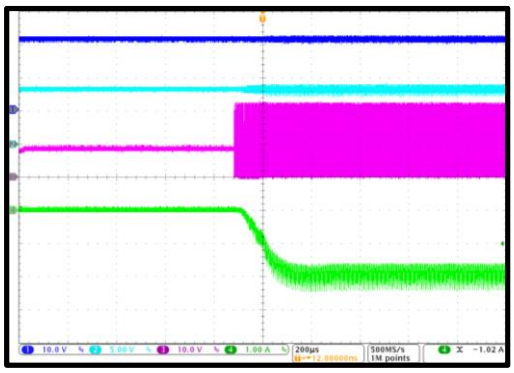
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T_A = 25°C, V_{CELL} = 3.2V, L = 4.7µH (DCR = 19.5mΩ), $I_{BALANCE}$ = 2A, unless otherwise noted.

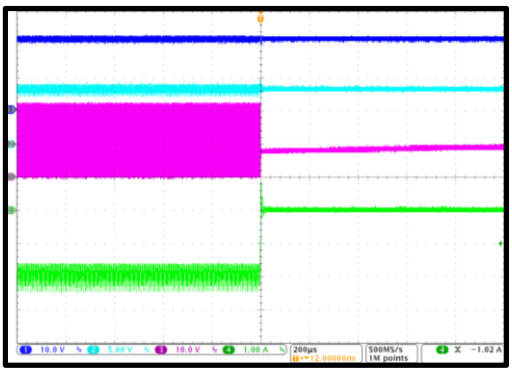
BOOST MODE ON when S2 ON

V_{V+} = 21V, V_{N2} = 8.4V, $I_{BALANCE}$ = 2A



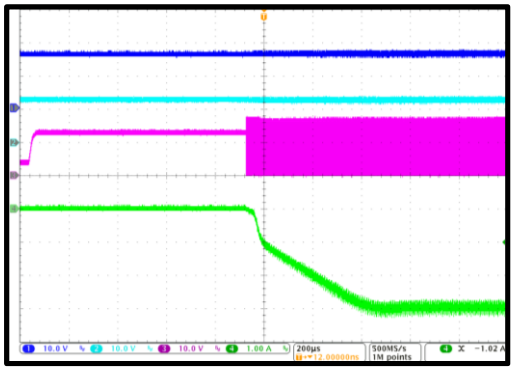
BOOST MODE OFF when S2 ON

V_{V+} = 21V, V_{N2} = 8.4V, $I_{BALANCE}$ = 2A



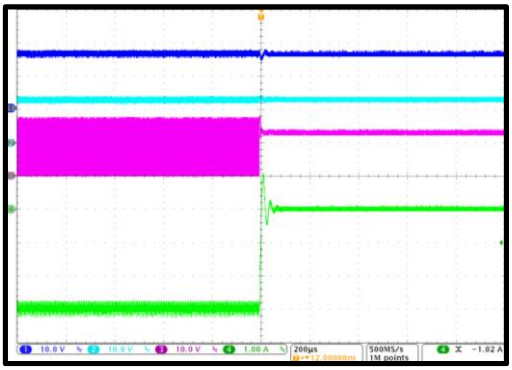
BOOST MODE ON when S4 ON

V_{V+}= 16V, V_{N4} = 12.8V, $I_{BALANCE}$ = 3A



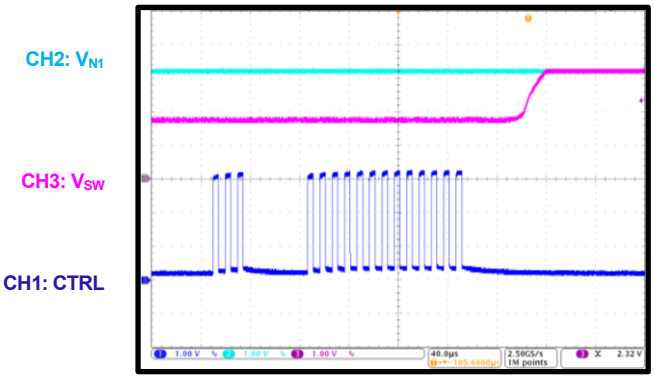
BOOST MODE OFF when S4 ON

V_{V+}= 16V, V_{N4} = 12.8V, $I_{BALANCE}$ = 3A



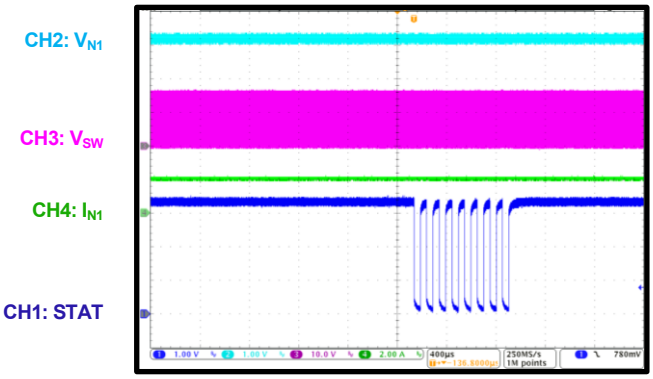
CTRL Command Test

V_{N1} = 3.2V, Write addr0(3) and S1 ON (13) command.



STAT Test

S1 ON, BUCK Mode, Read Status



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FUNCTIONAL BLOCK DIAGRAM

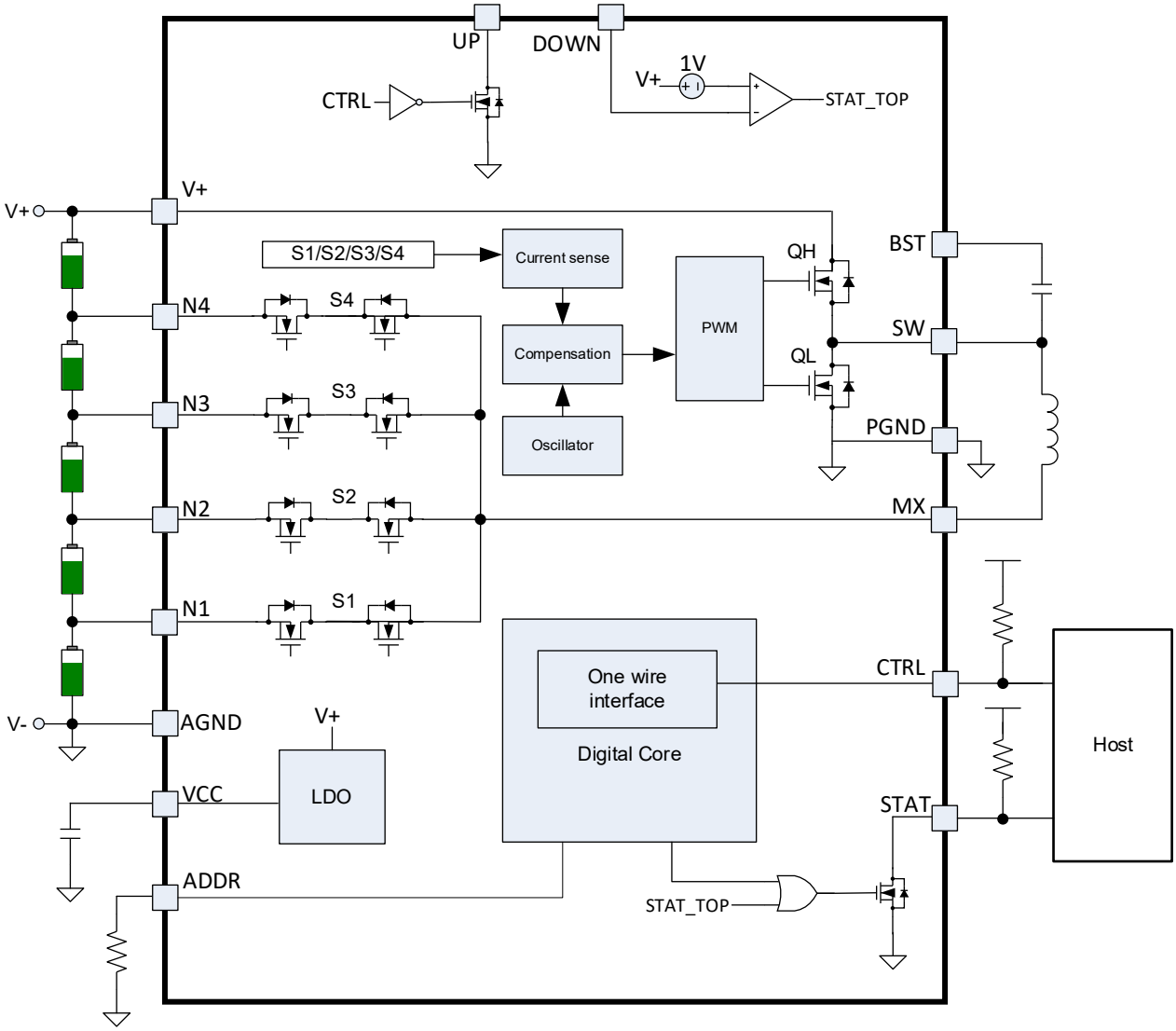


Figure 1: Functional Block Diagram

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OPERATION

Overview

To maximize useful pack capacity and life, series-cells must be kept within a constrained state-of-charge (SOC) range as they are charged and discharged. This is accomplished by balancing each individual cell, typically via passive balancing where charge is removed via a resistive load across each cell.

The MP2645A offers an alternative to passive balancing using a highly efficient charge transfer between cells. This allows for faster balancing, less heat generation, improved energy efficiency, and increased system runtime.

Each MP2645A supports balancing for 2 to 5 series cells with a small footprint.

A host controls and configures the MP2645A through 1-wire interface (CTRL pin). Referring to Figure 1, the switching FETs (QH and QL) provide the basis for the regulated buck or boost action. A host command sets the current direction (BUCK or BOOST) and current is transferred among the 5 cell group by controlling the four switches, S1-S4.

Figure 2 describes a simple balancing algorithm for a single MP2645A. Figure 3 shows a typical result using this algorithm when balancing 5-cells.

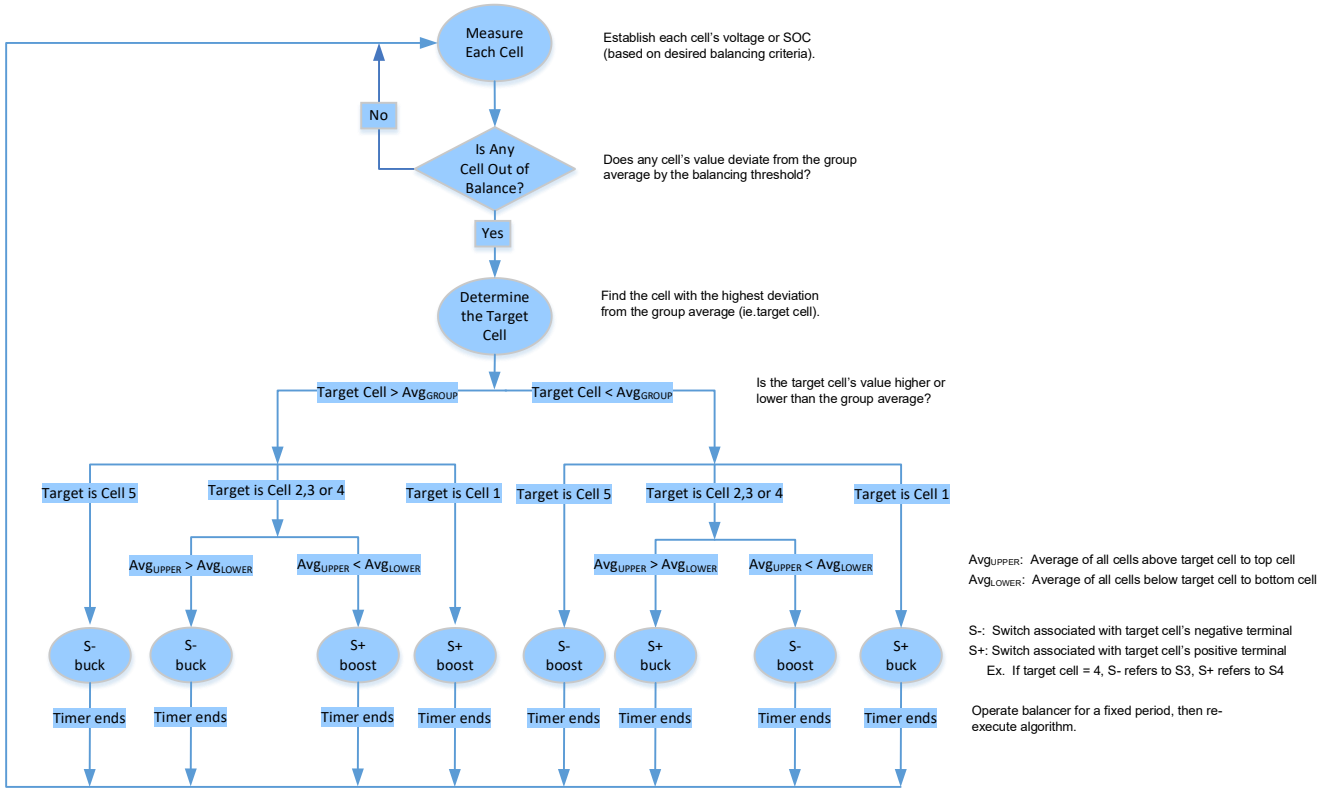


Figure 2: Balance Flowchart Example

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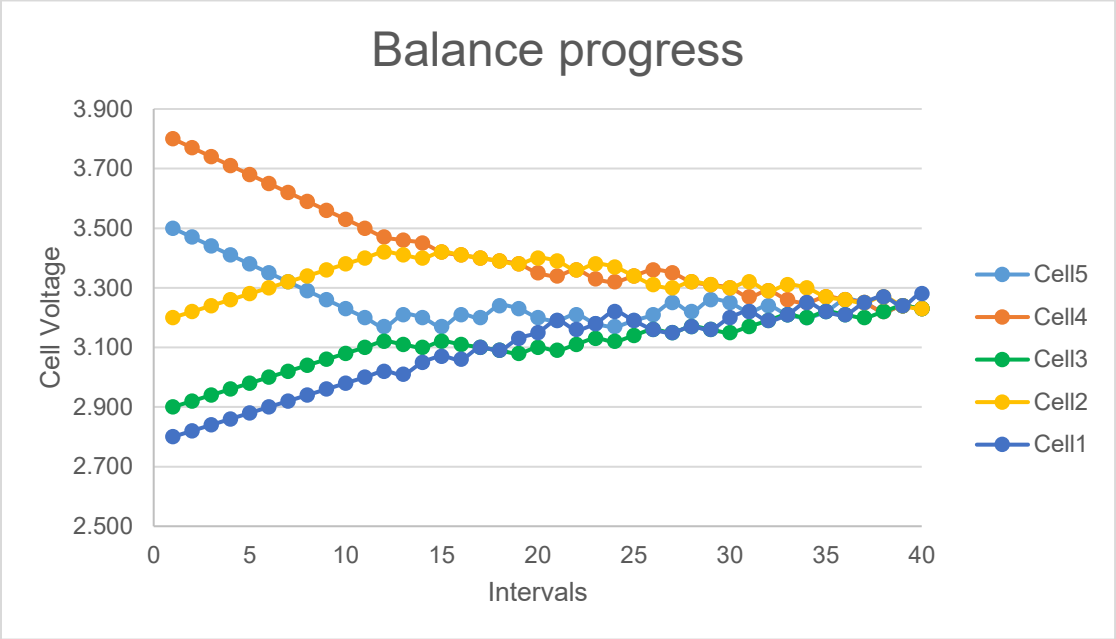


Figure 3: Balance Progress Example

Multi Group Balancing

Systems with more than 5 cells require multiple MP2645A, where the cells for each MP2645A will overlap with its adjacent MP2645A. This allows a string of MP2645A to transfer energy across the entire pack. Using the proposed balancing algorithm described in Figure 2, where each MP2645A operates independently, will achieve a balanced state. However, balancing across multiple MP2645A can be optimized with an additional algorithm that utilizes the overlapping cell(s).

Figure 4 provides an example, where 9-cells are covered by 2 MP2645A that share cell 5. If the group 1 and group 2 values (SOC or V) are imbalanced, balancing time can be reduced with the following strategy:

If $Avg_{GROUP1} > Avg_{GROUP2}$

Group1: turn on S4 + boost

Group2: turn on S1 + boost

If $Avg_{GROUP1} < Avg_{GROUP2}$

Group1: turn on S4 + buck

Group2: turn on S1 + buck

Figure 5 describes this "inter-group" balancing algorithm when there is one shared cell between adjacent MP2645A.

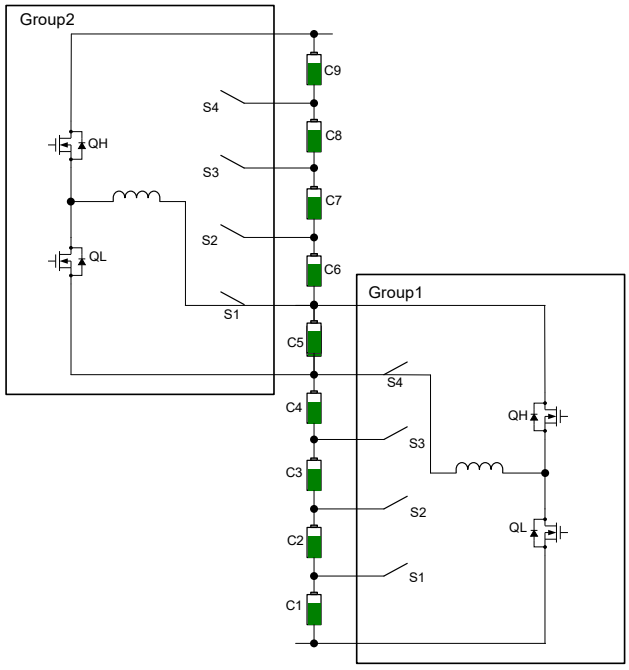


Figure 4: Balance Among Groups

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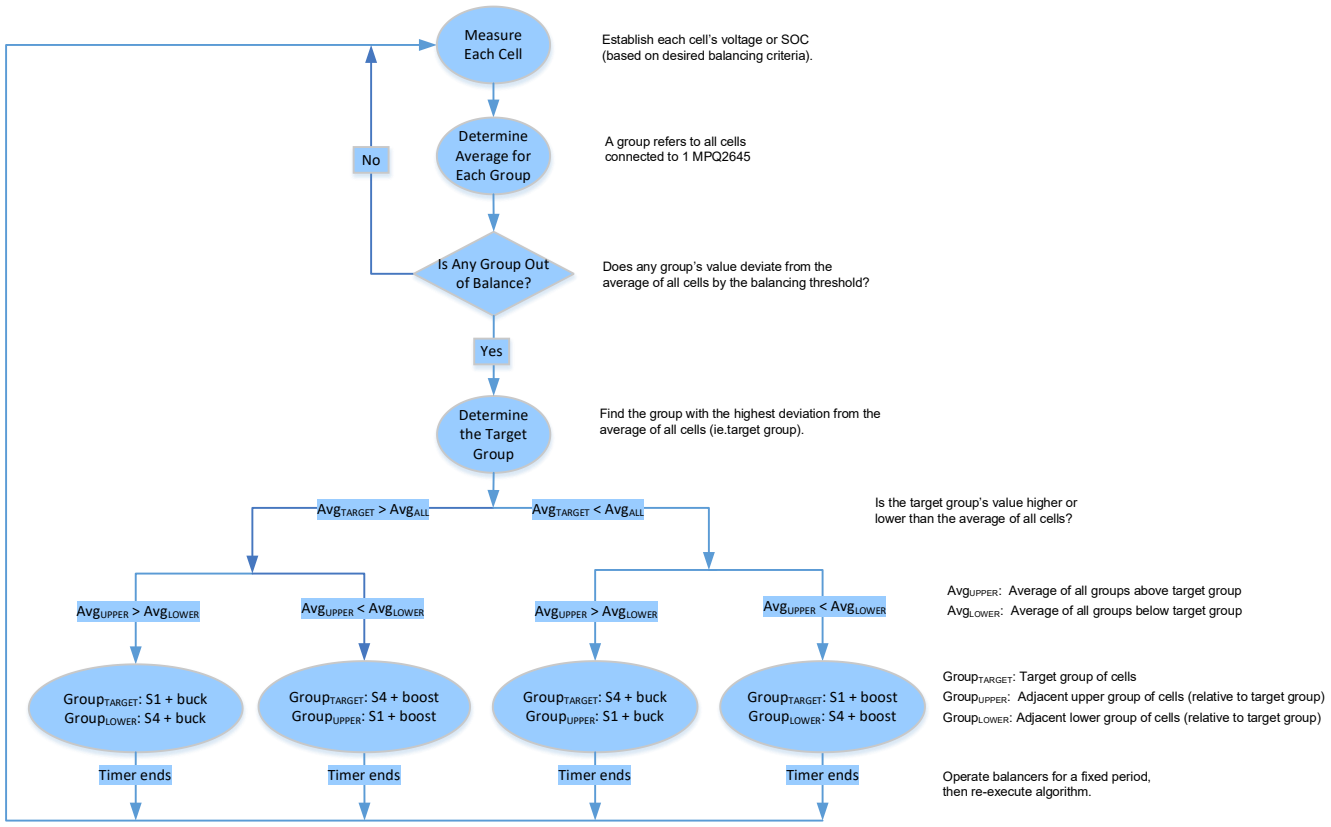


Figure 5: Balance Flowchart among Groups Example

Address Setting

The MP2645A supports operation for up to 8 stacked devices (up to 33 cells with 1 overlap cell between each MP2645A). They can be operated from one control input signal from the host.

To target commands to a specific MP2645A in a stack, each MP2645A is configured with an address, using the ADDR pin. The ADDR pin sources a 5uA zero-temperature coefficient current. A single resistor from ADDR to ground is used to set 1 of 8 addresses.

Single Wire Interface

The device is controlled from a single wire interface on the CTRL pin.

When the CTRL pin is kept logic high, the device is in sleep mode with minimum quiescent current consumption.

The device will wake up when the CTRL pin is pulled low and will be ready to accept commands after the initialization time, t_{INIT}. The host then sends commands by driving a sequence of pulses on the CTRL pin. The address and commands are based on the number of pulses sent. See Table 1 for the ADDR and COMMAND list.

These simple pulse trains always start and end with logic low, and a wide range of pulse lengths are acceptable (see CTRL Interface specifications). Short pulses, as specified by the minimum t_{LOW} and t_{HIGH}, will be ignored. Long pulses, as specified by the maximum t_{LOW} and t_{HIGH}, will reset the device's pulse counter.

Table 1 lists the pulse sequences for MP2645A control. The pulse format for CTRL signals is ADDR-N followed by COMMAND-N.

The MP2645A offers one broadcast command, pulse#2, that will disable all active balancers in the chain. As a broadcast command, an address is not required for this command. i.e. the "broadcast off" is pulse #2 and executed as 0->1->0->1->0.

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After sending the command, the host must hold the CTRL pin low for longer than tSTORE. The MP2645A will then recognize the pulse number and execute the associated command.

Bringing the CTRL pin high will place the MP2645A into sleep mode to reduce power.

Commands can be placed in sequence with the CTRL pin staying low between commands. Bringing the CTRL pin high will place the MP2645A into sleep mode to reduce power.

Figure 6 depicts the CTRL pin timing requirements. Figure 7 shows an effective command sequence.

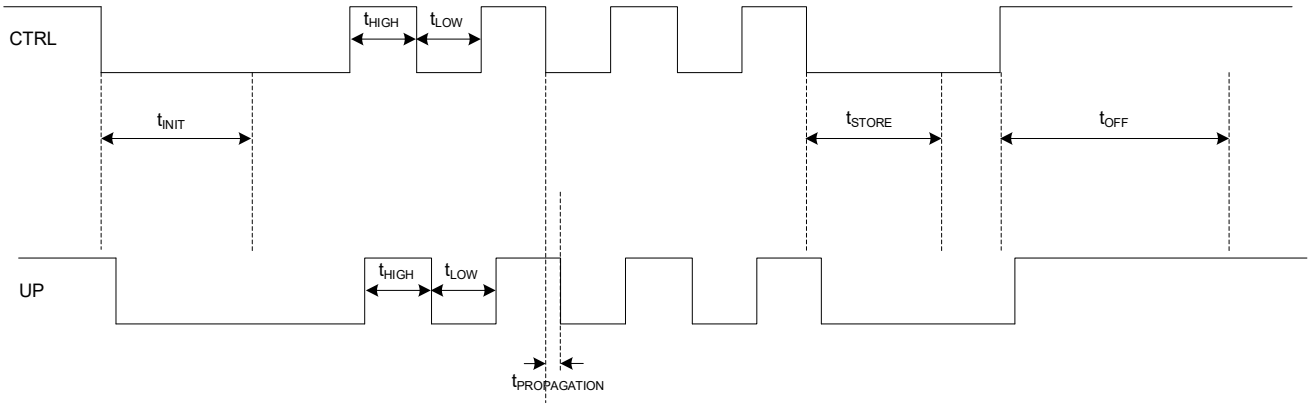


Figure 6: CTRL Input Timing Requirement

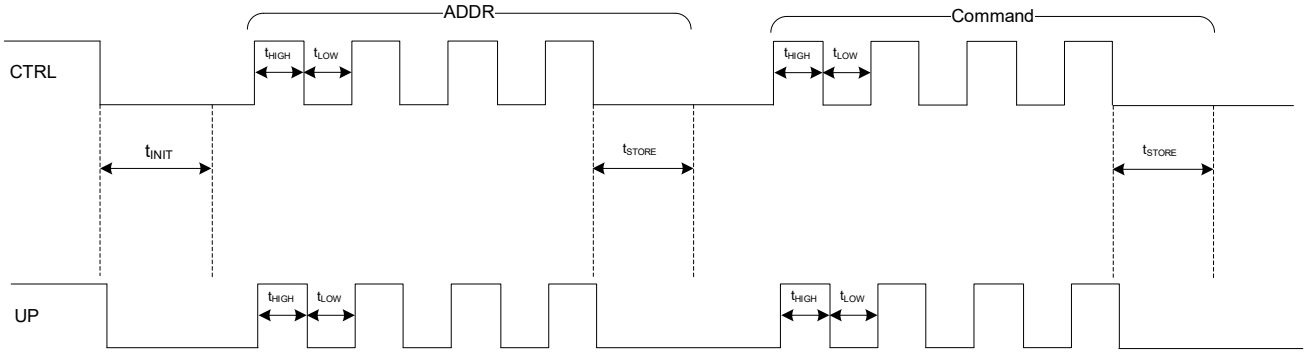


Figure 7: Effective Command Format

STAT Output

The MP2645A provides a status signal which is activated by a READ_STATUS command. When a READ_STATUS command is received, the part will generate a pulse train on the STAT pin that represents the device status. The status signal is a 50% duty cycle, 10kHz pulse train. That status signal can also be configured for 100kHz operation via OTP. Contact MPS for custom OTP settings. By counting the pulse numbers, the host can acknowledge the working status of each MP2645A.

Table 2 provides the STAT results.

Stacked Operation (UP and DOWN pins)

To transfer the CTRL command to the devices in the stack, MP2645A uses a 2-wire stackable interface as shown in Figure 8.

The MP2645A uses the UP pin to transfer the CTRL pin input signal to the upper device. When the CTRL pin input is pulled logic low, the UP pin output is also pulled low with a minimum propagation delay to drive the upper device's CTRL pin. Thus, UP pin copies the CTRL pin signal and transfers to the upper device one by one.

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The MP2645A uses the DOWN pin to transfer the STAT pin output signal to the lower device. The DOWN pin is driven by the upper device's STAT output. For the lower device, when the DOWN pin is seen lower than its V+ pin for a threshold, the lower device will "OR" the signal to its STAT pin output. Thus, DOWN pin copies the upper devices' STAT pin signal and transfers to the lower devices one by one.

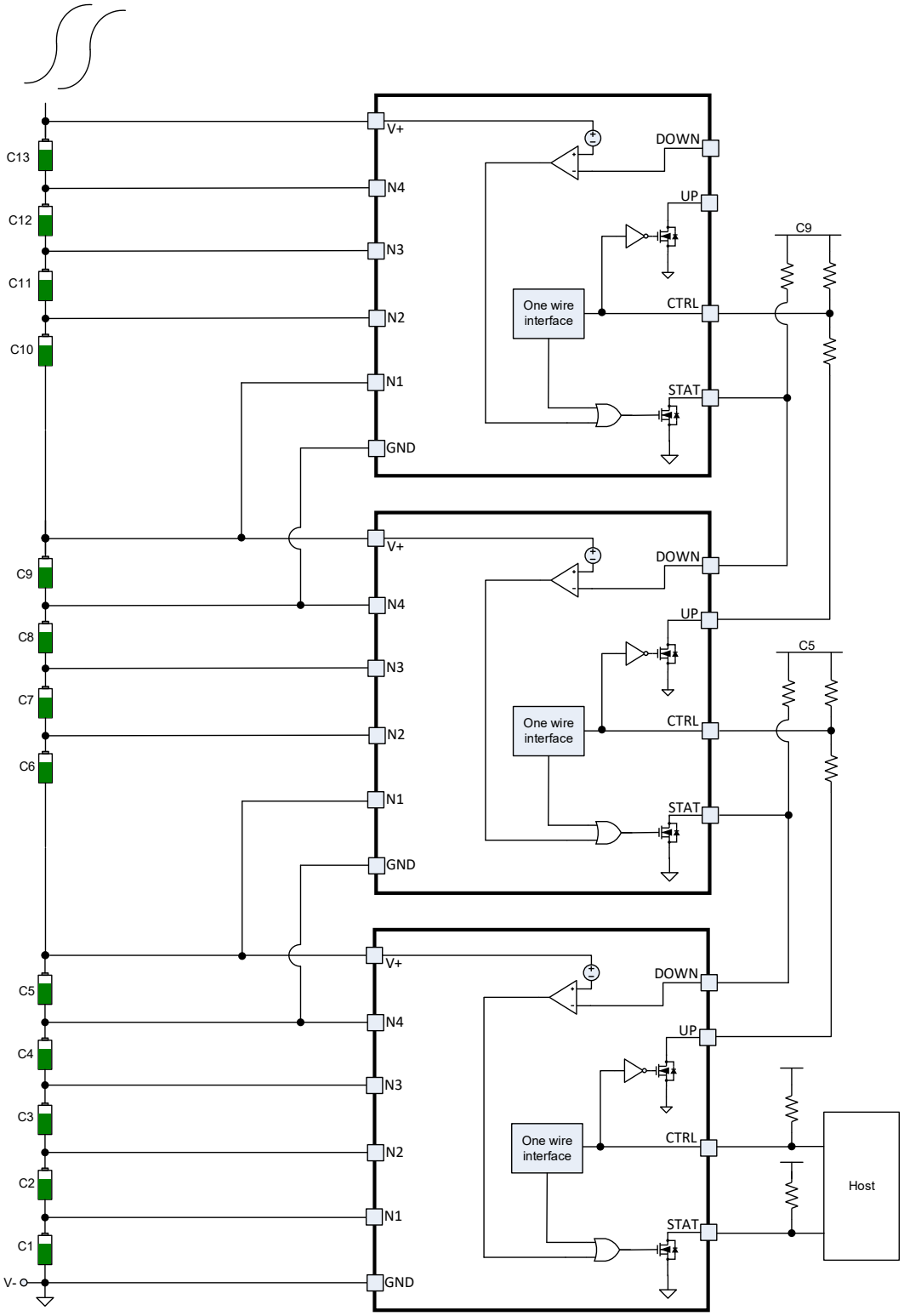


Figure 8: Stack Communication

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Watchdog Timeout

To confirm proper host communication, the MP2645A integrates a watchdog timer. In the event of a watchdog time-out, the MP2645A will automatically terminate any balancing operation.

By default, the watchdog timer is factory programmed to enabled with 40sec. Contact MPS for setting watchdog timer default enabled/disabled.

Any pulse on CTRL pin will reset the watchdog timer.

Over Voltage Protection

The MP2645A has built in over voltage protection (OVP) with a fix threshold of 26V. When V+ pin is higher than this OVP threshold, the switcher stops immediately.

After an OVP event, the host needs to re-start the MP2645A by sending a new command.

Thermal Shutdown Protection

The MP2645A has built in thermal shutdown protection (TSD) with a fix threshold of 150°C. When the device die temperature reaches the TSD threshold, the switcher stops immediately.

After a TSD event, the host needs to re-start the MP2645A by sending a new command to make the device resume action.

Command Repeating

The MP2645A has command redundancy for communication noise immunity. Once enabled, the address command and/or action command must be repeated twice to be an effective phrase. Contact MPS for parts with command repeating enabled.

Frequency Dither Function

The MP2645A supports frequency dither function for further improve the EMI performance. The dither function can be enabled/disabled by one-time-programming (OTP) in factory. Once dither function is enabled, the frequency dithers with +/-10% range.

One Time Programming

The MP2645A has one-time-programming (OTP) capability to configure the default setup of some functions and parameters. Please refer to table 3 for the OTP map and default values. Contact MPS for custom OTP configurations.

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Table 1: CTRL Configuration Table

Pulse #	Function	Command	Description
1	Empty	N/A	No function
2	Command-2	BROADCAST_OFF	Turn OFF everything. No address is needed
3	ADDR-0	Device 0 Address	Specific device address per each device's ADDR pin configuration. To address a specific device, host needs to send ADDR-N, followed by COMMAND-N
4	ADDR-1	Device 1 Address	
5	ADDR-2	Device 2 Address	
6	ADDR-3	Device 3 Address	
7	ADDR-4	Device 4 Address	
8	ADDR-5	Device 5 Address	
9	ADDR-6	Device 6 Address	
10	ADDR-7	Device 7 Address	
11	COMMAND-11	READ_STATUS	Initiate status pulses from addressed device (via STAT pin).
12	COMMAND-12	SN OFF	Turn OFF command for SN SN OFF also set BUCK_BOOST_OFF
13	COMMAND-13	S1 ON	Turn ON command for SN
14	COMMAND-14	S2 ON	
15	COMMAND-15	S3 ON	
16	COMMAND-16	S4 ON	
17	COMMAND-17	BUCK_BOOST_OFF	Turn OFF command for converter
18	COMMAND-18	BUCK_ON	Turn ON command for buck converter
19	COMMAND-19	BOOST_ON	Turn ON command for boost converter
20	COMMAND-20	BROADCAST_RESUME	This command resumes the balance operation before last BROADCAST_OFF command. No address is needed for this command.
21	COMMAND-21	0.5A Balance Current	Balance current regulation setting Range: 0.5A – 4A Step: 0.25A Offset: 0.5A Default: 2A (b'0110, OTP)
22	COMMAND-22	0.75A Balance Current	
23	COMMAND-23	1A Balance Current	
24	COMMAND-24	1.25A Balance Current	
25	COMMAND-25	1.5A Balance Current	
26	COMMAND-26	1.75A Balance Current	
27	COMMAND-27	2A Balance Current	
28	COMMAND-28	2.25A Balance Current	
29	COMMAND-29	2.5A Balance Current	
30	COMMAND-30	2.75A Balance Current	
31	COMMAND-31	3A Balance Current	
32-35	Empty	N/A	No function
36	COMMAND-36	Watchdog ON	Turn ON watchdog (Configurable via OTP)
37	COMMAND-37	Watchdog OFF	Turn OFF watchdog (Configurable via OTP)

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Table 2: STAT output Table

Pulse #	Status
1	Empty
2	Empty
3	Device is alive, idle
4	S1 is turned on, idle
5	S2 is turned on, idle
6	S3 is turned on, idle
7	S4 is turned on, idle
8	S1 is turned on, buck is operating
9	S2 is turned on, buck is operating
10	S3 is turned on, buck is operating
11	S4 is turned on, buck is operating
12	S1 is turned on, boost is operating
13	S2 is turned on, boost is operating
14	S3 is turned on, boost is operating
15	S4 is turned on, boost is operating
16	Empty
17	V+ OVP

Table 3: OTP Table

OTP Items	Description	MP2645A-0000	MP2645A-0001
DITHER_EN	1: Frequency dither is on 0: Frequency dither is off	0	1
ADDR_CNT	1: Repeating address pulse twice to initiate one-wire communication 0: Repeating address pulse once to initiate one-wire communication	0	0
DATA_CNT	1: Repeating data pulse twice to initiate one-wire communication 0: Repeating data pulse once to initiate one-wire communication	0	0
PULSE_WIDTH	1: Effective pulse width among 20μs~250μs 0: Effective pulse width among 3μs ~22μs	0	0
T_STORE	1: 300μs 0: 30μs	0	0
WTD_EN	1: Enable watchdog 0: Disable watchdog	1	1
STAT_CTRL	1: STAT frequency 100kHz 0: STAT frequency 10kHz	0	0
I_BALANCE[3:0]	Balance current regulation setting Range: 0.5A – 4A Step: 0.25A Offset: 0.5A Default: 2A (b'0110)	0110	0110

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TYPICAL APPLICATION CIRCUITS

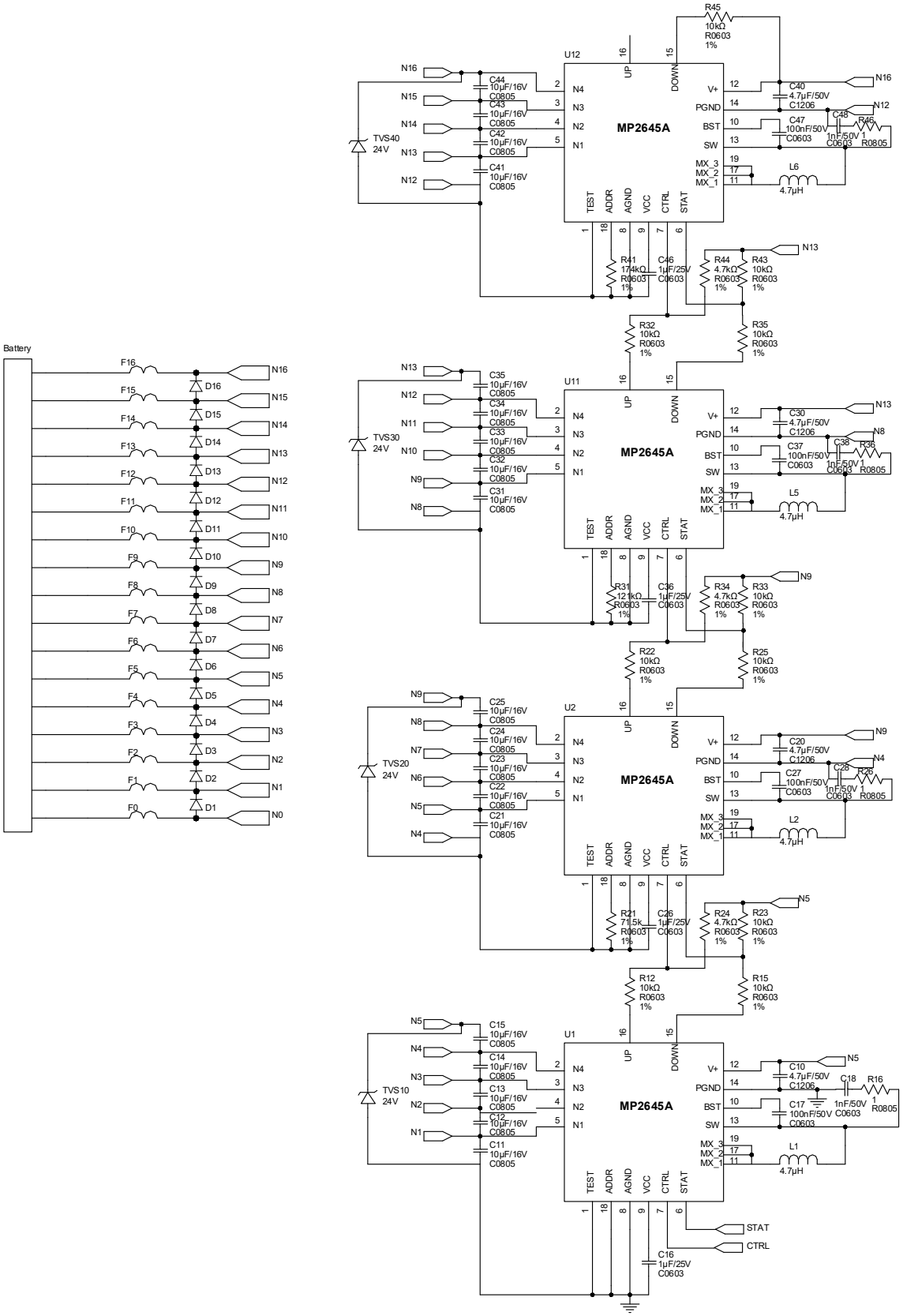


Figure 9: Typical Application Circuit for 16 Cells

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Table 4: The Key BOM of Figure 9

Qty	Ref	Value	Description	Package	Manufacturer
4	C10, C20, C30, C40	4.7μF	Ceramic Capacitor; 50V; X7R	1206	Any
19	C11, C12, C13, C14, C15, C21, C22, C23, C24, C25, C31, C32, C33, C34, C35, C41, C42, C43, C44	10μF	Ceramic Capacitor; 16V; X7R	0805	Any
4	C16, C26, C36, C46	1μF	Ceramic Capacitor; 25V; X7R	0603	Any
4	C17, C27, C37, C47	100nF	Ceramic Capacitor; 25V; X7R	0603	Any
4	C18, C28, C38, C48	1nF	Ceramic Capacitor; 50V; C0G	0603	Any
10	R12, R22, R32, R23, R33, R43, R15, R25, R35, R45	10kΩ	Film Resistor; 5%	0603	Any
1	R21	71.5kΩ	Film Resistor; 1%	0603	Any
1	R31	121kΩ	Film Resistor; 1%	0603	Any
1	R41	174kΩ	Film Resistor; 1%	0603	Any
3	R24, R34, R44	4.7kΩ	Film Resistor; 5%	0603	Any
4	R16, R26, R36, R46	1Ω	Film Resistor; 1%	0805	Any
4	L1, L2, L3, L4	4.7μH	Inductor; 6A	Any	Any
4	TVS10, TVS20, TVS30, TVS40	24V	TVS Diode	SMA	Any
16	D1-D16	1A/40V	Diode	SMA	Any

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APPLICATION INFORMATION

Selecting the inductor

A 4.7μH (+/-20%) inductor is required for proper operation. The inductor saturation current should be above 5A.

Selecting the V+ capacitor

The V+ capacitance decouples the switching converter and absorbs the switching ripple current. The minimum capacitance required is 2.2μF, and a 4.7μF capacitor is recommended. The capacitors should be with good temperature characteristic and 50V rating.

Selecting the N1-N4 capacitor

The 5 capacitors at N1-N4 nodes are the converter output capacitors. The minimum capacitance required is 2.2μF, and 10μF capacitors are recommended. The capacitors should be with good temperature characteristics and >=16V rating.

Selecting the snubber

A snubber is must required at the switching node for proper operation. The recommended snubber value is 1nF/1Ω. Please note that the 1Ω snubber resistor should be with 0805 size package.

Configuring the UP pin

A resistor divider (R_{UP_H} and R_{UP_L}) transfers the UP pin signal to the upper device. R_{UP_L} is recommended as 10kΩ fixed, while R_{UP_H} needs to be adjusted in real application, refer to Figure 10.

1. Make sure that the resistor divider is pulled up to a sufficient voltage rail. When U1's UP pin is off (high Z), U2's CTRL pin is pulled up by R_{UP_H} to C5+. Since U2's GND pin is connected to C4+, there is one cell voltage on U2's CTRL pin. It should be guaranteed that this one cell voltage is higher than CTRL pin's logic high voltage threshold (considering cable voltage drop). E.g. if the application needs to support a low voltage cell, the pull up rail of the divider can be connected higher to C6+ for sufficient pull up voltage.
2. Adjust R_{UP_H} to make sure the low level of U2's CTRL pin is lower than U2' AGND (on C4+). With the configuration in figure 10, assume every battery cell has same voltage, U2's CTRL pin low level is at $V_{CTRL_L} = 5 \times V_{CELL} \times \frac{R_{UP_L}}{R_{UP_H}+R_{UP_L}}$, where V_{CELL} is the battery cell voltage. The V_{CTRL_L} should be sufficiently lower than C4+($4 \times V_{CELL}$), and some headroom should be reserved considering battery voltage variations and cable voltage drop.

Configuring the DOWN pin

A pair of resistors (R_{DOWN_H} and R_{DOWN_L}) transfers the DOWN pin signal from the upper device to the lower device. Both R_{DOWN_H} and R_{DOWN_L} are recommended as 10kΩ fixed.

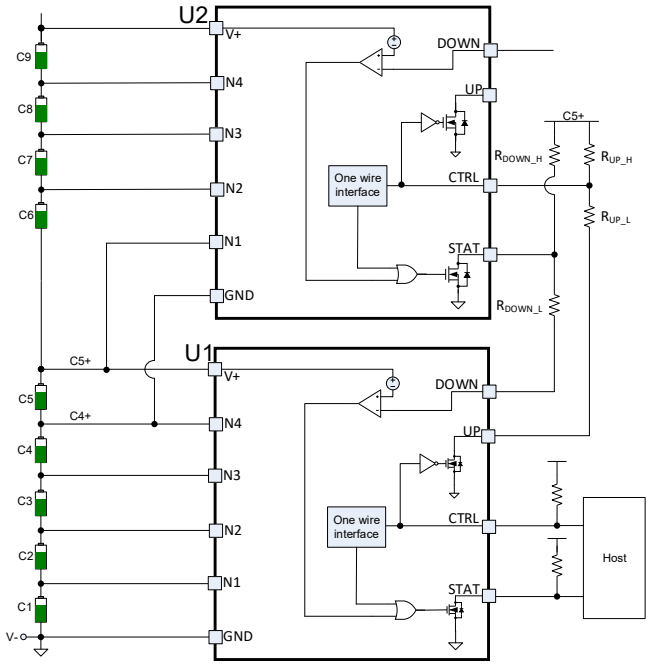


Figure 10: UP and DOWN Pin Resistors

PCB layout Guide

PCB layout is important to meet specified noise, efficiency, and stability requirements. For the best results, refer to the guidelines below:

1. Place the V+ capacitor on the same layer as the IC and right close to the IC. Use short and wide copper plane. The PGND trace should be the widest.
2. Place vias as many as possible right close to PGND pin to the ground plane. The PGND to ground plane parasitic impedance must be minimized.

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3. The right side of IC is crowded, below things should be prioritized in sequence.
    a. PGND trace must be as widest as possible.
    b. V+ trace is secondly wide.
    c. SW trace is thirdly wide. SW trace can be beneath the V+ capacitor.
    d. MX trace current is not high, narrower is fine.
4. The snubber capacitor resistor should also on the same layer of IC, and they should have a short and wide copper connection between PGND (V+ capacitor ground node) and SW node.
5. Connect AGND pin to the ground plane with a via. Also the VCC capacitor should be close to the IC.
6. Connect the IC's pins to as many copper planes as possible to conduct heat away from the IC.
7. It is recommended with a 4 layers board with outside layer 2Oz and inside layer 1Oz copper thickness.
8. Ensure that the number and physical size of the vias is sufficient for a current path.

Figure 11 shows a high-frequency current path. In this figure, the high-frequency path (the high-side MOSFET, low-side MOSFET and the V+ capacitor) must be minimized.

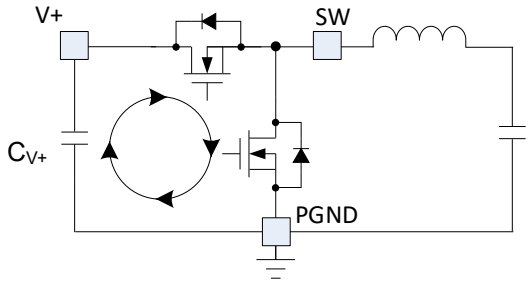


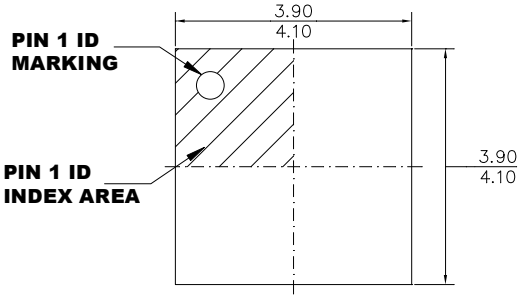
Figure 11: High Frequency Current Path

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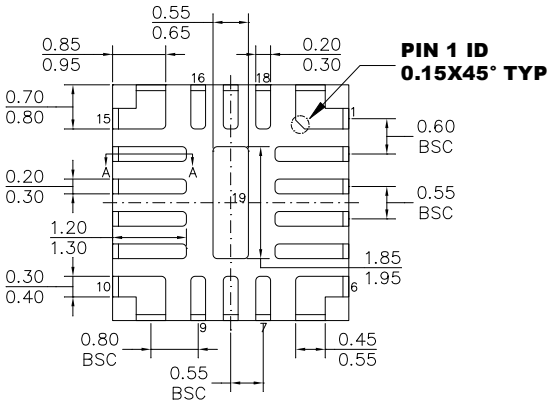
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PACKAGE INFORMATION

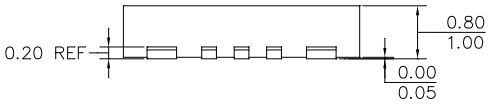
QFN-19 (4mmx4mm)



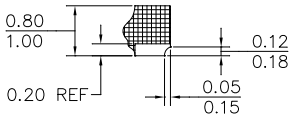
TOP VIEW



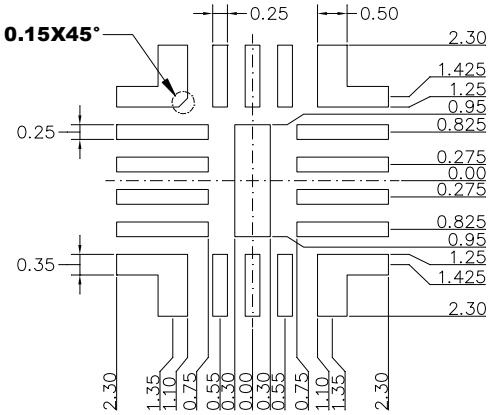
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

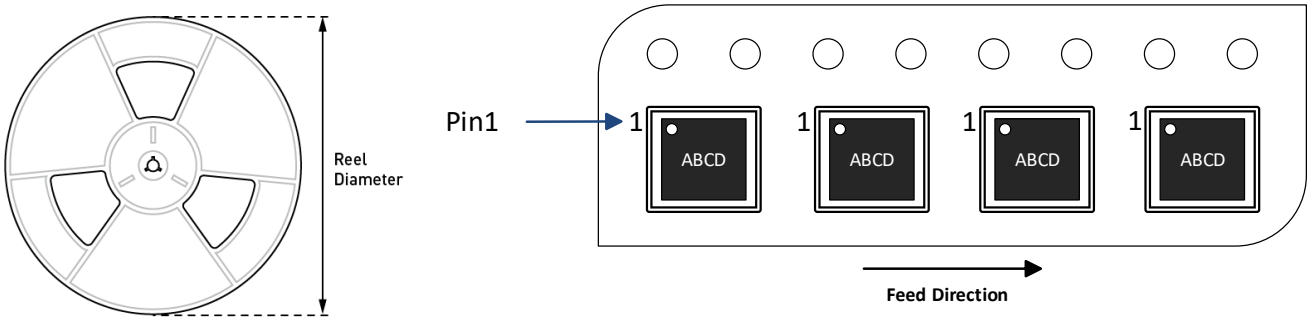
NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2645AGRE-xxxx-Z	QFN-19 (4mmx4mm)	5000	N/A	N/A	13in.	12mm	8mm

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