

Description:

This N+P Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.

Features:

N-Channel: $V_{DS}=40V, I_D=40A, R_{DS(on)} < 6m\Omega @ V_{GS}=10V$ (Typ: $5m\Omega$)

P-Channel: $V_{DS}=-40V, I_D=-40A, R_{DS(on)} < 13m\Omega @ V_{GS}=-10V$ (Typ: $9m\Omega$)

- 1) Low gate charge.
- 2) Green device available.
- 3) Advanced high cell density trench technology for ultra low $R_{DS(on)}$.
- 4) Excellent package for good heat dissipation.
- 5) MSL3

Package Marking and Ordering Information:

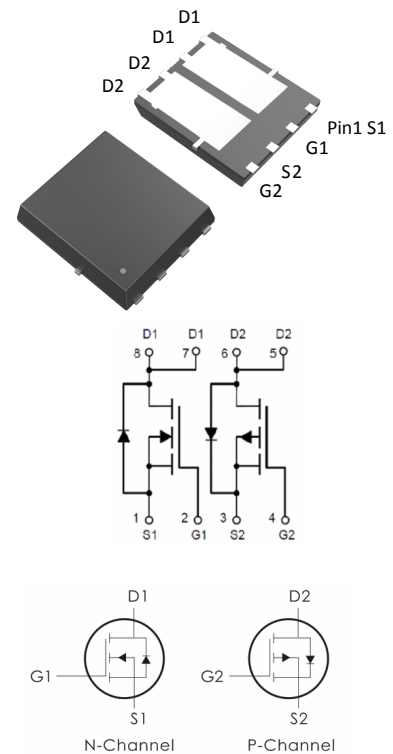
Part NO.	Marking	Package	Packing
DON639C	N639C	DFN5*6-8D	5000 pcs/Reel

Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
I_D	Continuous Drain Current- $T_C=25^\circ C^1$	40	-40	A
	Continuous Drain Current- $T_C=100^\circ C^1$	28	-28	
I_{DM}	Pulsed Drain Current ²	160	-160	A
E_{AS}	Single pulse avalanche energy ³	90	90	mJ
P_D	Power Dissipation - $T_C=25^\circ C$	38	40	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ C$

Thermal Characteristics:

Symbol	Parameter	N-CH	P-CH	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Cast	3.3	3.1	$^\circ C/W$



N-Channel Electrical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Sourctce Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	40	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =40V	---	---	1	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0A	---	---	± 100	nA
On Characteristics						
V _{GS(th)}	Gate-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	1	---	2.5	V
R _{DS(ON)}	Drain-Source On Resistance ⁴	V _{GS} =10V, I _D =10A	---	5	6	m Ω
		V _{GS} =4.5V, I _D =5A	---	7	9	m Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	---	2380	---	pF
C _{oss}	Output Capacitance		---	191	---	
C _{rss}	Reverse Transfer Capacitance		---	151	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DS} =20V, I _D =20A, R _{ENG} =3 Ω ,V _{GS} =10V	---	10	---	ns
t _r	Rise Time		---	29	---	ns
t _{d(off)}	Turn-Off Delay Time		---	42	---	ns
t _f	Fall Time		---	7	---	ns
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A	---	35	---	nC
Q _{gs}	Gate-Source Charge		---	10	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	10	---	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _{SD} =15A	---	---	1.2	V
I _S	Continuous Drain Current	V _D =V _G =0V	---	---	33.3	A
I _{SM}	Pulsed Drain Current		---	---	133.3	A
T _{rr}	Reverse Recovery Time	I _F =20A, T _J =25 °C	---	11	---	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/us	---	5	---	nC

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : $T_J=25^{\circ}C, V_{DD}=20V, V_G=10V, L=0.5mH$
4. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

Test Circuit

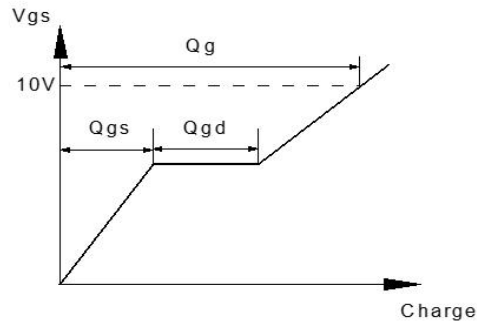
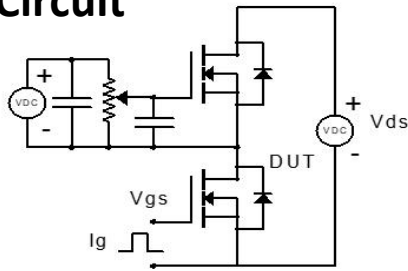


Figure 1: Gate Charge Test Circuit & Waveform

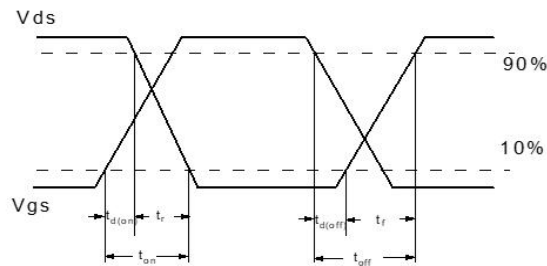
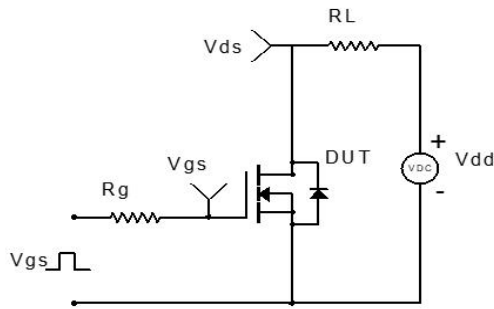


Figure 2: Resistive Switching Test Circuit & Waveform

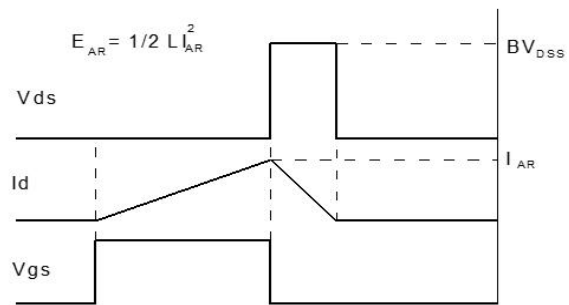
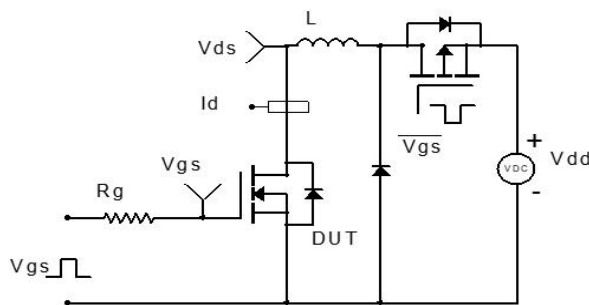


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

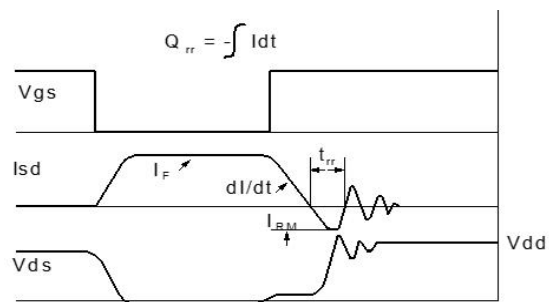
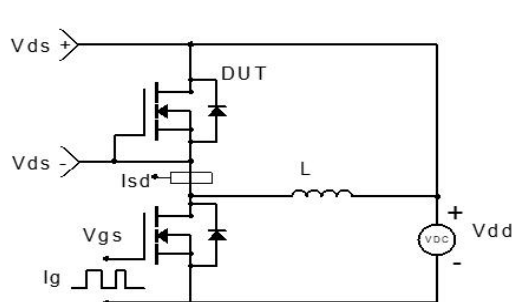


Figure 4: Diode Recovery Test Circuit & Waveform

P-Channel Electrical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	-40	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =-40V	---	---	-1	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0A	---	---	± 100	nA
On Characteristics						
V _{GS(th)}	Gate-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	-1	-1.6	-2.5	V
R _{DS(ON)}	Drain-Source On Resistance ⁴	V _{GS} =-10V, I _D =-10A	---	9	13	m Ω
		V _{GS} =-4.5V, I _D =-5A	---	13	17	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	---	2100	---	pF
C _{oss}	Output Capacitance		---	270	---	
C _{rss}	Reverse Transfer Capacitance		---	215	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = -20V, I _D =-11A V _{GS} = -10V, R _{GEN} =2.5 Ω	---	11	---	ns
t _r	Rise Time		---	21	---	ns
t _{d(off)}	Turn-Off Delay Time		---	53	---	ns
t _f	Fall Time		---	29	---	ns
Q _g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-20V, I _D =-11A	---	35	---	nC
Q _{gs}	Gate-Source Charge		---	6.5	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	7.6	---	nC
Drain-Source Diode Characteristics						
I _S	Continuous Drain to Source Diode	V _D =V _G =0V	---	---	-33.3	A
I _{SM}	Pulsed Drain to Source Diode		---	---	-133.3	---
T _{rr}	Reverse Recovery Time	I _F =-11A, T _J =25 °C dI/dt=100A/us	---	-35	---	ns
Q _{rr}	Reverse Recovery Charge		---	-40	---	nC
V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} =0V, I _S =-11A	---	---	-1.2	V

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : $T_J=25^{\circ}C, V_{DD}=-20V, V_G=-10V, L=1mH$
4. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

Test Circuit

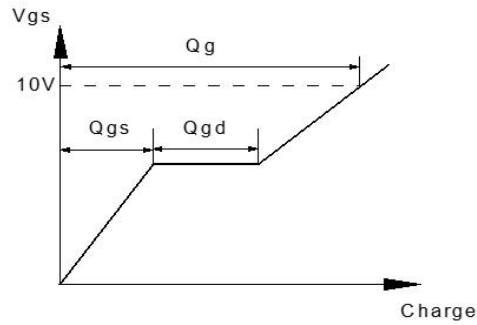
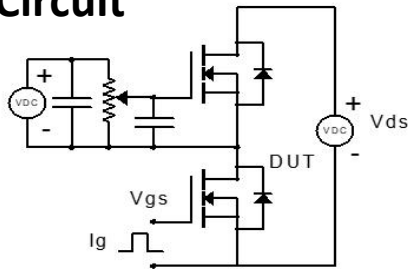


Figure 1: Gate Charge Test Circuit & Waveform

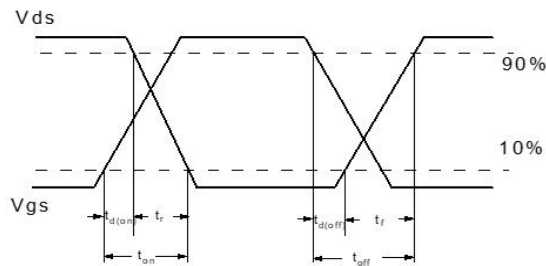
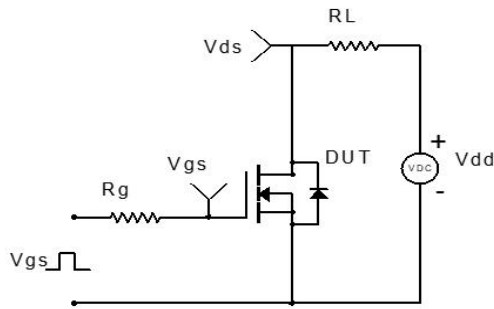


Figure 2: Resistive Switching Test Circuit & Waveform

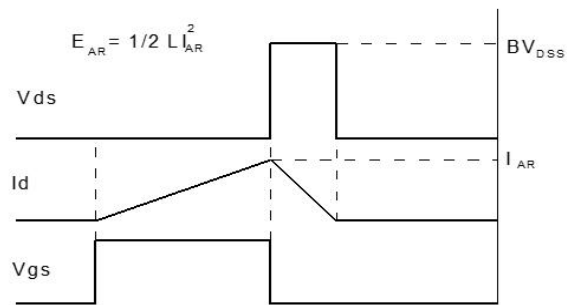
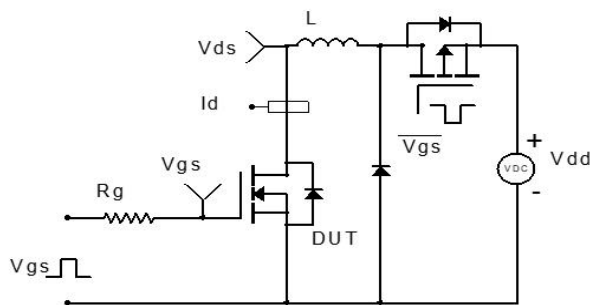


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

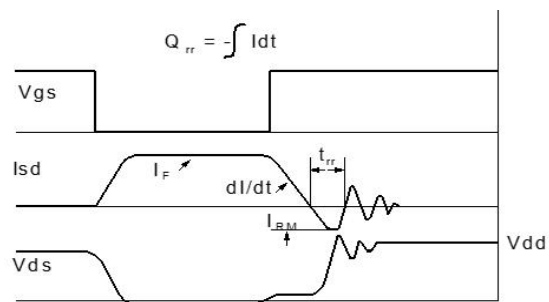
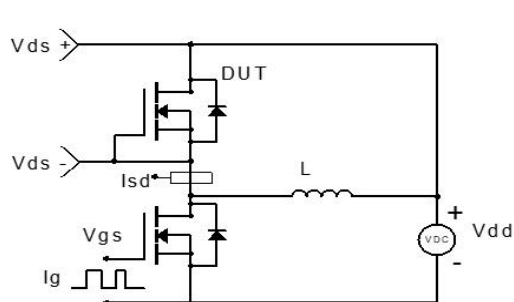
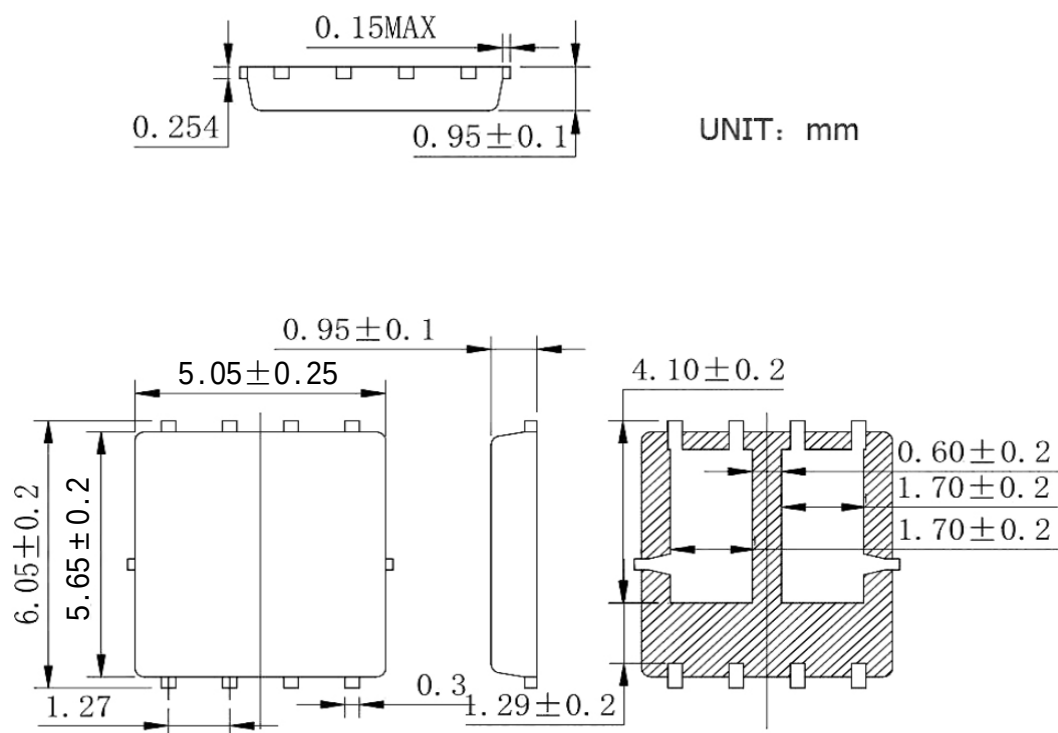


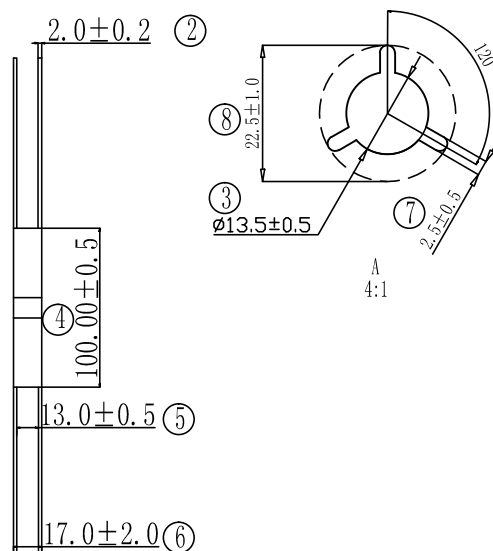
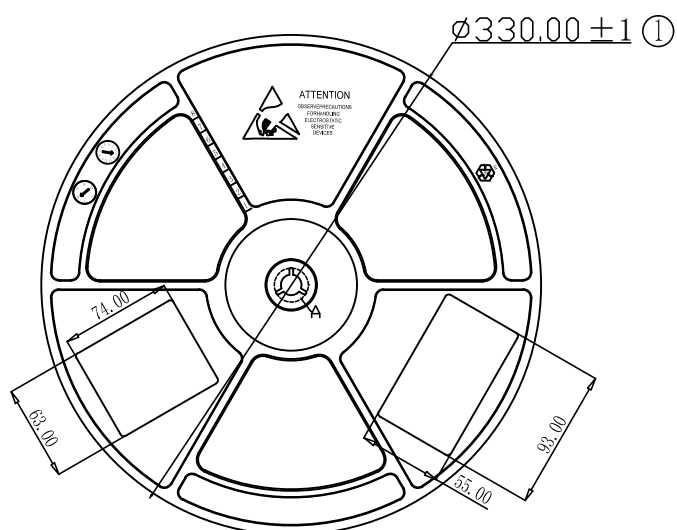
Figure 4: Diode Recovery Test Circuit & Waveform

DFN5×6-8D Package Information:

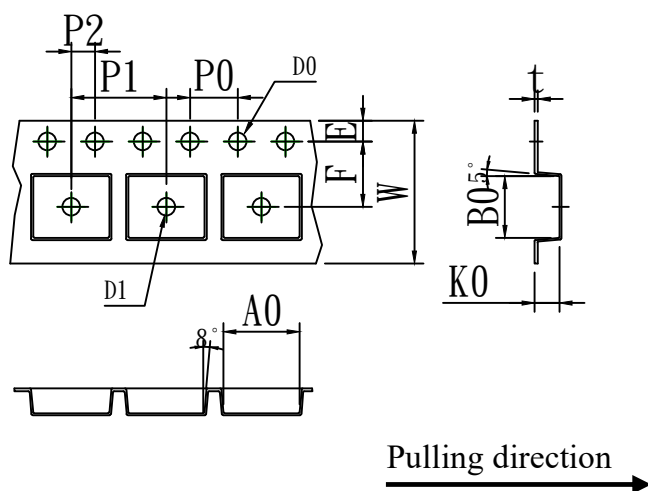


Tape & Reel Information

Dimensions in mm



Symbol	A0	B0	K0	D0	D1	P0	P1	10*P0
Spec	6.15 ± 0.10	5.40 ± 0.10	1.30 ± 0.10	1.55 ± 0.10	1.55 ± 0.10	4.00 ± 0.10	8.00 ± 0.10	40.00 ± 0.10
Symbol	W	E	F	P2	t			
Spec	12.00 ± 0.10	1.75 ± 0.10	5.50 ± 0.10	2.00 ± 0.10	0.20 ± 0.05			



Marking Information:

①. Doingter LOGO

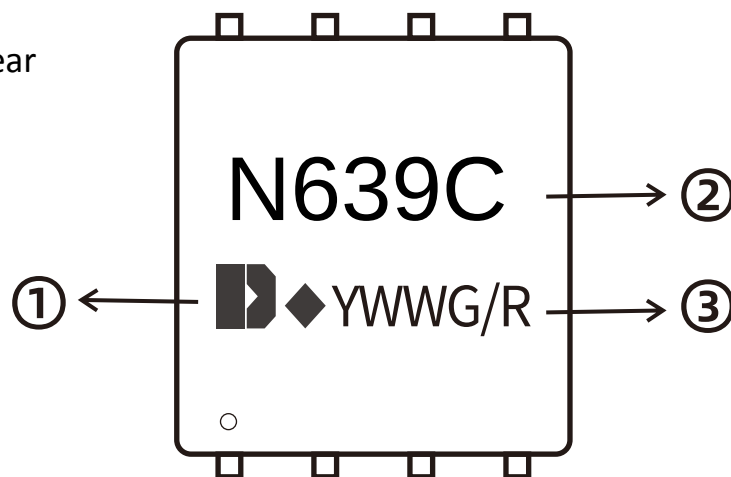
②. Part NO.

③. Date Code(YWWG / R)

Y : Year Code , last digit of the year

WW : Week Code(01-53)

G/R : G(Green) /R(Lead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2026-02-02	Release of final version

Attention :

- Information furnished in this document is believed to be accurate and reliable. However, Shenzhen Doingter Semiconductor Co.,Ltd. assumes noresponsibility for the consequences of use without consideration for such information nor use beyond it.
- Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Shenzhen Doingter complies with the agreement. Products and information provided in this document have no infringement of patents.
- Shenzhen Doingter assumes noresponsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.



Is

a registered trademark of Shenzhen Doingter Semiconductor Co., Ltd. Copyright © 2013

Shenzhen DoingterSemiconductor Co.,Ltd. Printed All rights reserved.