

DDR4 SDRAM

ZD2G8 ZD1G16

Features

- $V_{DD} = V_{DDQ} = 1.2V \pm 60mV$
- $V_{PP} = 2.5V, -125mV, +250mV$
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- T_C maximum up to 95°C
 - 64ms, 8192-cycle refresh up to 85°C
 - 32ms, 8192-cycle refresh at >85°C to 95°C
- 16 internal banks (x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability

- Connectivity test
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability
- MBIST-PPR support (Die Revision F only)

Options¹

- Configuration
 - 4 Gig x 4
 - 2 Gig x 8
 - 1 Gig x 16
- 78-ball FBGA package (Pb-free) – x4, x8
 - 10mm x 11mm – Rev. B
 - 9mm x 11mm – Rev. E
 - 7.5mm x 11mm – Rev. F
- 96-ball FBGA package (Pb-free) – x16
 - 10mm x 13mm – Rev. B
 - 9mm x 13mm – Rev. E
 - 7.5mm x 13mm – Rev. F
- Timing – cycle time
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.682ns @ CL = 21 (DDR4-2933)
- Operating temperature
 - Commercial ($0^\circ \leq T_C \leq 95^\circ C$)
 - Industrial ($-40^\circ \leq T_C \leq 95^\circ C$)
- Die Revision

Marking

4G4
2G8
1G16
VA
JC
SA
RC
KD
TB
-062E
-068
None
IT
:B, :E, :F

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on <http://www.zettadevice.com> for available offerings.

Table 1: Key Timing Parameters

Speed Grade ¹	Data Rate (MT/s)	Target CL-nRCD-nRP	t_{AA} (ns)	t_{RCD} (ns)	t_{RP} (ns)
-062E	3200	22-22-22	13.75	13.75	13.75
-068	2933	21-21-21	14.32 (13.75)	14.32 (13.75)	14.32 (13.75)

Notes: 1. Refer to the Speed Bin Tables for additional details.

Table 2: Addressing

Parameter	4096 Meg x 4	2048 Meg x 8	1024 Meg x 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	256K (A[17:0])	128K (A[16:0])	128K (A[16:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size ¹	512B	1KB	2KB

Notes: 1. Page size is per bank, calculated as follows:

Page size = $2^{\text{COLBITS}} \times \text{ORG}/8$, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

Figure 1: Order Part Number Example

Example Part Number: ZD2G8Z42BD8SA-062E

