

GENERAL DESCRIPTION

The LW81XX Series is a group of voltage regulators with high accuracy, high speed, low drop-out, reverse current protection, high ripple rejection and fast discharge function.

The series consists of a voltage reference, an error amplifier, a driver transistor, a current limiter, a thermal protection circuit, a reverse current protection circuit and a phase compensation circuit.

Output voltage is selectable from 0.8V to 5.0V which fixed by laser trimming technologies, Step=100mV.

The LW81XX Series is available in DFN2x2-6L and SOT23-5L packages.

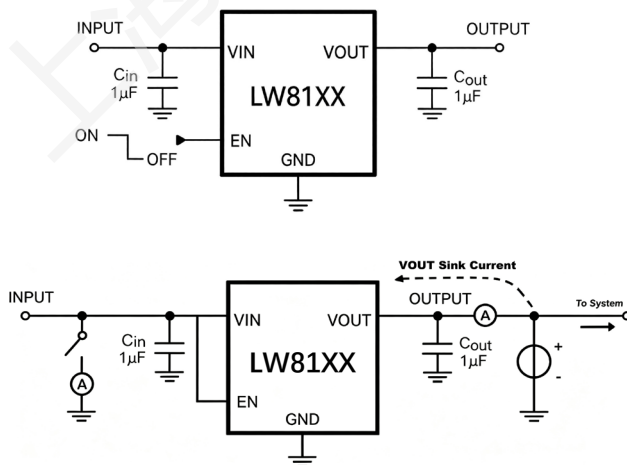
FEATURES

- Low Quiescent Current: 28 μ A(Typ.)
- Operating Voltage Range: from 1.8V to 7.0V
- Output Voltage Range: from 0.8V to 5.0V
- Max Output Current: 750mA
- Output Accuracy: $\pm 1.0\%$ @+25 $^{\circ}$ C
- Low Dropout Voltage: 230mV@750mA/3.3V
- High PSRR: 75dB@1kHz, 10mA
- Current Limiting Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Fast Discharge Function
- Excellent Line and Load Transient Response
- Reverse Current Protection Function
- Stable with 1 μ F Output Capacitor

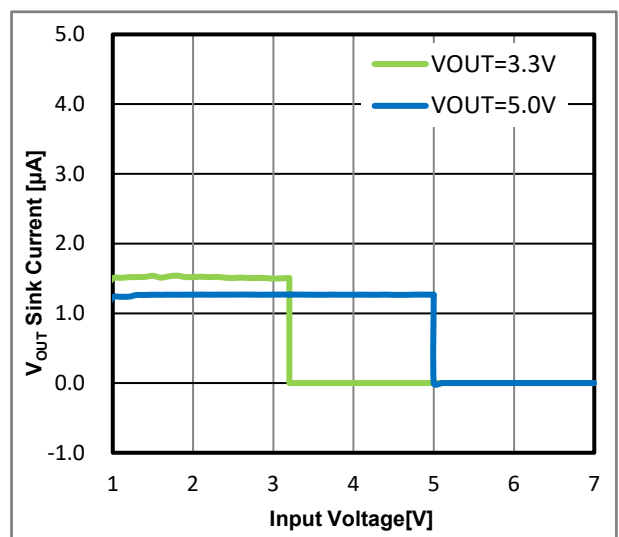
APPLICATIONS

- Battery-Powered Devices
- Reference Voltage Sources
- USB products and HDMI Equipment
- Other Low Voltage Power Supplies

TYPICAL APPLICATION CIRCUIT



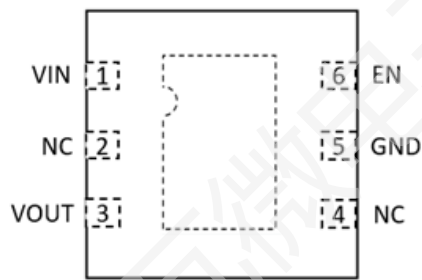
TYPICAL PERFORMANCE CHARACTERISTICS



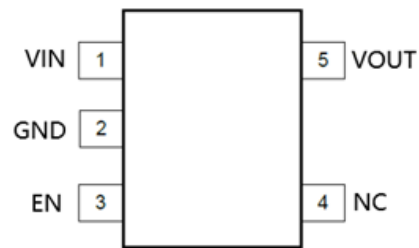
PIN DESCRIPTION:

PIN No		SYMBOL	DESCRIPTION
DFN2x2-6L	SOT23-5L		
1	1	VIN	Input Voltage Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 1μF from VIN pin to ground.
5	2	GND	Ground pin
6	3	EN	Enable pin. Drive EN greater than VENH to turn on the regulator. Drive EN less than VENL to put the low-dropout regulator (LDO) into shutdown mode.
2,4	4	NC	Not Connection. Ground this pin for better thermal performance.
3	5	VOOUT	Output Voltage Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 1μF from VOOUT pin to ground.
Thermal pad	--	Pad	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

PIN ASSIGNMENT:



DFN2x2-6L (Type-A)



SOT23-5L

MARK INFORMATION:

DFN2X2-6L

XX: VOLTAGE

YY: DATE CODE

LW81XX
YYYYY

SOT23-5L

XX: VOLTAGE

YY: DATE CODE

LW81XX
YYYYY

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾:(T_A =25℃, unless otherwise specified.)

SYMBOL	ITEM		RATING	UNIT
V _{IN}	Supply Voltage		-0.3~8.0	V
V _{EN}	EN Pin Voltage		-0.3~8.0	V
V _{OUT}	V _{OUT} pin Voltage		-0.3~ (V _{IN} +0.3)	V
V _(ESD)	ESD Susceptibility, HBM ⁽²⁾		± 4000	V
R _{θJA}	Junction-to-ambient Thermal Resistance ⁽³⁾	DFN2x2-6L	80	℃/W
		SOT23-5L	210	
T _J	Junction Temperature Range		-40~150	℃
T _{STG}	Storage Temperature Range		-40~150	℃
T _{SOLDER}	Lead Temperature (Soldering)		260℃, 10s	

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
2. per ANSI/ESDA/JEDEC JS-001
3. Device mounted on FR-4 PCB, Refer to JESD51-3 for detailed information on the board construction

RECOMMENDED OPERATING RANGE:

SYMBOL	ITEM	VALUE	UNIT
V _{IN}	V _{IN} Supply Voltage	1.8~7.0	V
V _{EN}	EN Pin Voltage	0~7.0	V
V _{OUT}	V _{OUT} Pin Voltage	0.8~5.0	V
I _{OUT}	Output Current	0~0.75	A
T _J	Junction Temperature Range	-40~125	℃

ELECTRICAL CHARACTERISTICS:

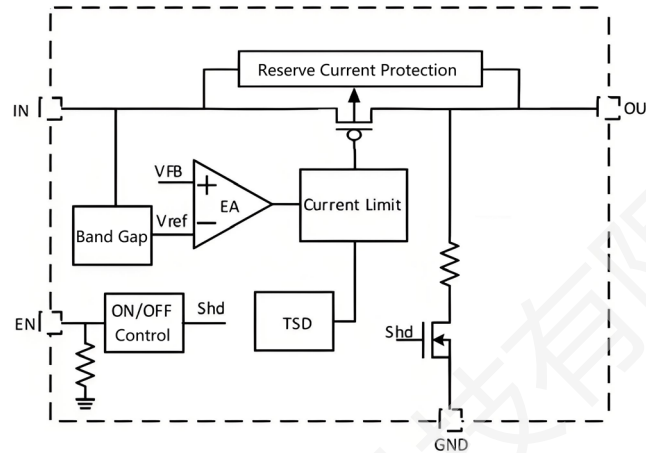
$V_{IN}=V_{OUT(NOM)}+1V$ or $+2V$, whichever is greater, $C_{IN}=C_{OUT}=1\mu F$, unless otherwise specified, typical values are at $T_A=25^{\circ}C$.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
V_{IN}	Input Voltage		1.8		7.0	V
V_{OUT}	Output Accuracy	$I_{OUT}=1mA$	-1.0		1.0	%
I_{LIM}	Current Limit ⁽¹⁾		0.85	1.1		A
I_Q	Quiescent Current	$V_{IN}=V_{EN}=V_{OUT}+1V$, No Load		28	45	μA
I_{SHD}	Shutdown Current	$V_{IN}=7.0V$, $V_{EN}=0V$			0.1	μA
V_{DROP}	Dropout Voltage ⁽¹⁾⁽²⁾	$V_{OUT}=3.3V$	$I_{OUT}=300mA$	95		mV
			$I_{OUT}=500mA$	160		
			$I_{OUT}=750mA$	230		
		$V_{OUT}=5.0V$	$I_{OUT}=300mA$	75		
			$I_{OUT}=500mA$	120		
			$I_{OUT}=750mA$	165		
$\frac{\Delta V_{OUT}}{(\Delta V_{IN} * V_{OUT(NOM)})}$	Line Regulation	$V_{IN}=V_{OUT}+1V$ to $7.0V$, $I_{OUT}=1mA$		0.05	0.2	%/V
ΔV_{OUT}	Load Regulation	$1mA \leq I_{OUT} \leq 750mA$		10	60	mV
I_{SHORT}	Short Current ⁽¹⁾	$V_{OUT}=0V$		65		mA
V_{ENH}	EN High Voltage	$V_{IN}=1.8V$ to $7.0V$, $I_{OUT}=1mA$	1.5			V
V_{ENL}	EN Low Voltage				0.5	V
T_{STR}	Startup Time	From V_{EN} 'L' $\rightarrow$ 'H' to $95\% * V_{OUT}$, $C_{OUT}=1\mu F$, No Load		50		μs
PSRR	Power Supply Rejection Ratio	$V_{IN}=4.3V$, $V_{OUT}=3.3V$ $V_{PP}=0.5V$, $I_{OUT}=10mA$ $C_{IN}=0.22\mu F$, $C_{OUT}=1\mu F$	$f=217Hz$	74		dB
			$f=1KHz$	75		
			$f=10KHz$	70		
e_n	Output Voltage Noise	$V_{IN}=4.3V$, $V_{OUT}=3.3V$, $f=10Hz$ to $100kHz$	$I_{OUT}=0mA$	21		μV_{RMS}
			$I_{OUT}=10mA$	31		
I_{REV}	Reverse Current ⁽³⁾	$V_{EN}=V_{IN}=0V$, $V_{OUT}=7.0V$		0.01	0.5	μA
I_{REVS}	V_{OUT} Pin Sink Current ⁽⁴⁾	$V_{EN}=V_{IN}=6.0V$, $V_{OUT}=7.0V$		1.5	2.5	μA
T_{SD}	Thermal Shutdown	Temperature rising		160		$^{\circ}C$
ΔT_{SD}	TSD Hysteresis	Temperature falling		20		$^{\circ}C$
$R_{DISCHRG}$	Output Discharge Resistance	$V_{IN}=7V$, $V_{EN}=0V$		80		Ω

NOTES:

1. Guaranteed by design
2. The dropout voltage is defined as $V_{IN} - V_{OUT}$, when $V_{OUT} = 95\% * V_{OUT(NOM)}$
3. Reverse Current (I_{REV}) flows from V_{OUT} to V_{IN}
4. V_{OUT} Pin Sink Current (I_{REVS}) flows from V_{OUT} to GND

SIMPLIFIED BLOCK DIAGRAM:



DETAIL OPERATION DESCRIPTION:

The LW81XX Series is a low noise, high PSRR, low drop-out voltage regulator. It consists of a current limiter circuit, a driver transistor, a precision voltage reference, a thermal protection circuit, a reverse current protection circuit and an error correction circuit, and is compatible with low ESR ceramic capacitors. The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter.

Reverse Current Protection

The LW81XX series includes reverse current protection to prevent the damage as a result of current flow from V_{OUT} pin to the V_{IN} pin when the power supply is connected to the V_{OUT} pin. When V_{IN} is smaller than V_{OUT} , the reverse current protection works and suppress the reverse current to $0.5\mu A$ (MAX.). When V_{IN} is smaller than V_{OUT} , the V_{OUT} pin sink current flowing from the V_{OUT} pin to the GND pin is $1.5\mu A$ (TYP.) as the IC operation current. Please also note when an external power supply is connected to the V_{OUT} pin, please use it within 7.0V.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold through the switch. When a heavy load or

short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

Thermal Shutdown

When the junction temperature of the built-in driver transistor reaches the temperature limit level ($160^{\circ}C$ TYP.), the thermal shutdown circuit operates and the driver transistor will be turned OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of $140^{\circ}C$ (TYP.) as the thermal shutdown release threshold.

Chip Enable

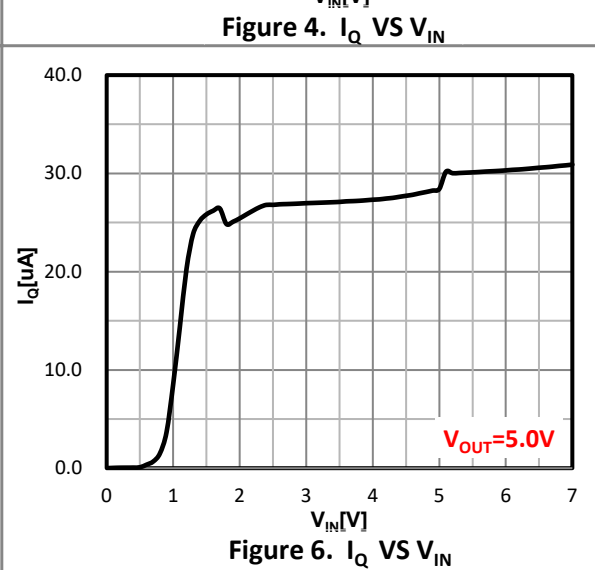
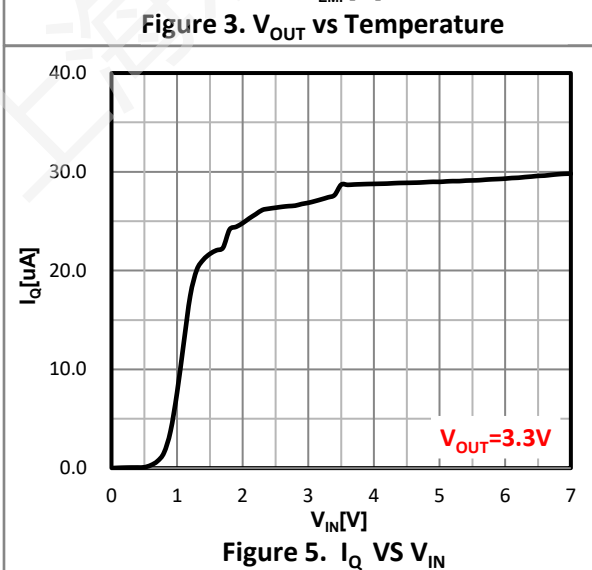
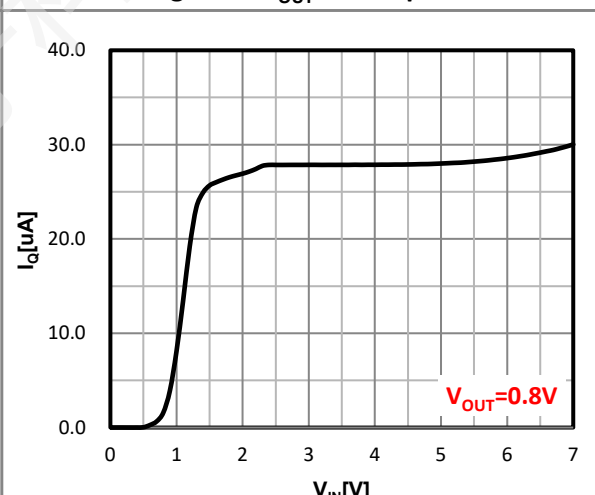
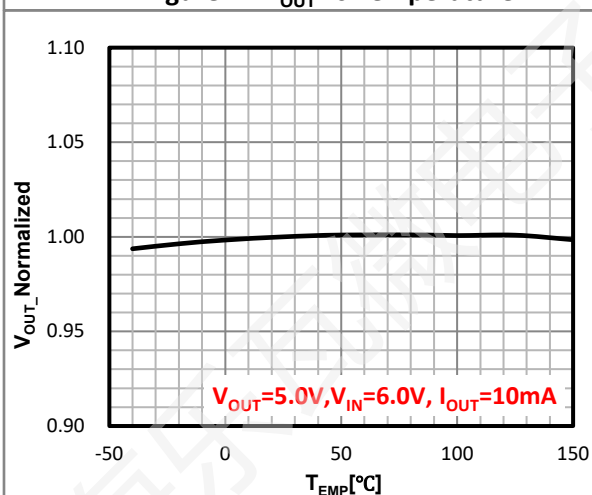
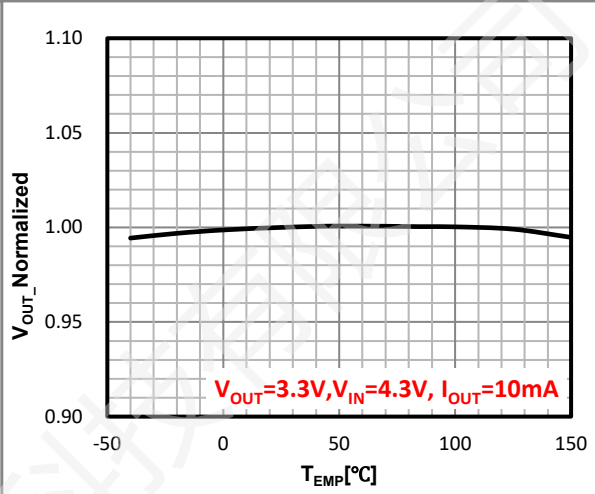
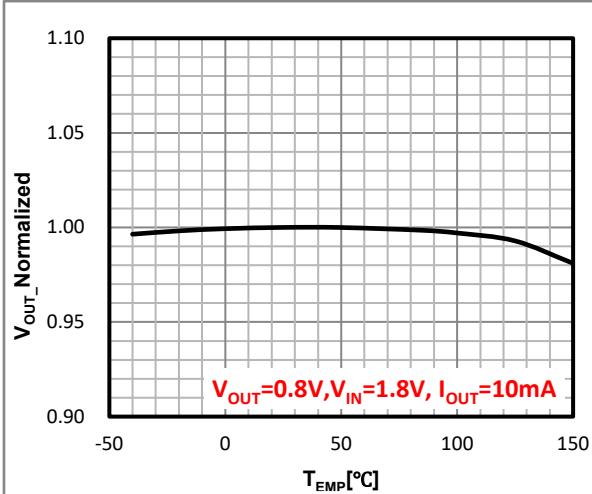
The LW81XX series can be turned off via the EN pin signal. In shutdown mode, output at the V_{OUT} pin will be pulled down to the GND.

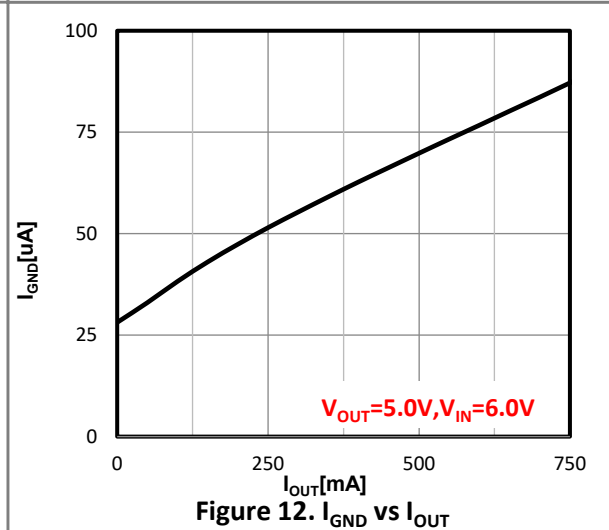
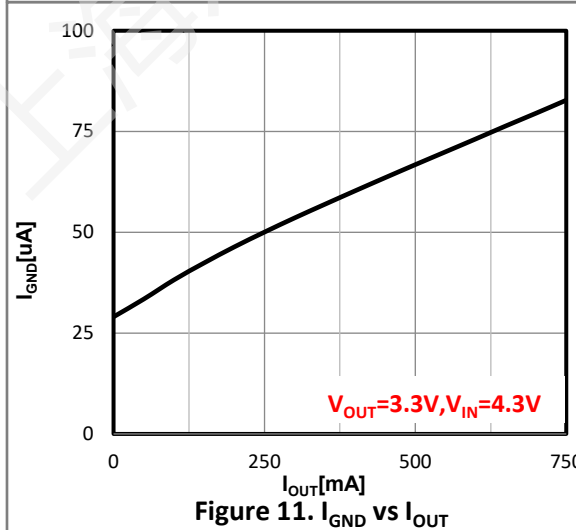
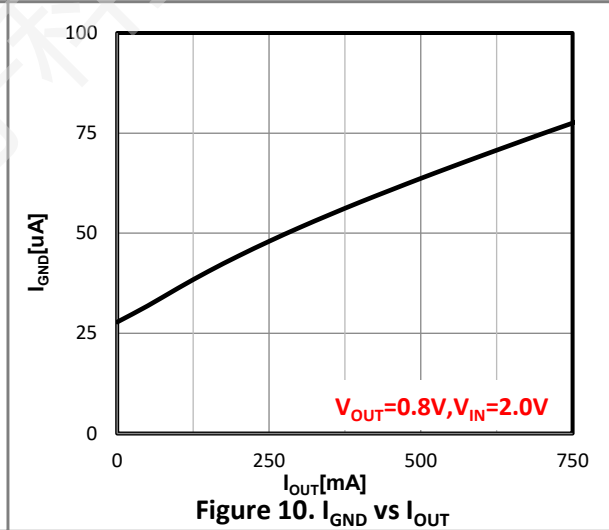
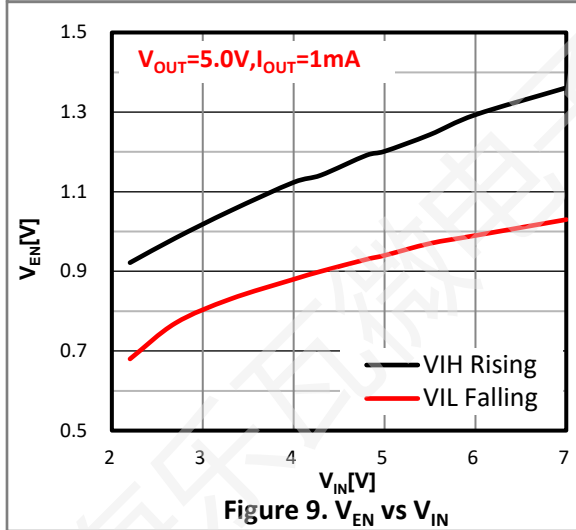
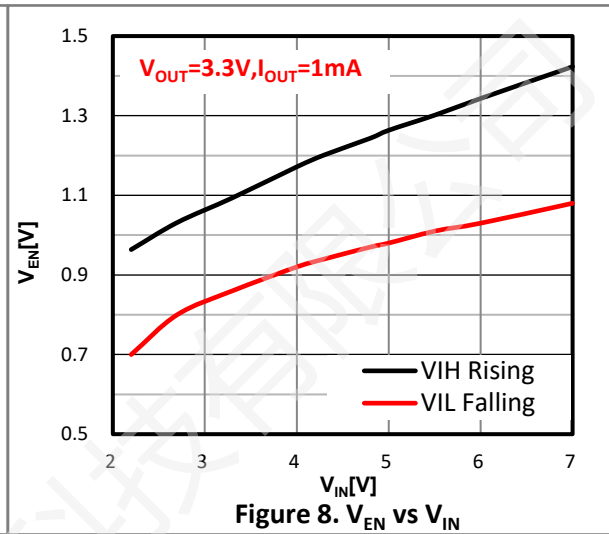
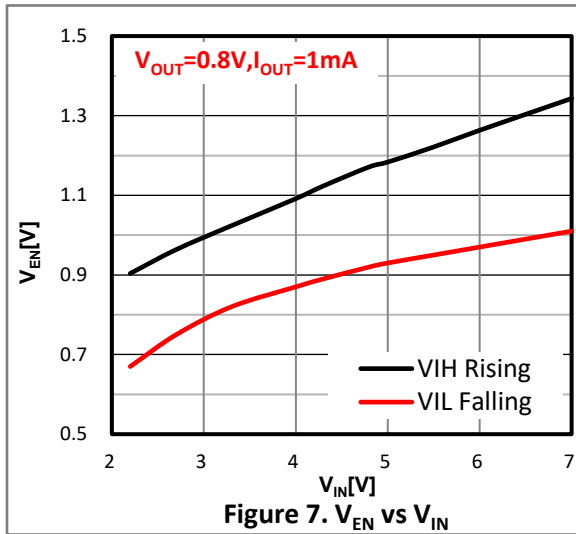
The LW81XX series has a pull-down resistor in order to operate normally even the EN pin is floating.

If the EN pin voltage is set with the specified voltage range, the logic is fixed and the IC will operate normally.

TYPICAL OPERATING CHARACTERISTICS:

(Tested under $T_A = 25^\circ\text{C}$, $C_{IN} = C_{OUT} = 1\mu\text{F}$, unless otherwise specified)





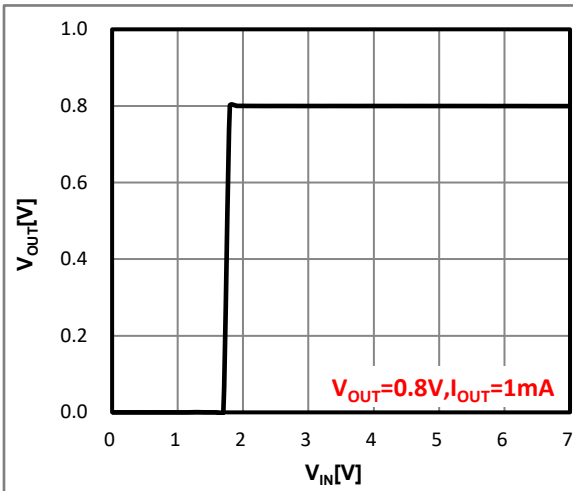


Figure 13. V_{OUT} vs V_{IN}

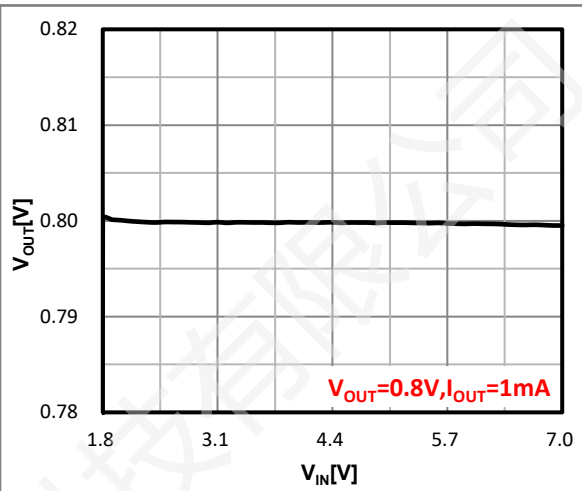


Figure 14. Line Regulation

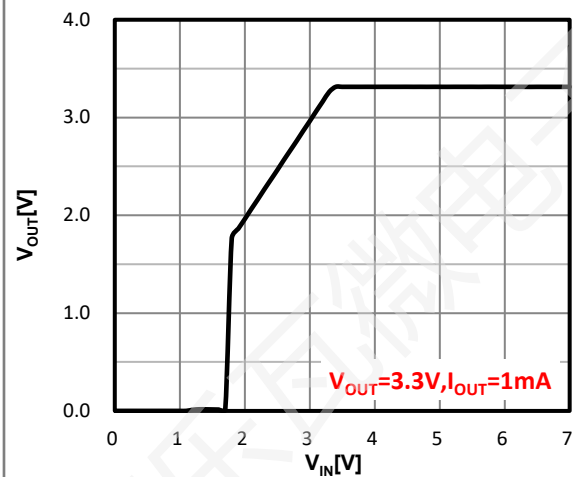


Figure 15. V_{OUT} vs V_{IN}

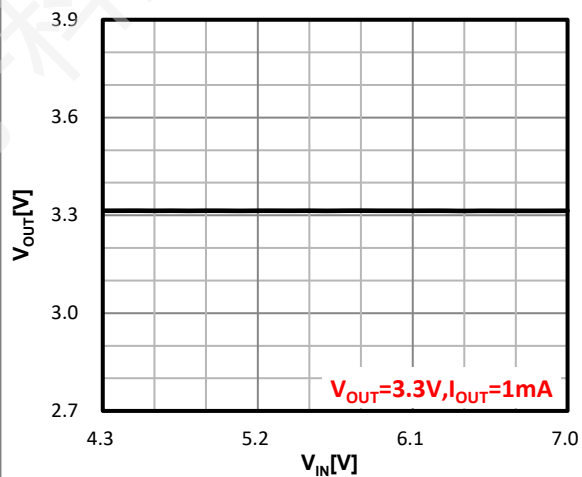


Figure 16. Line Regulation

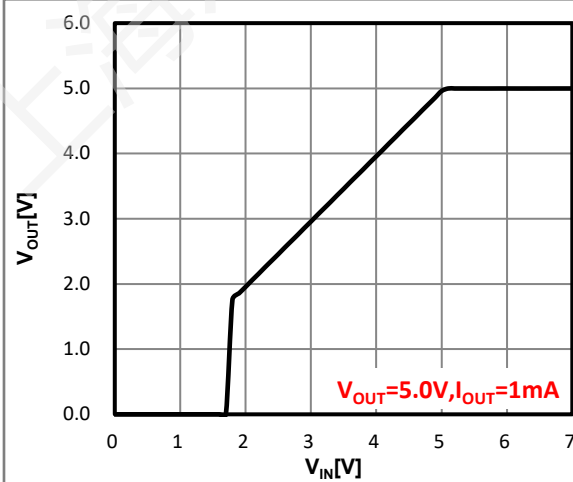


Figure 17. V_{OUT} vs V_{IN}

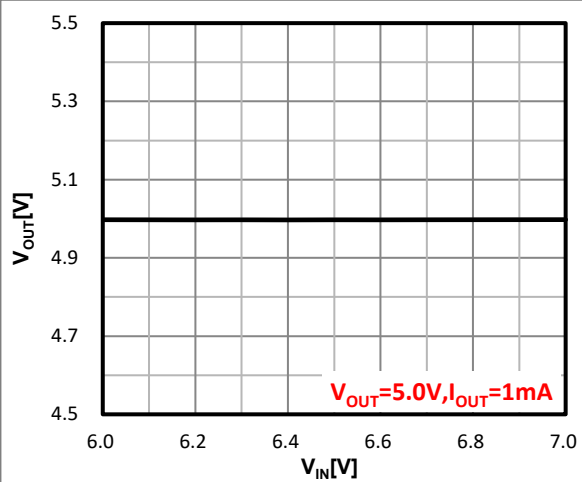


Figure 18. Line Regulation

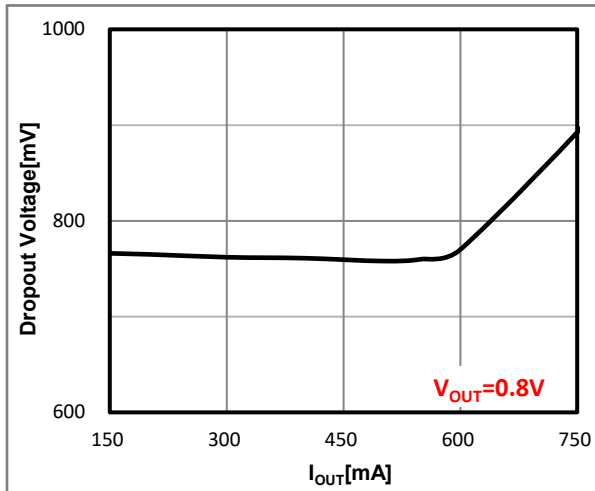


Figure 19. Dropout Voltage VS I_{OUT}

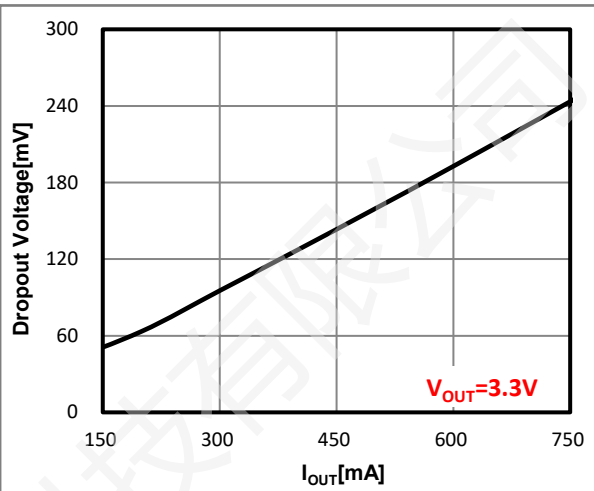


Figure 20. Dropout Voltage VS I_{OUT}

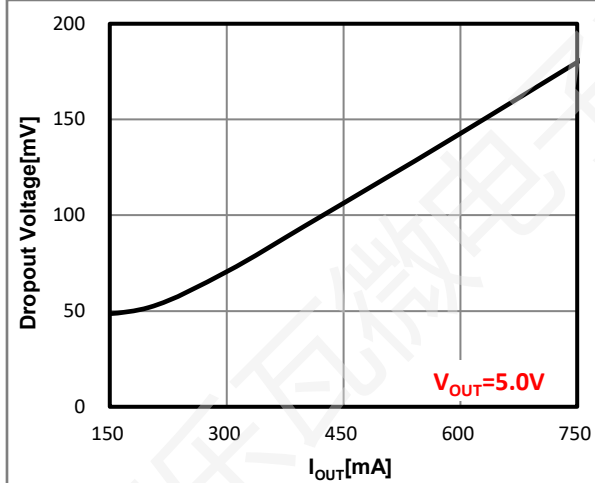


Figure 21. Dropout Voltage VS I_{OUT}

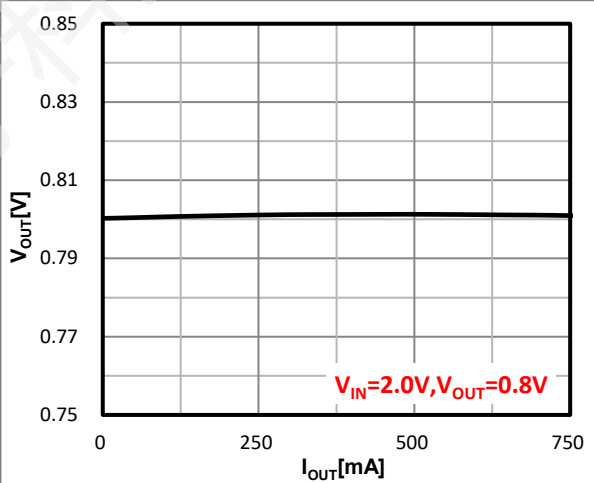


Figure 22. Load Regulation

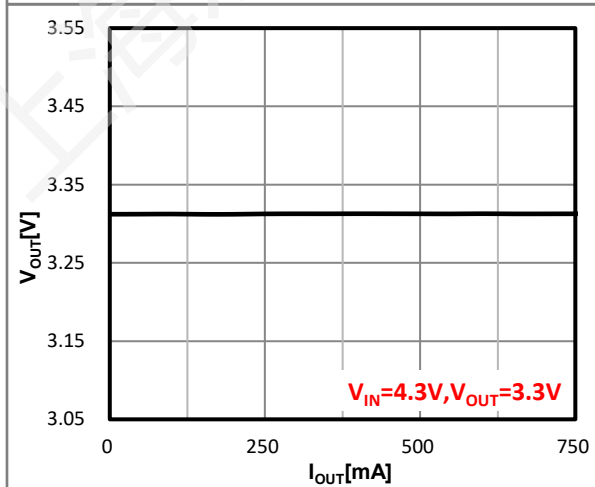


Figure 23. Load Regulation

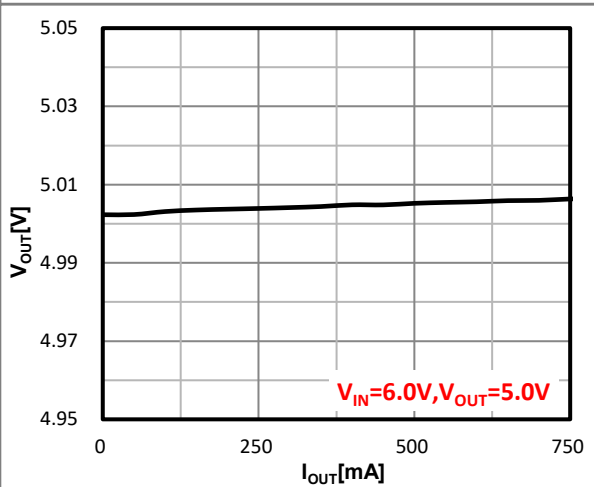
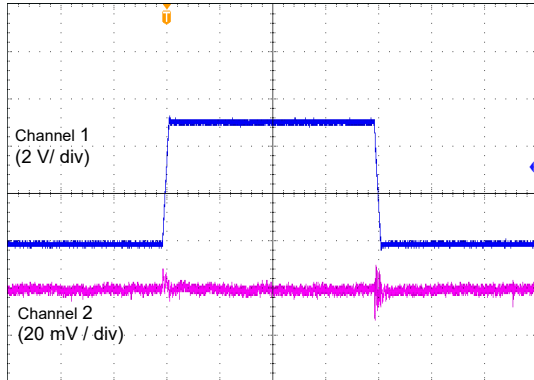


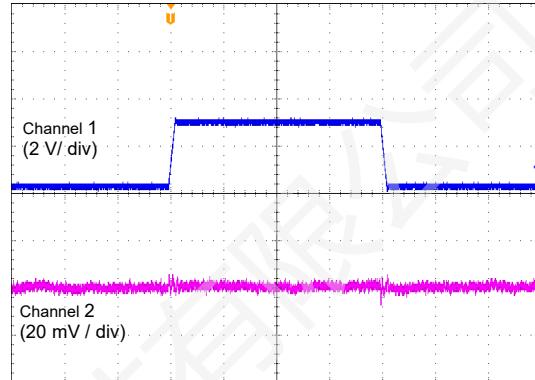
Figure 24. Load Regulation



Time (100µs / div)

Channel 1 = V_{IN} , channel 2 = V_{OUT} , $V_{IN}=1.8V \rightarrow 7.0V$,
 $t_R=t_F=10\mu s$, $V_{OUT}=0.8V$, $I_{OUT}=10mA$

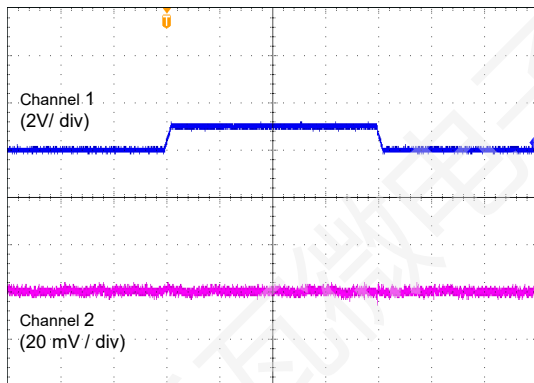
Figure 25. Line Transient



Time (100µs / div)

Channel 1 = V_{IN} , channel 2 = V_{OUT} , $V_{IN}=4.3V \rightarrow 7.0V$,
 $t_R=t_F=10\mu s$, $V_{OUT}=3.3V$, $I_{OUT}=10mA$

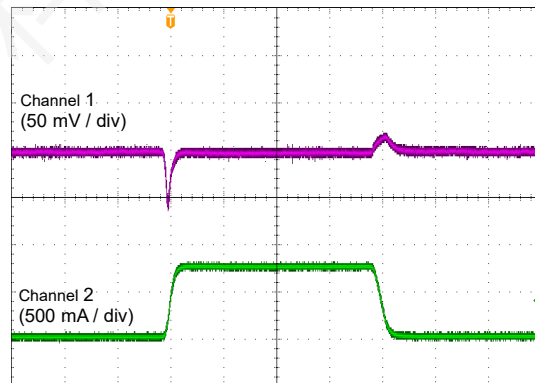
Figure 26. Line Transient



Time (100 µs / div)

Channel 1 = V_{IN} , channel 2 = V_{OUT} , $V_{IN}=6.0V \rightarrow 7.0V$,
 $t_R=t_F=10\mu s$, $V_{OUT}=5.0V$, $I_{OUT}=10mA$

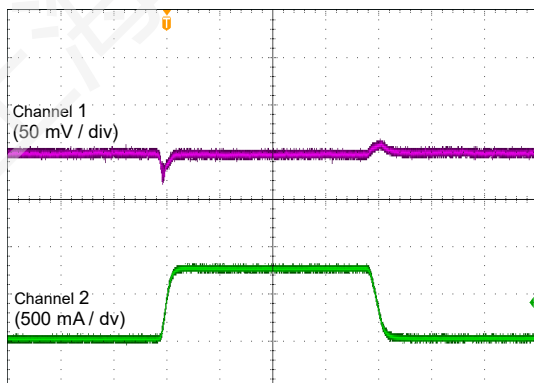
Figure 27. Line Transient



Time (40 µs / div)

Channel 1 = V_{OUT} , channel 2 = I_{OUT} , $V_{IN}=2.0V$, $V_{OUT}=0.8V$
 $C_{IN}=C_{OUT}=1\mu F$

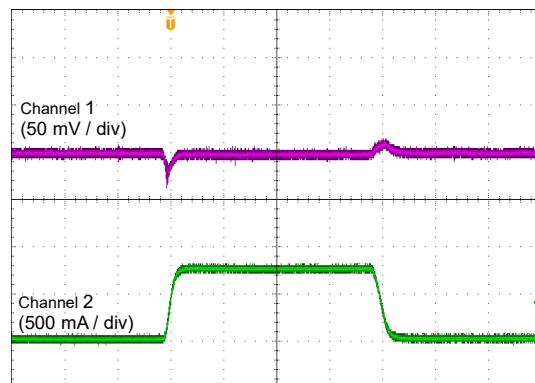
Figure 28. Load Transient (1 mA to 750mA)



Time (40 µs / div)

Channel 1 = V_{OUT} , channel 2 = I_{OUT} , $V_{IN}=4.3V$, $V_{OUT}=3.3V$
 $C_{IN}=C_{OUT}=1\mu F$

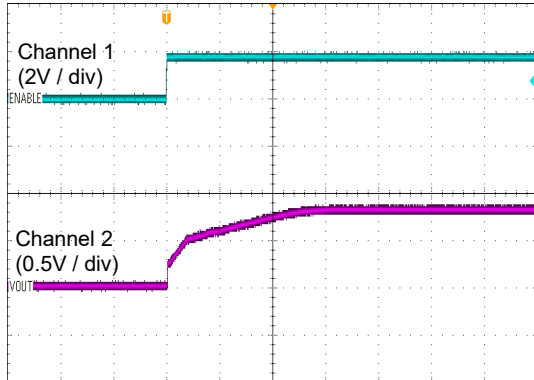
Figure 29. Load Transient (1 mA to 750mA)



Time (40 µs / div)

Channel 1 = V_{OUT} , channel 2 = I_{OUT} , $V_{IN}=6.0V$, $V_{OUT}=5.0V$
 $C_{IN}=C_{OUT}=1\mu F$

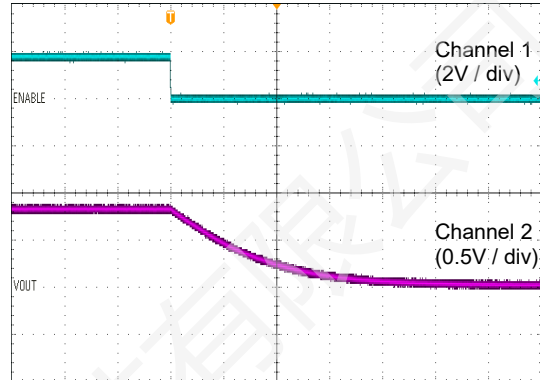
Figure 30. Load Transient (1 mA to 750mA)



Time (40 μ s / div)

Channel 1 = EN, channel 2 = V_{OUT} , $V_{IN}=1.8V$, EN=0 $\rightarrow$ 1.8V, $V_{OUT}=0.8V$, $C_{IN}=C_{OUT}=1\mu F$, No Load

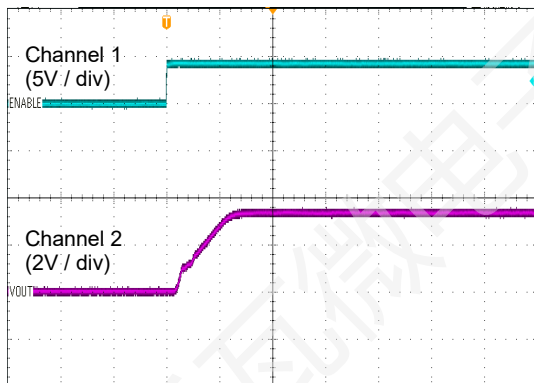
Figure 31. Power-Up with Enable



Time (40 μ s / div)

Channel 1 = EN, channel 2 = V_{OUT} , $V_{IN}=1.8V$, EN=1.8 $\rightarrow$ 0V, $V_{OUT}=0.8V$, $C_{IN}=C_{OUT}=1\mu F$, No Load

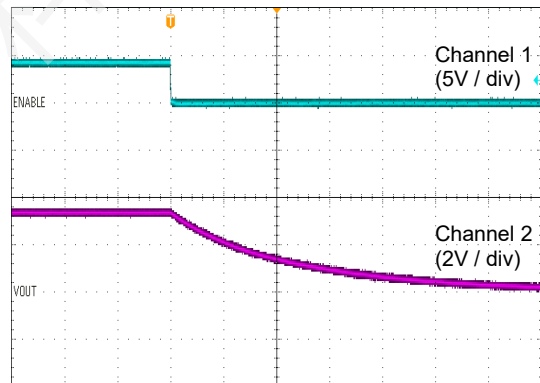
Figure 32. Shut-Down with Enable



Time (40 μ s / div)

Channel 1 = EN, channel 2 = V_{OUT} , $V_{IN}=4.3V$, EN=0 $\rightarrow$ 4.3V, $V_{OUT}=3.3V$, $C_{IN}=C_{OUT}=1\mu F$, No Load

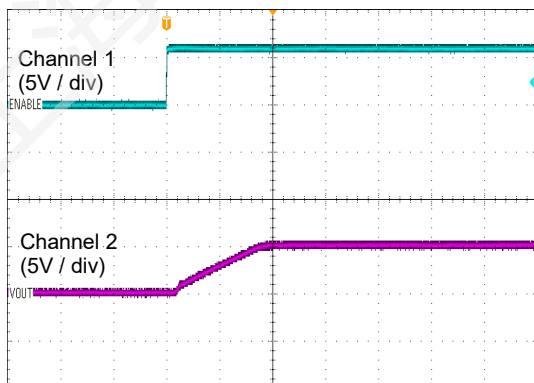
Figure 33. Power-Up with Enable



Time (40 μ s / div)

Channel 1 = EN, channel 2 = V_{OUT} , $V_{IN}=4.3V$, EN=4.3 $\rightarrow$ 0V, $V_{OUT}=3.3V$, $C_{IN}=C_{OUT}=1\mu F$, No Load

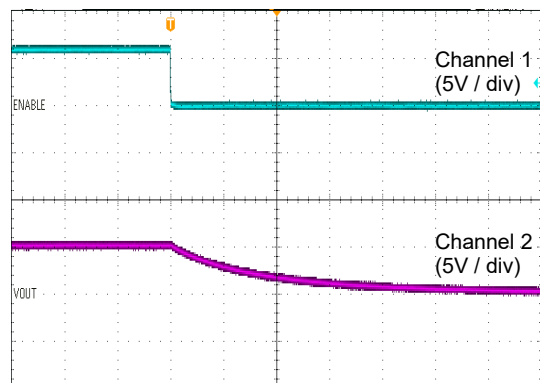
Figure 34. Shut-Down with Enable



Time (40 μ s / div)

Channel 1 = EN, channel 2 = V_{OUT} , $V_{IN}=6.0V$, EN=0 $\rightarrow$ 6.0V, $V_{OUT}=5.0V$, $C_{IN}=C_{OUT}=1\mu F$, No Load

Figure 35. Power-Up with Enable



Time (40 μ s / div)

Channel 1 = EN, channel 2 = V_{OUT} , $V_{IN}=6.0V$, EN=6.0 $\rightarrow$ 0V, $V_{OUT}=5.0V$, $C_{IN}=C_{OUT}=1\mu F$, No Load

Figure 36. Shut-Down with Enable

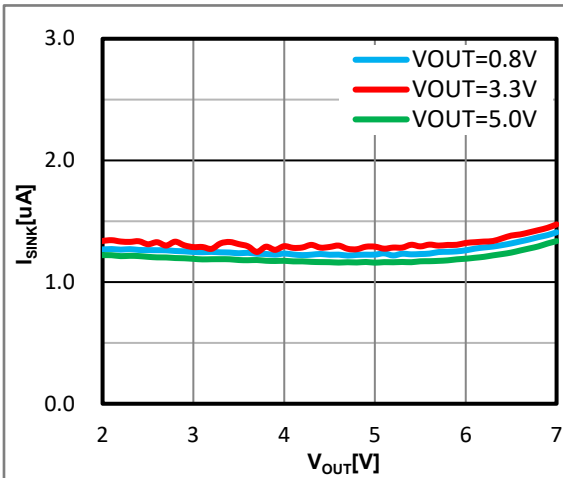


Figure 37. V_{OUT} Sink Current VS Output Voltage

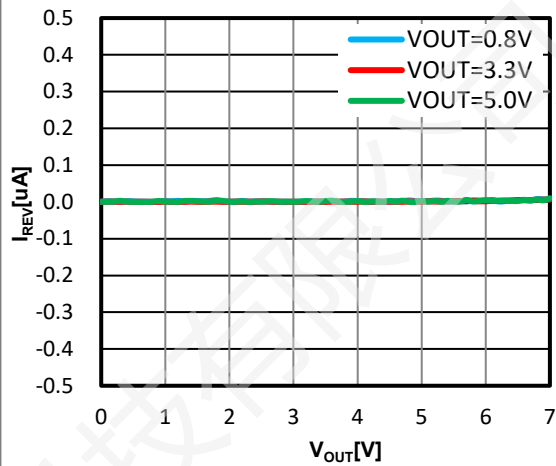
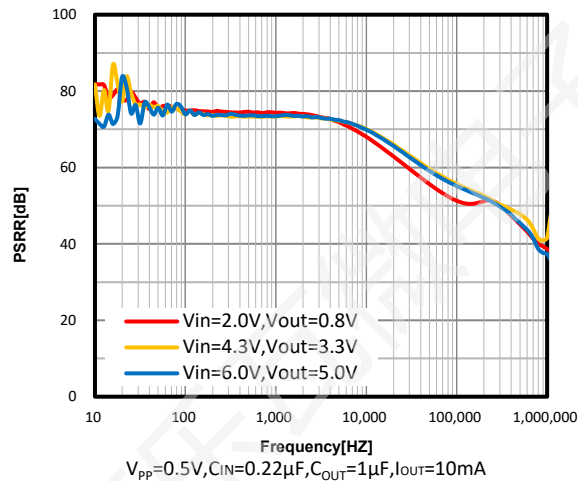
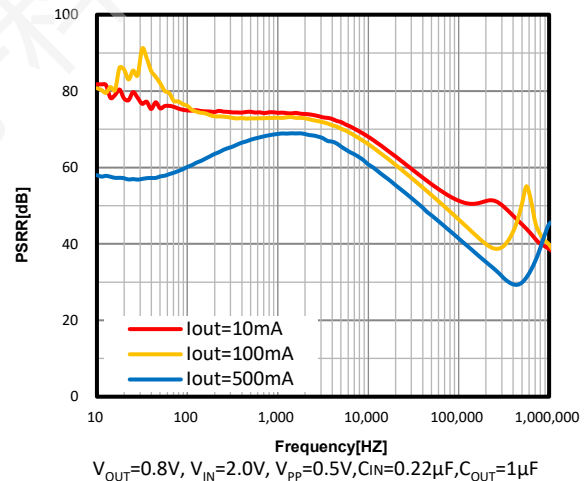


Figure 38. Reverse Current VS Output Voltage



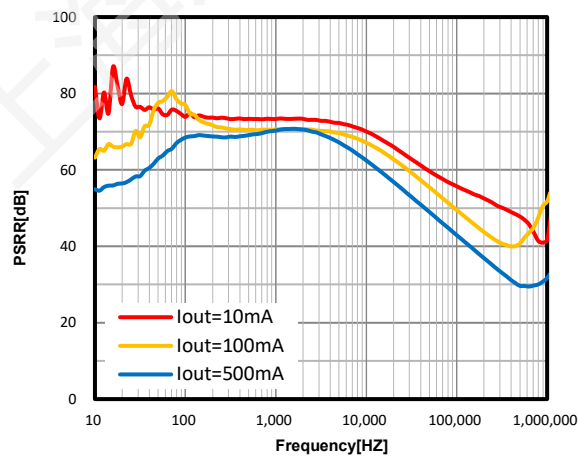
$V_{PP}=0.5V, C_{IN}=0.22\mu F, C_{OUT}=1\mu F, I_{OUT}=10mA$

Figure 39. PSRR vs Frequency



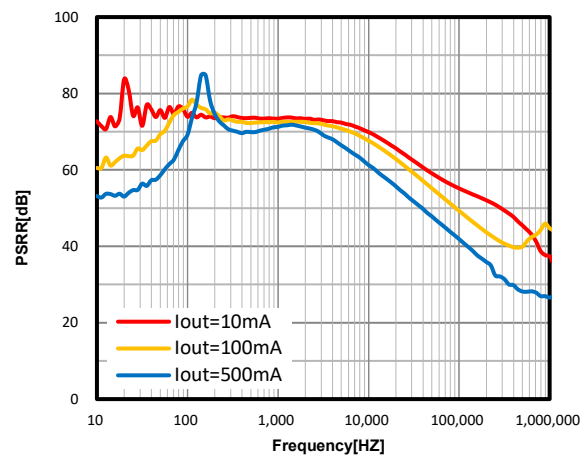
$V_{OUT}=0.8V, V_{IN}=2.0V, V_{PP}=0.5V, C_{IN}=0.22\mu F, C_{OUT}=1\mu F$

Figure 40. PSRR vs Frequency



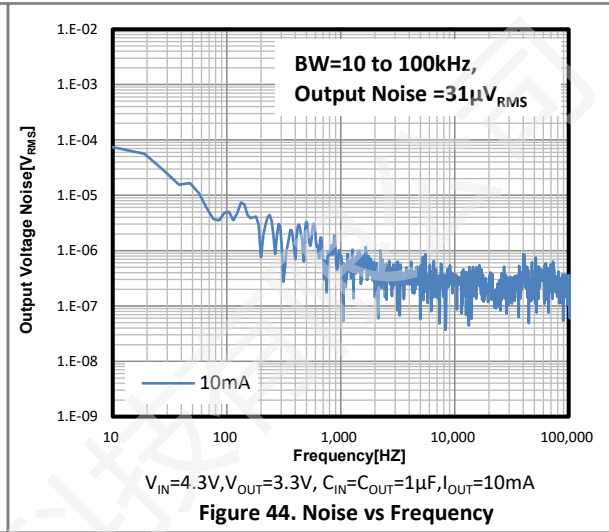
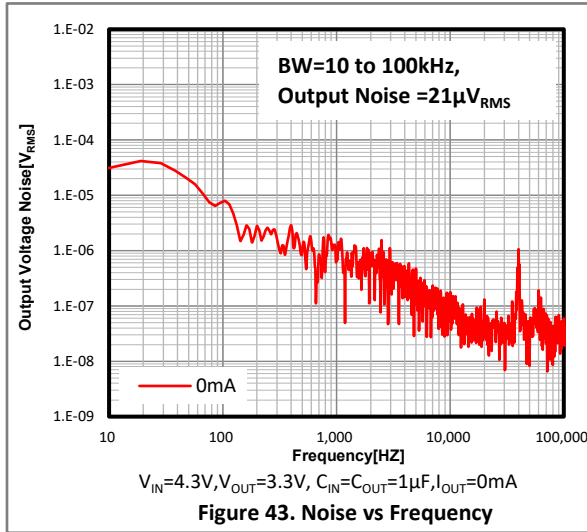
$V_{OUT}=3.3V, V_{IN}=4.3V, V_{PP}=0.5V, C_{IN}=0.22\mu F, C_{OUT}=1\mu F$

Figure 41. PSRR vs Frequency



$V_{OUT}=5.0V, V_{IN}=6.0V, V_{PP}=0.5V, C_{IN}=0.22\mu F, C_{OUT}=1\mu F$

Figure 42. PSRR vs Frequency



APPLICATION INFORMATION:

● Input Capacitor Selection

Like any low-dropout regulator, the external capacitors used with the LW81XX Series must be carefully selected for regulator stability and performance. Using a capacitor whose value is $\geq 1\mu\text{F}$ on the LW81XX Series input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

● Layout considerations

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device.

● Output Capacitor Selection

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LW81XX Series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ on the LW81XX Series output ensures stability. An appropriate output capacitor can reduce noise and improve load transient response and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of the LW81XX Series and returned to a clean analog ground.

ORDER INFORMATION:

LW81①②③④⑤⑥

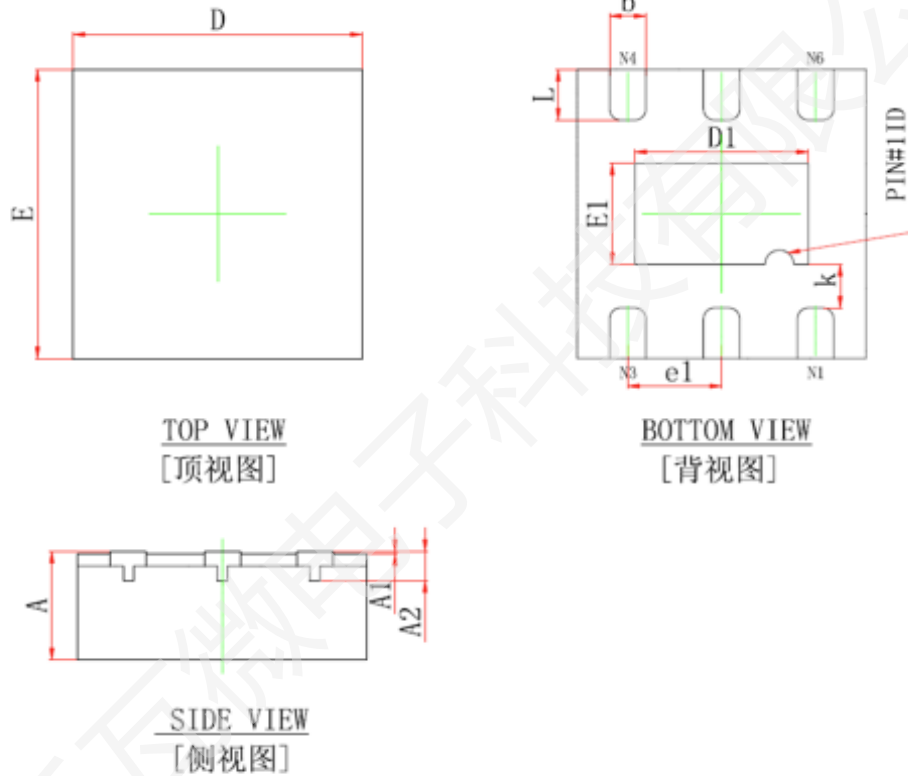
Designator	Item	Symbol	Description
①②	Output Voltage	08~50	e.g. 1.2V → ①=1, ②=2
③④⑤⑥	Packages	A22G	DFN2x2-6L(Type-A)
		A23E	SOT23-5L

Part #	Output Voltage	Package	Shipping
LW8108A22G	0.8V	DFN2x2-6L(Type-A)	3000 Pcs/ Tape & Reel
LW8112A22G	1.2V		
LW8115A22G	1.5V		
LW8118A22G	1.8V		
LW8128A22G	2.8V		
LW8130A22G	3.0V		
LW8133A22G	3.3V		
LW8136A22G	3.6V		
LW8142A22G	4.2V		
LW8150A22G	5.0V		
LW8108A23E	0.8V	SOT23-5L	3000 Pcs / Tape & Reel
LW8112A23E	1.2V		
LW8115A23E	1.5V		
LW8118A23E	1.8V		
LW8128A23E	2.8V		
LW8130A23E	3.0V		
LW8133A23E	3.3V		
LW8136A23E	3.6V		
LW8142A23E	4.2V		
LW8150A23E	5.0V		

If customers have special output voltage requirements, please contact us.

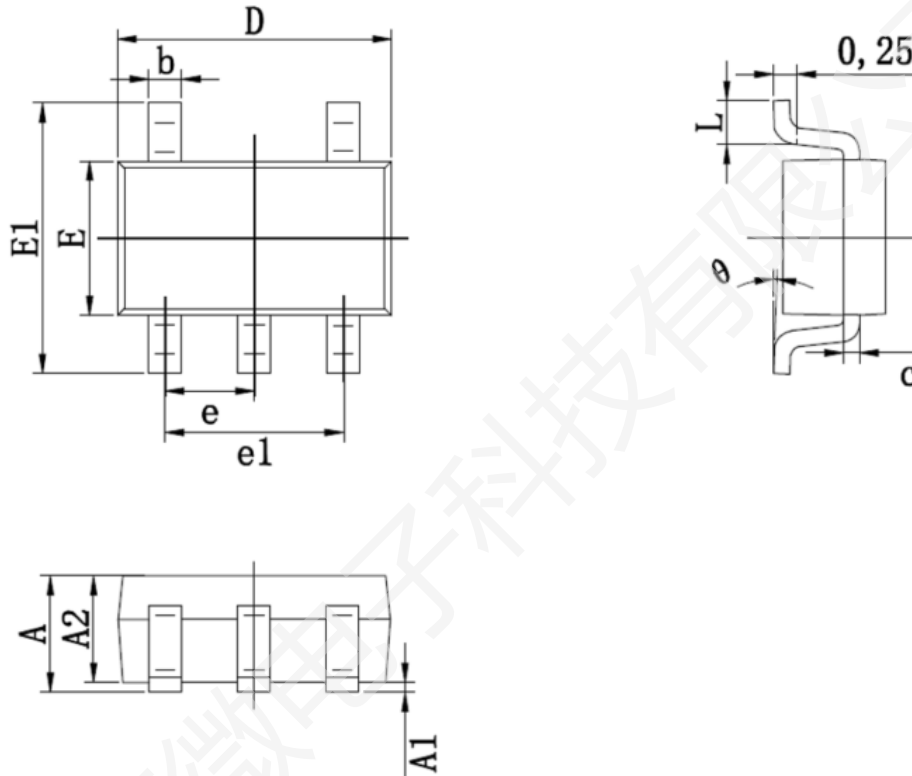
PACKAGE OUTLINE:

DFN2x2-6L Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	1.150	1.250	0.045	0.049
E1	0.650	0.750	0.026	0.030
b	0.200	0.300	0.008	0.012
e1	0.650TYP.		0.026TYP.	
k	0.200MIN.		0.008MIN.	
L	0.300	0.400	0.012	0.016

SOT23-5L Package



COMMON DIMENSION (MM)			
PKG	SOT23-5L		
Symbol	MIN	NOM	MAX
A	—	—	1.300
A1	0.010	—	0.150
A2	1.050	1.100	1.150
b	0.300	0.350	0.400
c	0.125	0.150	0.175
D	2.870	2.920	2.980
E	1.550	1.610	1.670
E1	2.650	2.850	3.000
e	0.95 BSC		
e1	1.800	1.900	2.000
L	0.300	0.450	0.600
θ	0°	4°	8°

Revision History:

Revision	Date	Descriptions
Rev 0.1	Sep.2023	Initial Version
Rev 1.0	Nov.2023	Formal Version
Rev 1.1	Sep.2026	Added some parameters for the 0.8V and 5V versions

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Mailing Address: Unit 02&04&05, 10th Floor, Building 5, No.666 Shengxia Road, No.122 Yindong Road,
China (Shanghai) Pilot Free Trade Zone
Shanghai Lewa Micro-electronics Technology Co., Ltd