GENERAL DESCRIPTION

The LW8400 is a high speed, high ripple rejection, fast discharge and low dropout voltage linear regulator.

The LW8400 consists of a voltage reference, an error amplifier, a driver transistor, a current limiter, a thermal protection circuit, a power-good circuit and a phase compensation circuit.

The LW8400 output voltage supports an externally adjustable output range of 0.8V to 5.0V, Which satisfies most advanced ICs which may require supply voltage to be 0.9V -1.2V.

The LW8400 has a power good state pin(PG) which used to indicate the status of the output voltage.

The LW8400 is available in DFN2x2-6L package.

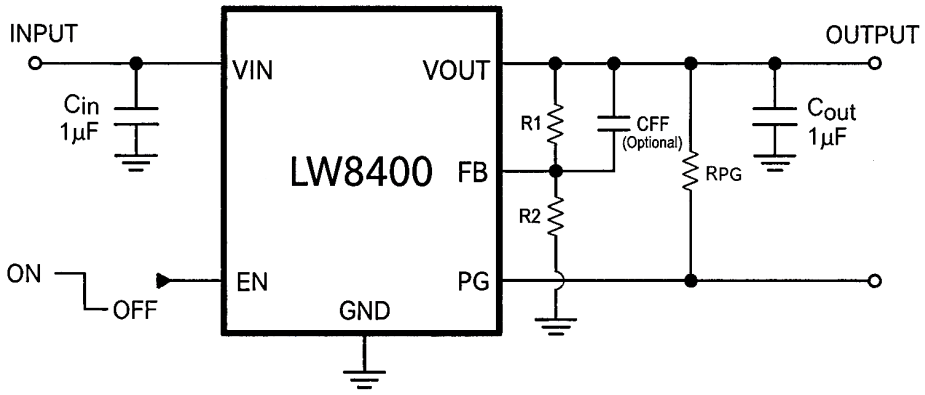
FEATURES

- Low Quiescent Current: 28μA(Typ.)
- Operating Voltage Range: from 1.8V to 7.0V
- Adjustable Output Voltage Range: from 0.8V to 5.0V
- Max Output Current: 1000mA
- Output Accuracy: ±1.0%@+25℃
- Low Dropout Voltage: 330mV@1000mA/3.3V
- High PSRR: 75dB@1kHz, 10mA
- Current Limiting Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Fast Discharge Function
- Excellent Line and Load Transient Response
- Support Power-Good Indicator Function
- Stable with 1μF Output Capacitor

APPLICATIONS

- Battery-Powered Devices
- Reference Voltage Sources
- USB products and HDMI Equipment
- Other Low Voltage Power Supplies

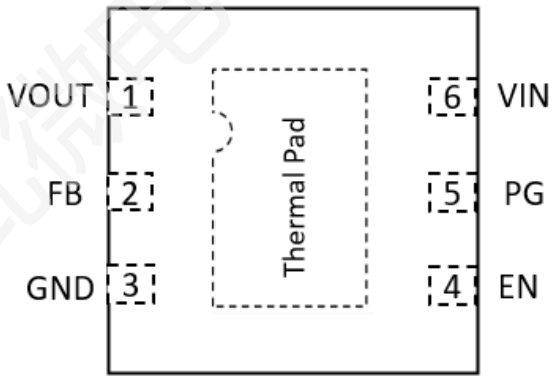
TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTION:

PIN No	SYMBOL	DESCRIPTION
1	VOUT	Output Voltage Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 1μF from V_{OUT} pin to ground.
2	FB	Output Feedback Connection. Connect FB to a resistor divider between OUT and GND to adjust the output voltage from 0.8V to 5.0V
3	GND	Ground pin.
4	EN	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
5	PG	Open-Drain PG Output. Pull-up PG to an external power supply. PG pulls low if FB drops below 82% of its set value. PG goes high after FB rises above 95% of its set value. The PG pin can be left floating if not used.
6	VIN	Input Voltage Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 1μF from V_{IN} pin to ground.
Thermal pad	--	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

PIN ASSIGNMENT:

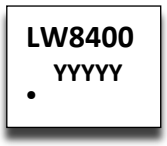


MARK INFORMATION:

DFN2x2-6L

XX: VOLTAGE

YY: DATE CODE



ABSOLUTE MAXIMUM RATINGS (1):

(T_A =25℃, unless otherwise specified.)

SYMBOL	ITEM	RATING	UNIT
V_{IN}	Supply Voltage	-0.3~8.0	V
V_{EN}	EN Pin Voltage	-0.3~8.0	V
V_{FB}	FB Pin Voltage	-0.3~8.0	V
V_{PG}	PG pin Voltage	-0.3~8.0	V
V_{OUT}	V_{OUT} pin Voltage	-0.3~ (V_{IN}+0.3)	V
$V_{(ESD)}$	ESD Susceptibility, HBM(2)	±2000	V
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance (3)	80	℃/W
T_J	Junction Temperature Range	-40~150	℃
T_{STG}	Storage Temperature Range	-40~150	℃
T_{SOLDER}	Lead Temperature (Soldering)	260℃, 10s	

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

2. per ANSI/ESDA/JEDEC JS-001

3. Device mounted on FR-4 PCB, Refer to JESD51-3 for detailed information on the board construction

RECOMMENDED OPERATING RANGE:

SYMBOL	ITEM	VALUE	UNIT
V_{IN}	V_{IN} Supply Voltage	1.8~7.0	V
V_{EN}	EN Pin Voltage	0~7.0	V
V_{FB}	FB Pin Voltage	0~7.0	V
V_{PG}	PG Pin Voltage	0~7.0	V
V_{OUT}	V_{OUT} Pin Voltage	0.8~5.0	V
I_{OUT}	Output Current	0~1.0	A
T_J	Junction Temperature Range	-40~125	℃

ELECTRICAL CHARACTERISTICS:

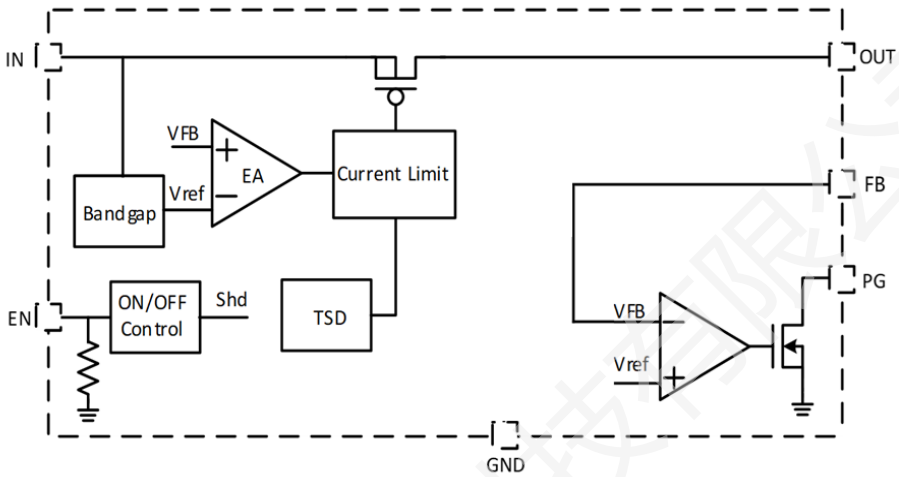
V_{IN}=$V_{OUT(NOM)}$+1V or +2V, whichever is greater, C_{IN}= C_{OUT}=1μF, unless otherwise specified, typical values are at T_A= 25℃.

Symbol	Parameter	Conditions		MIN	TYP	MAX	Units
V_{IN}	Input Voltage			1.8		7.0	V
V_{FB}	Feedback voltage(1)	V_{OUT}=V_{FB}			0.8		V
V_{OUT}	Output Accuracy	I_{OUT}= 1mA		-1.0		1.0	%
I_{LIM}	Current Limit(2)			1.1	1.45		A
I_Q	Quiescent Current	V_{OUT}=V_{FB} ,No Load			28	45	μA
I_{SHD}	Shutdown Current	V_{IN}=7.0V, V_{EN}=0V				0.1	μA
V_{DROP}	Dropout Voltage(2) (3)	V_{OUT}=3.3V	I_{OUT}=300mA		95		mV
			I_{OUT}=500mA		160		
			I_{OUT}=1000mA		330		
		V_{OUT}=5.0V	I_{OUT}=300mA		75		
			I_{OUT}=500mA		120		
			I_{OUT}=1000mA		250		
ΔV_{OUT}/ (ΔV_{IN}*$V_{OUT(NOM)}$)	Line Regulation	V_{IN}= V_{OUT} +1V to 7.0V, I_{OUT}=1mA			0.05	0.2	%/V
ΔV_{OUT}	Load Regulation	1mA≤I_{OUT}≤1000mA			10	60	mV
I_{SHORT}	Short Current	V_{OUT}=0V			100		mA
V_{ENH}	EN High Voltage	V_{IN}=1.8V to 7.0V, I_{OUT}=1mA		1.5			V
V_{ENL}	EN Low Voltage					0.5	V
T_{STR}	Startup Time	From V_{EN} 'L'→'H' to 95%*V_{OUT},No Load			50		μs
PSRR	Power Supply Rejection Ratio	V_{IN}= 4.3V, V_{OUT}=3.3V	f=217Hz		74		dB
		V_{PP}=0.5V,I_{OUT}=10mA	f=1KHz		75		
		C_{IN}=0.22μF,C_{OUT}=1μF	f=10KHz		70		
e_n	Output Voltage Noise	V_{IN}= V_{OUT}+1V f=10Hz to 100kHz	I_{OUT}=0mA		50×V_{OUT}		μV_{RMS}
			I_{OUT}=10mA		52×V_{OUT}		
PG_{HTH}	PG high threshold	V_{OUT} increasing		87	91	95	%V_{OUT}
PG_{LTH}	PG low threshold	V_{OUT} decreasing		82	86	90	%V_{OUT}
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT}＜PG_{LTH}, I_{SINK} =1mA			120	400	mV
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT}＞PG_{HTH}, V_{PG} = 7.0 V				500	nA
t_{PGDH}	PG delay time rising	Time from 92% V_{OUT} to 20% of PG			200		μs
t_{PGDL}	PG delay time falling	Time from 90% V_{OUT} to 80% of PG			5		μs
T_{SD}	Thermal Shut Down	Temperature rising			160		℃
△T_{SD}	TSD Hysteresis	Temperature falling			20		℃

NOTES:

1. When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
2. Guaranteed by design
3. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} =95%*$V_{OUT(NOM)}$

SIMPLIFIED BLOCK DIAGRAM:



DETAIL OPERATION DESCRIPTION:

The LW8400 is a low noise, high PSRR, low drop-out voltage regulator. It consists of a current limiter circuit, a driver transistor, a precision voltage reference, a thermal protection circuit, a reverse current protection circuit and an error correction circuit, and is compatible with low ESR ceramic capacitors. The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold through the switch. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

Thermal Shutdown

When the junction temperature of the built-in driver transistor reaches the temperature limit level (160℃ TYP.), the thermal shutdown circuit operates and the driver transistor will be turned OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of 140℃ (TYP.) as the thermal shutdown release threshold.

Chip Enable

The LW8400 can be turned off via the EN pin signal. In shutdown mode, output at the V_{OUT} pin will be pulled down to the GND. The LW8400 has a pull-down resistor in order to operate normally even the EN pin is floating. If the EN pin voltage is set with the specified voltage range, the logic is fixed and the IC will operate normally.

Power-Good Function

The power-good circuit monitors the voltage at the V_{OUT} pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds PG_{HTH}, the PG pin becomes high impedance. By connecting a pull-up resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device. Using a pull-up resistor from 10 kΩ to 100 kΩ is recommended.

TYPICAL OPERATING CHARACTERISTICS:

(Tested under T_A =25°C,C_{IN}= C_{OUT}=1μF,unless otherwise specified)

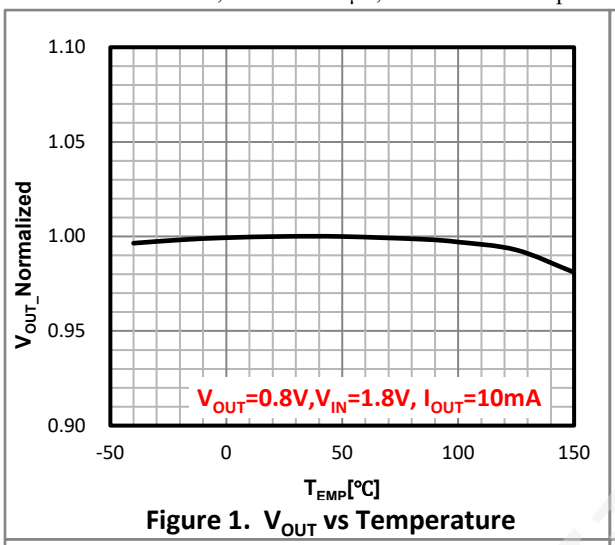


Figure 1. V_{OUT} vs Temperature

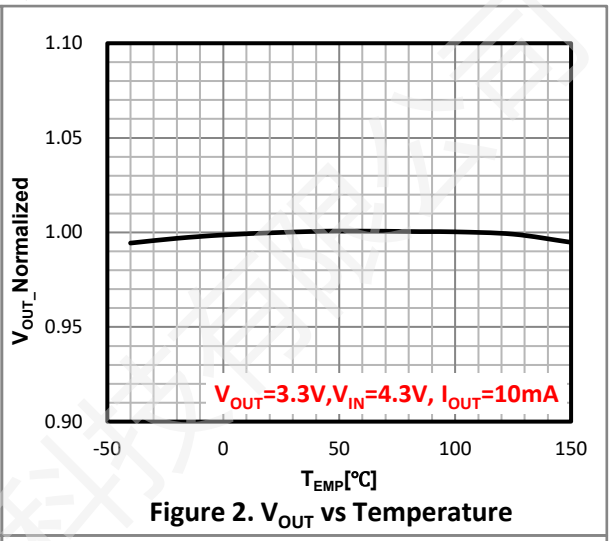


Figure 2. V_{OUT} vs Temperature

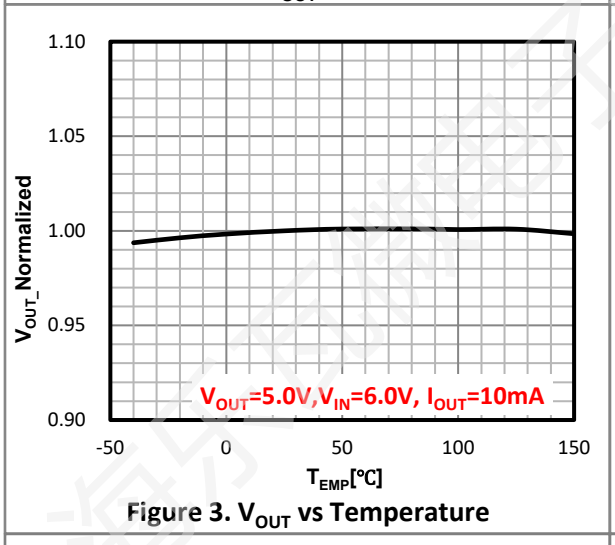


Figure 3. V_{OUT} vs Temperature

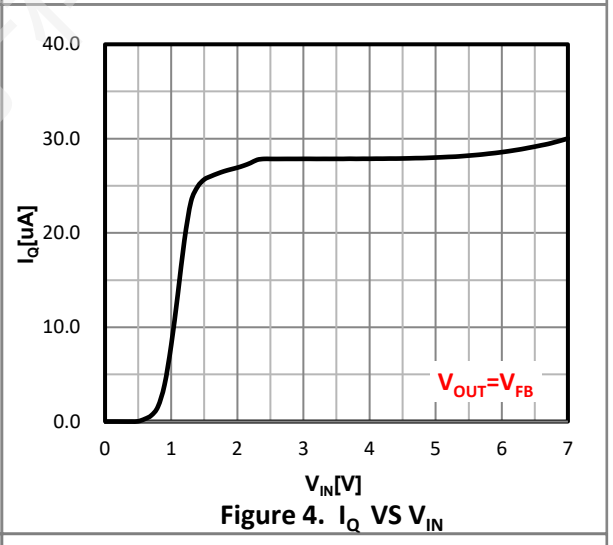


Figure 4. I_Q VS V_{IN}

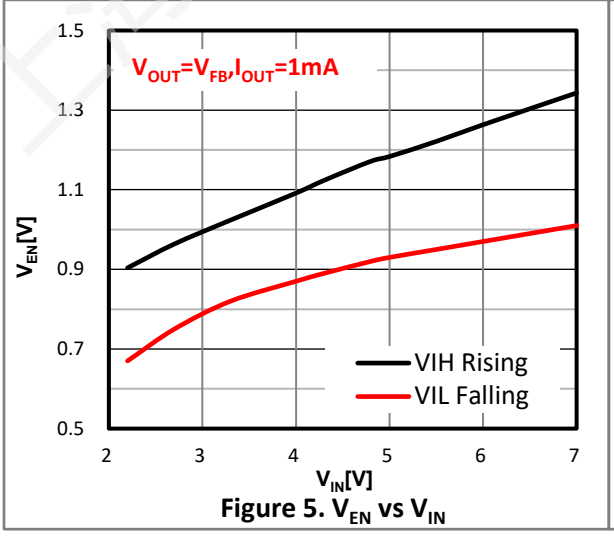


Figure 5. V_{EN} vs V_{IN}

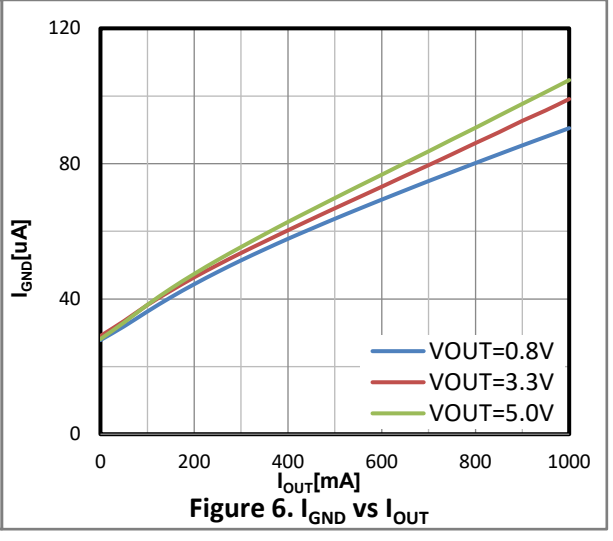


Figure 6. I_{GND} vs I_{OUT}

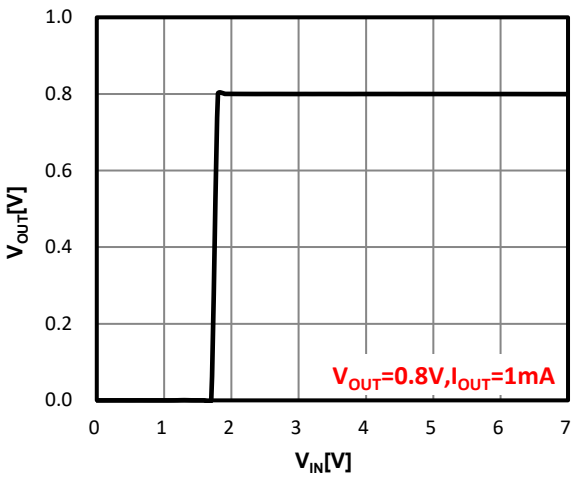


Figure 7. V_{OUT} vs V_{IN}

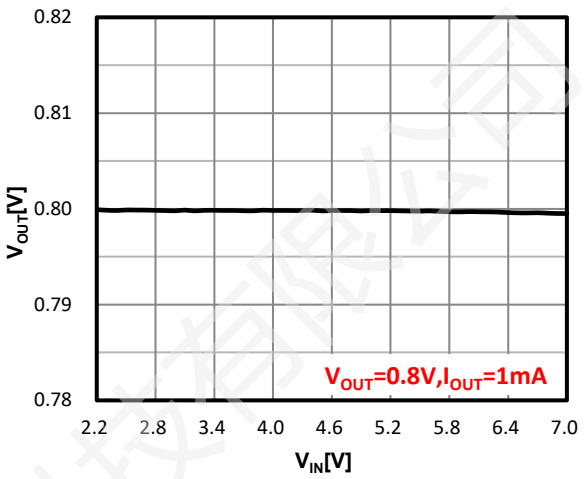


Figure 8. Line Regulation

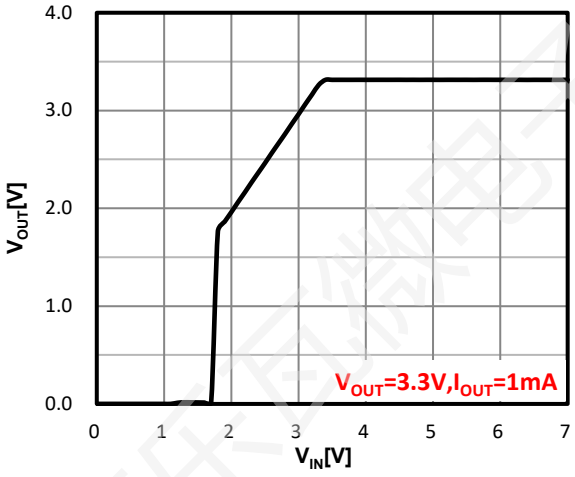


Figure 9. V_{OUT} vs V_{IN}

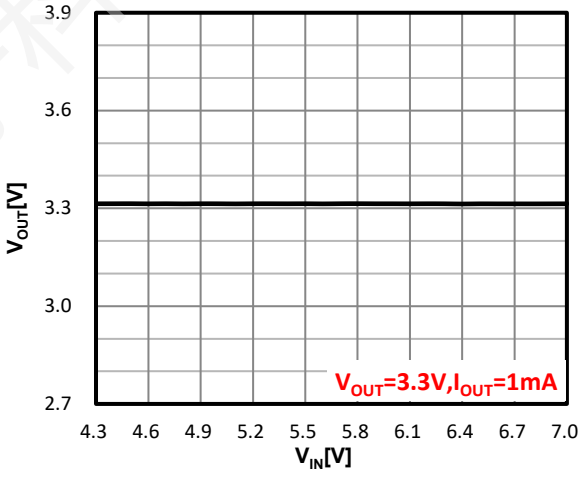


Figure 10. Line Regulation

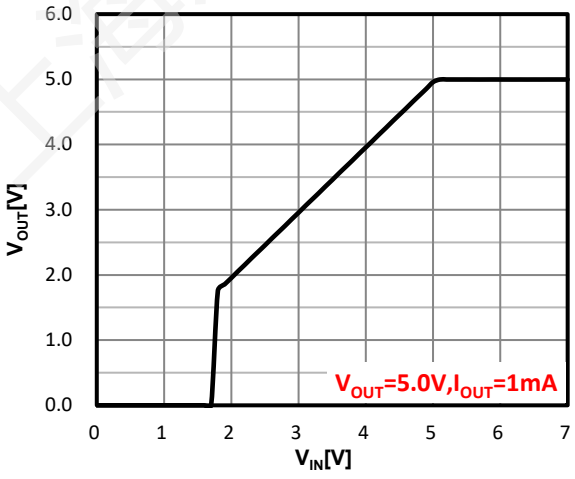


Figure 11. V_{OUT} vs V_{IN}

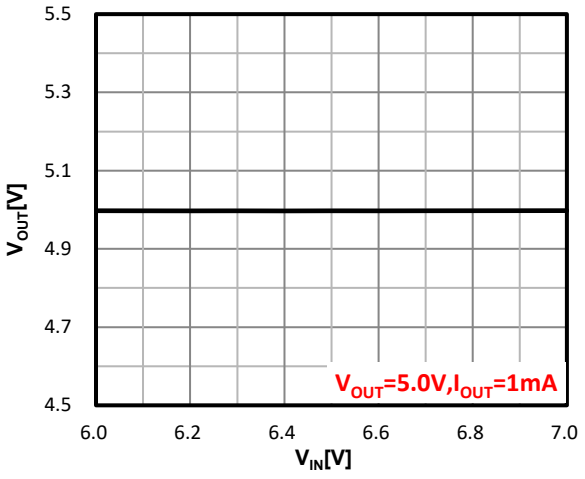


Figure 12. Line Regulation

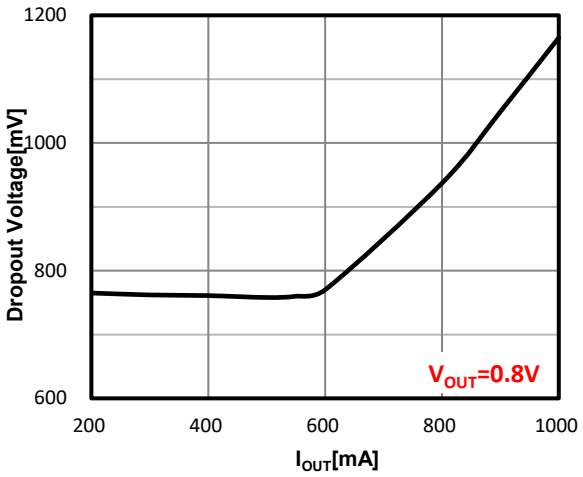


Figure 13. Dropout Voltage VS I_{OUT}

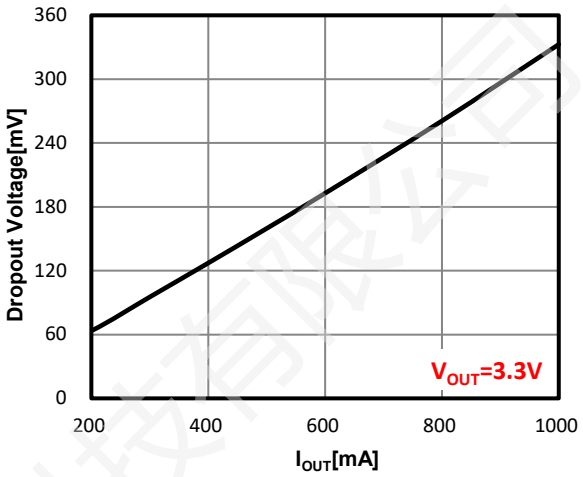


Figure 14. Dropout Voltage VS I_{OUT}

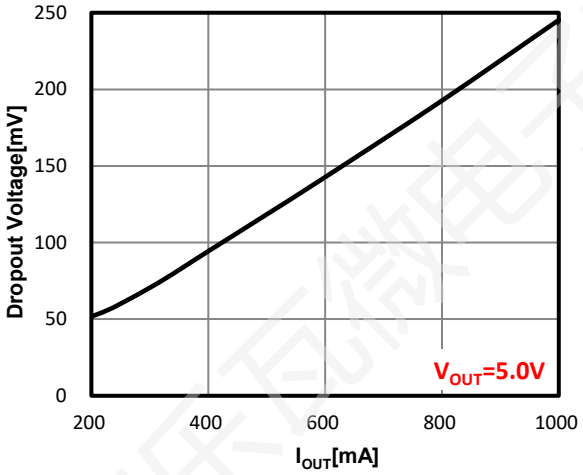


Figure 15. Dropout Voltage VS I_{OUT}

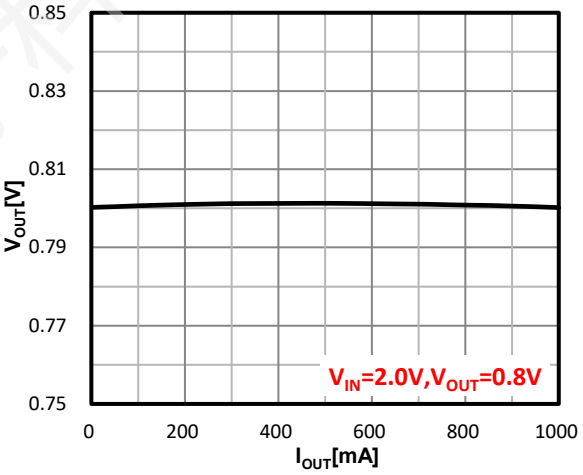


Figure 16. Load Regulation

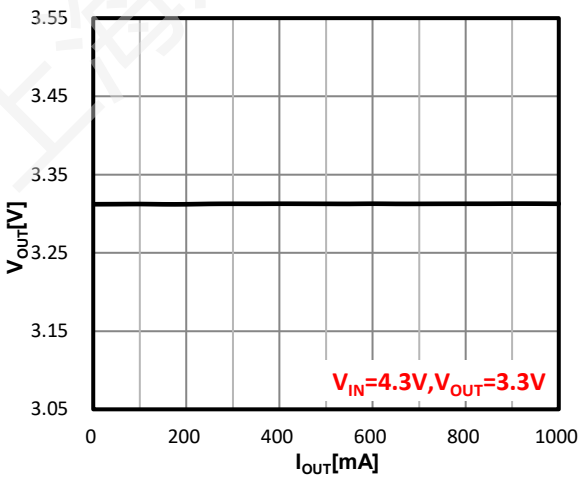


Figure 17. Load Regulation

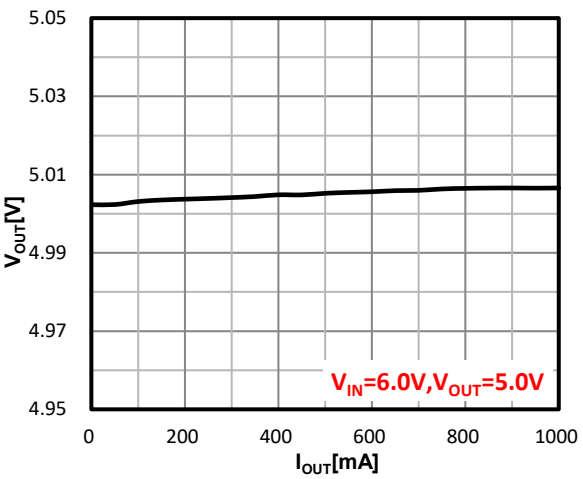
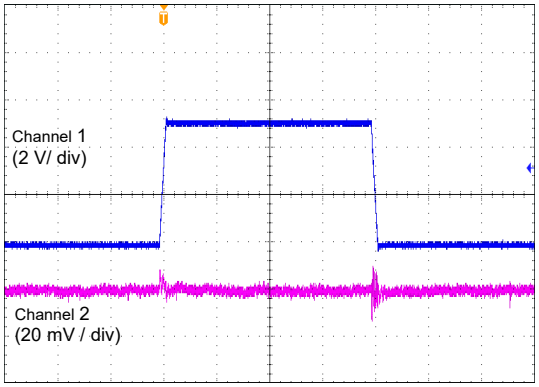


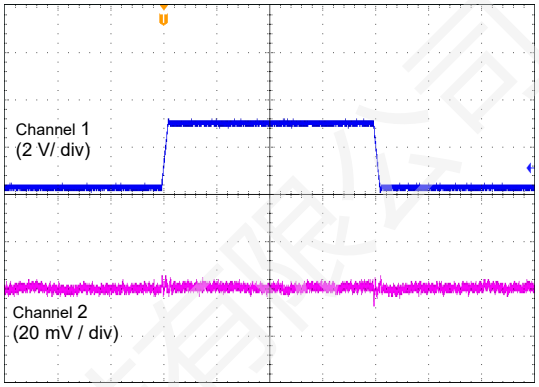
Figure 18. Load Regulation



Time (100µs / div)

Channel 1 = V_{IN}, channel 2 =V_{OUT}, V_{IN}=1.8V→7.0V,
t_R=t_F=10µs, V_{OUT}=0.8V, I_{OUT}=10mA

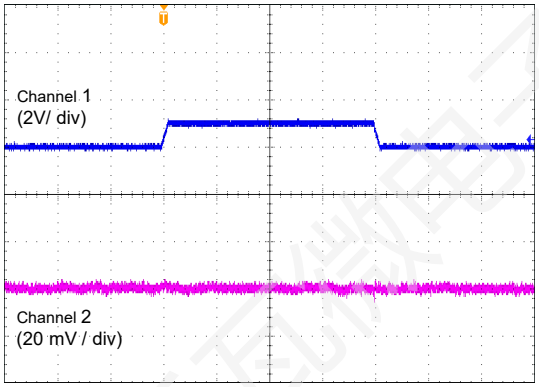
Figure 19. Line Transient



Time (100µs / div)

Channel 1 = V_{IN}, channel 2 =V_{OUT}, V_{IN}=4.3V→7.0V,
t_R=t_F=10µs, V_{OUT}=3.3V, I_{OUT}=10mA

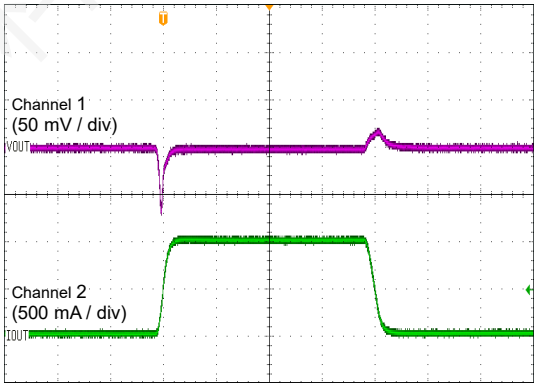
Figure 20. Line Transient



Time (100 µs / div)

Channel 1 = V_{IN}, channel 2 =V_{OUT}, V_{IN}=6.0V→7.0V,
t_R=t_F=10µs, V_{OUT}=5.0V, I_{OUT}=10mA

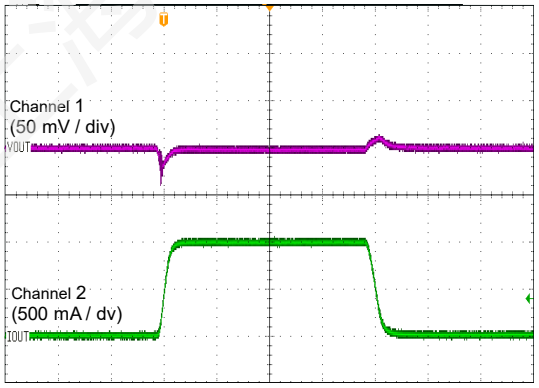
Figure 21. Line Transient



Time (40 µs / div)

Channel 1 = V_{OUT}, channel 2 =I_{OUT}, V_{IN}=2.0V, V_{OUT}=0.8V
C_{IN}=C_{OUT}=1µF

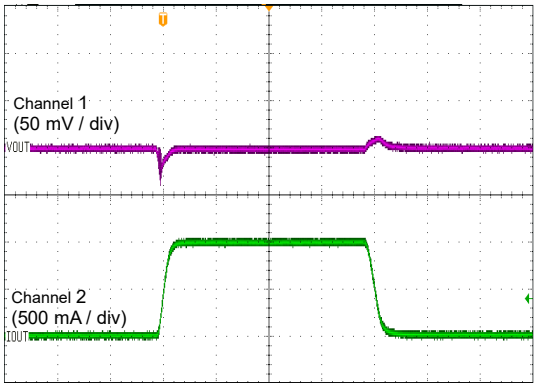
Figure 22. Load Transient (1 mA to 1A)



Time (40 µs / div)

Channel 1 = V_{OUT}, channel 2 =I_{OUT}, V_{IN}=4.3V, V_{OUT}=3.3V
C_{IN}=C_{OUT}=1µF

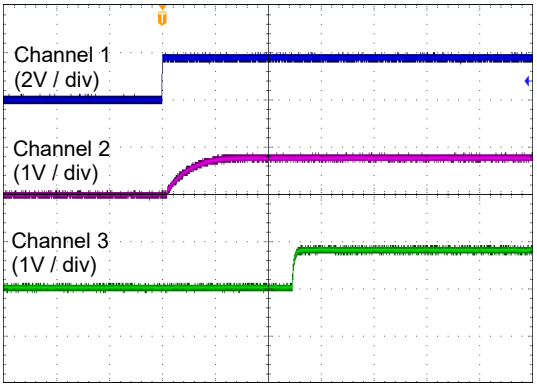
Figure 23. Load Transient (1 mA to 1A)



Time (40 µs / div)

Channel 1 = V_{OUT}, channel 2 =I_{OUT}, V_{IN}=6.0V, V_{OUT}=5.0V
C_{IN}=C_{OUT}=1µF

Figure 24. Load Transient (1 mA to 1A)

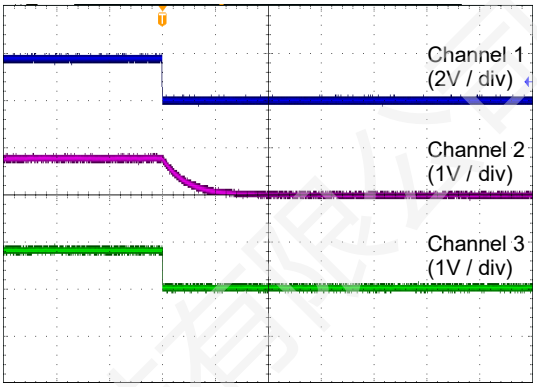


Time (100 µs / div)

Channel 1 = EN Channel 2 =V_{OUT} Channel 3 =PG

V_{IN}=1.8V,EN=0→1.8V,V_{OUT}=0.8V,C_{IN}=C_{OUT}=1µF,R_L=100Ω

Figure 25. Power-Up with Enable

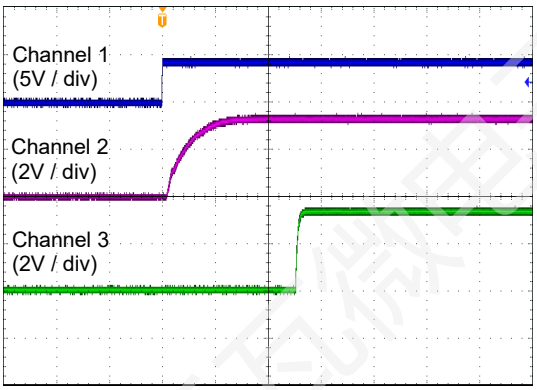


Time (100 µs / div)

Channel 1 = EN Channel 2 =V_{OUT} Channel 3 =PG

V_{IN}=1.8V,EN=1.8→0V,V_{OUT}=0.8V,C_{IN}=C_{OUT}=1µF,R_L=100Ω

Figure 26. Shut-Down with Enable

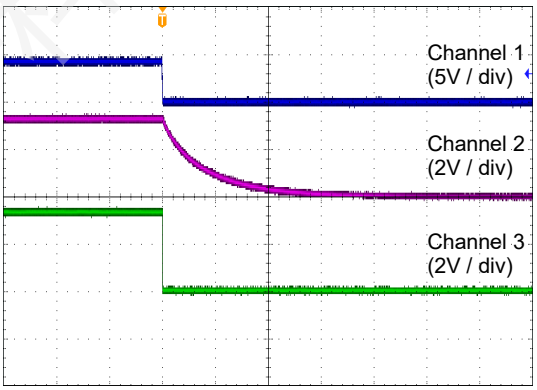


Time (100 µs / div)

Channel 1 = EN Channel 2 =V_{OUT} Channel 3 =PG

V_{IN}=4.3V,EN=0→4.3V,V_{OUT}=3.3V,C_{IN}=C_{OUT}=1µF,R_L=100Ω

Figure 27. Power-Up with Enable

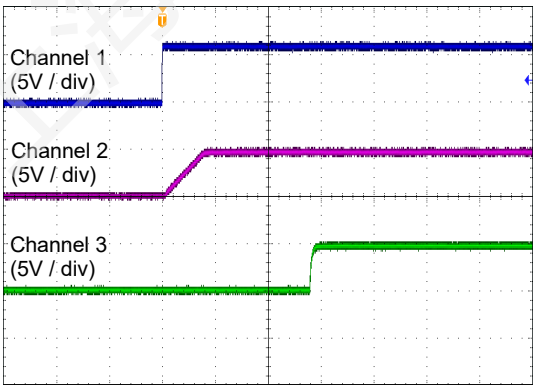


Time (100 µs / div)

Channel 1 = EN Channel 2 =V_{OUT} Channel 3 =PG

V_{IN}=4.3V,EN=4.3→0V,V_{OUT}=3.3V,C_{IN}=C_{OUT}=1µF,R_L=100Ω

Figure 28. Shut-Down with Enable

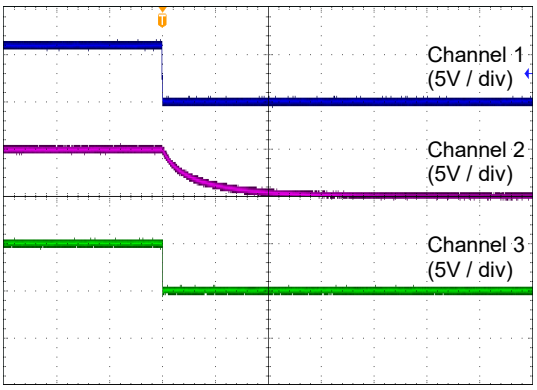


Time (100 µs / div)

Channel 1 = EN Channel 2 =V_{OUT} Channel 3 =PG

V_{IN}=6.0V,EN=0→6.0V,V_{OUT}=5.0V,C_{IN}=C_{OUT}=1µF,R_L=100Ω

Figure 29. Power-Up with Enable

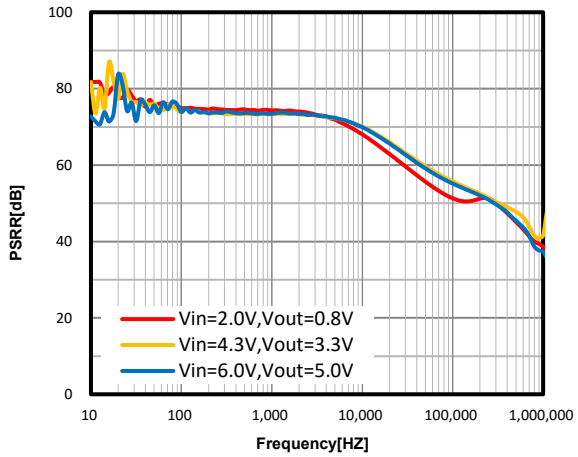


Time (100 µs / div)

Channel 1 = EN Channel 2 =V_{OUT} Channel 3 =PG

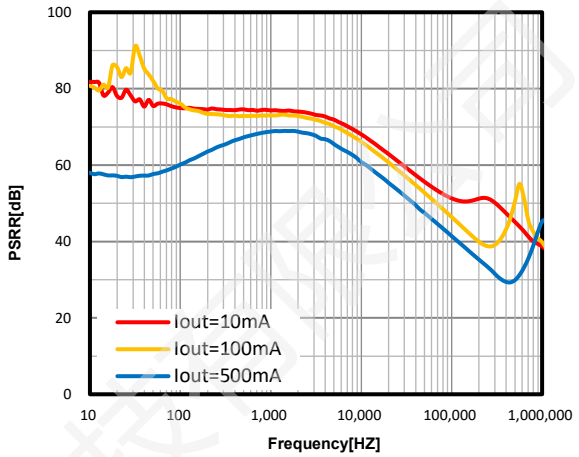
V_{IN}=6.0V,EN=6.0→0V,V_{OUT}=5.0V,C_{IN}=C_{OUT}=1µF,R_L=100Ω

Figure 30. Shut-Down with Enable



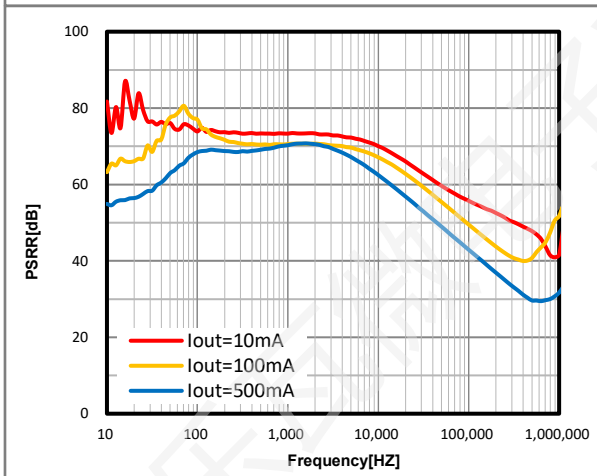
V_{PP}=0.5V,C_{IN}=0.22μF,C_{OUT}=1μF,I_{OUT}=10mA

Figure 31. PSRR vs Frequency



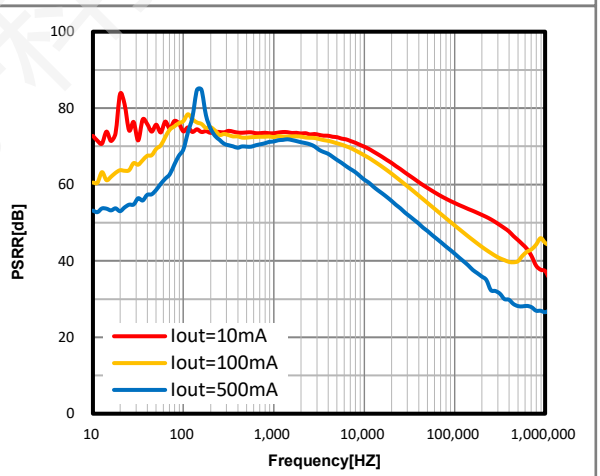
V_{OUT}=0.8V, V_{IN}=2.0V, V_{PP}=0.5V,C_{IN}=0.22μF,C_{OUT}=1μF

Figure 32. PSRR vs Frequency



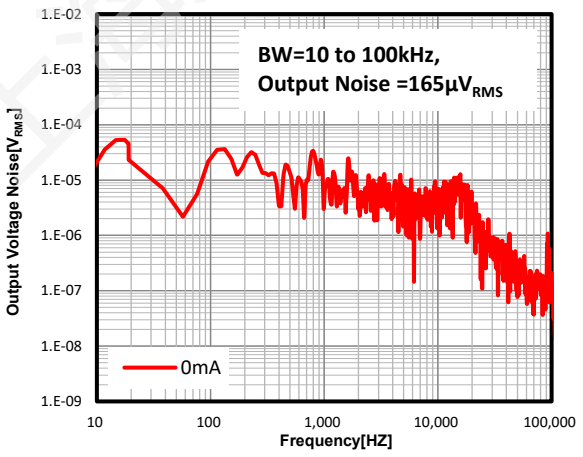
V_{OUT}=3.3V, V_{IN}=4.3V, V_{PP}=0.5V, C_{IN}=0.22μF,C_{OUT}=1μF

Figure 33. PSRR vs Frequency



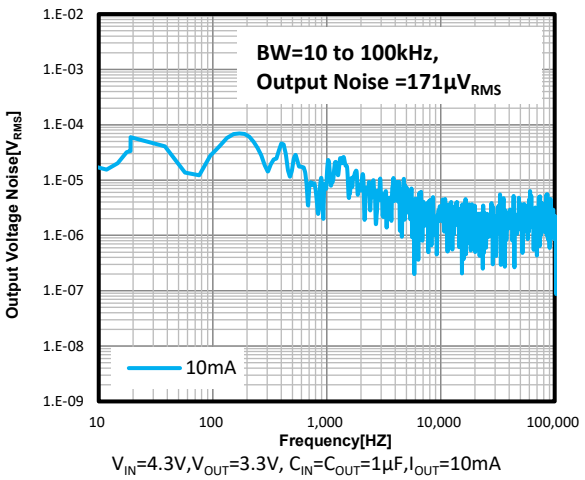
V_{OUT}=5.0V, V_{IN}=6.0V, V_{PP}=0.5V, C_{IN}=0.22μF,C_{OUT}=1μF

Figure 34. PSRR vs Frequency



V_{IN}=4.3V,V_{OUT}=3.3V, C_{IN}=C_{OUT}=1μF,I_{OUT}=0mA

Figure 35. Noise vs Frequency



V_{IN}=4.3V,V_{OUT}=3.3V, C_{IN}=C_{OUT}=1μF,I_{OUT}=10mA

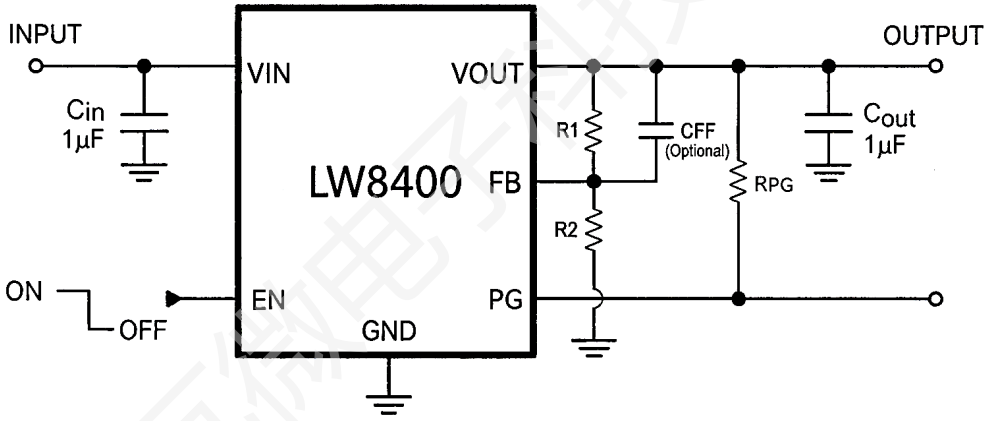
Figure 36. Noise vs Frequency

APPLICATION INFORMATION:

NOTE

Information in the following applications sections is not part of the Lewa component specification, and LW-Micro does not warrant its accuracy or completeness. LW-Micro's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

- **Adjustable Device Feedback Resistors**



The LW8400 requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following Equation ①:

$$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2}) \quad ①$$

Note: To ensure that the output voltage is not affected by the I_{FB} value, the resistance value of the voltage divider resistor needs to satisfy the following Equation ②:

$$R_1 + R_2 \leq V_{OUT}/(100 \times I_{FB}) \quad ②$$

- **Feed-Forward Capacitor (C_{FF})**

For the adjustable-voltage device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. The higher capacitance C_{FF} can be used; however, the startup time increases.

- **Input and Output Capacitor Selection**

Like any low-dropout regulator, the external capacitors used with The LW8400 must be carefully selected for regulator stability and performance. Using a capacitor whose value is ≥1μF on The LW8400 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

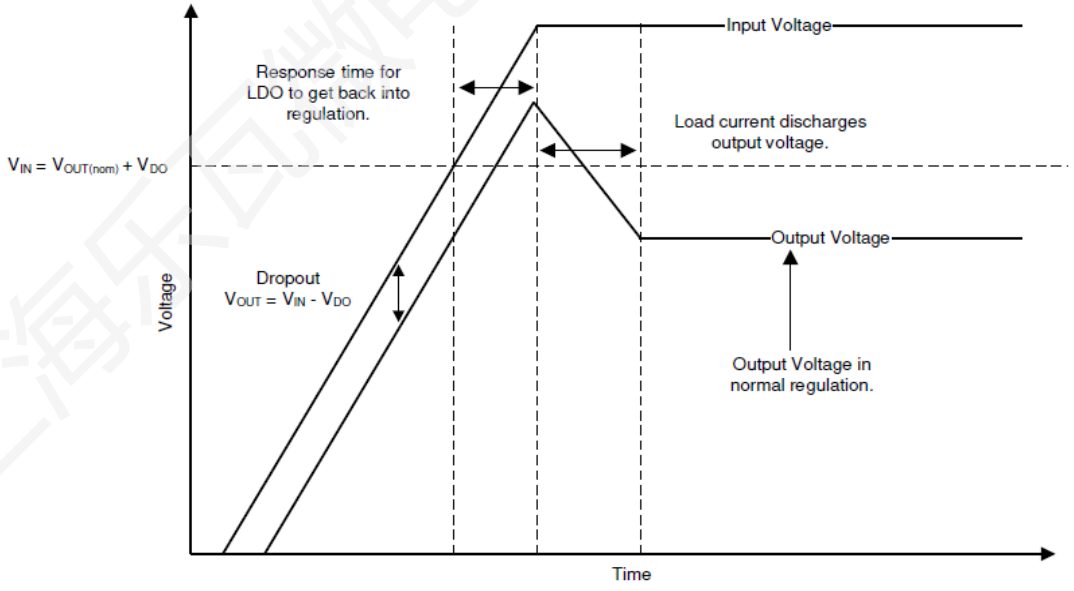
The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LW8400 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF on The LW8400 output ensures stability. An appropriate output capacitor can reduce noise and improve load transient response and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of The LW8400 and returned to a clean analog ground.

- **Dropout Voltage**

The LW8400 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (VDO), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. VDO scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

- **Exiting Dropout**

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in the following picture, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.



- **Power Dissipation (P_D)**

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation ③ calculates power dissipation (P_D).

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) \quad ③$$

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation ④, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad ④$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the Thermal Information table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

- **Power-Good Function**

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds PG_{HTH}, the PG pin becomes high impedance. The open-drain output requires a pullup resistor. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing.

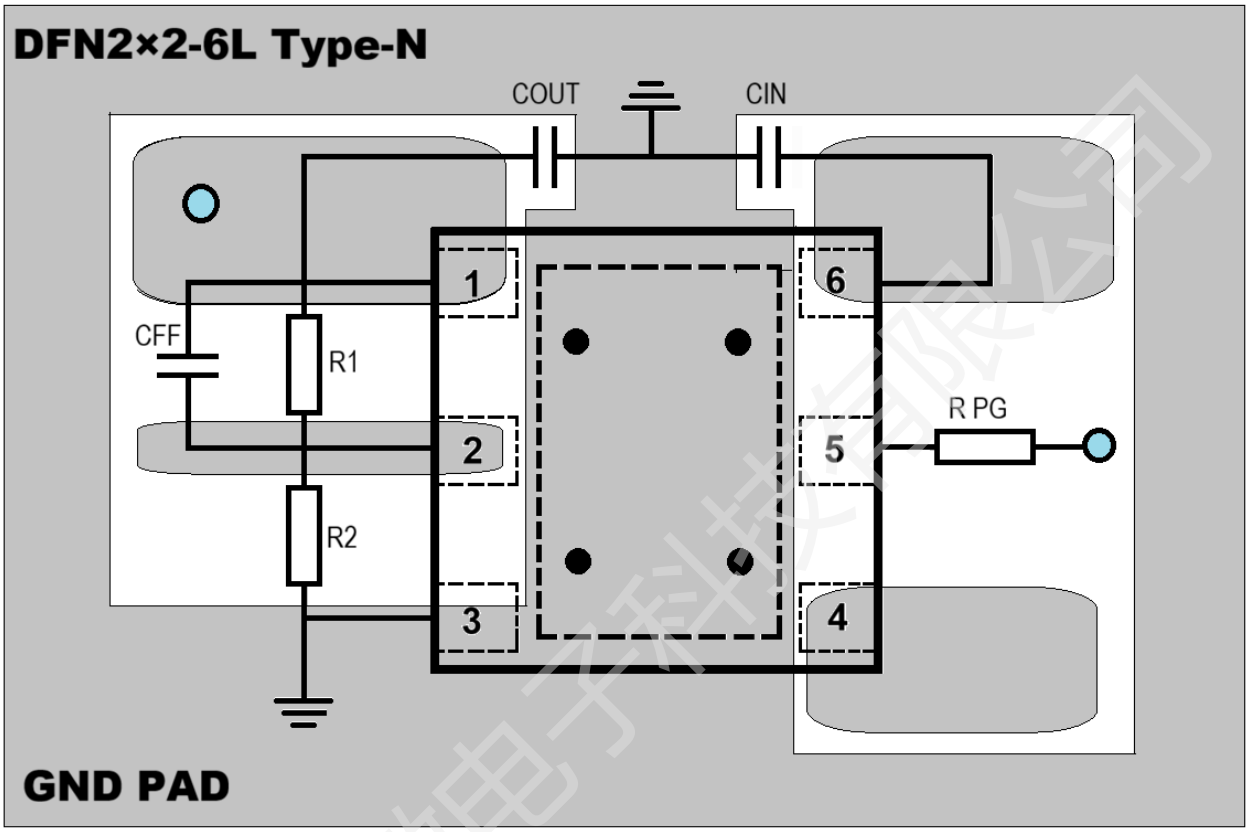
Additionally, the open-drain output can be tied to other open-drain outputs to implement AND logic. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended.

When using a feed-forward capacitor (C_{FF}), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note.

The state of PG is only valid when the device operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the V_{ENL}. When the input voltage falls below V_{ENL}, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

- **Layout Guidelines**

1) Place input and output capacitors as close to the device as possible.
2) Use copper planes for device connections in order to optimize thermal performance.
3) Place thermal vias around the device to distribute heat.
4) Place a tented thermal via directly beneath the thermal pad of the package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to acompromised solder joint on the thermal pad.



ORDER INFORMATION:

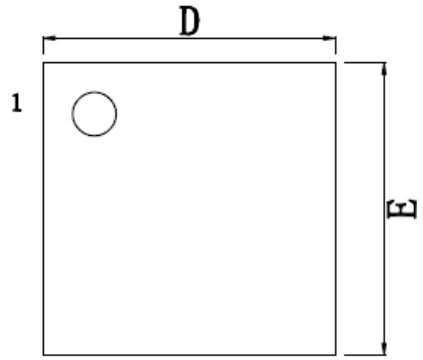
LW8400①②③④

Designator	Item	Symbol	Description
①②③④	Packages	N22G	DFN2x2-6L(Type-N)

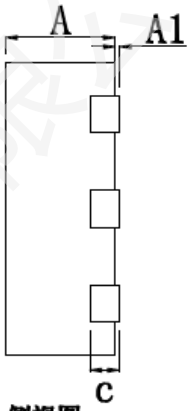
Part #	Output Voltage	Package	Shipping
LW8400N22G	Adj.	DFN2x2-6L	3000 Pcs/ Tape & Reel

PACKAGE OUTLINE:

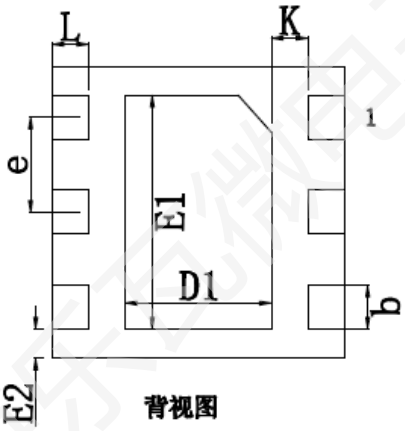
DFN2x2-6L Package



俯视图



侧视图



背视图

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.25	0.30	0.35
c	0.203 TYP		
D	1.95	2.00	2.05
D1	0.90	1.00	1.10
E	1.95	2.00	2.05
E1	1.55	1.60	1.65
E2	0.20 REF		
e	0.65 BSC		
K	0.25 REF		
L	0.20	0.25	0.30

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Revision History:

Revision	Date	Descriptions
Rev 0.1	Sep.2023	Initial Version
Rev 1.0	Nov.2024	Formal Version
Rev 1.1	Feb.2025	Update Applycation information
Rev 1.2	Sep.2026	Added some parameters for the 0.8V and 5V versions

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