

PRODUCT SPECIFICATION

C u s t o m e r : _____
P r o d u c t N a m e : Contactless Reader/Writer IC
P a r t N O : NF522
I s s u e D a t e : _____

Prepared	Checked	Customer Check
ChenTT	Zelig	

NF522 Universal Contactless RFID Reader Chip

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1. Product Overview

1.1 Product Description

NF522 is a highly integrated contactless reader that operates at 13.56MHz , it supports the following three protocol operating modes.

- > Supports ISO/IEC14443 TYPEA protocol reader mode
- > Supports ISO/IEC14443 TYPEB protocol reader mode
- > Supports ISO15693 protocol reader mode

NF522 has the features of low voltage, low power consumption, multi-interface and multi-protocol support. It is suitable for low power consumption, low voltage, low cost contactless reader applications.

1.2 Product Characteristics

Reader

- Supports ISO/IEC14443 TYPEA protocol reader mode
- Supports ISO/IEC14443 TYPEB protocol reader mode
- Supports ISO15693 protocol reader mode
- Supports M1 encryption
 - ISO14443 TYPEA Support communication rate 106kbps 、 212kbps 、 424kbps 、 848kbps
 - ISO14443 TYPEB Support communication rate 106kbps 、 212kbps 、 424kbps 、 848kbps
- ISO15693 supports single and dual subcarrier modes, with a maximum rate of 52.97kbps for single subcarrier and 26.69kbps for dual subcarrier.
- Reader operating distance up to 100mm

Low Power Mode

- Hard powerdown mode
- Soft powerdown mode
- Lpcd power card detection mode

Internal low-power ring oscillator external field RF voltage detection circuit

Clock and Peripheral Interface

- Internal oscillator circuit with external 27.12MHz crystal
- Pin-multiplexing design supports multiple host interfaces
- SPI up to 9Mbps
- I2C supports fast mode up to 400Kbps and hardware address programmable mode
- Serial UART , supports RS232 frame format, maximum communication rate 1.2Mbps
- Independent power supply for Host

RF transmitter driver is powered by a separate power supply up to 5.5V

- 64Byte transmit and receive buffer FIFO
- Configurable CRC16 data check algorithm
- Multi-function programmable timer
- Flexible interrupt output modes available

Operating Temperature: -40 °C to +125 °C (Industrial Grade)

1.3 Package Pinout

1.3. 1 NF522 package pinout

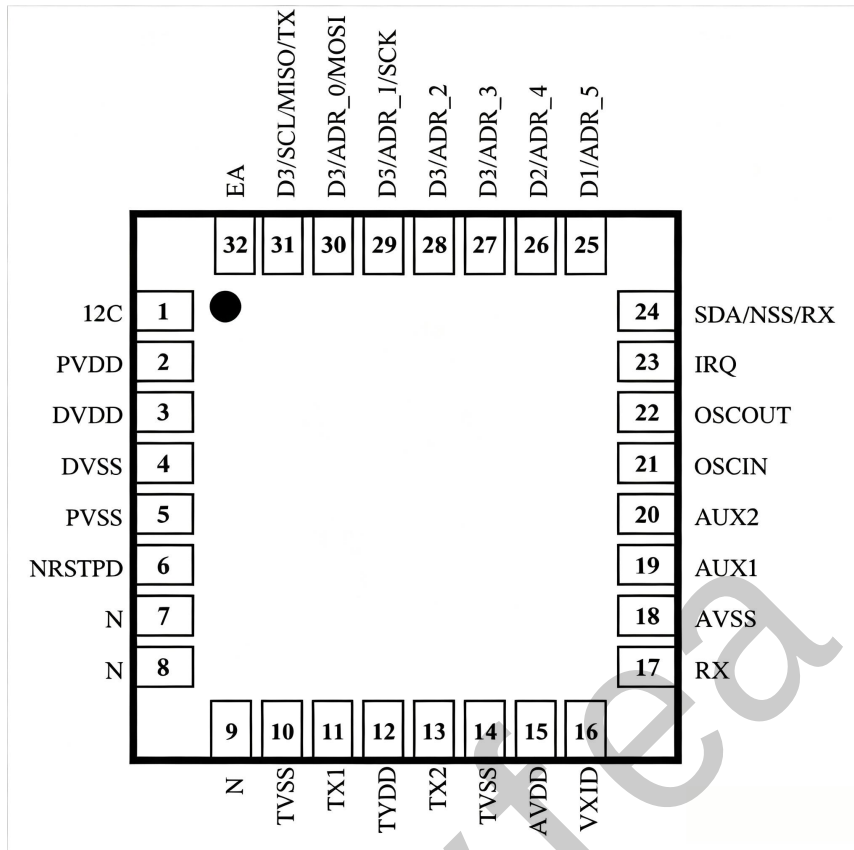


Figure 1-1NF522 QFN Package Pinout Diagram

1.3.2 Pin Definitions

PinNumber	Pin Name	Pin Type	Function
1	I2C	I	Communication type control selection
2	PVDD	P	Pin Power Supplies
3	DVDD	P	Digital Power Supply
4	DVSS	G	Digital Ground
5	PVSS	G	Pin Power Ground
6	NRSTPD	I	Reset and power-down inputs: Power-down: enabled when off; internal current sink turned off, oscillator is inhibited and input pins are disconnected from the external world Reset: active on rising edge

7	–	–	None
8	–	–	None
9	–	–	None
10	TVSS	G	Transmitter Output Stage 1 Ground
11	TX1	O	Transmitter 1 Modulated 13.56 MHz Energy Carrier Output
12	TVDD	P	Transmitter power supply power
13	TX2	O	Transmitter 2 Modulated 13.56 MHz energy carrier output
14	TVSS	G	Transmitter output stage 2 ground
15	AVDD	P	Analogue power supply
16	VMID	P	Internal Reference Voltage
17	RX	I	RF signal input
18	AVSS	G	Analogue ground
19	AUX1	O	Test Use
20	AUX2	O	Test Use
21	OSCIN	I	Input to the inverting amplifier of the crystal oscillator; also the externally; Input of the externally generated clock (fclk = 27.12MHz)
22	OSCOU	O	Output of the inverting amplifier of the crystal oscillator.
23	IRQ	O	Interrupt request output: indicates an interrupt event
24	SDA/NSS/RX	I/O	Serial data input and output lines for standard two-wire serial. SPI signal input UART data input
25	D1/ADR_5	I/O	Test Port IIC Bus Address 5
26	D2/ADR_4	I/O	Test Port IIC Bus Address 4
27	D3/ADR_3	I/O	Test Port IIC Bus Address 3
28	D4/ADR_2	I/O	Test Port IIC Bus Address 2
29	D5/ADR_1/SCK	I/O	Test Port IIC Bus Address 1 SPI Serial Clock Input
30	D6/ADR_0/MO SI	I/O	Test Port IIC Bus Address 0 SPI master output, slave input

31	D7/SCL/MISO/ TX	I/O	Test Port IIC Bus Address SPI host input, slave output UART data output
32	EA	I	Communication Interface Type Control Selection

1 Pin Type: I=Input, O=Output, I/O=Input/Output, P=Power, G=Ground

2. NF522 Register

2.1 Register Description

2.1.1 Page 0 Command and Status

2.1.1.1 CommandReg_address 01h Start and stop command execution.

Bit	7	6	5	4	3	2	1	0
Definition	Aldo_en	Power_en	Command					
Bit Weight	r/w	dy	dy	dy	dy	dy	dy	dy
Reset Value	1	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	Aldo_en	Analogue Power Switch
6	Power_en	Standby Enable
5-0	Command	Instruction register that activates an instruction based on the instruction code written by the master. Read this register for feedback on the instruction being executed.

2.1.1.2 Interrupt EnReg_address 02h

Interrupt request enabled

Bit	7	6	5	4	3	2	1	0
Definition	IrqIn v	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	IRqInv	Set to 1, the signal of pin IRQ is set to the inverse of the IRq bit in Register Status1Reg. Set to 0, the signal at pin IRQ is the same as the IRq bit.
6	TxIEn	Allows transmitter interrupt requests (indicated by the TxIRq bit) to be passed to pin IRQ.
5	RxIEn	Allow receiver interrupt requests (indicated by the RxIRq bit) to be passed to pin IRQ.
4	IdleIEn	Allow idle interrupt requests (indicated by the IdleIRq bit) to be passed to pin IRQ
3	HiAlertIEn	Allow a fill interrupt request (indicated by the HiAlertIEn bit) to be passed to pin IRQ
2	LoAlertIEn	Allow a fade-out interrupt request (indicated by the LoAlertIEn bit) to be passed to pin IRQ.
1	ErrIEn	Allow error interrupt requests (indicated by the ErrIRq bit) to be passed to pin IRQ
0	TimerIEn	Allow timer interrupt requests (indicated by the TimerIRq bit) to be passed to pin IRQ.

2.1.1.3 IRq Pin Config Reg_ address 03h CRC Interrupt Request Bit and Pin IRQ Configuration

Bit	7	6	5	4	3	2	1	0
Definition	IRqPushPull	RFU	RFU	RFU	RFU	CRCIEEn	RFU	RFU
Bit Weight	r/w	–	–	–	–	r/w	–	–
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	IRqPushPull	Set 1, pin IRQ operates as a standard CMOS output pad. Set 0, the IRQ pin operates as an open-drain output pad.
6–3	RFU	Reserved
2	CRCIEEn	Allows CRC interrupt requests (indicated by the CRCIRq bit) to be passed to pin IRQ.
1–0	RFU	Reserved.

2.1.1.4 Interrupt rqReg_ address 04h Control Interrupt Request Bit

Bit	7	6	5	4	3	2	1	0
Definition	Set	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Bit Weight	r/w	dy	dy	dy	dy	dy	dy	dy
Reset Value	1	0	0	0	0	4	0	0

Bit	Symbol	Definition
7	Set	set 1 sets the flag bit in InterruptrqReg; set 0 clears the flag bit in InterruptrqReg.
6	TxIRq	set 1 as soon as the last bit of transmit data is sent.
5	RxIRq	set 1 when the receiver detects the end of a valid data stream.
4	IdleIRq	set 1 when an instruction is executed or when CommandReg is changed to an Idle instruction
3	HiAlertIRq	set 1 when the HiAlert position of Register Status1Regis 1. In contrast to HiAlert, HiAlertIRq stores the event and can only be cleared by Set.
2	LoAlertIRq	set 1 when LoAlert position 1 of Register Status1Regis set. In contrast to LoAlert, LoAlertIRq stores the event and can only be cleared by Set.
1	ErrIRq	set 1 if there are any error bits in the Error register.
0	TimerIRq	set 1 when timer TimerValue decreases to 0.

Note:

1. For LoAlertIRq bit, it will be set to 1 if the condition is met.

2. For ErrIRq bit, you need to send a new command (e.g. Idle command) to Command register to clear the ErrorReg register, and then set ErrIRq to 1 to clear it.

2.1.1.5 DivIrqReg_ address 05h Control Interrupt Request Bit.

Bit	7	6	5	4	3	2	1	0
Definition	Set	RFU	RFU	RFU	RFU	CRCIRq	RFU	RFU
Bit Weight	r/w	—	—	—	—	dy	—	—
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	Set	set 1 sets the flag bit in InterruptrqReg; set 0 clears the flag bit in InterruptrqReg.
6-3	RFU	Reserved.
2	CRCIRq	set to 1 when the CRC instruction is active and all data processing is complete
1-0	RFU	Reserved.

2.1.1.6 ErrorReg_ address 06h

Displays the error status of the last executed instruction .

Bit	7	6	5	4	3	2	1	0
Definition	WrErr	RFU	RFU	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocoErr
Bit Weight	r	—	—	r	r	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	WrErr	When the data is written into the FIFO by the master chip during the execution of the M1 instruction, or when the data is written into the FIFO by the master chip between the last bit sent and the last bit received by the RF interface, set 1.
6-5	RFU	Reserved.
4	BufferOvfl	If the master or the internal state machine of NF522 (e.g. receiver) tries to write data to FIFO when FIFO is full, set 1.
3	CollErr	If a bit conflict is detected, set 1. This is automatically cleared during the receiver startup phase
2	CRCErr	Set 1 if CRC check fails.
1	ParityErr	Set 1 if parity check fails. Automatically cleared during the receiver startup phase.
0	ProtocoErr	ProtocoErr position 1 if an incorrect number of bytes are received for a data stream in the M1 instruction.

*Note: Executing a new command clears all error flags.

2.1.1.7 Status1Reg_ address 07h

Partial status bits

Bit	7	6	5	4	3	2	1	0
Definition	RFU	CRCErr	RFU	IRq	TRunning	FIFO0vfl	HiAlert	LoAlert
Bit Weight	—	r	—	r	r	r	r	r
Reset Value	0	0	0	1	0	0	0	1

Bit	Symbol	Definition
7	RFU	Reserved.
6	CRCErr	indicates that the CRC verification fails when the CRC verification instruction is executed , or when RxCRCEn in the ReceiveReg register is set to 1 , and set 1 .
5	RFU	Reserved.
4	IRq	indicates whether attention is requested by any interrupt source. (Related to the interrupt enable bit, refer to)
3	TRunning	Set 1 if the NF522's timer unit is running. (The value of TCounterValRegis decremented by one at the next timer clock.)
2	FIFOovfl	indicates that the internal capacity of the FIFO buffer is full.
1	HiAlert	When the number of bytes stored in the FIFO meets the following formula, set 1: $\text{HiAlert} = (64 - \text{FIFOLength}) \leq \text{WaterLevel}$ eg: FIFOLength = 60 , WaterLevel = 4 $\rightarrow$ HiAlert = 1 FIFOLength = 59 , WaterLevel = 4 $\rightarrow$ HiAlert = 0
0	LoAlert	When the number of bytes stored in the FIFO meets the following formula, set 1: $\text{LoAlert} = \text{FIFOLength} \leq \text{WaterLevel}$ eg: FIFOLength = 4 , WaterLevel = 4 $\rightarrow$ LoAlert = 1 FIFOLength = 5 , WaterLevel = 4 $\rightarrow$ LoAlert = 0

2.1.1.8 Status2Reg address 08h

Bit	7	6	5	4	3	2	1	0
Definition	Modem_state				M1_Done	M1_Error	RFU	RFU
Bit Weight	r	r	r	r	dy	dy	—	—
Reset Value	0	0	1	0	0	0	0	0

Bit	Symbol	Definition
7-4	Modem_State	NF522 Internal Command Status Current Status.
3	M1_Done	Indicates that the M1 Cryptol unit is turned on and all data communication with the card is in cipher text. Only valid in the reader mode of the M1 card, and is set 1 only after the M1 authentication command is successfully executed. This bit can be cleared by software.
2	M1_Error	Indicates that the authentication fails when executing the M1 authentication command, and is set 1. Only valid when executing the M1 authentication command.
1-0	RFU	Reserved.

2.1.1.9 FIFODataReg_ address 09h 64-byte FIFO buffer input and output .

Bit	7	6	5	4	3	2	1	0
Definition	FIFOData							
Bit Weight	dy	dy	dy	dy	dy	dy	dy	dy
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	FIFOData	64-byte FIFO buffer data input and output ports The FIFO buffer acts as a converter of all serial data inputs and outputs to parallel inputs and outputs.

2.1.1.10 FIFOLevelReg_ address 0Ah

Indicates the number of bytes stored in the FIFO buffer .

Bit	7	6	5	4	3	2	1	0
Definition	FlushFIFO		FIFOLength					
Bit Weight	w		r	r	r	r	r	r
Reset Value	0		0	0	0	0	0	0

Bit	Symbol	Definition
7	FlushFIFO	Set 1, clears the read/write pointer to the internal FIFO buffer and the BufferOvfl bit in ErrReg. Reading this bit always results in a 0.
6-0	FIFOLength	The number of bytes stored in the FIFO buffer is displayed. Writing data to the FIFODataReg register increases the FIFOLevel by one and reading FIFOLevel decreases it by one.

2.1.1.11 WaterLevelReg_ address 0Bh

Defines the voltage of the FIFO overflow or underflow alarm

Bit	7	6	5	4	3	2	1	0
Definition	RFU		WaterLevel					
Bit Weight	-		rw	rw	rw	rw	rw	rw
Reset Value	0		0	0	0	1	0	0

Bit	Symbol	Definition
7-6	RFU	Reserved.
5-0	WaterLevel	This register defines an alert voltage to indicate a FIFO buffer underflow or overflow. If the number of bytes remaining in the FIFO buffer space is less than or equal to the number of bytes defined by WaterLevel, HiAlert position 1 in Status1Reg. If the number of bytes in the FIFO is less than or equal to the number of bytes in WaterLevel, LoAlert position 1 in Status1Reg.

2.1.1.12 ControlReg_ address 0Ch Other control bits.

Bit	7	6	5	4	3	2	1	0
Definition	TStopNow	TStartNow	TPrescalEven	Eof_ op	RFU	select_outi	RFU	Select_Shape
Bit Weight	dy	dy	r/w	r/w	—	—	—	r/w
Reset Value	0	0	0	0	0	0	0	1

Bit	Symbol	Definition
7	TStopNow	Set 1 stops the timer immediately. Reading this bit always results in a 0.
6	TStartNow	Set 1 start the timer immediately. Reading this bit always results in a 0.
5	TPrescalEven	If TPrescalEven = 0, $f_{\text{Timer}} = 13.56\text{MHz}/(2 * \text{TPreScaler} + 1)$; If TPrescalEven = 1, $f_{\text{Timer}} = 13.56\text{MHz}/(2 * \text{TPreScaler} + 2)$; TPrescalEven initial value is 0.
4	Single_Eof_op	15639 Used to send eof only in 16slot collision avoidance.
3	RFU	Reserved.
2	Select_Outi	15693 Dual subcarrier decoding 1: selects outi1 as the decoding input 0: Selects outi2 as the decoding input
1	RFU	Reserved.
0	Select_Shape	Choosing a plastic surgery programme 1: Plastic surgery for single outi2 0: outi1, outi2 combined plasticity

2.1.1.13 CollByteBit PosReg_ address 0Eh Byte count and bit count for card conflicts to occur

Bit	7	6	5	4	3	2	1	0
Definition	Coll_Byte_Pos				Coll_Bit_Pos			
Bit Weight	r	r	r	r	r	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-4	Coll_Byte_Pos	The reader-writer indicates to the host chip the number of bytes that are in conflict
3-0	Coll_Bit_Pos	The reader indicates to the host chip the number of bits in conflict.

2.1.1.14 Ext Reg_ address 0Fh

Extended Register Entry

Bit	7	6	5	4	3	2	1	0
Definition	EX_MODE			EX_DATA				
Bit Weight	dy	dy	dy	dy	dy	dy	dy	dy
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-6	EX_MODE	Extended register access: 01:Write address mode:bit5~0 Write secondary address 10:Read address mode:bit5~0 Write secondary address 11: Write data mode:bit5~0 Write to expansion register data 00 :Write address mode:bit5~0 Read expansion register data
5-0	EX_DATA	Extension register address or data

2.2.2 Page 1 Communication

2.2.2.1 CRCPreset Reg_ address 11h Define the CRC processor preset

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	CRCPreset	
Bit Weight	—	—	—	—	—	—	w	w
Reset Value	0	0	0	0	0	0	1	1

Bit	Symbol	Definition
7-2	RFU	Reserved.
1-0	CRCPreset	Defines the CRC processor preset for the CalCRC instruction .
		Value
		Description
		00 0000
		01 6363
		10 A671
		11 FFFF

2.2.2.2 TxModeReg_ address 12h

Define the rate and frame format ofthe transmitted data

Bit	7	6	5	4	3	2	1	0
Definition	TxCRCEn		Send_Rate		RFU	Send_Mode		
Bit Weight	r/w		r/w	r/w	—	r/w	r/w	r/w
Reset Value	0		0	0	0	0	0	0

Bit	Symbol	Definition
7	TxCRCEn	Set 1 to enable CRC checksum generation during datatransmission.
6-4	Send_Rate	Define the data transmission rate
		Value Description
		000 106 kbit
		001 212 kbit
		010 424 kbit
		011 848 kbit
		100 26p29
		101 6p67
		110 13p24
		111 52p97
3	RFU	Reserved
2-0	Send_Mode	Define the frame format for data transmission
		Value Description
		000 Receive according to ISO/IEC 14443A protocol
		001 Received according to ISO/IEC 15963 4s protocol
		010 Receive according to ISO/IEC 15963_4d protocol
		011 Receive according to ISO/IEC 14443B protocol
		100 Receive according to ISO/IEC 15963 256s protocol
		101 Receive according to r ISO/IEC 15963 256d protocol
		110 Reserved
		111 Reserved

2.2.2.3 RxModeReg_ address 13h

Defines the receive data rate and frame format

Bit	7	6	5	4	3	2	1	0
Definition	RxCRCEn	Receive_Rate			RxMultiple	Receive_mode		
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	RxCRCEn	Set 1 to enable CRC checksum at data reception.
6-4	Receive_Rate	Define the data receive rate
		Value Description
		000 106 kbit
		001 212 kbit
		010 424 kbit
		011 848 kbit
		100 26p29

		101	6p67
		110	13p24
		111	52p97
3	RxMultiple	Set 0, the receiver stops the timer after receiving one data frame. Set 1 allows the receiver to receive multiple data frames. The timer does not stop automatically when this bit is set.	
2-0	Receive_mode	Defines the frame format for data reception.	
		Value	Description
		000	Receive according to ISO/IEC 14443A protocol
		001	Received according to ISO/IEC 15963 4s protocol
		010	Receive according to ISO/IEC 15963_4d protocol
		011	Receive according to ISO/IEC 14443B protocol
		100	Receive according to ISO/IEC 15963 256s protocol
		101	Receive according to r ISO/IEC 15963 256d protocol
		110	Reserved
		111	Reserved

2.2.2.4 TxControlReg_ address 14h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	TxControl				
Bit Weight	—	—	—	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-5	RFU	Reserved
4	TxControl	When this bit is set, 100% ASK modulation is enabled; when this bit is cleared, 10% ASK modulation is enabled;
3	InvTX2RFOn	If driver TX2 is enabled, the output signal of TX2 pin is inverted in this position.
2	Tx2CW	When this bit is cleared, Tx2CW enables to modulate the 13.56MHz energy carrier signal. When this bit is cleared, Tx2CW enables to modulate the 13.56MHz energy carrier signal.
1	Tx2RFEn	When this bit is clear, the output signal of TX2 pin will transmit the 13.56Mhz energy carrier signal modulated by the transmit data.
0	Tx1RFEn	When this bit is set, the output signal of TX1 pin will transmit the energy carrier signal at 13.56Mhz modulated by the transmit data.

2.2.2.5 Send Bit NumReg_ address 15h Number of bits of transmit data

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	Send_Bit_Num		
Bit Weight	–	–	–	–	–	r/w	r/w	r/w
Reset Value	0	0	0	0	0	1	1	1

Bit	Symbol	Definition
7-3	RFU	Reserved
2-0	Send_Bit_Num	Defines the number of bits sent by the reader/writer in each data frame

2.2.2.6 Send ByteNumReg_ address 16h

Number of bytes of transmitted data

Bit	7	6	5	4	3	2	1	0
Definition	Send_Byte_Num							
Bit Weight	w	w	w	w	w	w	w	w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	Send_Byte_Num	Defines the number of bytes sent by the reader/writer in a data stream.

2.2.2.7 Wait ParmReg_ address 17h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	Wait_Parm			
Bit Weight	–	–	–	–	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	0	1	0
Bit	Symbol			Definition				
7-4	RFU			Reserved				
3-0	Wait_Parm			receive wait time				

2.2.2.8 ReceiveBeginBit PosReg_ address 18h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	Receive_Begin_Bit_Pos			
Bit Weight	–	–	–	–	w	w	w	w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-4	RFU	Reserved
3-0	Receive_Begin_Bit_Pos	In the event of a conflict, the master chip specifies the bit from which the reader reads back the data.

2.2.2.9 ReceiveByteNumLReg_ address 19h

The number of bytes received in one of the receiver's data streams is 8 bits lower.

Bit	7	6	5	4	3	2	1	0
Definition	Receive_Byte_Num							
Bit Weight	r	r	r	r	r	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	Receive_Byte_Num	The reader indicates to the master chip the number of bytes received in the previous data stream 8 bits lower.

2.2.2.10 ReceiveByteNumHReg_ address 1Ah

The number of bytes received by one of the receiver's data streams is one bit higher.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	Receive_Byte_Num_H
Bit Weight	–	–	–	–	–	–	–	r
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-1	RFU	Reserved
0	Receive_Byte_Num_H	The reader indicates to the host chip the number of bytes read in the previous data stream 1 bit higher.

2.2.2.11 ReceiveStateReg_ address 1Bh Received

result status of the receiver

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	Receive_Error	Receive_Coll	Receive_Done
Bit Weight	—	—	—	—	—	r	r	r
Reset	0	0	0	0	0	0	0	0
Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-3	RFU	Reserved
2	Receive_Error	The reader indicates to the master that an error has occurred in reception.
1	Receive_Coll	The reader indicates to the master that a conflict has occurred in reception.
0	Receive_Done	The reader indicates to the master that reception is complete.

2.2.2.12 UARTBaud Reg_ address 1Fh Selects the speed of the serial UART interface .

Bit	7	6	5	4	3	2	1	0
Definition	BR_T0				BR_T1			
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	1	1	0	1	0	1	1

Bit	Symbol	Definition
7-5	BR_T0	BR_T0 can be used to adjust the transmission rate of UART, please refer to 3.2.1 for details.
4-0	BR_T1	BR_T1 can be used to adjust the transmission rate of UART, please refer to 3.2.1 for details.

2.2.3 Page 2 Configuration

2.2.3.1 CRCResult MSBReg_ address 21h CRC calculation results are shown

Bit	7	6	5	4	3	2	1	0
Definition	CRCResultMSB							
Bit Weight	r	r	r	r	r	r	r	r
Reset Value	1	1	1	1	1	1	1	1

Bit	Symbol	Definition
7-0	CRCResultMSB	Show the high byte data of the CRC calculation result. It is only valid when the CRCReady position in the Status1Reg register is 1.

2.2.3.2 CRCResult LSBReg_ address 22h CRC calculation results are shown

Bit	7	6	5	4	3	2	1	0
Definition	CRCResultLSB							
Bit Weight	r	r	r	r	r	r	r	r
Reset Value	1	1	1	1	1	1	1	1
Bit	Symbol	Definition						
7-0	CRCResultLSB	Show the low byte data ofthe CRC calculation result. It is only valid when the CRCReady position in the Status1Reg register is 1.						

2.2.3.3 Sv1Reg_ address 23h

Bit	7	6	5	4	3	2	1	0
Definition	Sv1							
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	Sv1	Configure the reference voltage (analogue signal decoding related)

Note: Suggested configuration values are: 0x20,0x40. For low power supply noise, 0x10 or 0x08 can be configured.

2.2.3.4 RxgainReg_ address 26h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	Rxgain					RFU
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	1	1	1	1	0

Bit	Symbol	Definition
7-6	RFU	Reserved
5-1	Rxgain	Receive Gain: 00000:48dB 00001:46dB 0001x:43dB 00100:46dB 00101:44dB 0011x:41dB 01x00:43dB 01x01:41dB 01x1x:39dB 100xx:24dB 101xx:21dB 11xxx:19dB
0	RFU	Reserved

Note: The default value is sufficient.

2.2.3.5 P_CWConductanceReg_ address 28h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	P_CWConductance					
Bit Weight	—	—	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	1	0

Bit	Symbol	Definition
7-6	RFU	Reserved
5-0	P_CWConductance	PMOS Power Tube

Note: Suggested configuration value is: 0x09~0x2f (the number of transmitter power tube groups, generally can observe the antenna carrier amplitude of about 20V or so) .

2.2.3.6 ModConductanceReg_ address 29h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	ModConductance					
Bit Weight	–	–	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	1	0

Bit	Symbol	Definition
7–6	RFU	Reserved
5–0	ModConductance	Recess depth (the lower the recess the deeper the recess)

2.2.3.7 TModeReg_ address 2Ah

Defines the timer settings.

Bit	7	6	5	4	3	2	1	0
Definition	TAuto	RFU	RFU	TAutoRestart	TPrescaler_Hi			
Bit Weight	r/w	–	–	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	TAuto	Set 1 to automatically start counting at the end of a transmission in all communication modes and at any communication speed. In 106 kbit/s M1 mode and ISO 14443B mode, if the RxMultiple bit in register RxModeReg is 0, the timer stops after bit 5 (1 start bit, 4 data bits). In all other modes, if the RxMultiple bit in register RxModeReg is 0, the timer stops at bit 4. If RxMultiple is 1, the timer never stops. In this case, the timer can be stopped by setting TStopNow bit 1 in ControlReg. Set 0 indicates that the timer is not affected by the protocol
6–5	RFU	Reserved
4	TAutoRestart	Set 1 causes the timer to automatically restart the Count-down count from TReloadValue instead of stopping after the count decreases to 0. Set 0, timer decreases to 0, TimerIRq position 1.
3–0	TPrescaler_Hi	Defines the high 4 bits of TPrescaler. If TPrescalEven in ControlReg is 0, $f_{\text{Timer}} = 13.56\text{MHz} / (2 * \text{TPreScaler} + 1)$; If TPrescalEven in ControlReg is 1, $f_{\text{Timer}} = 13.56\text{MHz} / (2 * \text{TPreScaler} + 2)$; where TPreScaler = [TPrescaler_Hi : TPrescaler_Lo] (12 bits)

2.2.3.8 TPrescalerLoReg_ address 2Bh The lower 8 bits of the timer prescaler .

Bit	7	6	5	4	3	2	1	0
Definition	TPrescaler_Lo							
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	0	0	0

Bit	Symbol	Definition
7-0	TPrescaler_Lo	Defines the lower 8 bits of the TPrescaler. f_{Timer} calculation formula is described in the TPrescaler_Hi bit of the TModeReg register.

2.2.3.9 TReload HiReg_ address 2Ch Overloaded value for 16-bit timer.

Bit	7	6	5	4	3	2	1	0
Definition	TReloadVal_Hi							
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	TReloadVal_Hi	Defines the high 8 bits of TReloadReg. Each time the timer starts, it automatically loads TReloadVal. The timer automatically loads TReloadVal each time the timer starts, and changing this register only affects the timer the next time it starts.

2.2.3.10 TReload LoReg_ address 2Dh

Bit	7	6	5	4	3	2	1	0
Definition	TReloadVal_Lo							
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	TReloadVal_Lo	Defines the low 8 bits ofTReloadReg. Each time the timer starts, it automatically loads TReloadVal. The timer automatically loads TReloadVal each time the timer starts, and changing this register only affects the timer the next time it starts.

2.2.3.11 TCounterValHiReg_ address 2Eh The current value of the timer .

Bit	7	6	5	4	3	2	1	0
Definition	TCounterVal_Hi							
Bit Weight	r	r	r	r	r	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	TCounterVal_Hi	The current value of the timer, 8 bits high.

2.2.3.12 TCounterValLoReg_ address 2Fh The current value of the timer .

Bit	7	6	5	4	3	2	1	0
Definition	TCounterVal_Lo							
Bit Weight	r	r	r	r	r	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7-0	TCounterVal_Lo	The current value of the timer, 8 bits low.

2.2.4 Page 3 Test

2.2.4.1 Test PinEnReg_ address 33h Test Signal Direction Configuration

Bit	7	6	5	4	3	2	1	0
Definition	RFU	TestPinEn						RFU
Bit Weight	—	r/w	r/w	r/w	r/w	r/w	r/w	—
Reset Value	0	1	1	1	1	1	1	0

Bit	Symbol	Definition
7	RFU	Reserved
6-1	TestPinEn	Controls the direction of test IO port D5-D0 1: Output 0 : Input
0	RFU	Reserved

2.2.4.2 Test PinValueReg_ address 34h Test Signal Output Voltage Configuration

Bit	7	6	5	4	3	2	1	0
Definition	UseIO	TestPinValue						RFU
Bit Weight	r/w	r/w	r/w	r/w	r/w	r/w	r/w	–
Reset Value	0	0	0	0	0	0	0	0

Bit	Symbol	Definition
7	UseIO	0 : D5-D0 is used as test signal, output according to TestPin_Sel. 1 : Output the level of D5-D0 according to the TestPinValue register value .
6-1	TestPinValue	IO Port Output Specific Value
0	RFU	Reserved

2.2.4.3 ClkDelayiReg_ address 35h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	ClkDelayi					
Bit Weight	–	–	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	1	1	0	0	1

Bit	Symbol	Definition
7-6	RFU	Reserved
5-0	ClkDelayi	When Hand_set is 0 , it is the result of auto calibration, indicating the current number of delay unit groups; When Hand_set is 1 , it is the number of groups of delay unit turned on manually.

2.2.4.4 ClkDelaySet Reg_ address 36h

Bit	7	6	5	4	3	2	1	0
Definition	Clkdelaydata_flag	Check_full	Hand_set	Flip_angle				
Bit Weight	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	0	0	1

Bit	Symbol	Definition
7	Clkdelaydata_flag	Delay module reaches specified phase difference
6	Check_full	Delay unit fully open without inversion
5	Hand_set	1 to manually configure the number of delay groups, 0 to automatically run to a specified angle
4-0	Flip_angle	Valid if Hand_set is 0 5 'd00-5' d 16 can be matched. 00 is 180 ° , gradient is 11.25 ° , e.g. 02 is 157.5 ° .

Note: If bit 4-0 is to be modified, a command (0x 8 1) needs to be written to the command register and delayed after the modification.

2.2.5 Expansion Registers

2.2.5.1 LpcdCtrl_ address 0F/01h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	RFU	RFU	calibEn	lpcdEn
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	0	0

Bit	Symbol	Definition
1	calibEn	0 , non-calibration state. 1 , perform calibration.
0	lpcdEn	0, not in LPCD mode 1, enter LPCD mode.

2.2.5.2 LpcdClkCalib_ address 0F/02h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	rc27mCalib	rc32kCalib	rcCalib	lfvcCalib
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	1	1	0	0

Bit	Symbol	Definition
3	rc27mCalib	Set 1 to perform auto-calibration of the ring oscillator RC27M.
2	rc32kCalib	Set 1 performs automatic calibration of ring oscillator RC32K.
1	rcCalib	Set 1 to perform timing calibration
0	lfvcCalib	Set 1, the low frequency timer performs timing calibration.

2.2.5.3 LpcdTxCtrl address 0F/03h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	LpcdTxCtrl				
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	1	1	0	1	1

Bit	Symbol	Definition
4-0	LpcdTxCtrl	Calibration and T3 phase of LPCD mode, control of carrier transmission.

2.2.5.4 LpcdPCwConductance address 0F/04h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		LpcdPCwConductance					
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	1	0

Bit	Symbol	Definition
5-0	LpcdPCwConductance	PCW control for calibration and LPCD modes.

2.2.5.5 LpcdNCwConductance address 0F/05h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	RFU	LpcdNCwConductance		
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	0	1

Bit	Symbol	Definition
5-0	LpcdNCwConductance	NCW control for calibration and LPCD modes.

2.2.5.6 LpcdAnalogen_ address 0F/06h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	tvddSel	vmidEn	aldoEn	sbias2	opapd
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	0	0

Bit	Symbol	Definition
5	RFU	Reserved
4	tvddSel	Calibration and LPCD mode T3 stage TVDDsel control.
3	vmidEn	Calibration and LPCD mode large T2, T3 stage VMID control.
2	aldoEn	T1 phase control in LPCD mode.
1	sbias2	Calibrated and LPCD mode sbias2 control.
0	opapd	T1 and T2 phase control in LPCD mode.

2.2.5.7 LpcdRxgain_ address 0F/07h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	Rxgain				
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	0	1

Bit	Symbol	Definition
4-0	LpcdRxgain	Calibration and LPCD Mode Gain

2.2.5.8 LpcdT1Cfg_ address 0F/08h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	T1TimeConf			
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	1	1

Bit	Symbol	Definition
3-0	T1TimeConf	Time Slice Configuration for T1: $T1_time = (T1TimeConf + 2) * 100ms$

2.2.5.9 LpcdT2Cfg_ address 0F/09h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	T2TimeConf				
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	1	0	0	1	0

Bit	Symbol	Definition
4-0	T2TimeConf	Time Slice Configuration for T2: $T2_time = (T2TimeConf + 2) * 10us$

2.2.5.10 LpcdT3Cfg_ address 0F/0Ah

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	T3TimeConf			
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	1	0

Bit	Symbol	Definition
3-0	T3TimeConf	Time Slice Configuration for T3: $T3_time = (T3TimeConf + 2) * 9.4us$

2.2.5.11 LpcdAutoWupCfg_ address 0F/0Bh

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	AwakeEn	AwakeTime		
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	0	0

Bit	Symbol	Definition
3	Awake En	Wake-up enable, when set to 1, starts wake-up timing in lpcd mode and gives an interrupt flag according to awake_time timing.
2-0	Awake Time	Time slice configuration for automatic wake-up: 000 : 6 seconds 001 : 12 seconds 010 : 15 minutes 011 : 30 minutes 100 : 1 hours 101 : 1.8 hours 110 : 3.6 hours 111 : 7.2 hours

2.2.5.12 LpcdThreshold hi_ address 0F/0Ch

Bit	7	6	5	4	3	2	1	0
Definition	Ex Mode		RFU	Lpcd Threshold hi				
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00		0	0	0	0	0	0

Bit	Symbol	Definition
4-0	Lpcd Threshold hi	Upper threshold for detection

2.2.5.13 Lpcd Threshold lo_ address 0F/0Dh

Bit	7	6	5	4	3	2	1	0
Definition	Ex Mode		RFU	Lpcd Threshold lo				
Bit Weight	r/w		r/w	r/w	r/w	r/w	r/w	r/w

Reset Value	00	0	0	0	0	0	0
Bit	Symbol	Definition					
4-0	Lpcd Threshold lo	Lower threshold for detection					

2.2.5.14 IrqSet_ address 0F/0Eh

Bit	7	6	5	4	3	2	1	0
Definition	ExMode	RFU	RFU	RFU	LpcdIrqEn	LpcdIrqpushpull	LpcdIrqinv	
Bit Weight	r	r	r	r	r/w	r	r	
Reset Value	00	0	0	0	0	0	1	

Bit	Symbol	Definition
2	LpcdIrqEn	Lpcd IrqEn= 1 , LPCD related interrupt status is output to the IRQ pin of the chip.
1	LpcdIrqpushpull	irqpulldpush backup of interrupt configuration registers
0	LpcdIrqinv	irqinv backup of interrupt configuration registers

2.2.5.15 IrqStatus_ address 0F/0Fh

Bit	7	6	5	4	3	2	1	0
Definition	ExMode	RFU	RFU	AwakeIrq	CalibIrq	CalibErrIrq	CardIrq	
Bit Weight	r	r	r	r/w	r/w	r/w	r/w	
Reset Value	00	0	0	0	0	0	0	

Bit	Symbol	Definition
3	AwakeIrq	1 Flags the end ofthe automatic wake-up timer.
2	CalibIrq	1 Flag that the tuning mode has completed a level detection.
1	CalibErrIrq	1 Flag Tuning mode has not completed a level detection.
0	CardIrq	1 Flag lpcd mode detected external card.

2.2.5.16 Vmid Bdtime_ address 0F/ 11h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	VmidBdtime				
Bit Weight	r		w/r	w/r	w/r	w/r	w/r	w/r
Reset Value	00		0	0	0	0	0	0

Bit	Symbol	Definition
4:0	VmidBdtime	vmid build time configuration

2.2.5.17 Lpcd Fastdete_ address 0F/ 12h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	RFU	delayTime		Fastdete
Bit Weight	r		r	r	r	w/r	w/r	w/r
Reset Value	00		0	0	0	1	1	0

Bit	Symbol	Definition
2:1	delayTime	Detection delay time; Fastdete = 1 valid 00: 1us 01:2us 10:3us 11:4us
0	Fastdete	1: Fast detection 0: slow detection

2.2.5.18 Sensitivity_ address 0F/ 13h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	RFU	RFU	Sensitivity	
Bit Weight	r		r	r	r	r	w/r	w/r
Reset Value	00		0	0	0	0	0	0

Bit	Symbol	Definition
1:0	Sensitivity	Detection Sensitivity : 00: 1 group apart 01 : 2 groups apart 10 : 4 groups apart

2.2.5.19 LpcdADCValue_ address 0F/ 14h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU		LpcdADCValue			
Bit Weight	r		r	r	r	r	r	r
Reset Value	0		0	0	0	0	0	0

Bit	Symbol	Definition
4-0	LpcdADCValue	The detection returns a result : If LpcdADCValue < LpcdThreshold hi or LpcdADCValue > LpcdThreshold lo occurs, it is assumed that a card has entered the RF field.

2.2.5.20 CLKCONF_ address 0F/ 16h

Bit	7	6	5	4	3	2	1	0
Definition	ExMode		RFU	RFU	oscEn	rcoscEn	sysclk	lpcdXtal
Bit Weight	r		r	r	w/r	w/r	w/r	w/r
Reset Value	0		0	0	1	0	0	0

Bit	Symbol	Definition
3	oscEn	0, external crystal off ; 1, external crystal on
2	rcoscEn	0, RC27M off ; 1, RC27M on
1	sysclk	0, External crystal is used as system clock. 1, Internal RC27M is used as system clock.
0	lpcdXtal	0, LPCD mode uses internal RC27M clock 1, LPCD mode uses external crystal clock

3. Host Interfaces

3.1 Host Interface Configuration

The NF522 supports UART, SPI, and IIC interface types, and automatically detects the connected interface type after power-on reset.

The interface type is identified by selecting the level configuration of pin EA and I2C. The following table shows the corresponding selection configuration of EA and I2C configuration:

NF522		Interface Type		
Pin Number	Pin Name	UART	SPI	IIC
1	I2C	0	0	1
32	EA	0	1	EA
31	D7	TX	MISO	SCL
30	D6	—	MOSI	ADDR_0
29	D5	—	SCK	ADDR_1
28	D4	—	—	ADDR_2
27	D3	—	—	ADDR_3
26	D2	—	—	ADDR_4
25	D1	—	—	ADDR_5
24	SDA	RX	NSS	SDA

Table3- 1 Connection methods for different interface types

3.2 UART Interface

The NF522's UART interface consists of an input pin RX and an output pin TX. The UART interface is compatible with the RS232 serial interface. The UART interface is compatible with RS232 serial interface. Different baud rates can be configured through registers, and the interface is designed to comply with the standard UART protocol, with speeds ranging from 7200bit/s to 1.2Mbit/s.

3.2. 1 Baud rate configuration for UART transmission

The baud rate can be changed by configuring the BR_T0 and BR_T1 factors of the UART_BAUD register, and the default rate is 9.6 kbit/s.

BR_TN	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1-32	33-64	33-64	33-64	33-64	33-64	33-64	33-64

Table3-2 BR_T0 and BR_T1 Settings

transfer speed(kbit/s)	UART_BAUD		Transfer speed accuracy(%)
	Decimal	Hexadecimal	
7.2	250	FA	-0.25
9.6	235	EB	0.32
14.4	218	DA	- 0.25
19.2	203	CB	0.32
38.4	171	AB	0.32
57.6	154	9A	-0.25
115.2	122	7A	-0.25
128	116	74	-0.06
230.4	90	5A	-0.25
460.8	58	3A	-0.25
921.6	28	1C	1.45
1228.8	21	15	0.32

Table 3-3 Baud Rate Configuration for UART Transmission

The UART baud rates in the above table are calculated according to the following formula:

When $BR_TO = 0$:

$$transfer_speed = \frac{27.12}{BRT1+1}$$

When $BR_TO \neq 0$:

$$transfer_speed = \frac{27.12}{2^{(BRT0-1)} \times (BRT1+33)}$$

Note: Transmission rates higher than 1228.8kbit/s are not supported.

3.2.2 UART Frame Format

Bit	Length	Value
Starting Bit (SA)	1 bit	0
Data field	8 bit	data
Stop bit (SO)	1 bit	1

Table 3-4 UART Frame Format

Note: UART protocol communication LSB is transmitted first and without parity bit.

3.2.3 Address byte of the UART

Address byte: The first byte is the address byte, which meets the following format. The highest bit defines the communication mode, the middle 6 bits define the communication address, and the last bit is reserved.

7	6	5	4	3	2	1	0
1=write 0=read	addressA5-A0						Reserved

Table 3-5 Address Byte Format

3.3 SPI Interface

The NF522's SPI interface communicates as a Slave, and is designed to comply with the standard SPI protocol, with a maximum rate of 12M/s, compatible with modes 0 and 3.

3.4 IIC Interface

3.4.1 7-bit address

During transmission on the I2C bus, the first byte after the start state is the destination address that the Master selects for the Slave. This is shown in the figure below:

bit6(MSB)	bit5	bit4	bit3	bit2	bit1	bit0	R/W(LSB)
-----------	------	------	------	------	------	------	----------

Figure 3-1 First Byte after START

The device address is the first byte of communication on the I2C bus and is used to determine which slave node the bus master is communicating with.

The I2C interface provides a device address locking method. After the reset is released, based on the level of the EA pin, the level of the rest of the current interface pins will be detected and locked into the device address.

Assuming EA = 0, the high I2C address defaults to 0101, and the levels of pins d4, d5, and d6 and 0101 form the I2C device address.

Assuming EA = 1, ADDR_5~ADDR_0 are determined by pins d1, d2, d3, d4, d5, d6, and ADDR_6 is 0 by default.

In both of the above defaults, the address signal is latched immediately after the reset is released, and subsequent pin changes will not change the I2C address until the next reset is released and the address is latched again.

I2C address	ADDR_6	ADDR_5	ADDR_4	ADDR_3	ADDR_2	ADDR_1	ADDR_0
Pin	0	D1	D2	D3	D4	D5	D6

Table 3-6 Hardware Address Definitions for IIC

3.4.2 I2C write data

I2C data is written in the following sequence:

- The first byte of each data transfer gives the device address, as required by the I2C bus protocol.
- The second byte is the register address.
- This is followed by N bytes of data

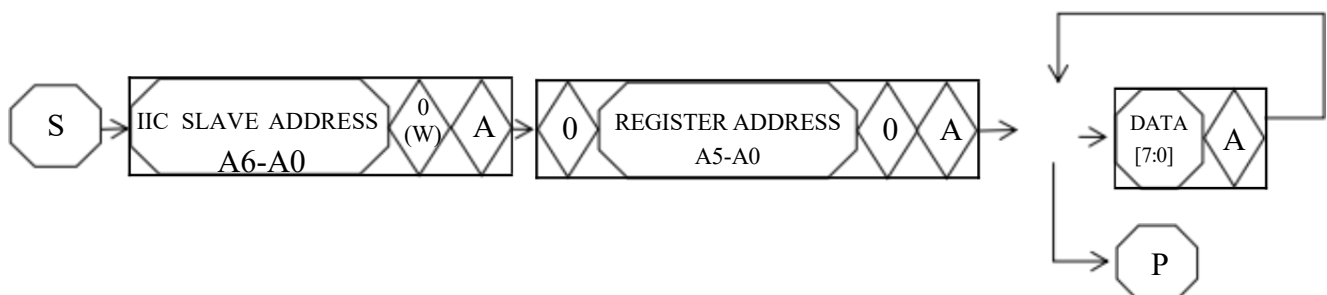


Figure 3-2 I2C Write Data Timing

3.4.3 I2C Read Data Timing

I2CThe data readout ofthe I2C bus follows the following sequence:

- First, the register address is accessed first, i.e. the first byte of each data transfer gives the device address and the second byte the register address, as required by the I2C bus protocol.
- Then the start condition is restarted and the device address and read signal are given.
- Receive N bytes of data.

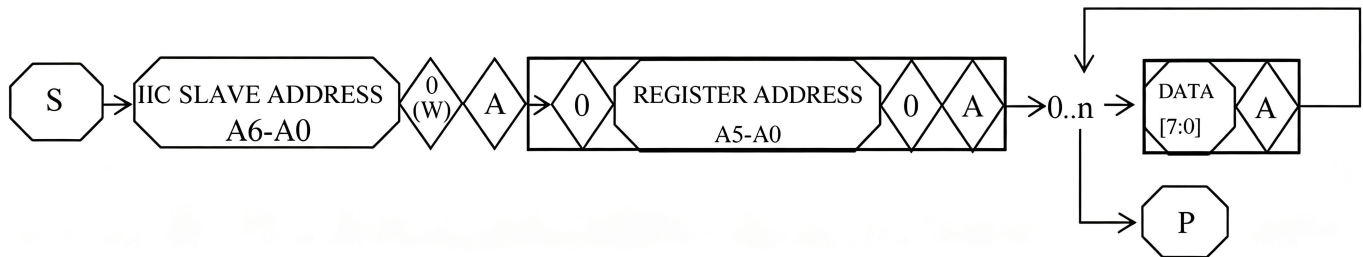


Figure 3-3 I2C Read Data Timing

3.5 Expanded Register Access

The expansion registers ofthe NF522 adopt two levels of address access, which can be accessed by all Host interfaces. The address of level 1 is 0F, and the address of level 2 is 6 bits. Through normal read/write operation of 0F register, the data can be read/written to the expansion registers according to the following table:

7 (MSB)	6	5	4	3	2	1	0
01	Write Extended Register L2 Address						
10	Read Extended Register Secondary Address						
11	Write Extended Register Data						
00	Read Extended Register Data						

Table 3-7 Expanded Register Byte Definitions

3.5. 1 Write Expansion Register Data

The write data method for non-expansion registers is:

- Write the target register address and set to communication write.
- Write the target register data.

Write data to the expansion register consists of the following 4 steps:

1. Write the OF register and set it to communication write.
2. Write the target level 2 register address (01b+6 bit level 2 address).
3. Write the OF register and set to communication write.
4. Write target 2 register data (11b + 6 bits of data)..

	Byte0	Byte1	Byte2	Byte3
Input	OF+W	01 b +Ex_ reg_addr	OF+W	11b+Ex_reg_data
Output	---	---	---	---

Table 3-8 Write Data Flow

3.5.2 Read Expansion Register Data

The way to read data from a non-expanded register is:

1. write the target register address and device for communication read.
2. Receive the target register data.

The read data of the extended register consists of the following four steps:

1. Write OF register and set communication read. 2.
2. Write the target level 2 register address (10b+6 is the level 2 address).
3. Write the OF register and set it to communication read.
4. Receive the target register data (00b+6 is the target data).

	Byte0	Byte1	Byte2	Byte3
Input	OF+W	10b+Ex_ reg_addr	OF+R	---
Output	---	---	---	00b+Ex_ reg_data

Table 3-9 Read Data Flow

4. Low Power Mode

The NF522 supports three low-power modes to adapt to different power consumption requirements:

- Hard power down mode
- Soft power down mode
- Low power card detection mode

4.1 Hard power down

The Hard Power Down mode of the NF522 shuts down the power supply to the digital circuits, shuts down the analogue power supply, shuts down the crystal and the internal RC oscillator, so that the bi-directional IO pins and the input pins are isolated from the external connections, and the values of the registers and FIFOs are lost.

When NPD is held low for a long period of time, the chip enters HPD mode. When NPD pin is pulled high and held high, the chip exits HPD mode and all circuits are re-run and initialised.

4.2 Soft power down

By setting the PowerDown bit of Command register to 1, the NF522 chip will enter Soft Power Down mode and switch off the crystal, the input and output pins will remain unchanged, so the registers, FIFO buffer contents and configuration will remain unchanged.

By setting the PowerDown bit of Command register to 0, NF522 chip will exit SPD mode, if you use external crystal as system clock, you need to wait for the crystal to stabilise before you can use it.

4.3 Low power card detection

The Low Power Detection Card of NF522 provides the function of low power detection card. Before entering the LPCD mode, it is necessary to configure LpcdEn of the expansion register LpcdCtrl to be 1, and the chip will enter the LPCD mode. Under the LPCD mode, the input/output pins remain unchanged in the original state, so the registers, FIFO buffer contents and configuration remain unchanged. The chip will exit LPCD mode once a card is detected or a wake-up timer occurs.

4.4 RF Off Mode

In RF off mode the NF522 shuts down the RF transmitter driver circuitry and also shuts down the RF field, which is turned on and off by setting the Txcontrol register [4:0] bits.

5. Command Set

5.1 Overview

The operation of the NF522 is determined by a state machine that can execute a series of instructions, which are executed by writing the command code to the CommandReg register, and the necessary parameters or data for the instructions are exchanged through the FIFO buffer.

5.2 NF522 command description

command	command code (hexadecimal)	Function Description
StartUp	3F	Run the reset and initialisation process
Idle	00	Null command to cancel the current command execution
Transmit	1A	Send FIFO cache data
Receive	16	Activate the receiver circuit
Transceive	1E	Sends the data cached in the FIFO and activates the receiver circuit automatically after sending.

CalcCRC	12	Start CRC coprocessor
M1_Strat	14	Start M1 encrypted communication
M1_Stop	15	Cancel M1 encrypted communication

Note: When writing to the Command register, note that the command needs to be either the highest bit of the upper register (cmd | 0x80).

6. Typical Application Circuit

A typical application diagram based on the NF522 is given below. When using a single antenna, one of the TX can be left unconnected. (Note: The antenna impedance is adjusted to 40~50 ohms.)

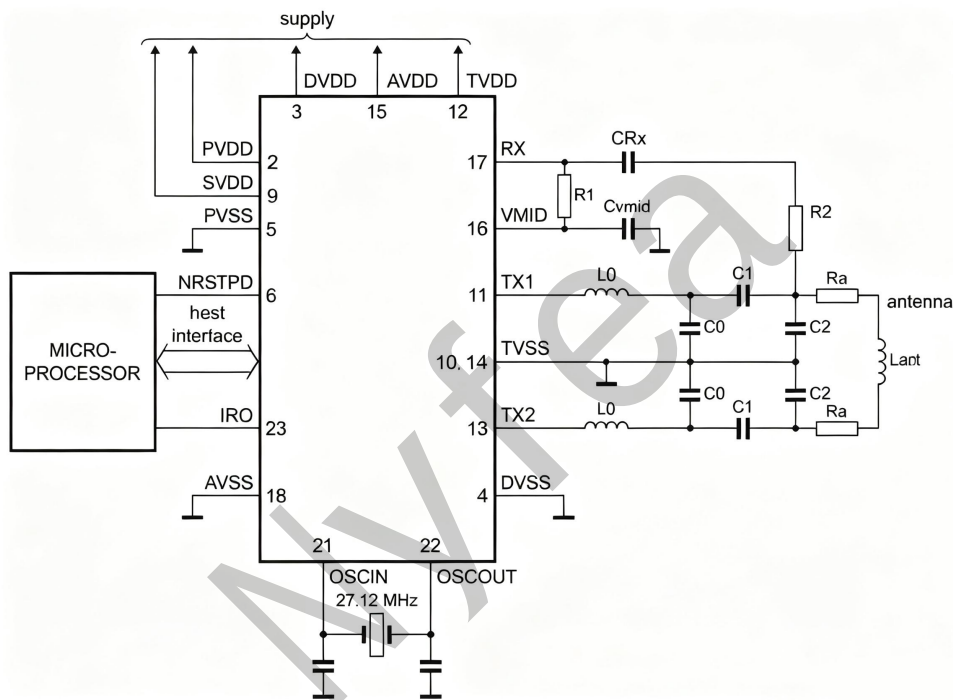


Figure 6-1 Typical Application Diagram

7. Electrical Parameter

7.1 Limit Rated Parameters

Symbol	Parameter	Min	Max	Unit
T _{amb. abs}	Storage Temperature	-40	+125	°C
AVDD	DC supply voltage	2.6	5.5	V
ESD (HMB)			8	KV
ESD (CDM)			500	V

Table 7- 1 NF522 Limit Rated Parameters

Note: If the applied conditions exceed the ratings of the limit rating parameters, permanent damage will be caused to the chip.

7.2 Operating Condition

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T _{amb}	Ambient Temperature	—	-40	+25	+125	°C
TVDD	Transmit Power Supply	AVSS=PVSS=TVSS=DVSS=0V	2.0	3.3	5.0	V
PVDD	Pin Power Supply	AVSS=PVSS=TVSS=DVSS=0V	2.0	3.3	5.0	V
AVDD	Analogue Power Supply	AVSS=PVSS=TVSS=DVSS=0V	2.3	3.3	5.0	V
DVDD	Digital Power Supply	AVSS=PVSS=TVSS=DVSS=0V	2.3	3.3	5.0	V

Table 7-2 NF522 Operating Voltage Conditions

7.3 Operating Electrical Parameters

Symbol	Parameter	Condition	Typ	Unit
I _{DVDD}	Digital Circuits Operating Current	Power up, before transmitting carrier	4.94	mA
		CW= 2 , transmitting carrier	6.97	mA
		SPD mode	263	uA
		HPD mode	0	uA
I _{AVDD}	Analogue Circuits Operating Current	Power up, before transmitting carrier	4.08	mA
		CW=2 , transmitting carrier	4.11	mA
		SPD mode	1	nA
		HPD mode	0	uA
	Transmitter Circuit Operating Current	TX1 and TX2 suspended , TX1EN and TX2EN= 1	3.9(CW= 1)	mA
			4.34(CW=2)	mA

I_{TVDD}		TX1 and TX2 suspended TX1EN and TX2EN= 1	0	uA
I_{LPCD}	LPCD Operating Current	AVDD= TVDD=3.3V (Using an external clock)	9.27	uA

Table 7-3 NF522 Electrical Parameter

8. Package Information

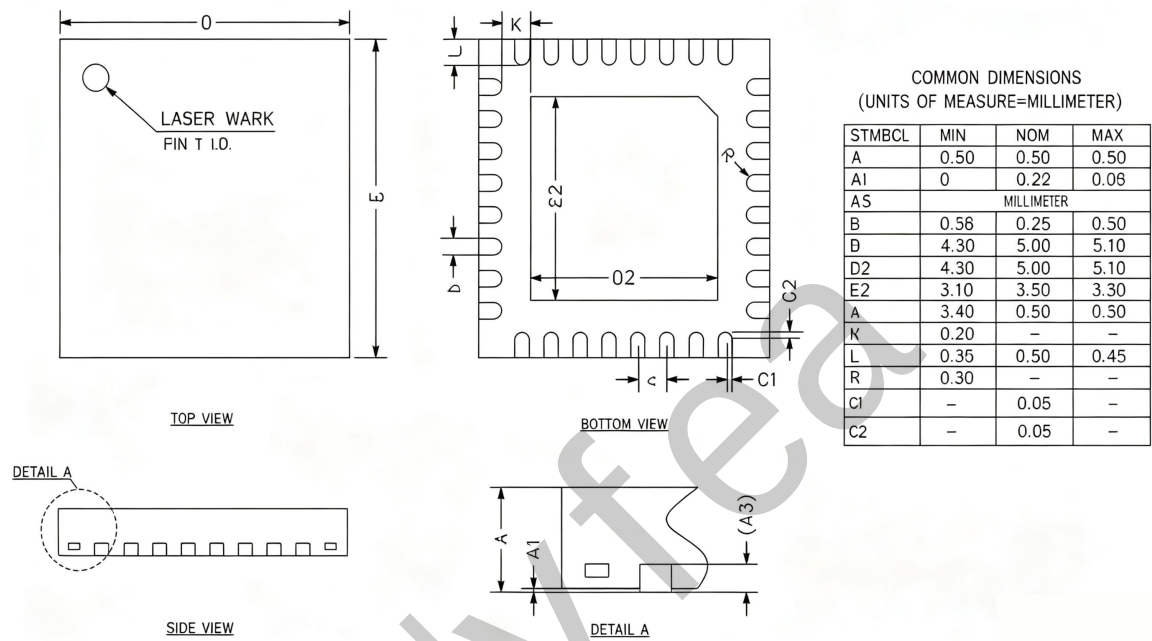


Figure 8- 1 Package Information