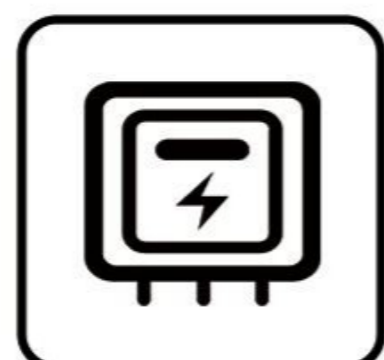


TDSEMIC

拓電半導體

自主封測 品質把控 售後保障

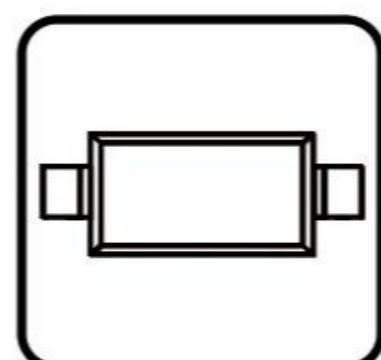
WEB | WWW.TDSEMIC.COM



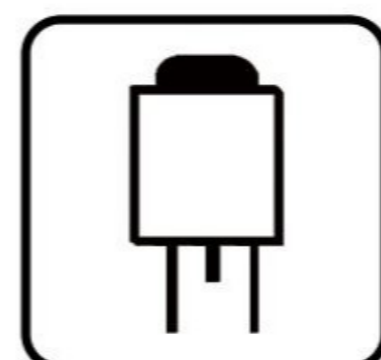
電源管理



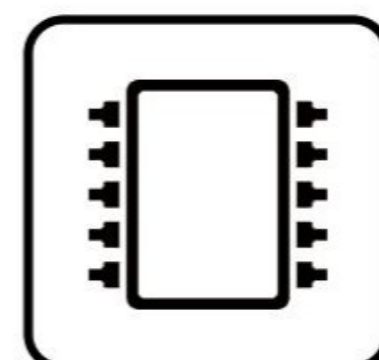
顯示驅動



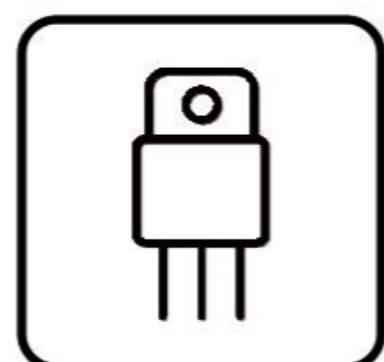
二三極管



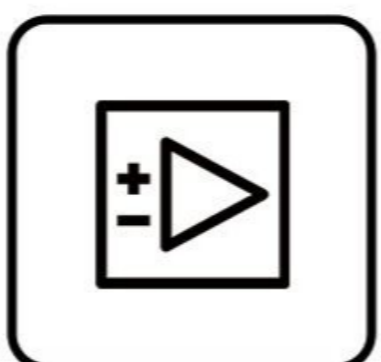
LDO穩壓器



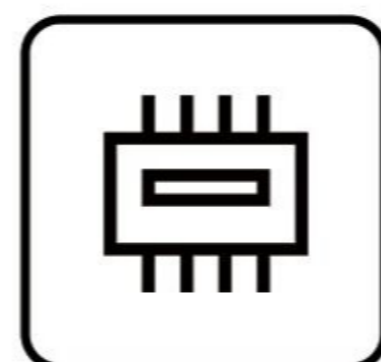
觸摸芯片



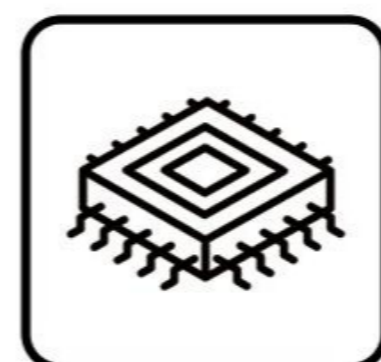
MOS管



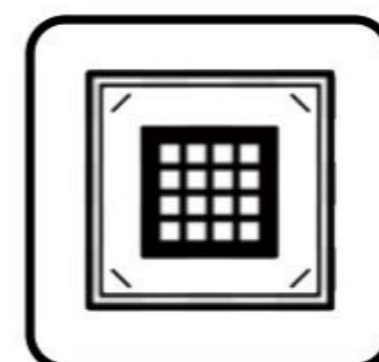
運算放大器



存儲芯片



MCU



串口通信

TD4409

產品規格說明書



General Description:

The **TD4409** is the single P-Channel logic enhancement mode power field effect transistors to provide excellent RDS(on), low gate charge and low gate resistance. It's up to -30V operation voltage is well suited in switching mode power supply, SMPS, notebook computer power management and other battery powered circuits.

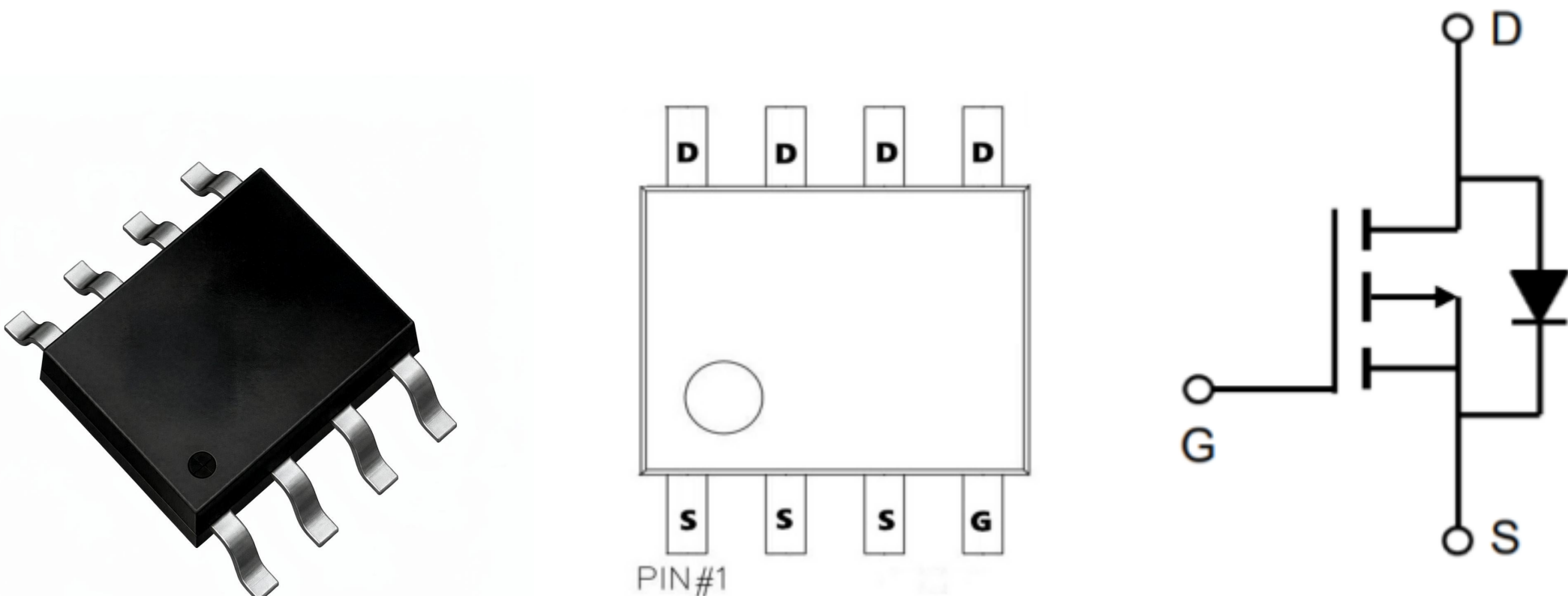
Features:

- RDS(ON)<7.5m @VGS=10V (P-Ch)
- RDS(ON)< 13 m @VGS=4.5V (P-Ch)
- Super high density cell design for extremely low RDS(ON)
- Exceptional on-resistance and maximum DC current

Applications:

- Switching power supply, SMPS
- Battery Powered System
- DC/DC Converter
- DC/AC Converter
- Load Switch

SOP-8 Pin Configuration



Package Marking and Ordering Information

Product ID	Package	Marking	QTY(PCS)	Packing method
TD4409	SOP-8	4409	3000	Reel

Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ -10V ^{1,6}	-18	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ -10V ^{1,6}	-8.8	A
I _{DM}	Pulsed Drain Current ²	-53	A
EAS	Single Pulse Avalanche Energy ³	-80	mJ
I _{AS}	Avalanche Current	-40	A
P _D @T _C =25°C	Total Power Dissipation ⁴	90	W
T _{STG}	Storage Temperature Range	-55 to 175	°C
T _J	Operating Junction Temperature Range	-55 to 175	°C
R _{θJA}	Thermal Resistance Junction-ambient ¹ (t≤10S)	20	°C/W
	Thermal Resistance Junction-ambient ¹ (Steady State)	50	°C/W

$R_{\theta JC}$	Thermal Resistance Junction-case ¹	1.6	$^{\circ}C/W$
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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-20A$	---	5.6	7.5	$m\Omega$
		$V_{GS}=-4.5V, I_D=-15A$	---	9.5	13	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	---	-2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^{\circ}C$	---	---	-1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^{\circ}C$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	1.2	---	Ω
Q_g	Total Gate Charge (-10V)	$V_{DS}=-15V, V_{GS}=-10V, I_D=-18A$	---	60	---	nC
Q_{gs}	Gate-Source Charge		---	9	---	
Q_{gd}	Gate-Drain Charge		---	15	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-20A$	---	17	---	ns
T_r	Rise Time		---	40	---	
$T_{d(off)}$	Turn-Off Delay Time		---	55	---	
T_f	Fall Time		---	13	---	
C_{iss}	Input Capacitance	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$	---	3450	---	pF
C_{oss}	Output Capacitance		---	255	---	
C_{rss}	Reverse Transfer Capacitance		---	140	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	-70	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^{\circ}C$	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F=-20A, di/dt=100A/\mu s, T_J=25^{\circ}C$	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	72	---	nC

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The EAS data shows Max. rating . The test condition is $V_{DD}=-50V, V_{GS}=-10V, L=0.1mH, I_{AS}=-40A$

4.The power dissipation is limited by 150 $^{\circ}C$ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation

6.The maximum current rating is package limited.

Typical Characteristics

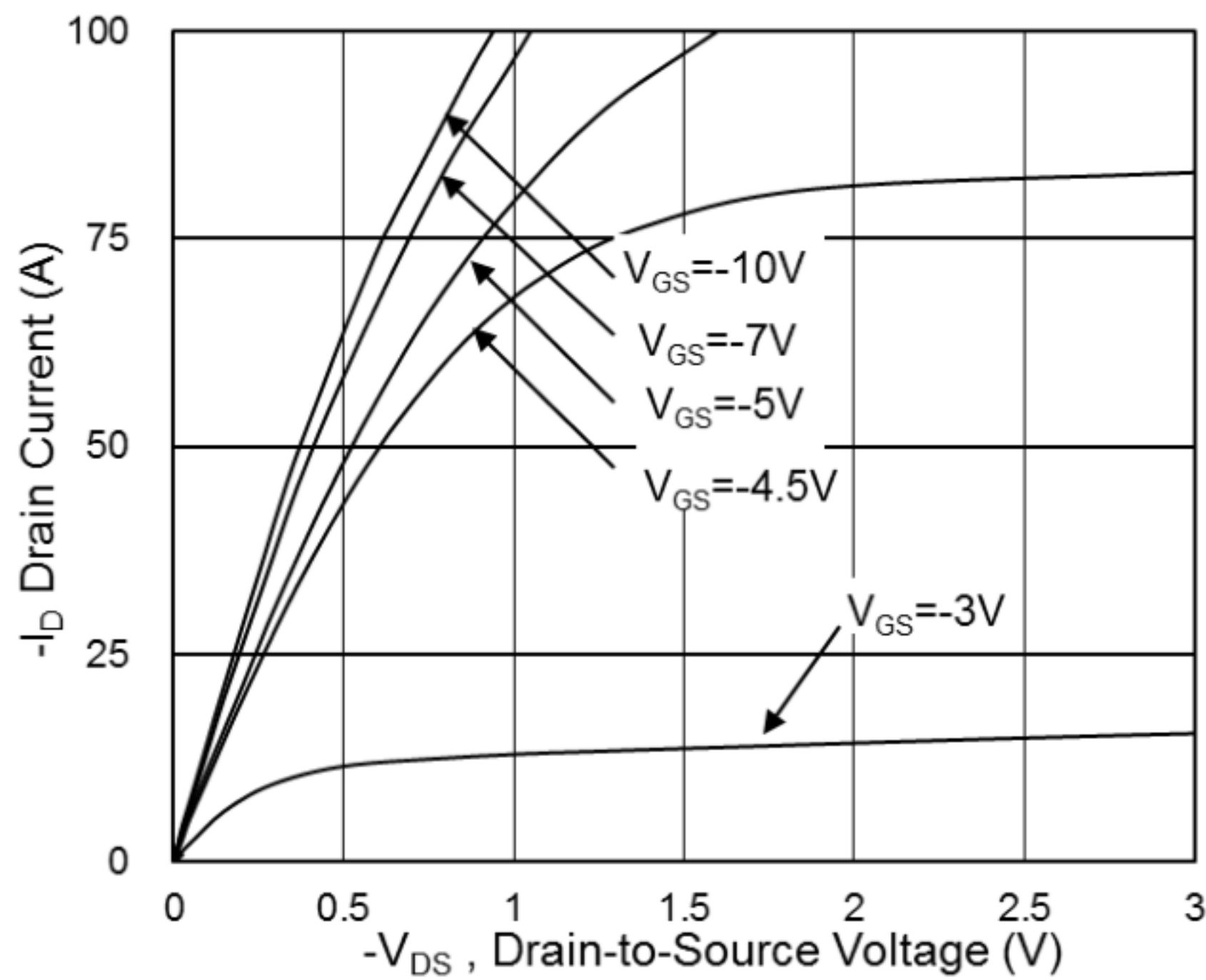


Fig.1 Typical Output Characteristics

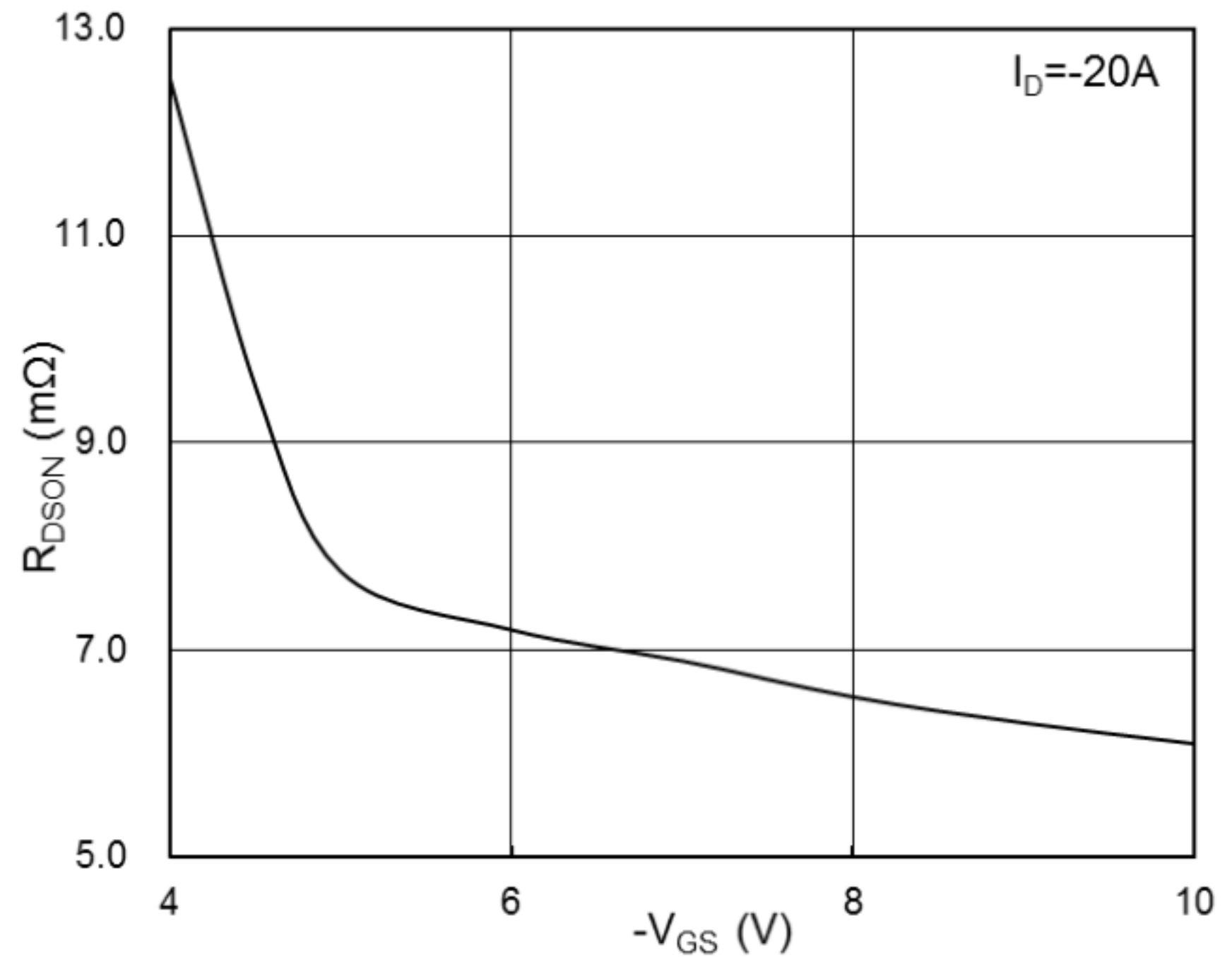


Fig.2 On-Resistance vs. Gate-Source Voltage

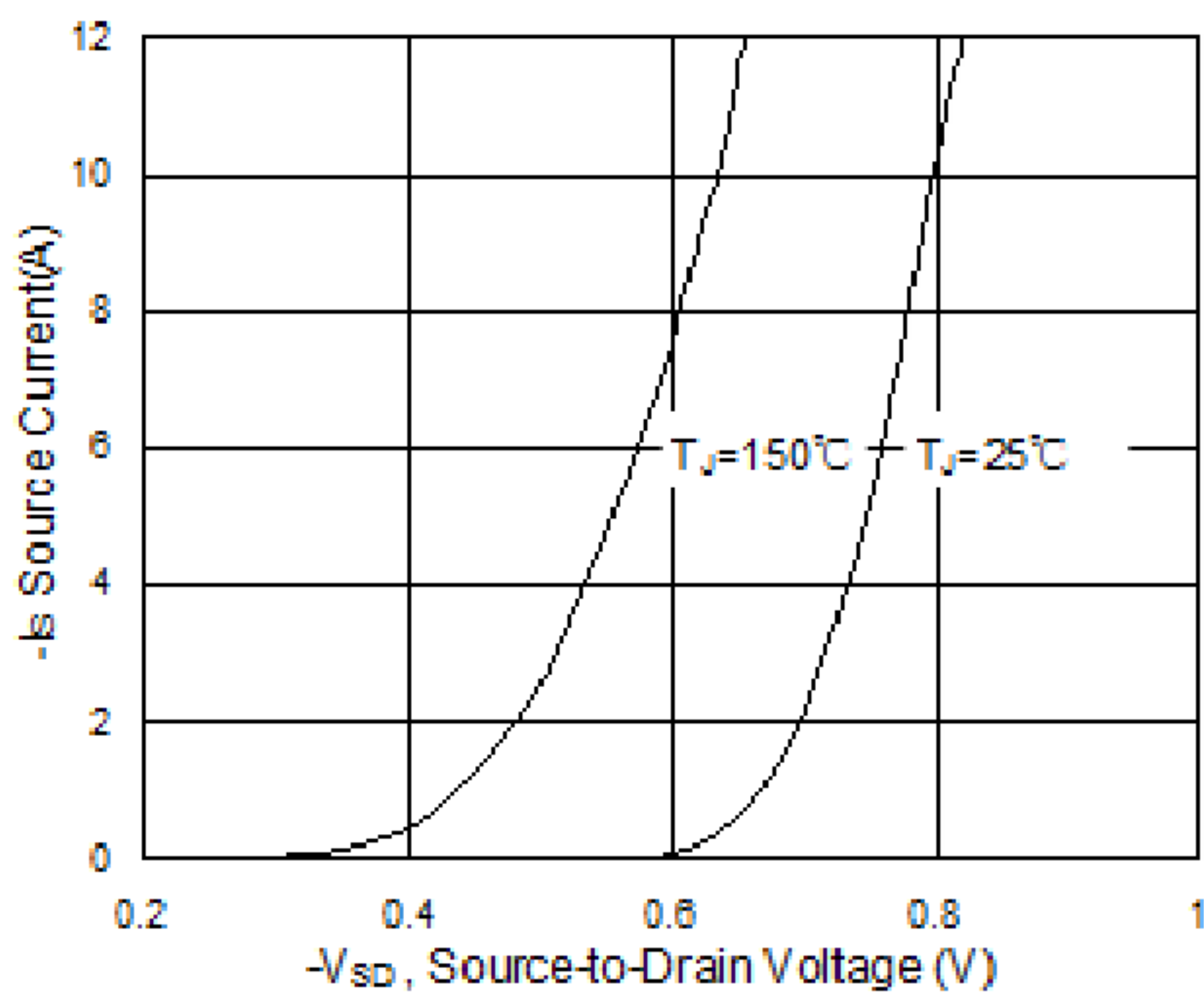


Fig.3 Forward Characteristics of Reverse

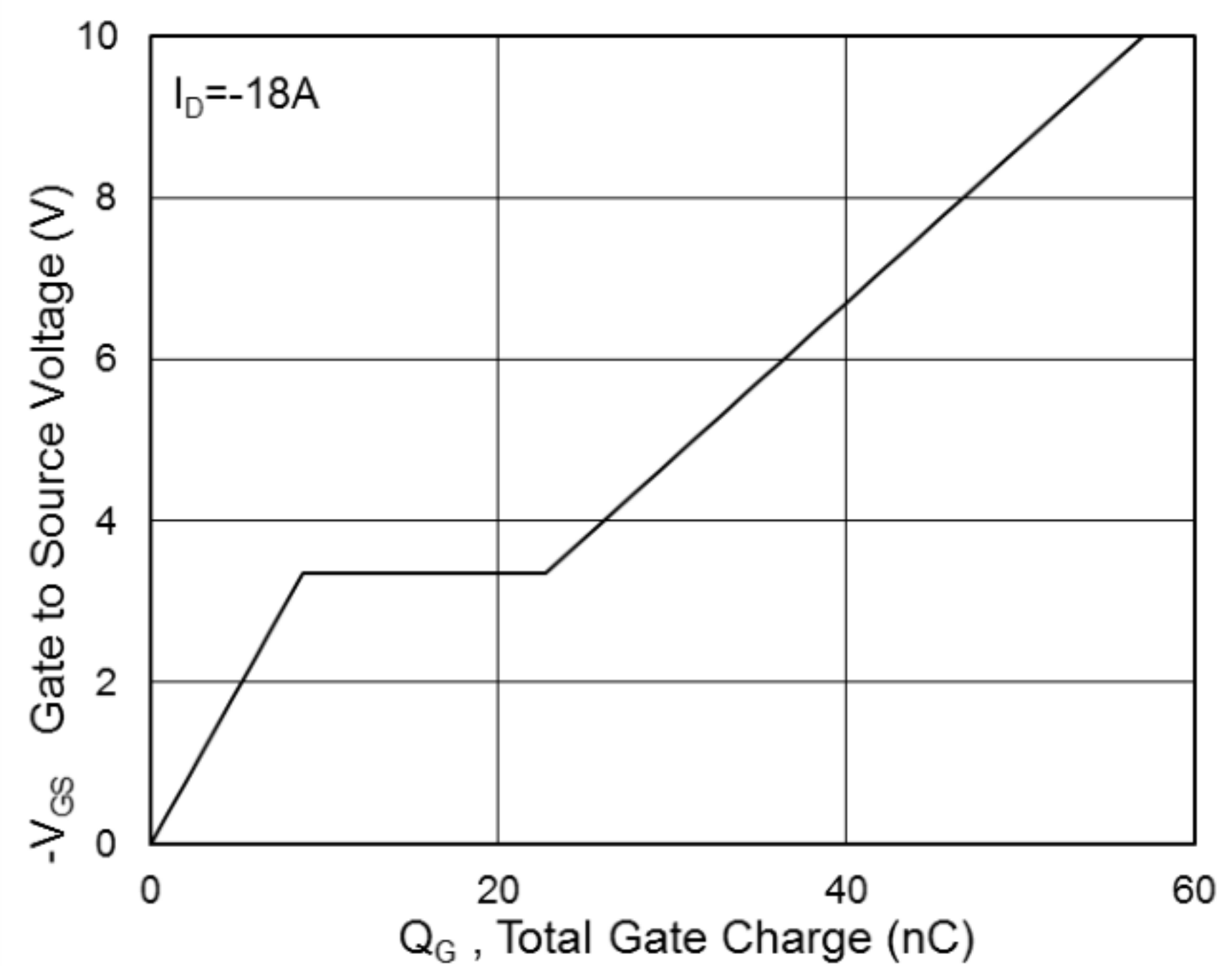


Fig.4 Gate-Charge Characteristics

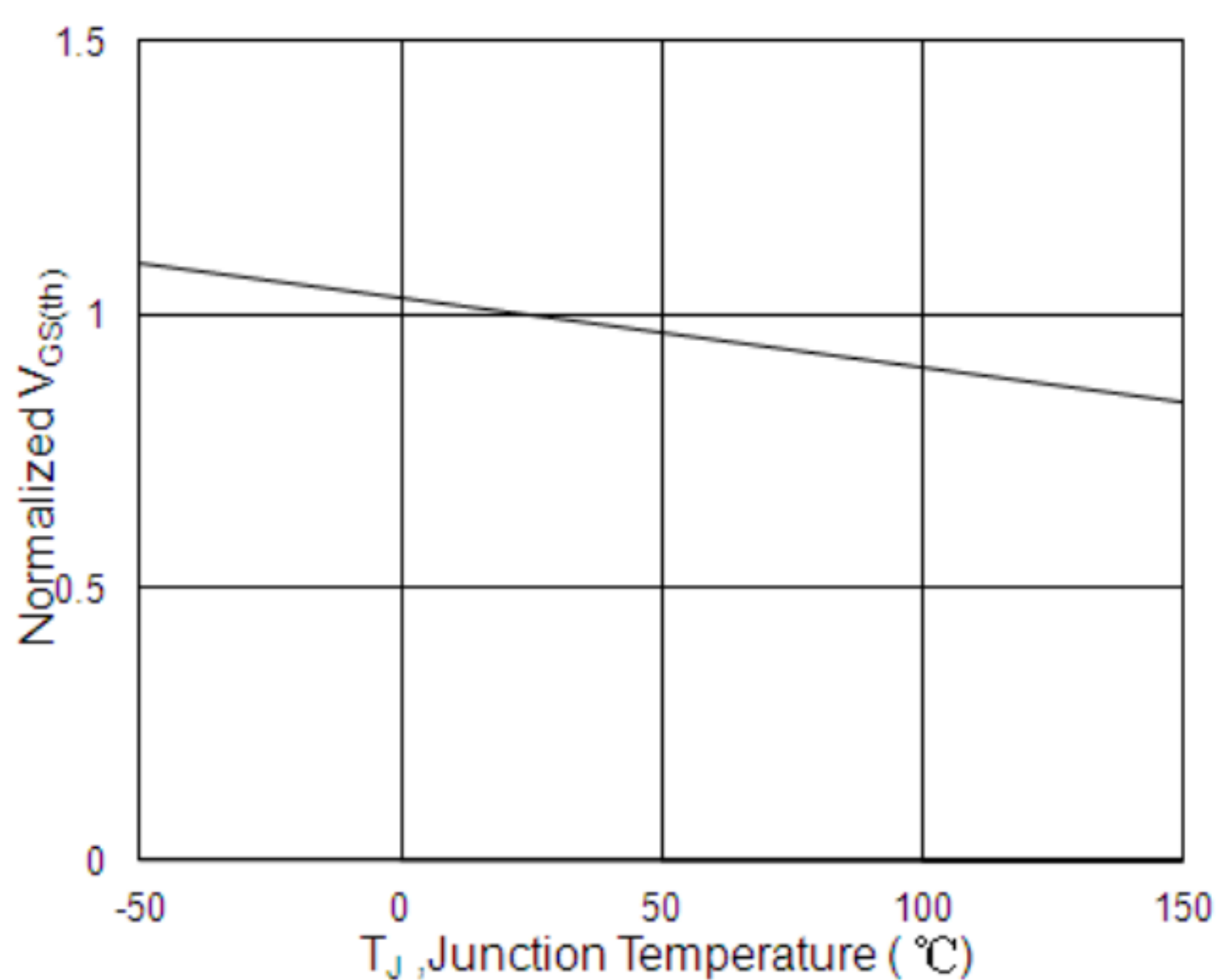


Fig.5 Normalized $-V_{GS(th)}$ vs. T_J

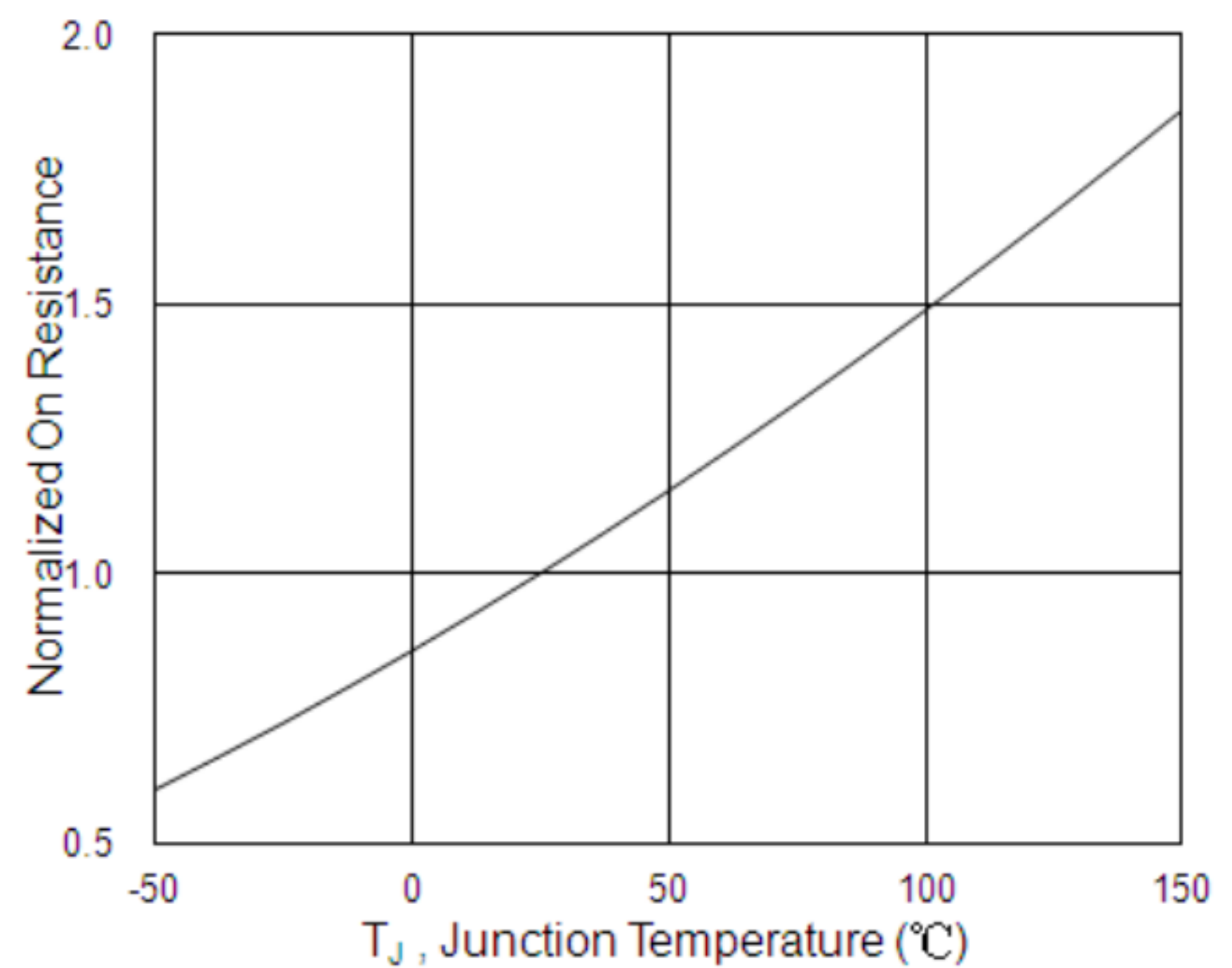


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

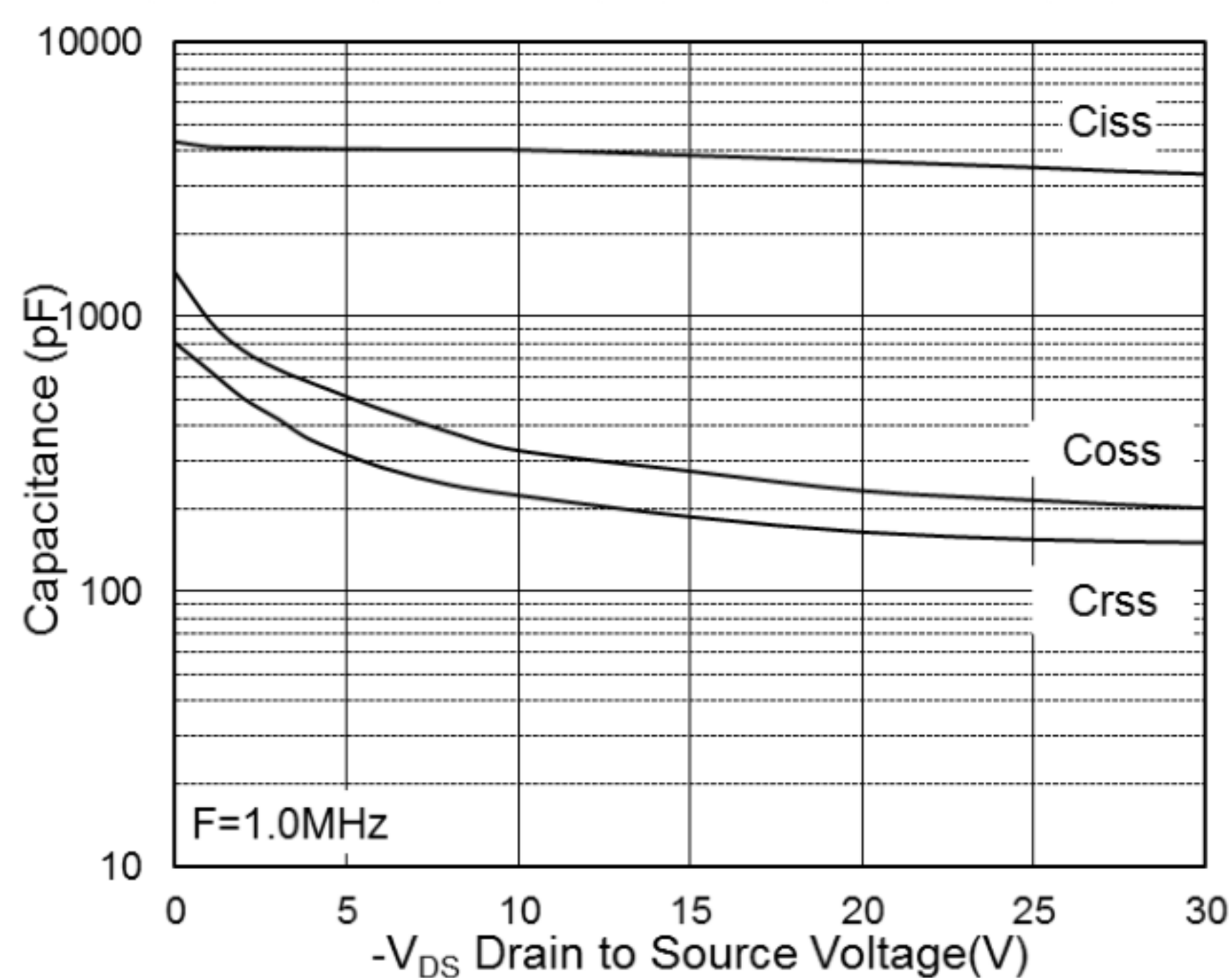


Fig.7 Capacitance

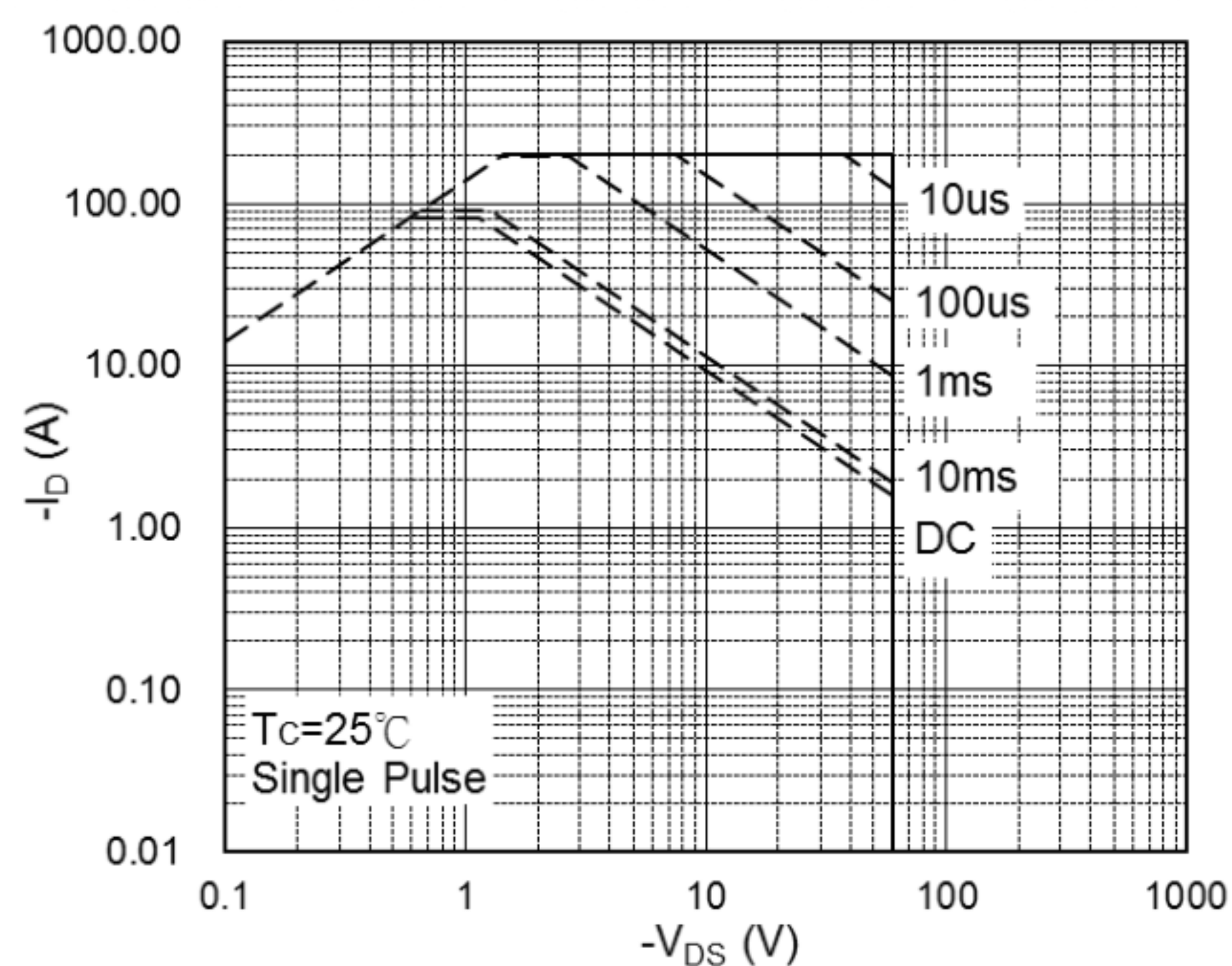


Fig.8 Safe Operating Area

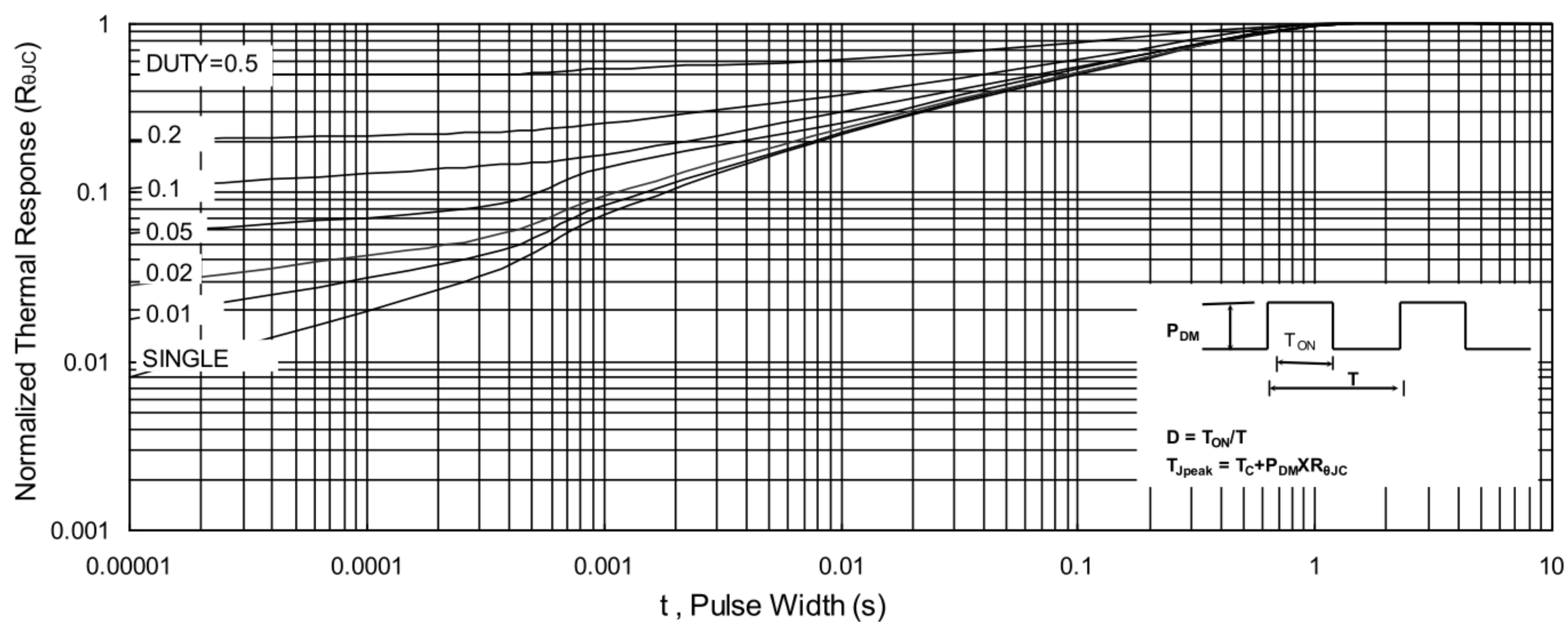


Fig.9 Normalized Maximum Transient Thermal Impedance

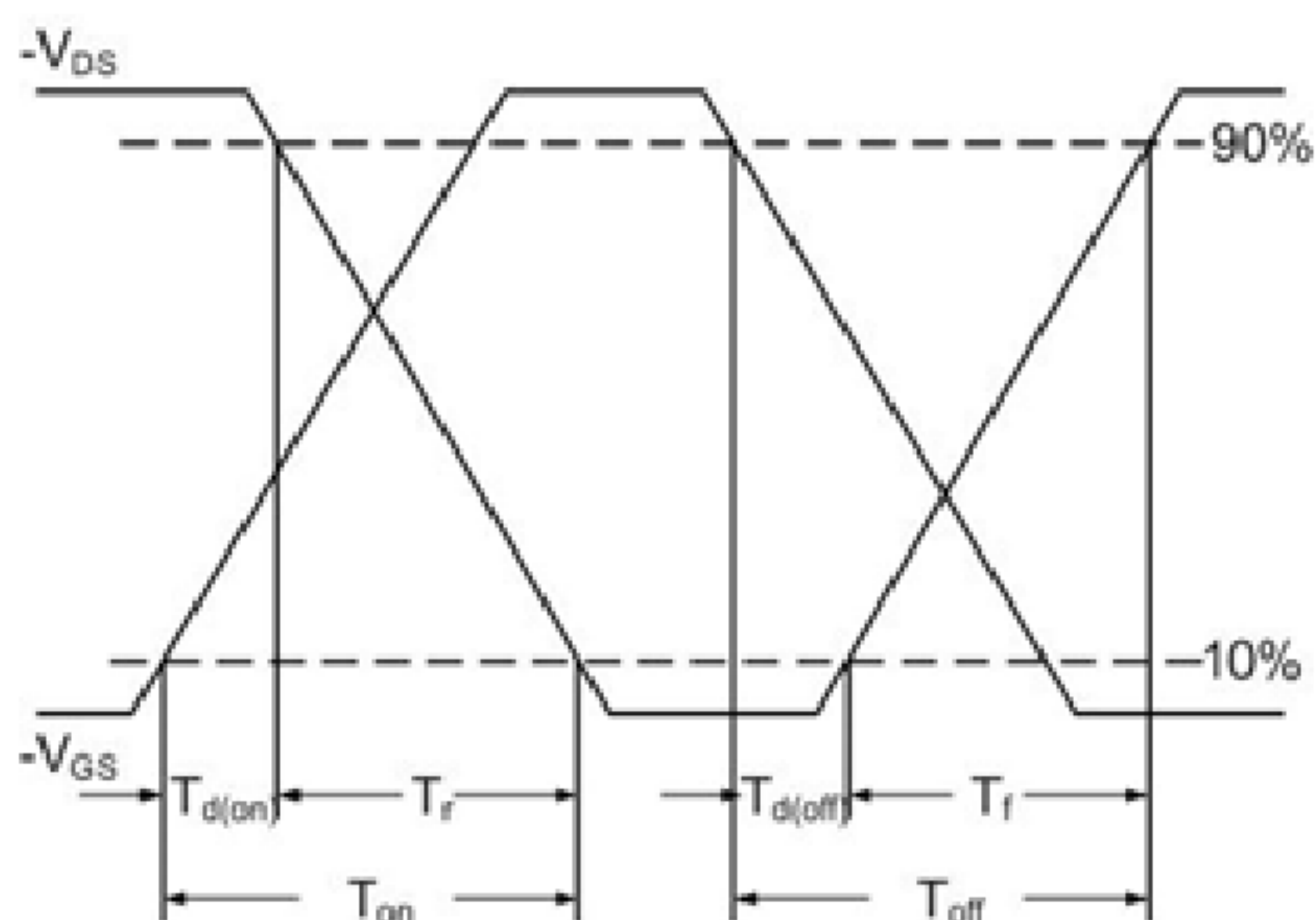


Fig.10 Switching Time Waveform

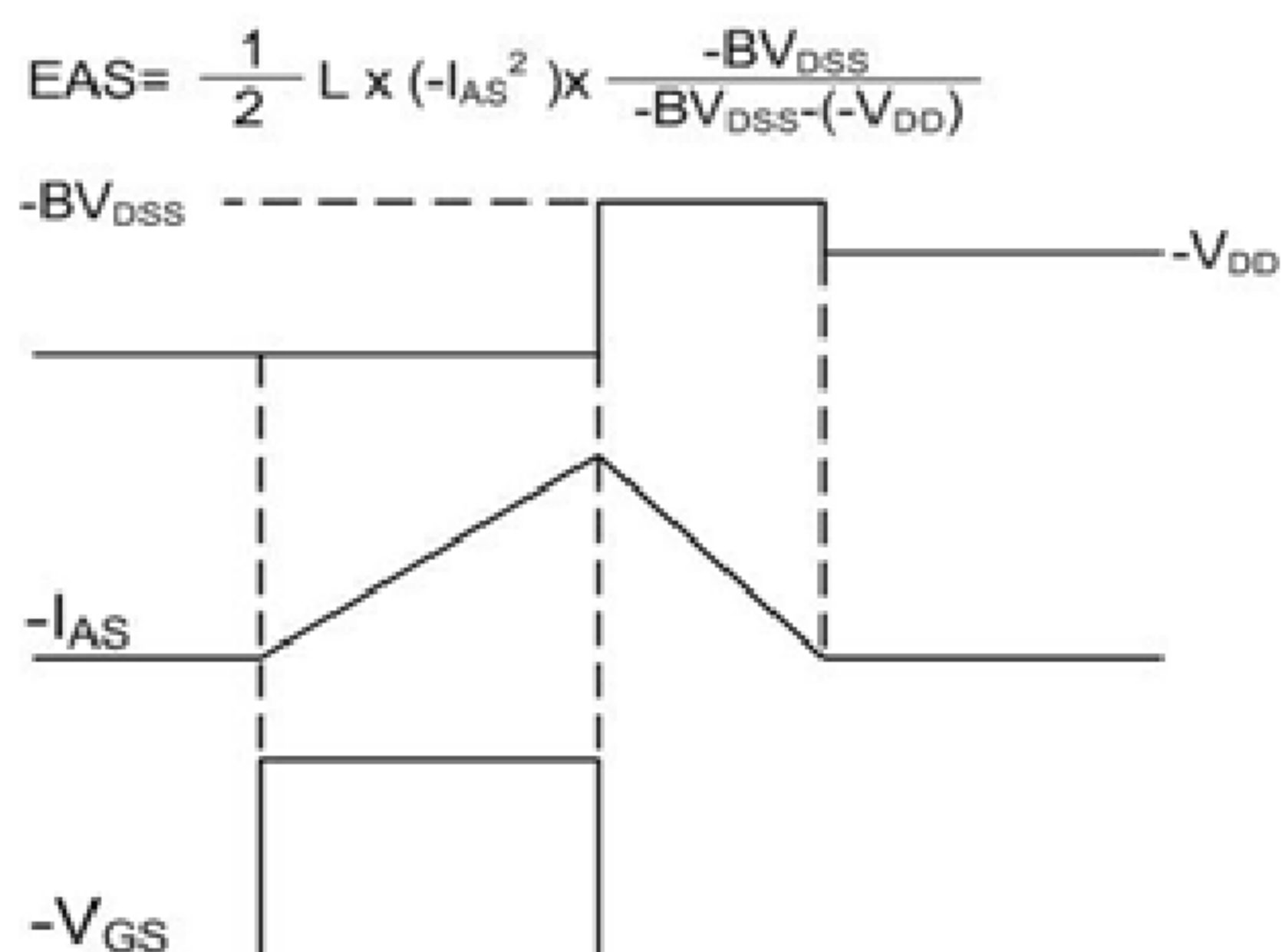
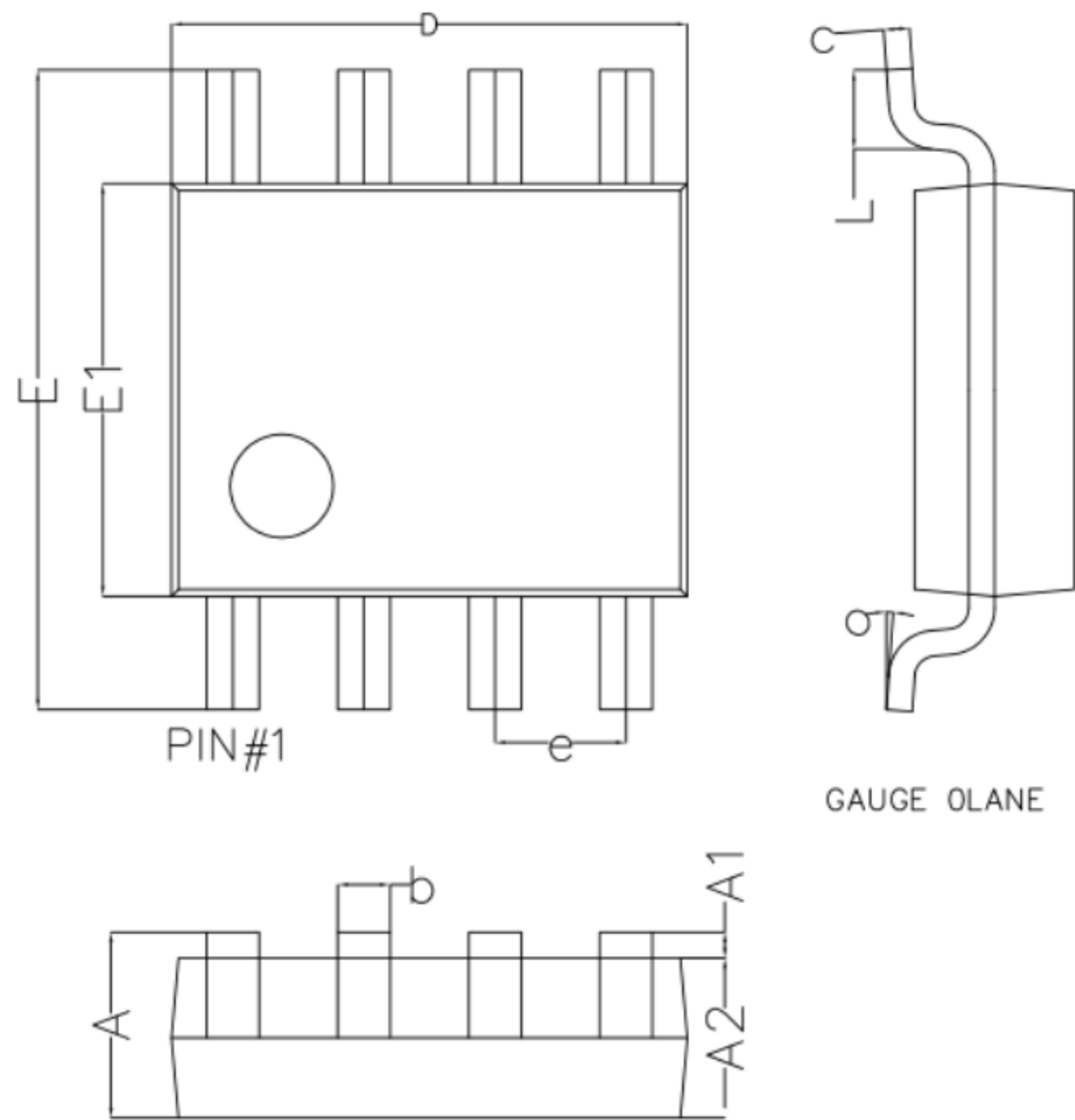


Fig.11 Unclamped Inductive Switching Waveform

SOP8 Package outline



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270 (BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°