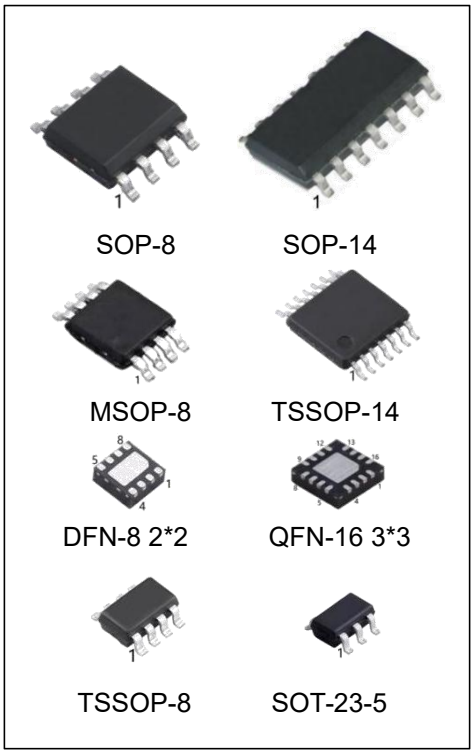
Micro-Power 1.5 MHz, Low-Noise, RRIO, 1.8 V Precision Amplifiers

Features

- Precision: ±350 μV Maximum Input Offset Voltage
- Low Noise: 25 nV/√Hz at 1 kHz
- 1.5 MHz GBW for Unity-Gain Stable
- Micro-Power: 85 μA Supply Current Per Amplifier
- Single 1.8 V to 5.5 V Supply Voltage Range at 0 ℃ to 70 ℃
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Extended Temperature Range: −40℃ to +125℃



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
TLV9001M5/TR-HG	SOT-23-5	1OGF	REEL	3000pcs/reel
TLV9002M/TR-HG	SOP-8	V9002	REEL	2500pcs/reel
TLV9002MM/TR-HG	MSOP-8	1GNX,OBBI	REEL	3000pcs/reel
TLV9002M8/TR-HG	SOT-23-8	T902	REEL	3000pcs/reel
TLV9002DQ2/TR-HG	DFN-8 2*2	1GMH	REEL	5000pcs/reel
TLV9004M/TR-HG	SOP-14	TLV9004	REEL	2500pcs/reel
TLV9004MT/TR-HG	TSSOP-14	V9004	REEL	2500pcs/reel
TLV9004LQ/TR-HG	QFN-16 3*3	T9004	REEL	5000pcs/reel

General Description

The TLV900x family of single-, dual-, and quad- channel amplifiers provides input offset voltage correction for low offset (maximum 350 μV) and drift (0.8 μV/℃) through the use of proprietary techniques. Featuring rail-to-rail input and output swings, and low quiescent current (typical 85 μA) combined with a wide bandwidth of 1.5 MHz and very low noise (25 nV/√Hz at 1 kHz) makes this family very attractive for a variety of batterypowered applications such as handsets, tablets, notebooks, and portable medical devices. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the TLV900x amplifiers provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 500 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection (3.5-kV HBM). The TLV900x amplifiers are optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V) at the temperature range of 0 ℃ to 70 ℃, and operation at voltages from +2.0 V (±1.0 V) to +5.5 V (±2.75 V) over the extended temperature range of −40 ℃ to +125 ℃.

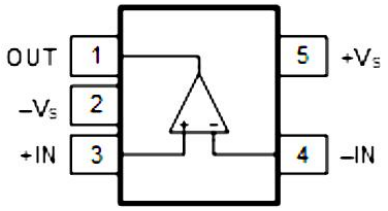
The TLV9001 (single) is available in both SOT23-5 packages. The TLV9002 (dual) is offered in DFN-8, SOP-8, SOT23-8 and MSOP-8 packages. The quad channel TLV9004 is offered in QFN-16, SOP-14 and TSSOP-14 packages.

Applications

- Battery-Powered Instruments: Consumer, Industrial, Medical, Notebooks
- Wireless Chargers
- Audio Outputs
- Sensor Signal Conditioning: Sensor Interfaces, Loop-Powered, Active Filters
- Wireless Sensors: Home Security, Remote Sensing, Wireless Metering

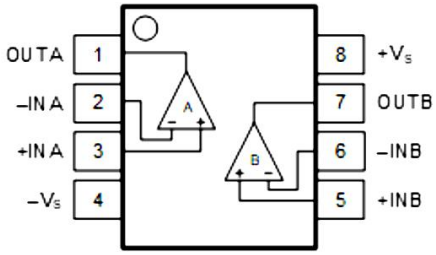
Pin Configurations (Top View)

TLV9001



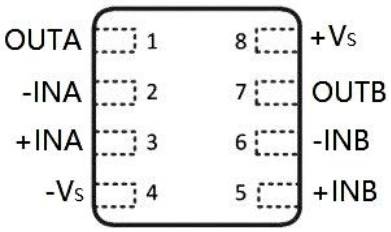
SOT-23-5

TLV9002



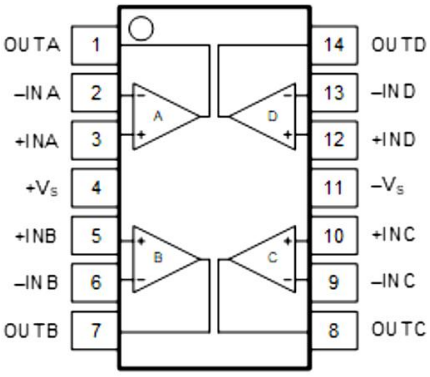
SOP-8/MSOP-8

TLV9002



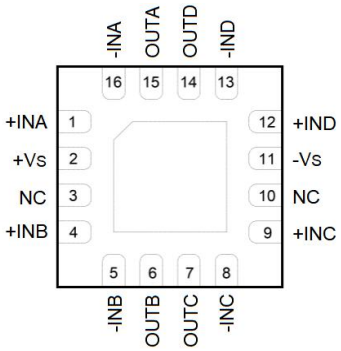
DFN-8 2*2

TLV9004



SOP-14/TSSOP-14

TLV9004



QFN-16 3*3

Pin Description

Symbol	Description
–IN	Inverting input of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} + 0.1 V).
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as –IN.
$+V_S$	Positive power supply. The voltage is from 2.0 V to 5.5 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 2.0 V to 5.5 V.
$–V_S$	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 2.0 V to 5.5 V.
OUT	Amplifier output.

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	10.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.5 V to V_{S+} + 0.5 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 ℃ to +150 ℃
Junction Temperature, T_J	150 ℃
lead Temperature Range (Soldering 10 sec)	260 ℃

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9(1)	3 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014(2)	2 000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

Electrical Characteristics

V_S = 5.0 V, T_A = +25℃, V_{CM} = V_S /2, V_O = V_S /2, and R_L = 10 kΩ connected to V_S /2, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = −40 to +125 ℃.

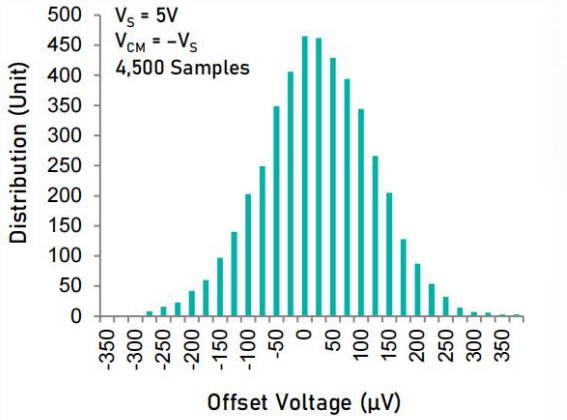
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	TLV9001, TLV9002		±100	±350	μV
		TLV9004		±120	±500	
Offset voltage drift	V_{OS} TC	T_A = -40 to +125 ℃		**±0.8**	**±2.3**	μV/ºC
Power supply rejection ratio	PSRR	V_S = 2.0 to 5.5 V, V_{CM} < V_{S+} - 2V	80	112		dB
		T_A = -40 to +125 ℃	**75**			
INPUT BIAS CURRENT						
Input bias current	I_B			1		pA
		T_A = +85 ℃		150		
		T_A = +125 ℃		500		
Input offset current	I_{OS}			1		pA
NOISE						
Input voltage noise	V_n	f = 0.1 to 10 Hz		5.6		$μV_{P-P}$
Input voltage noise density	e_n	f = 10 kHz		22		nV/√ Hz
		f = 1 kHz		25		
Input current noise density	I_n	f = 1 kHz		3		fA/√ Hz
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}		V_{S-}-0.1		V_{S+}+0.1	V
Common-mode rejection ratio	CMRR	V_S = 5.5 V, V_{CM} = -0.1 to 5.6 V	80	96		dB
		V_{CM} = 0 to 5.3 V, T_A = -40 to +125 ℃	**75**			
		V_S = 2.0 V, V_{CM} = -0.1 to 2.1 V	78	90		
		V_{CM} = 0 to 1.8 V, T_A = -40 to +125 ℃	**72**			
INPUT IMPEDANCE						
Input capacitance	C_{IN}	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{VOL}	R_L = 10 kΩ, V_O = 0.05 to 3.5 V	90	105		dB
		T_A = -40 to +125 ℃	**85**			
		R_L = 600 Ω, V_O = 0.15 to 3.5 V	85	100		
		T_A = -40 to +125 ℃	**80**			
FREQUENCY RESPONSE						
Gain bandwidth product	GBW			1.5		MHz
Slew rate	SR	G = +1, C_L = 100 pF, V_O = 1.5 to 3.5 V		1.2		V/μs
Total harmonic distortion + noise	THD+N	G = +1, f = 1 kHz, V_O = 0.5 V_{RMS}		0.002		%

Settling time	t_S	To 0.1%, G = +1, 1V step		1.2		μs
		To 0.01%, G = +1, 1V step		1.5		
Overload recovery time	t_{OR}	V_{IN} * Gain > V_S		2		μs
OUTPUT						
High output voltage swing	V_{OH}	R_L = 10 kΩ	V_{S+}–19	V_{S+}–11		mV
		R_L = 600 Ω	V_{S+}–275	V_{S+}–200		
Low output voltage swing	V_{OL}	R_L = 10 kΩ		V_{S-}+8	V_{S-}+14	mV
		R_L = 600 Ω		V_{S-}+135	V_{S-}+185	
Short-circuit current	I_{SC}	Source current through 10Ω		45		mV
		Sink current through 10Ω		55		
POWER SUPPLY						
Operating supply voltage	V_S	T_A = 0 to +70 ℃	1.8		5.5	V
		T_A = −40 to +125 ℃	**2.0**		**5.5**	
Quiescent current (per amplifier)	I_Q			85	135	μA
		T_A = −40 to +125 ℃			**170**	
THERMAL CHARACTERISTICS						
Operating temperature range	T_A		-40		+125	ºC
Package Thermal Resistance	θ_{JA}	SOT23-5		190		ºC/W
		DFN-8 2x2		24		
		MSOP-8		201		
		SOP-8		125		
		TSSOP-8		160		
		QFN-16 3x3		65		
		TSSOP-14		112		
		SOP-14		115		

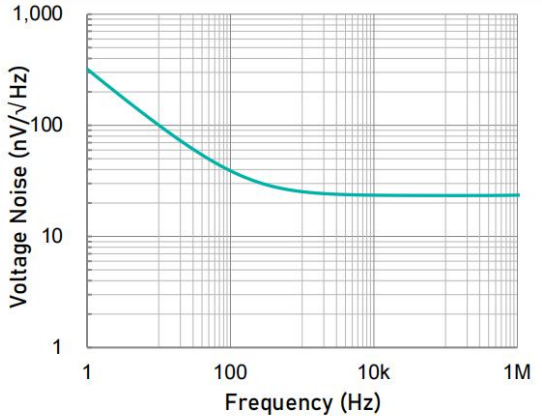
Note:Operating temperature range: -40°C to +125°C. This product is designed for industrial grade applications. For automotive grade versions compliant with AEC-Q100, please conduct internal screening per the standard or contact our sales team for availability.

Typical Performance Characteristics

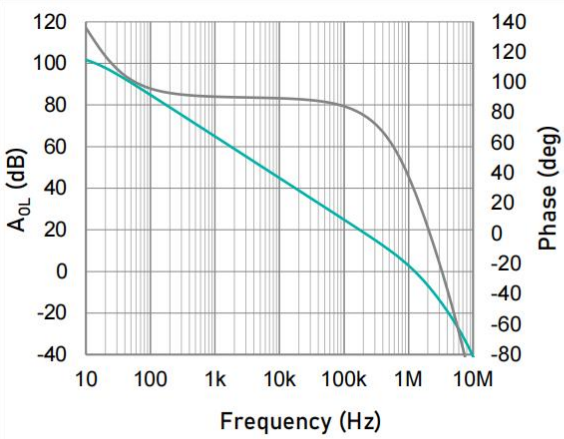
At T_A = +25℃, V_{CM} = V_S /2, and R_L = 10kΩ connected to V_S /2, unless otherwise noted.



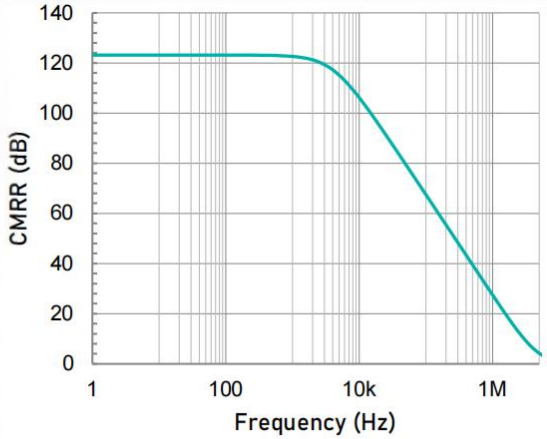
Offset Voltage Production Distribution



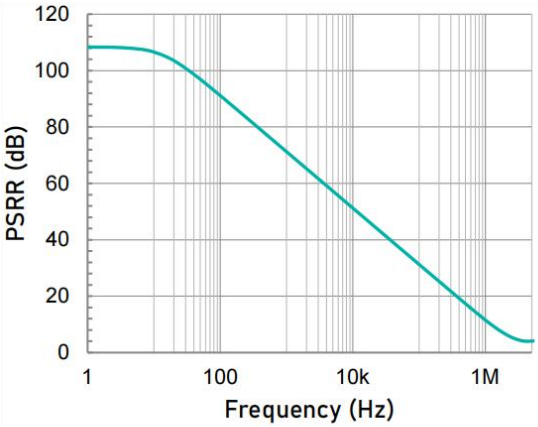
Input Voltage Noise Spectral Density as a function of Frequency.



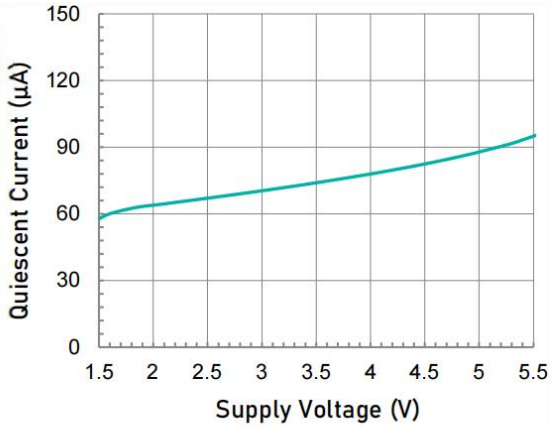
Open-loop Gain and Phase as a function of Frequency.



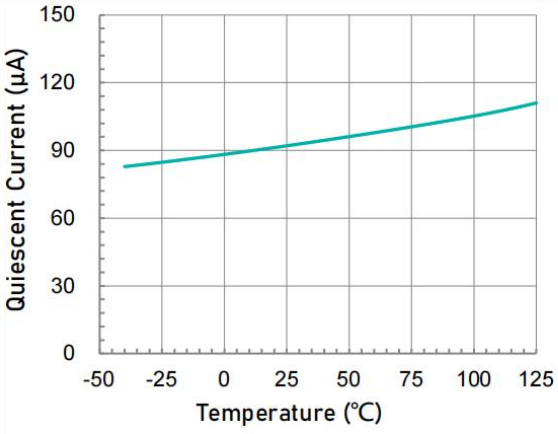
Common-mode Rejection Ratio as a function of Frequency.



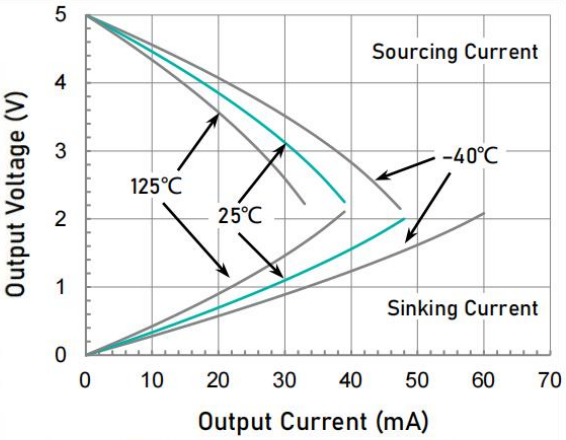
Power Supply Rejection Ratio as a function of Frequency.



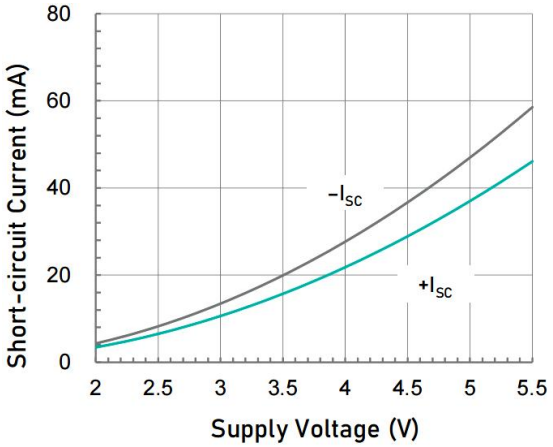
Quiescent Current as a function of Supply Voltage.



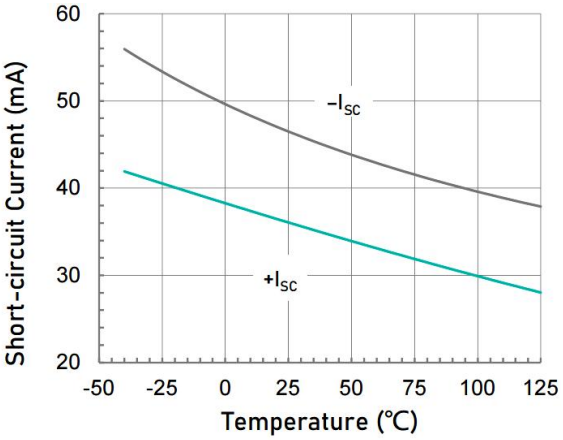
Quiescent Current as a function of Temperature.



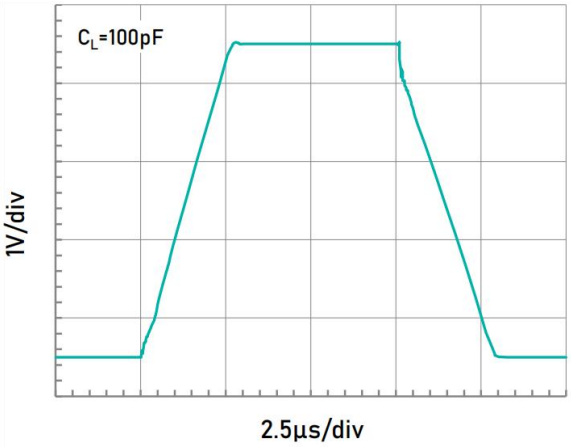
Output Voltage Swing as a function of Output Current.



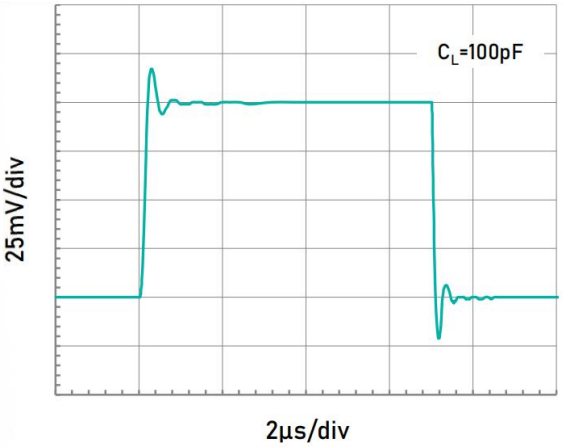
Short-circuit Current as a function of Supply Voltage.



Short-circuit Current as a function of Temperature.



Large Signal Step Response.



Small Signal Step Response.

Application Notes

The TLV900x is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V at the temperature range of 0 ℃ to 70 ℃, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10- kΩ loads connected to any point between VS+ and ground. The input common-mode voltage range includes both rails, and allows the TLV900x family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The TLV900x features 1.5-MHz bandwidth and 1.2- V/μs slew rate with only 85-μA supply current per amplifier, providing good ac performance at very low power consumption. DC applications are also well served with a low input noise voltage of 25-nV/√Hz at 1-kHz, low input bias current, and an input offset voltage of 120-μV typically. The typical offset voltage drift is 0.8-μV/℃, over the full temperature range the input offset voltage changes only 200-μV (120-μV to 200-μV).

OPERATING VOLTAGE

The TLV900x family is optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V) at the temperature range of 0 ℃ to 70 ℃, and fully specified and ensured for operation from 2.0 V to 5.5 V (±1.0 V to ±2.75 V). In addition, many specifications apply from –40 ℃ to +125 ℃. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages (V_{S+} to V_{S-}) higher than +10 V can permanently damage the device.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the TLV900x series extends 100-mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an Nchannel input differential pair in parallel with a Pchannel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}–1.4 V to the positive supply, whereas the Pchannel pair is active for inputs from 100-mV below the negative supply to approximately V_{S+}–1.4 V. There is a small transition region,typically V_{S+}–1.2 V to V_{S+}–1 V, in which both pairs are on. This 200-mV transition region can vary up to 200-mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}–1.4 V to V_{S+}–1.2 V on the low end, up to V_{S+}–1 V to V_{S+}–0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the TLV900x during normal operation is approximately 1-pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

INPUT EMI FILTER AND CLAMP CIRCUIT

Figure 1 shows the input EMI filter and clamp circuit. The TLV900x op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500-mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 20-mA as stated in the Absolute Maximum Ratings.

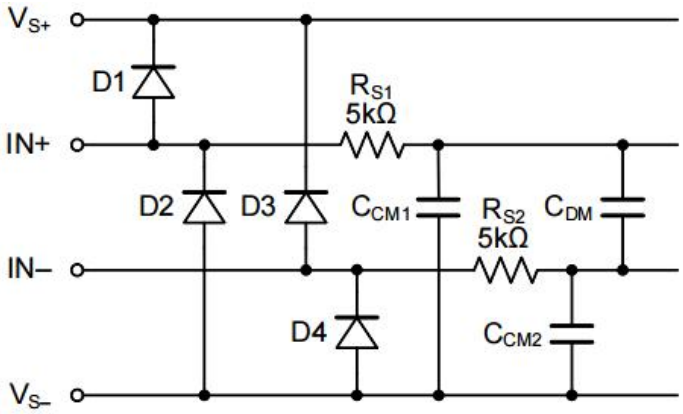


Figure 1. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the TLV900x family iscomposed of two 5-kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the −3 dB low-pass cutoff frequencies at 35-MHz for common-mode signals, and at 22-MHz for differential signals.

RAIL-TO-RAIL OUTPUT

Designed as a micro-power operational amplifier, the TLV900x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 50-kΩ, the output swings typically to within 5-mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 600-Ω, the output swings typically to within 200-mV of the positive supply rail and within 135-mV of the negative supply rail.

CAPACITIVE LOAD AND STABILITY

The TLV900x family can safely drive capacitive loads of up to 500-pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to overshooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the TLV900x op-amps must drive a load exceeding 500-pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

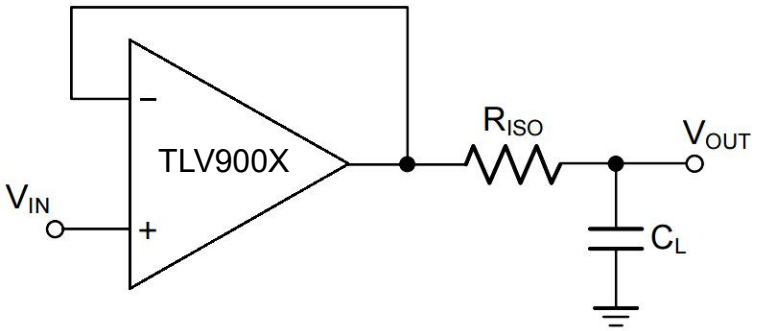


Figure 2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 3. It provides DC accuracy as well as AC stability. The $R_F$provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

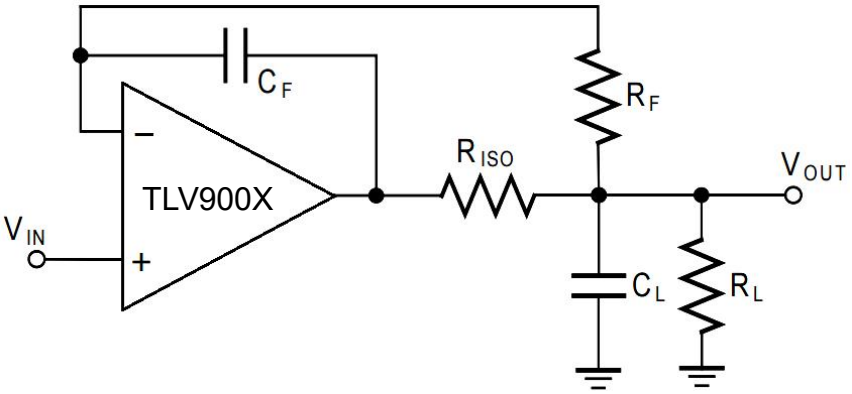


Figure 3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

OVERLOAD RECOVERY

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV900x family is approximately 2-μs.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all opamp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The TLV900x op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$\mathbf{EMIRR = 20 \log (V_{IN_PEAK} / \Delta V_{OS})}$$

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the TLV900x op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 4 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

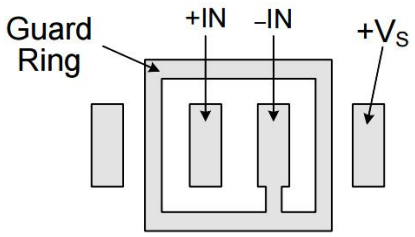


Figure 4. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-toboard trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal,resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

DIFFERENTIAL AMPLIFIER

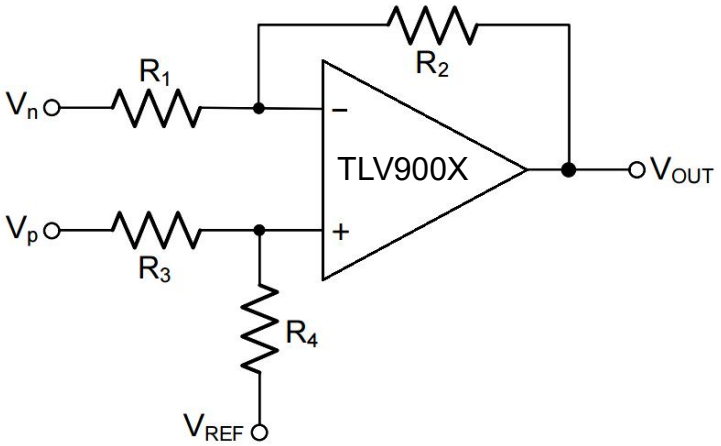
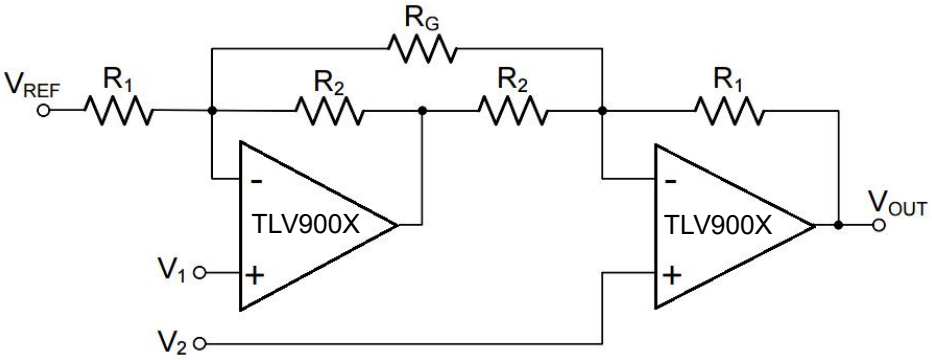


Figure 5. Differential Amplifier

The circuit shown in Figure 5 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then: $V_{OUT} = (V_p – V_n) \times R_2/R_1 + V_{REF}$

INSTRUMENTATION AMPLIFIER



$$V_{OUT} = (V_1 - V_2)(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}) + V_{REF}$$

Figure 6. Instrumentation Amplifier

The TLV900x family is well suited for conditioning sensor signals in battery-powered applications. Figure 6 shows a two op-amp instrumentation amplifier, using the TLV900x op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

BUFFERED CHEMICAL SENSORS

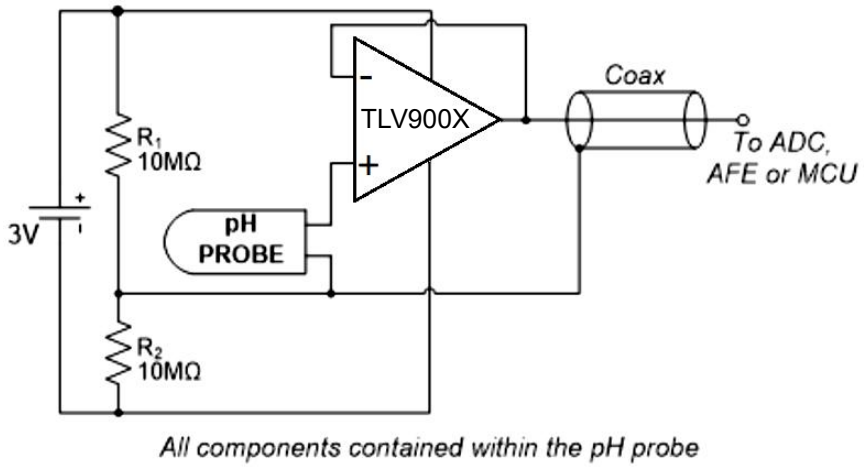


Figure 7. Buffered pH Probe

The TLV900x family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in Figure 7eliminates expansive low-leakage cables that that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. A TLV900x op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

MOTOR PHASE CURRENT SENSING AMPLIFIER

The current sensing amplification shown in Figure 8 has a slew rate of 2πfVPP for the output of sine wave signal, and has a slew rate of $2fV_{PP}$ for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10 kHz to 20 kHz, and one cycle time is 100 μs for a 10 kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 8 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t_{SR}) due to the op-amp's slew rate, and the measurement settling time (t_{SET}). For a 3-shunt solution in motor phase current sensing, if the smaller duty cycle of the PWM is defined at 45% (In fact, the phase with minimum PWM duty cycle, such as 5%, is not detected current directly, and it can be calculated from the other two phase currents), and the tSR is required at 20% of a total time window for a phase current monitoring, in case of a 3.3 V motor control system (3.3 V MCU with 12-bit ADC), the op-amp's slew rate should be more than:

3.3V / (100μs× 45% × 20%) = 0.37 V/μs

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.

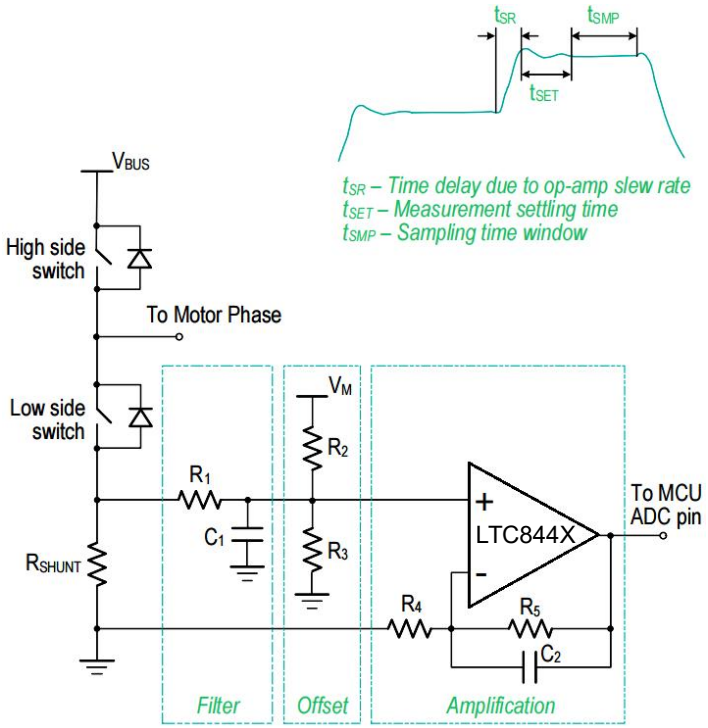
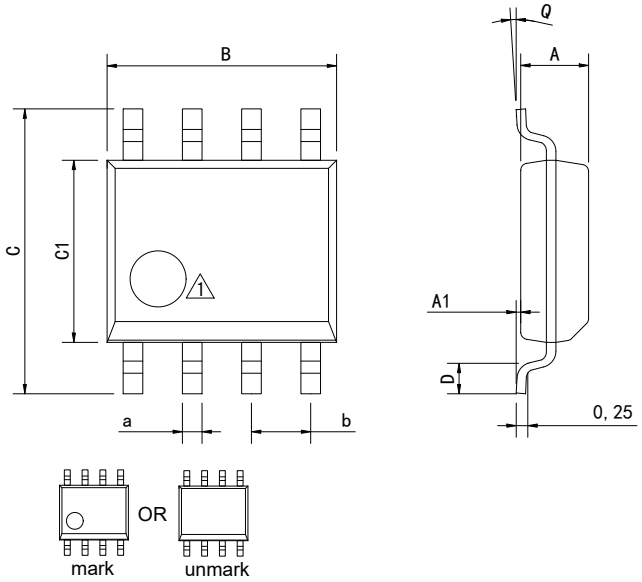


Figure 8. Current Shunt Monitor Circuit

Physical Dimensions

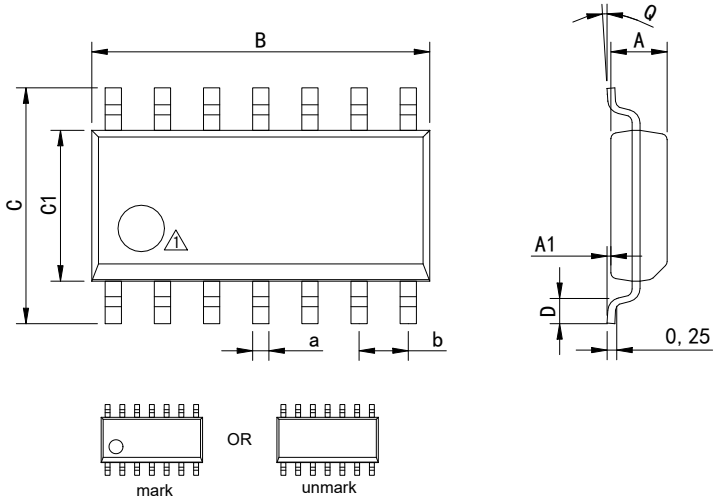
SOP-8



1 Package top mark may be in lower left corner or unmark

Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

SOP-14

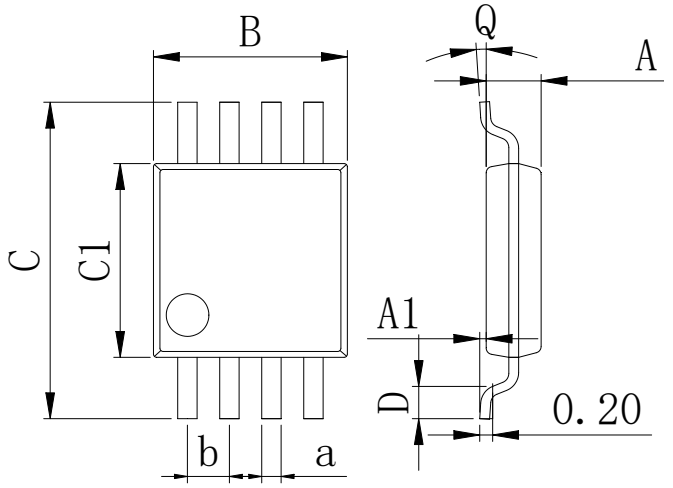


1 Package top mark may be in lower left corner or unmark

Dimensions In Millimeters(SOP-14)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.95	6.20	4.00	0.80	8°	0.45	

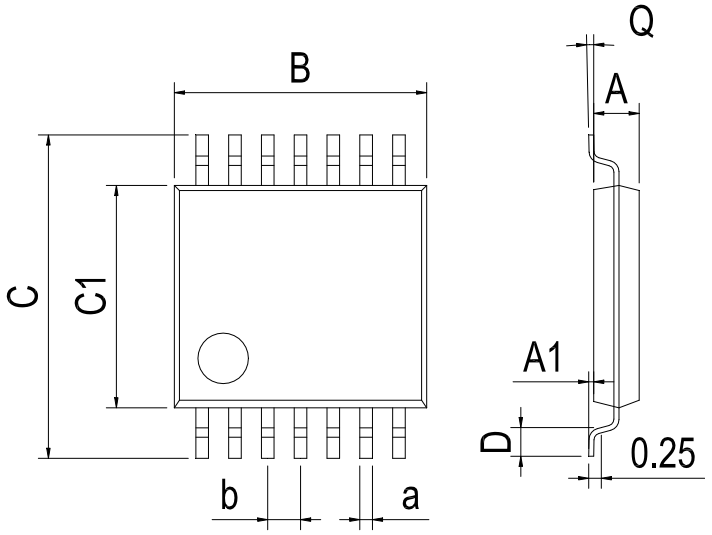
Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

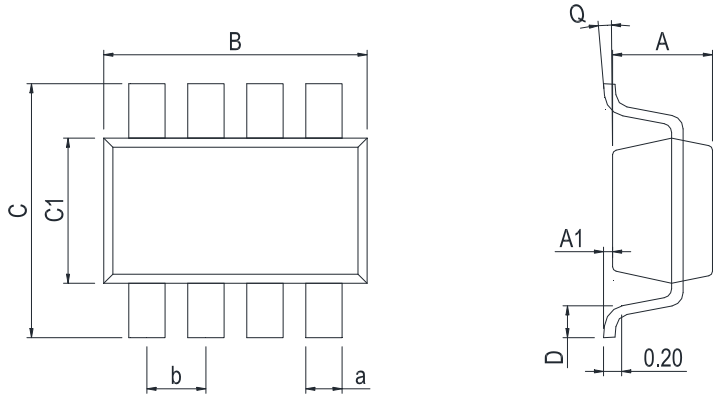
TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

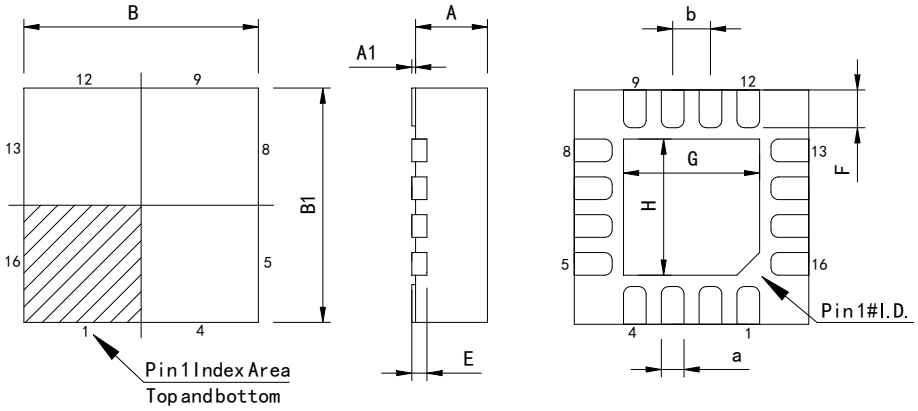
Physical Dimensions

SOT-23-8



Dimensions In Millimeters(SOT-23-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	1.00	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.65 BSC
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.50	

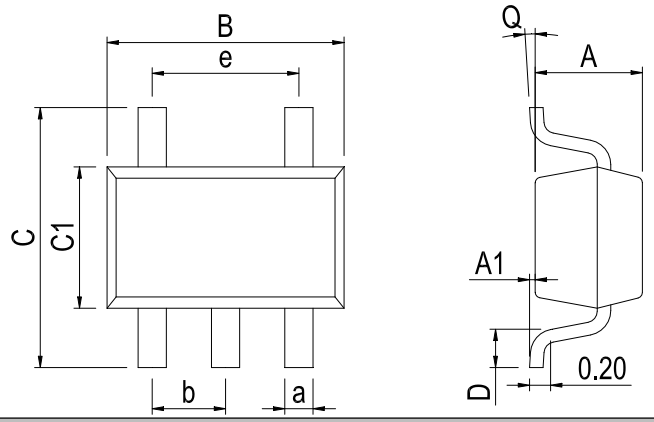
QFN-16 3*3



Dimensions In Millimeters(QFN-16 3*3)										
Symbol:	**A**	**A1**	**B**	**B1**	**E**	**F**	**G**	**H**	**a**	**b**
Min:	0.85	0	2.90	2.90	0.15	0.25	1.45	1.45	0.18	0.50TYP
Max:	0.95	0.05	3.10	3.10	0.25	0.45	1.85	1.85	0.30	

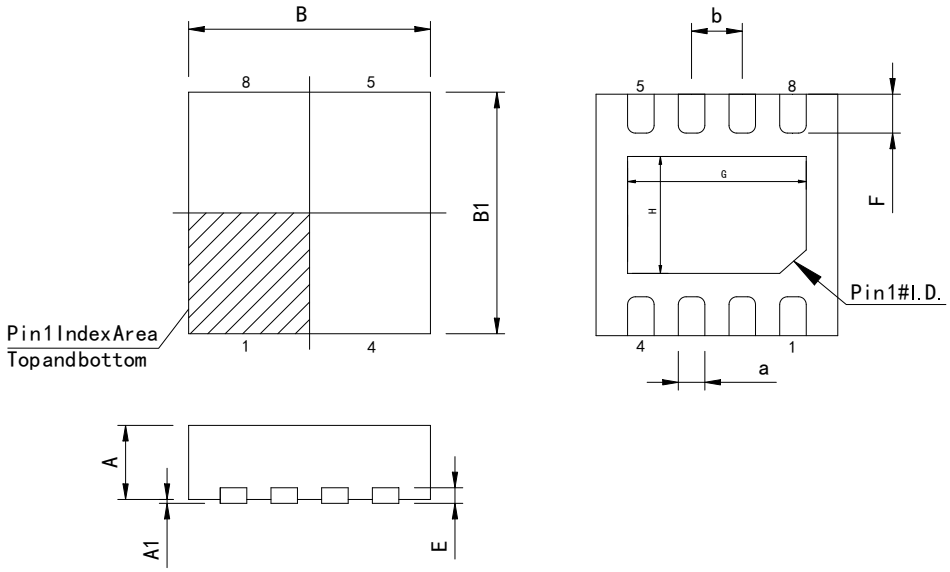
Physical Dimensions

SOT-23-5



Dimensions In Millimeters(SOT-23-5)										
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**	**e**
Min:	1.00	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.95 BSC	1.90 BSC
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.50		

DFN-8 2*2



Dimensions In Millimeters(DFN-8 2*2)										
Symbol:	**A**	**A1**	**B**	**B1**	**E**	**F**	**H**	**G**	**a**	**b**
Min:	0.85	0	1.90	1.90	0.15	0.25	0.8	1.5	0.18	0.50TYP
Max:	0.95	0.05	2.10	2.10	0.25	0.45	1.2	1.9	0.30	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V2.0	2017-9	New	1-22
V2.1	2026-1	Document Reformatting	1-22
V2.2	2026-10	Update DFN-8 and QFN-16 Dimension drawing	18、19

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