

TDSEMIC

拓電半導體

自主封測 品質把控 售後保障

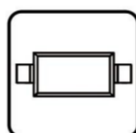
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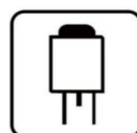
電源管理



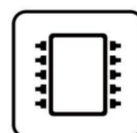
顯示驅動



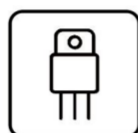
二三極管



LDO穩壓器



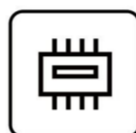
觸摸芯片



MOS管



運算放大器



存儲芯片



MCU



串口通信

TD4485

產品規格說明書

Description

The TD4485 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

Application

Battery protection

Load switch

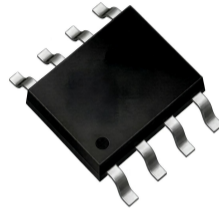
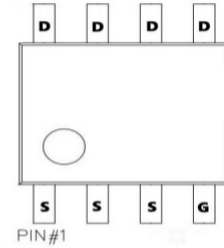
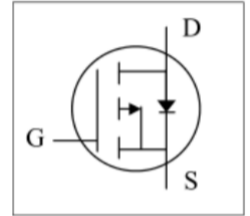
Uninterruptible power supply

General Features

$V_{DS} = -40V$ $I_D = -12A$

$R_{DS(ON)} = 15m\Omega @ V_{GS} = 10V$

$R_{DS(ON)} = 20m\Omega @ V_{GS} = 4.5V$



Package Marking and Ordering Information

Product ID	Package	Marking	QTY(PCS)	Packing method
TD4485	SOP-8L	4485	3000	Reel

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-12	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-10	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-10	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-8	A
I_{DM}	Pulsed Drain Current ²	-30	A
EAS	Single Pulse Avalanche Energy ³	15	mJ
I_{AS}	Avalanche Current	-54	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	52.1	W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.4	$^\circ C/W$

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-40	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.023	---	V/°C
R _{DS(on)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-12A	---	---	15	mΩ
		V _{GS} =-4.5V, I _D =-10A	---	---	20	
V _{GS(th)}	Gate Threshold Voltage		-1.0	-1.6	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient	V _{GS} =V _{DS} , I _D =-250μA	---	4.74	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-32V, V _{GS} =0V, T _J =25°C	---	---	1	μA
		V _{DS} =-32V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-18A	---	24	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	7	14	
Q _g	Total Gate Charge (-4.5V)		---	27.9	---	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-12A	---	7.7	---	
Q _{gd}	Gate-Drain Charge		---	7.5	---	
T _{d(on)}	Turn-On Delay Time		---	40	---	ns
T _r	Rise Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	35.2	---	
T _{d(off)}	Turn-Off Delay Time		---	100	---	
T _f	Fall Time		---	9.6	---	
C _{iss}	Input Capacitance		---	3500	---	pF
C _{oss}	Output Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	323	---	
C _{rss}	Reverse Transfer Capacitance		---	222	---	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-52	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-105	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-54A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

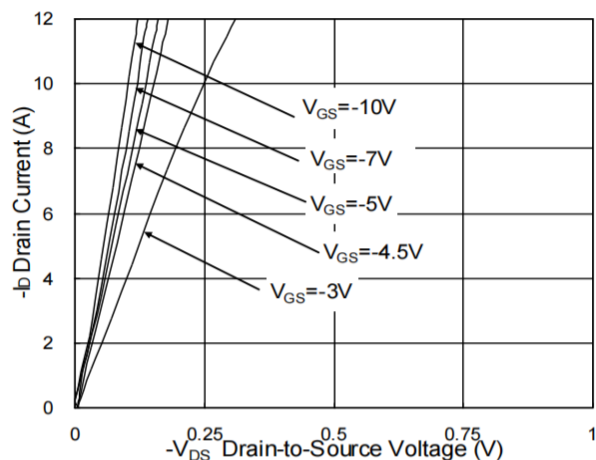


Fig.1 Typical Output Characteristics

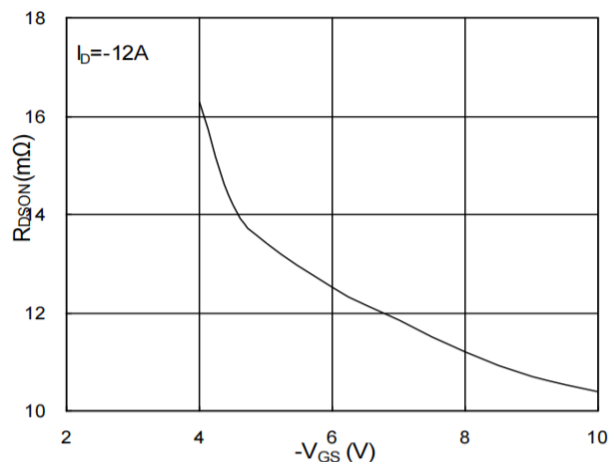


Fig.2 On-Resistance v.s Gate-Source

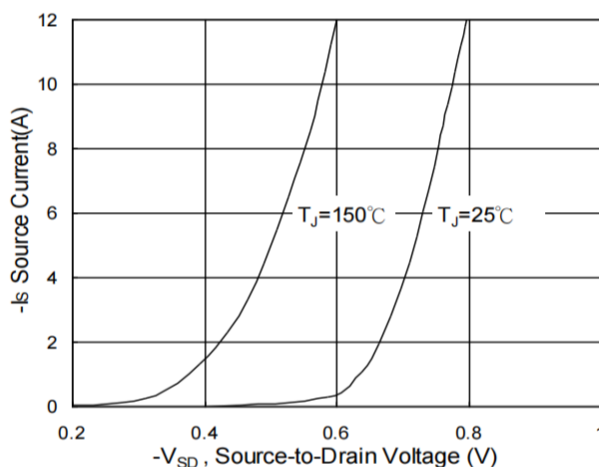


Fig.3 Forward Characteristics Of Reverse

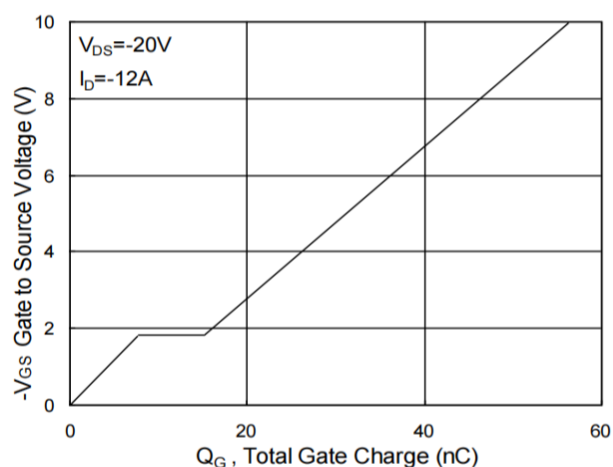


Fig.4 Gate-Charge Characteristics

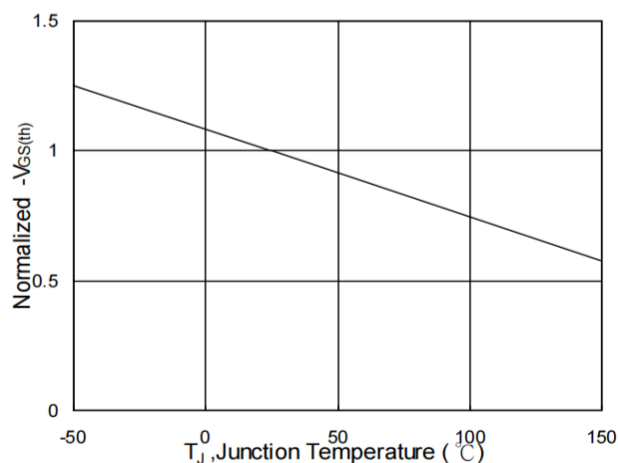


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

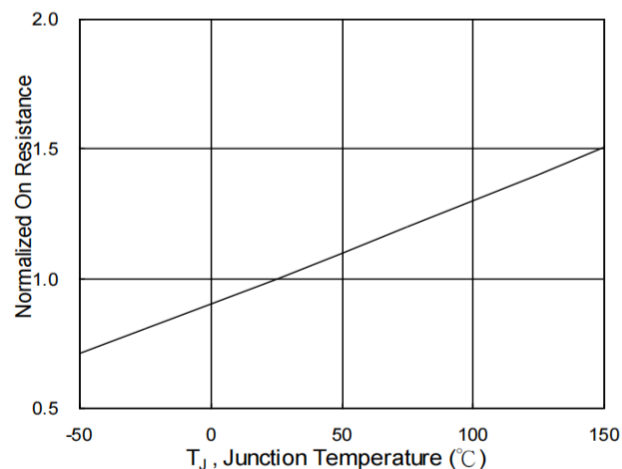


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

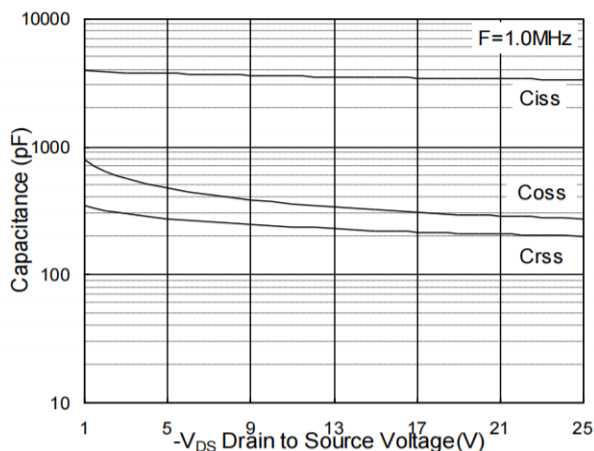


Fig.7 Capacitance

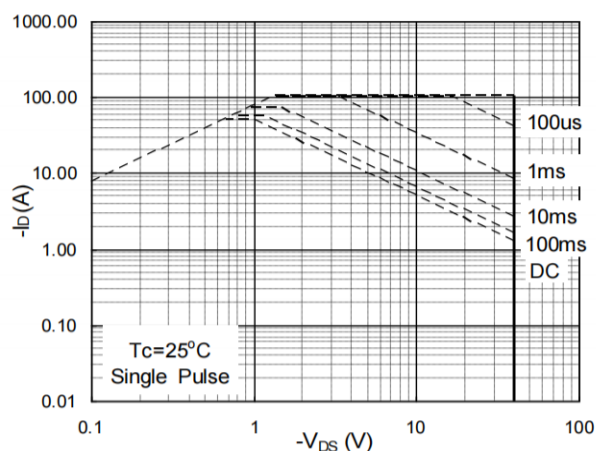


Fig.8 Safe Operating Area

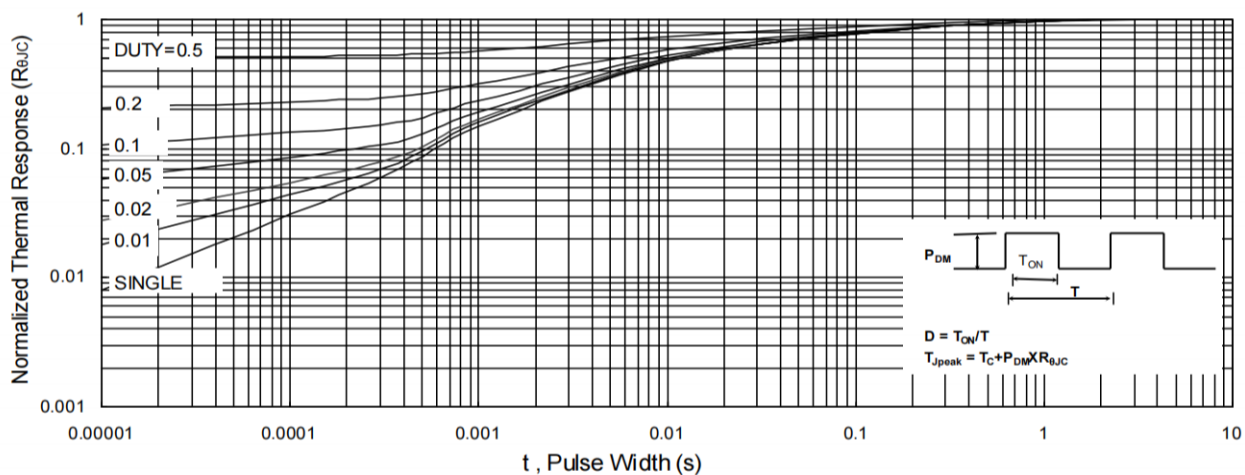


Fig.9 Normalized Maximum Transient Thermal Impedance

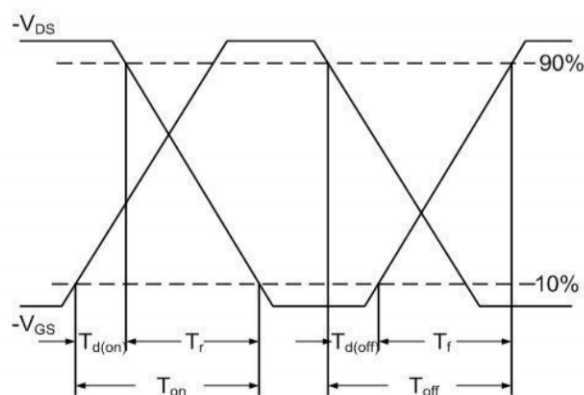


Fig.10 Switching Time Waveform

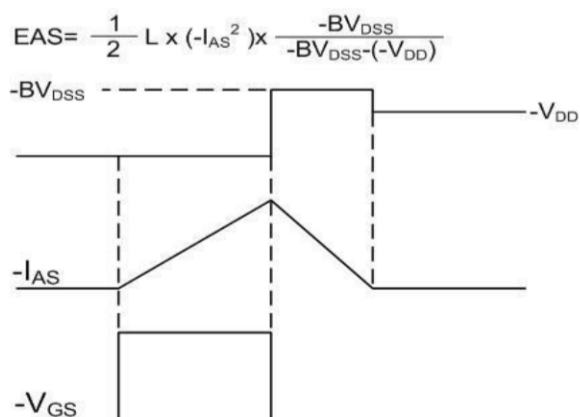
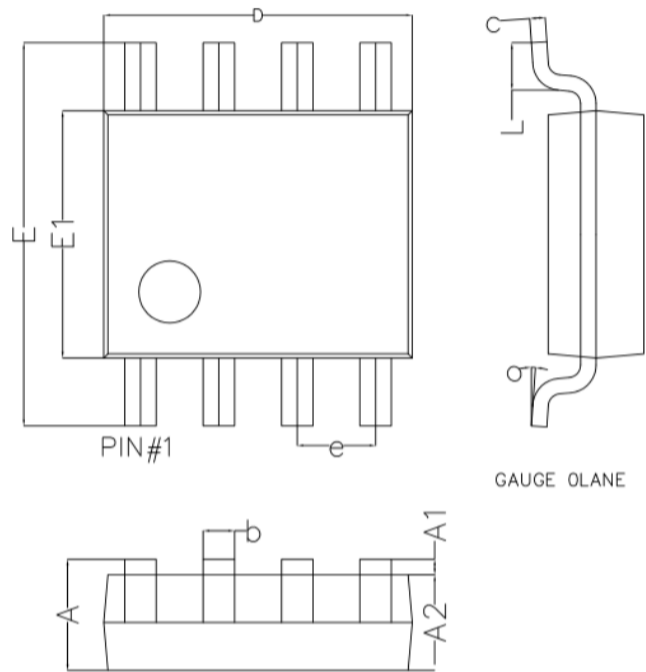


Fig.11 Unclamped Inductive Waveform

PACK SOP-8

SOP8 Package outline



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270 (BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°