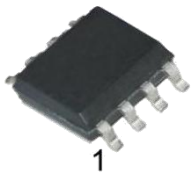
3.3V CAN Bus Transceivers

FEATURES

- Operates with a single 3.3V Supply
- Compatible With ISO 11898-2 Standard
- Low Power Replacement for the TJA1050 Footprint
- Bus Pin ESD Protection Exceeds ±16kV HBM
- High Input Impedance Allows for Up to 120 nodes
- Adjustable Driver Transition Times
- Low Current Standby Mode
- Data Rates up to 5Mbps
- Thermal Shutdown Protection
- Open Circuit Fail-Safe Design
- Glitch Free Power Up and Power Down Protection for Hot Plugging Applications



SOP-8

MSOP-8

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG65HVD230M/TR	SOP-8	HVD230	REEL	2500pcs/reel
HG65HVD230MM/TR	MSOP-8	HVD230	REEL	3000pcs/reel

DESCRIPTION

The HG65HVD230 controller area network (CAN) transceivers are compatible to the specifications of the ISO 11898-2 High Speed CAN Physical Layer standard (transceiver). These devices are designed for data rates up to 5Mbps, and include many protection features providing device and CAN network robustness. The HG65HVD230 transceivers are designed for use with 3.3V μP, MCU and DSP with CAN controllers, or with equivalent protocol controller devices. The devices are intended for use in applications employing the CAN serial communication physical layer in accordance with the ISO 11898 standard.

Designed for operation in especially harsh environments, these devices feature cross wire protection, loss of ground and over voltage protection, over temperature protection, as well as wide common mode range of operation.The CAN transceiver is the CAN physical layer and interfaces the single ended host CAN protocol controller with the differential CAN bus found in industrial, building automation, and automotive applications. These devices operate over a -2V to 7V common mode range on the bus.

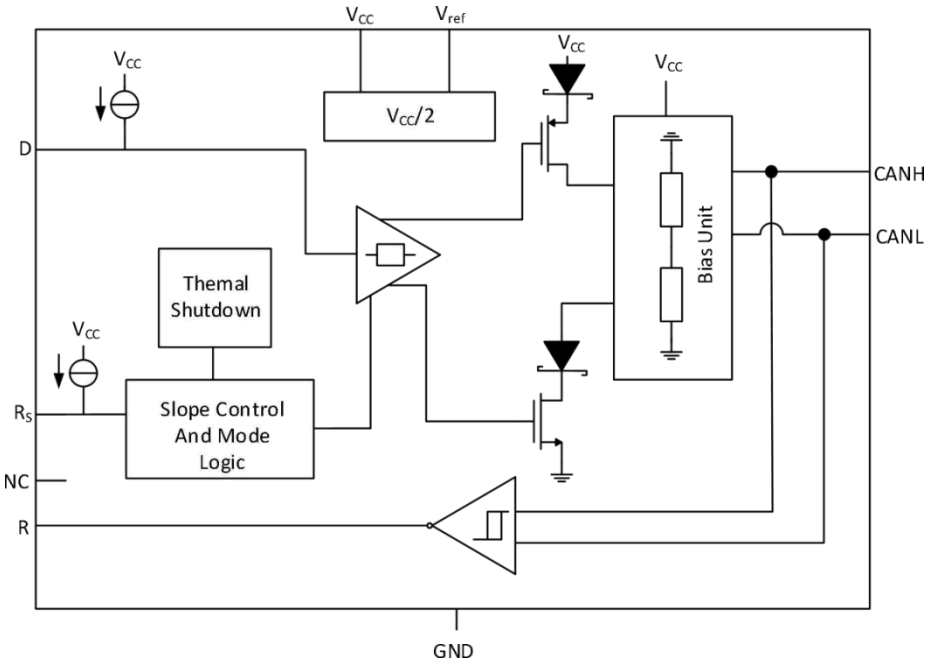
The Rs pin (pin 8) on the HG65HVD230 provides three different modes of operation: high speed mode, slope control mode, and low-power mode. The high speed mode of operation is selected by connecting the Rs pin to ground, allowing the transmitter output transistors to switch on and off as fast as possible with no limitation on the rise and fall slopes. The rise and fall slopes can also be adjusted by connecting a resistor in series between the Rs pin and ground. The slope will be proportional to the pin's output current.With a resistor Value of 10kΩ the device will have a slew rate of ~15V/μs, and with a resistor Value of 100kΩ the device will have a slew rate of ~10V/μs. See Application Information for more information.

The HG65HVD230 enters a low current standby mode (listen only) during which the driver is switched off and the receiver remains active if a high logic level is applied to the Rs pin. This mode provides a lower power consumption mode than normal mode while still allowing the CAN controller to monitor the bus for activity indicating it should return the transceiver to normal mode or slope control mode. The host controller (MCU, DSP) returns the device to a transmitting mode (high speed or slope control) when it wants to transmit a message to the bus or if during standby mode it received bus traffic indicating the need to once again be ready to transmit.

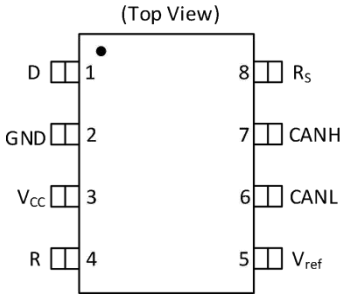
APPLICATIONS

- Industrial Automation, Sensors and Drive Systems
- Motor and Robotic Control
- Building and Climate Control (HVAC)
- Telecommunications and Base Station Control and Status
- CAN Bus Standards Such as CAN open

Block Diagram



Pin Configuration and Functions



SOP-8

Pin		Type	Description
Name	No.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), Also called TXD, driver input
GND	2	GND	Ground connection
V_{CC}	3	Supply	Transceiver 3.3V supply Voltage
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
V_{ref}	5	O	VCC /2 reference output pin
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
Rs	8	I	Mode select pin: strong pull down to GND = high speed mode, strong pull up to VCC = low power mode, 10kΩ to 100kΩ pull down to GND = slope control mode

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply Voltage,V_{CC}	–0.3	6	V
Voltage at any bus terminal (CANH or CANL)	–40	40	V
Digital Input and Output Voltage,VI (D or R)	–0.5	V_{CC} + 0.5	V
Receiver output current, I_O	–11	11	mA
Storage temperature, T_{stg}	–40	85	°C
Lead Temperature Range (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All Voltage Values, except differential I/O bus Voltages, are with respect to network ground terminal.

ESD Ratings

			Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM)	CANH, CANL and GND	±16000	V
		All pins	±4000	
	Charged-device model (CDM)		±1000	

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage,V_{CC}		3		3.6	V
Voltage at any bus terminal (common mode)V_{IC}		–2(1)		7	V
Voltage at any bus terminal (separately)V_I		–2.5		7.5	V
High-level input Voltage,V_{IH}	D, R	2			V
Low-level input Voltage,V_{IL}	D, R			0.8	V
Differential input Voltage,V_{ID} (see Figure 5)		–6		6	V
Input Voltage,$V_{(Rs)}$		0		V_{CC}	V
Input Voltage for standby or sleep,$V_{(Rs)}$		0.75V_{CC}		V_{CC}	V
Wave-shaping resistance, R_s		0		100	kΩ
High-level output current, I_{OH}	Driver	–40			mA
	Receiver	–8			
Low-level output current, I_{OL}	Driver			48	mA
	Receiver			8	
Thermal shutdown temperature			165		°C
Thermal shutdown hysteresis			10		
Operating free-air temperature(2), T_A		–40		125	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) Operating temperature range: -40°C to +125°C. This product is designed for industrial grade applications. For automotive grade versions compliant with AEC-Q100, please conduct internal screening per the standard or contact our sales team for availability.

Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

Parameter			Test Conditions		MIN	TYP(1)	MAX	UNIT
V_{OH}	Bus output Voltage	Dominant	V_I = 0V, See Figure 1 and Figure 3	CANH	2.45		V_{CC}	V
				CANL	0.5		1.0	
V_{OL}		Recessive	V_I = 3V, See Figure 1 and Figure 3	CANH		2.3		
				CANL		2.3		
$V_{OD(D)}$	Differential output Voltage	Dominant	V_I = 0V,	See Figure 1	1.5	2	3	V
			V_I = 0V,	See Figure 2	1.2	2	3	
$V_{OD(R)}$		Recessive	V_I = 3V,	See Figure 1	–120	0	12	mV
			V_I = 3V,	No load	–0.5	–0.2	0.05	V
I_{IH}	High-level input current		V_I = 2V		–10	-2.5	10	μA
I_{IL}	Low-level input current		V_I = 0.8V		–10	-6.0	15	μA
I_{OS}	Short-circuit output current		V_{CANH} = -2V		–250		250	mA
			V_{CANL} = 7V		–250		250	
C_o	Output capacitance		See receiver					
I_{CC}	Supply current	Standby	$V_{(Rs)}$ =V_{CC}			400	600	μA
		All devices	Dominant	V_I =0V,No load	Dominant		1	2	mA
			Recessive	V_I =V_{CC},No load	Recessive		1	2	

(1) All typical Values are at 25°C and with a 3.3V supply.

Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold Voltage	See Table 1				800	900	mV
V_{IT-}	Negative-going input Threshold Voltage				500	700		mV
V_{hys}	Hysteresis Voltage (V_{IT+} –$V_{IT–}$)					100		
V_{OH}	High-level output Voltage	-6V ≤V_{ID} ≤ 500mV,I_O = -8mA,See Figure 5			2.4			V
V_{OL}	Low-level output Voltage	900mV ≤V_{ID} ≤ 6V, I_O = 8mA, See Figure 5					0.4	
I_I	Bus input current	V_{IH} = 7V	V_{CC} = 0V	Other input at 0V, D = 3V	100		350	μA
		V_{IH} = -2V			–200		–30	
		V_{IH} = -2V	V_{CC} = 0V		–100		–20	
R_{Diff}	Differential input resistance	Pin-to-pin	$V_{(D)}$ = 3V		40	70	100	kΩ
R_I	CANH, CANL input resistance				20	35	50	kΩ

(1) All typical Values are at 25°C and with a 3.3V supply.

Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

Parameter			Test Conditions	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time,low-to-high-level output	$V_{(Rs)}$ = 0V	C_L = 50pF, See Figure 4		55	85	ns
		Rs with 10kΩ to ground			80	125	
		Rs with 100kΩ to ground			110	160	
t_{PHL}	Propagation delay time,high-to-low-level output	$V_{(Rs)}$ = 0V			80	120	ns
		Rs with 10kΩ to ground			130	180	
		Rs with 100kΩ to ground			170	240	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	$V_{(Rs)}$ = 0V		25			ns
		Rs with 10kΩ to ground		50			
		Rs with 100kΩ to ground		60			
t_r	Differential output signal rise time	$V_{(Rs)}$ = 0V		25	50	100	ns
t_f	Differential output signal fall time			30	40	70	ns
t_r	Differential output signal rise time	Rs with 10kΩ to ground		40	70	150	ns
t_f	Differential output signal fall time			45	60	100	ns
t_r	Differential output signal rise time	Rs with 100kΩ to ground		60	100	200	ns
t_f	Differential output signal fall time			70	90	140	ns

Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6		35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				10	ns
t_r	Output signal rise time				1.5	ns
t_f	Output signal fall time				1.5	ns

Switching Characteristics: Device

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions		MIN	TYP	MAX	UNIT
$t_{(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	$V_{(Rs)}$ = 0V	See Figure 8		90	130	ns
		Rs with 10kΩ to ground	See Figure 8		135	205	
		Rs with 100kΩ to ground	See Figure 8		180	260	
$t_{(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	$V_{(Rs)}$ = 0V	See Figure 8		120	140	ns
		Rs with 10kΩ to ground	See Figure 8		180	215	
		Rs with 100kΩ to ground	See Figure 8		240	280	

Device Control-Pin Characteristics

Over recommended operating conditions(unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
$t_{(WAKE)}$	wake-up time from standby mode with Rs	See Figure 7		0.5	1.5	μs
V_{ref}	Reference output Voltage	-5μA < $I_{(Vref)}$ < 5μA	0.45V_{CC}		0.55V_{CC}	V
		-50μA < $I_{(Vref)}$ < 50μA	0.4V_{CC}		0.6V_{CC}	
$I_{(RS)}$	Input current for high-speed	$V_{(Rs)}$< 1V	-450		0	μA

All typical values are at 25°C and with a 3.3V supply

Parameter Measurement Information

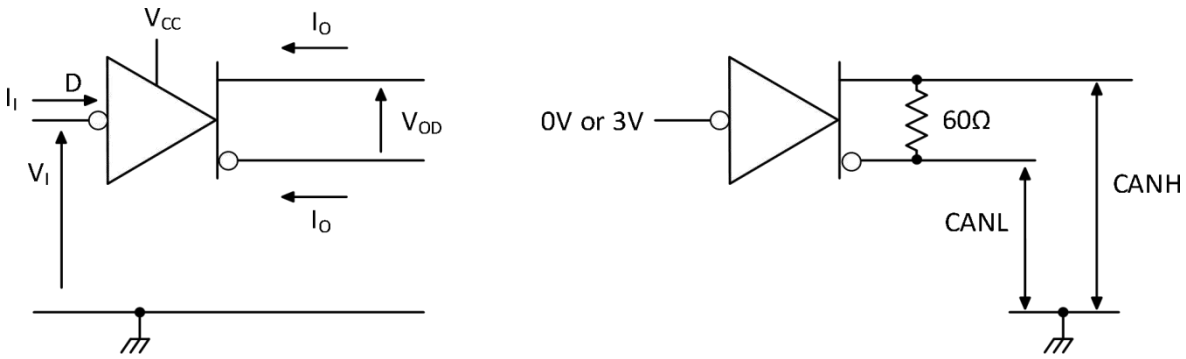


Figure1. Dirver Voltage and Current Definitions

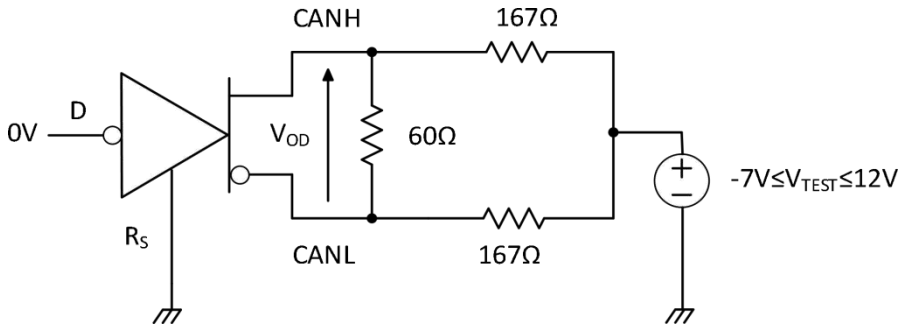


Figure2. Driver V_{OD}

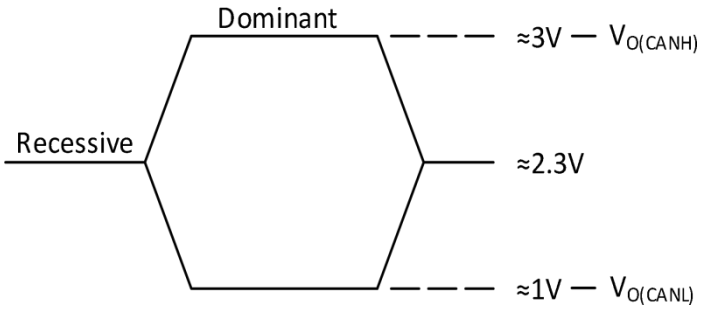
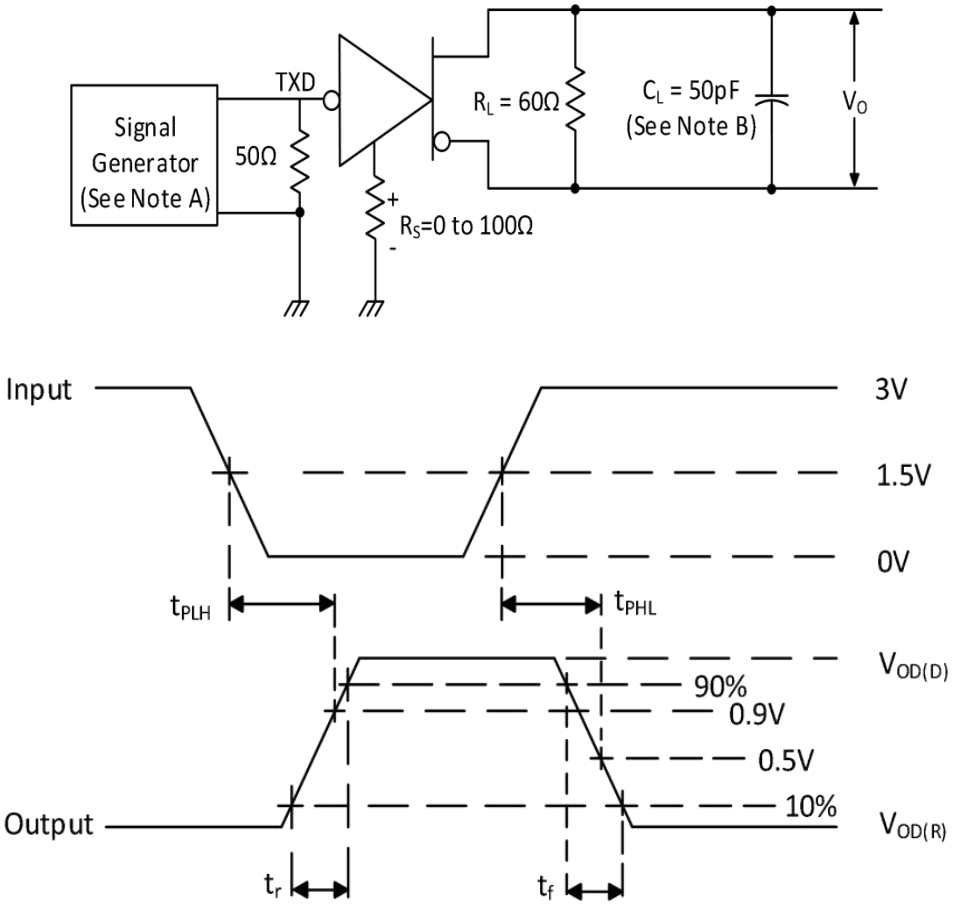


Figure3. Diver Output Voltage Definitions



A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. C_L includes fixture and instrumentation capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

$$V_{IC} = \frac{V_{I(CANH)} + V_{I(CANL)}}{2}$$

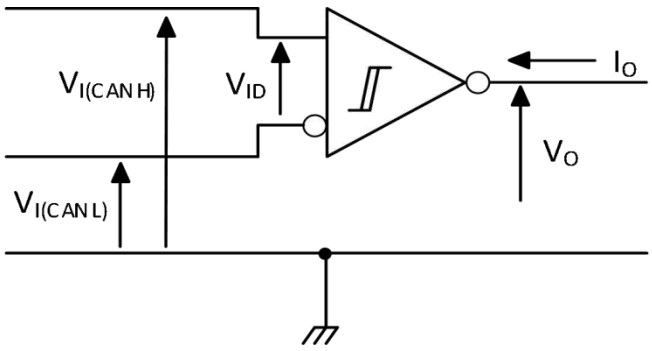
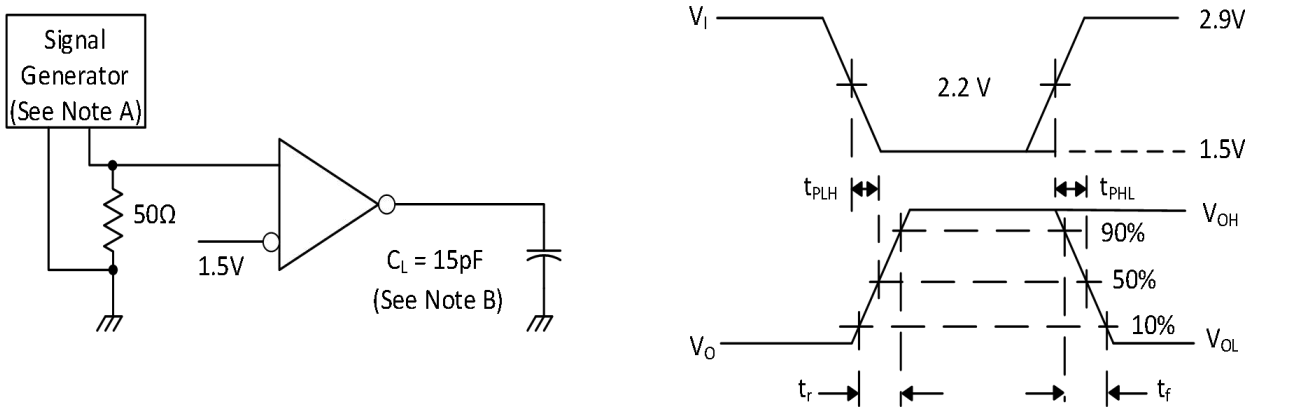


Figure 5. Receiver Voltage and Current Definitions



A. The Input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O= 50 Ω.

B. CL includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 1. Receiver Characteristics Over Common Mode With $V_{(Rs)}$=1.2V

V_{IC}	V_{ID}	V_{CANH}	V_{CANL}	R OUTPUT	
-2V	900mV	-1.55V	-2.45V	L	V_{OL}
7V	900mV	8.45V	6.55V	L	
1V	6V	4V	-2V	L	
4V	6V	7V	1V	L	
-2V	500mV	-1.75V	-2.25V	H	V_{OH}
7V	500mV	7.25V	6.75V	H	
1V	-6V	-2V	4V	H	
4V	-6V	1V	7V	H	
X	X	Open	Open	H	

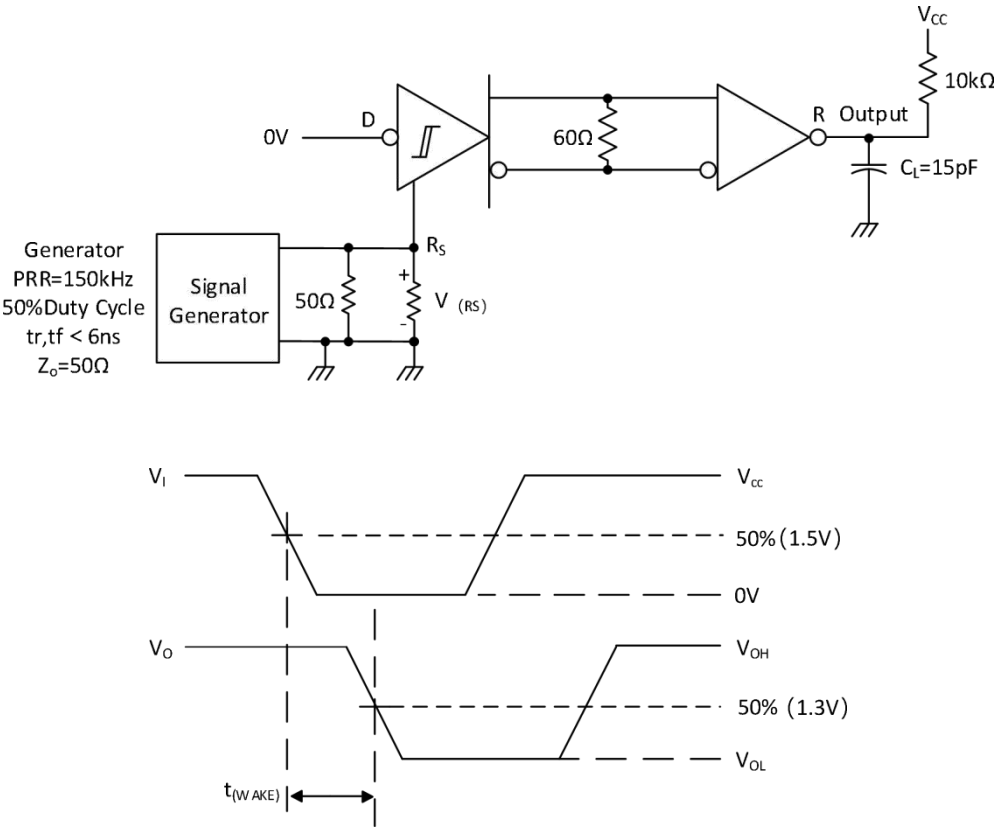
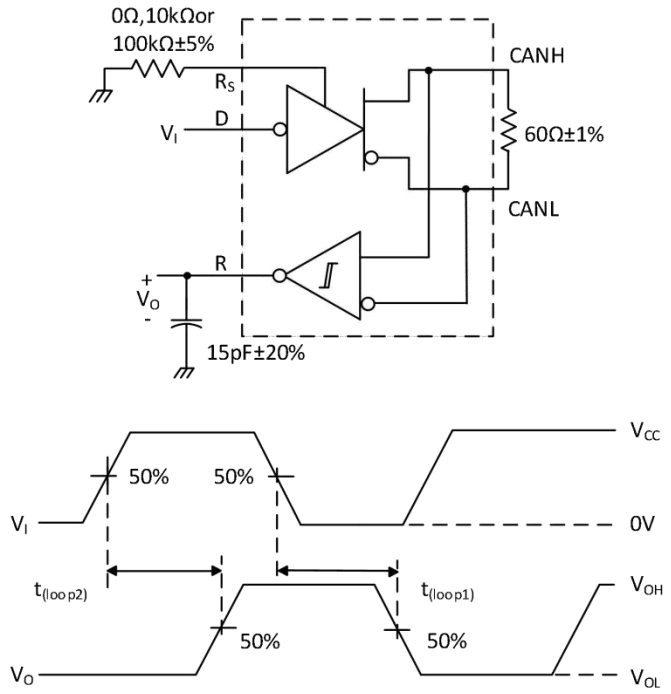


Figure7. $t_{(WAKE)}$ Test Circuit and Voltage Waveforms



A. All VI input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 6ns, Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. $t_{(LOOP)}$ Test Circuit and Voltage Waveforms

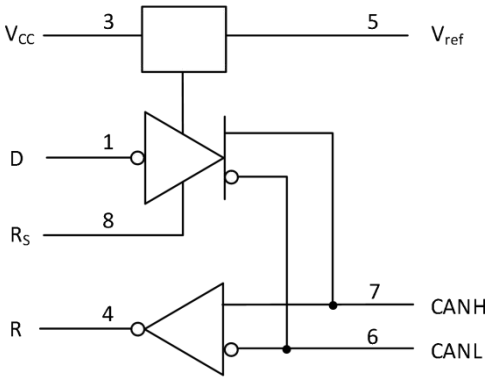


Figure 9. Logic Diagram (Positive Logic)

Slope Control Mode

Electromagnetic compatibility is essential in many applications while still making use of unshielded twisted pair bus cable to reduce system cost. Slope control mode was added to the HG65HVD230 devices to reduce the electromagnetic interference produced by the rise and fall times of the driver and resulting harmonics. These rise and fall slopes of the driver outputs can be adjusted by connecting a resistor from Rs (pin 8) to ground or to a logic low Voltage, as shown in Figure 10. The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor Value of 10kΩ to achieve a ~15V/μs slew rate, and up to 100kΩ to achieve a ~10V/μs slew rate as displayed in Figure 11.

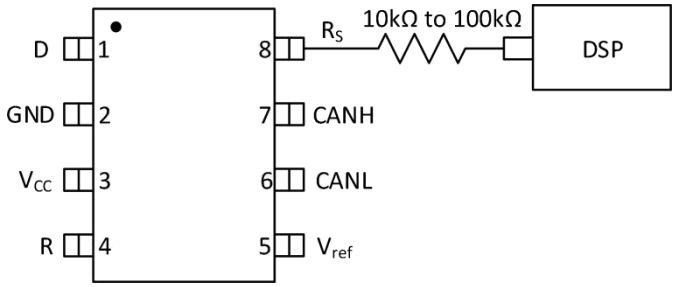


Figure10. Slope Control/Standby Connection to a DSP

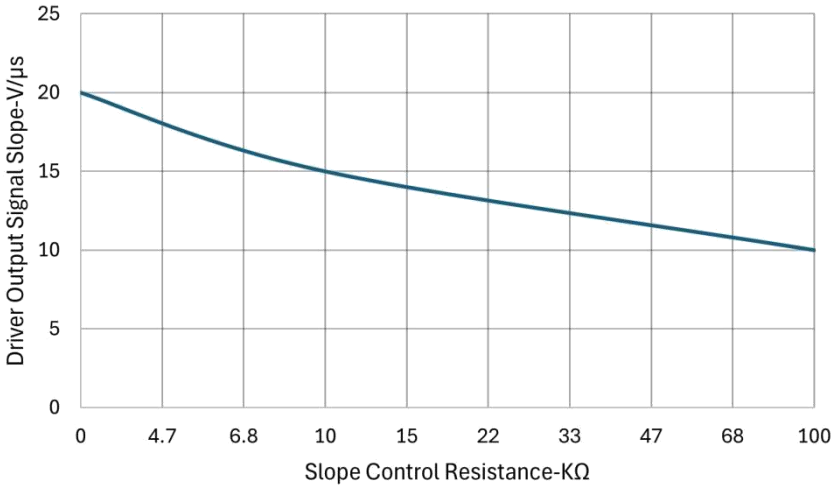


Figure 11. HG65HVD230 Driver Output Signal Slope Vs Slope Control Resistance Value

Standby Mode (Listen Only Mode)

If a logic high (> 0.75V_{CC}) is applied to Rs (pin 8) in Figure 10, the circuit of the HG65HVD230 enters a low-current, listen only standby mode, during which the driver is switched off and the receiver remains active. In this listen only state, the transceiver is completely passive to the bus. It makes no difference if a slope control resistor is in place as shown in Figure 10. The μP can reverse this low-power standby mode when the rising edge of a dominant state (bus differential Voltage > 900mV typical) occurs on the bus. The μP, sensing bus activity, reactivates the driver circuit by placing a logic low (< 1.2V) on Rs (pin 8).

The Babbling Idiot Protection

Occasionally, a runaway CAN controller unintentionally sends messages that completely tie up the bus (what is referred to in CAN jargon as a babbling idiot). When this occurs, the μP, MCU or DSP can engage the listen-only standby mode of the transceiver to disable the driver and release the bus, even when access to the CAN controller has been lost. When the driver circuit is deactivated, its outputs default to a high-impedance state (recessive).

Summary of Device Operating Modes

Table 2 shows a summary of the operating modes for the HG65HVD230.

Table 2. HG65HVD230 Operating Modes

Rs Pin	MODE		DRIVER	RECEIVER	RXD Pin
LOW,$V_{(Rs)}$ < 1.2V, strong pull down to GND	High Speed Mode		Enabled (ON) High Speed	Enabled (ON)	Mirrors Bus State (1)
LOW,$V_{(Rs)}$ < 1.2V, 10kΩ to 100kΩ pull down to GND	Slope Control Mode		Enabled (ON) with Slope Control	Enabled (ON)	Mirrors Bus State
HIGH,$V_{(Rs)}$ > 0.75VCC	Low Current Mode	Standby Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 3. HG65HVD230 Driver Functions

DRIVER (1)				
INPUT D	Rs	OUTPUTS		BUS STATE
		CANH	CANL	
L	$V_{(Rs)}$ < 1.2V (including 10kΩ to 100kΩ pull down to GND)	H	L	Dominant
H		Z	Z	Recessive
Open	X	Z	Z	Recessive
X	$V_{(Rs)}$ > 0.75VCC	Z	Z	Recessive

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 4. HG65HVD230 Receiver Functions

RECEIVER (1)		
DIFFERENTIAL INPUTS	Rs	OUTPUT R
V_{ID} ≥ 0.9V	X	L
0.5V <V_{ID} < 0.9V	X	?
V_{ID} ≤ 0.5V	X	H
Open	X	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

Application and Implementation

Application Information

This application section provides information concerning the implementation of the physical medium attachment layer in a CAN network according to the ISO 11898 standard. It presents a typical application circuit and test results, as well as discussions on slope control, total loop delay, and interoperability in 5V CAN systems.

CAN Bus States

The CAN bus has two states during powered operation of the device; dominant and recessive. A dominant bus state is when the bus is driven differently, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to V_{CC} / 2 Via the high-resistance internal resistors RI and R_{Diff} of the receiver, corresponding to a logic high on the D and R pins. See Figure 12 and Figure 13.

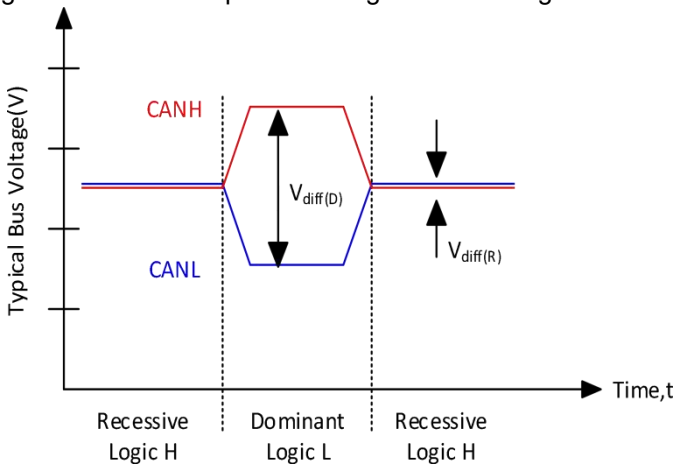


Figure 12.CAN Bus States(Physical Bit Representation)

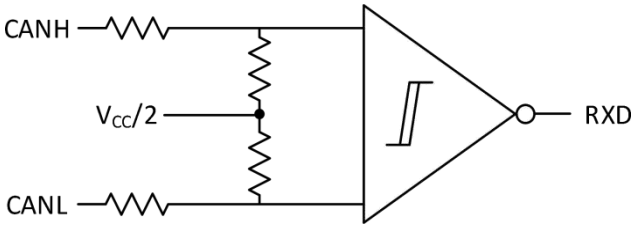


Figure 13. Simplified Recessive Common Mode Bias and Receiver

Typical Application

Figure 14 illustrates a typical application of the HG65HVD230 family. The output of the host μP's CAN controller (TXD) is connected to the transceivers driver input, pin D, and the transceivers receiver output, pin R, is connected to the input of the CAN controller (RXD). The transceiver is attached to the differential bus lines at pins CANH and CANL. Typically, the bus is a twisted pair of wires with a characteristic impedance of 120 Ω, in the standard half-duplex multi point topology of Figure 15. Each end of the bus is terminated with 120 Ω resistors in compliance with the standard to minimize signal reflections on the bus.

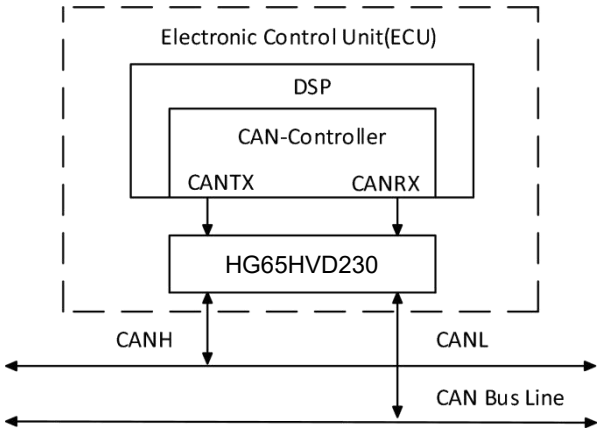


Figure 14. Details of a Typical CAN Node

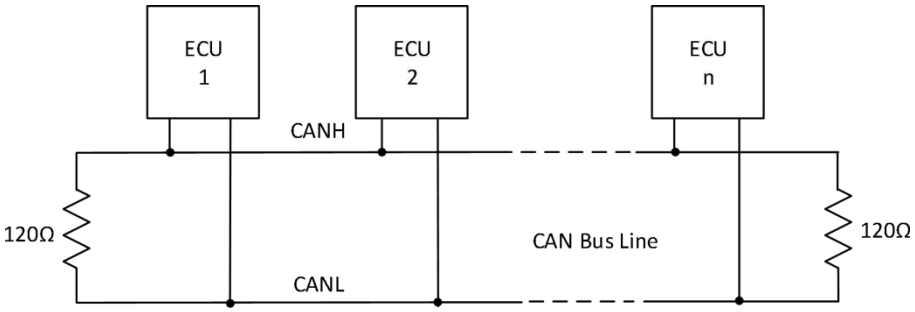


Figure 15. Typical CAN Network

CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

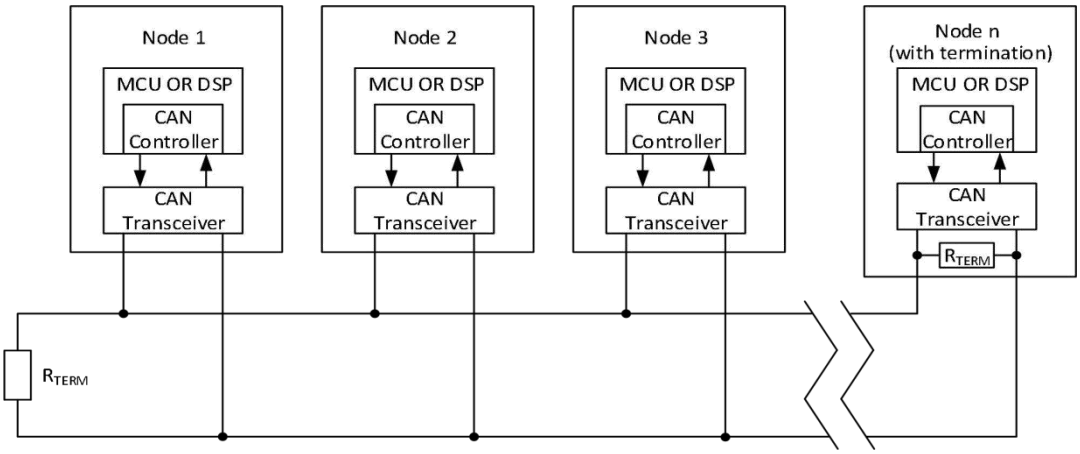


Figure 16. Typical CAN Bus

Termination is typically a 120 Ω resistor at each end of the bus. If filtering and stabilization of the common mode Voltage of the bus is desired, then split termination may be used (see Figure 17). Split termination utilizes two 60Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode Voltages at the start and end of message transmissions. Care should be taken in the power ratings of the termination resistors used. Typically the worst case condition would be if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition would be much higher than the transceiver's current limit.

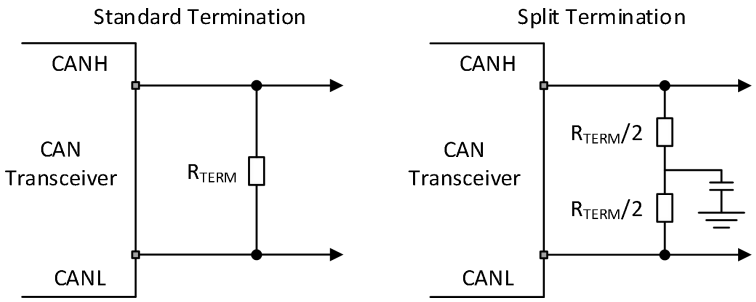


Figure 17. CAN Termination

Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (D pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs (CANH and CANL) to its output (R pin).

A typical loop delay for the HG65HVD230 transceiver is displayed in Figure 18. This loop delay will increase as the slope of the driver output is slowed during slope control mode. This increased loop delay means that there is a trade off between the total bus length able to be used and the driver's output slope used Via the slope control pin of the device.

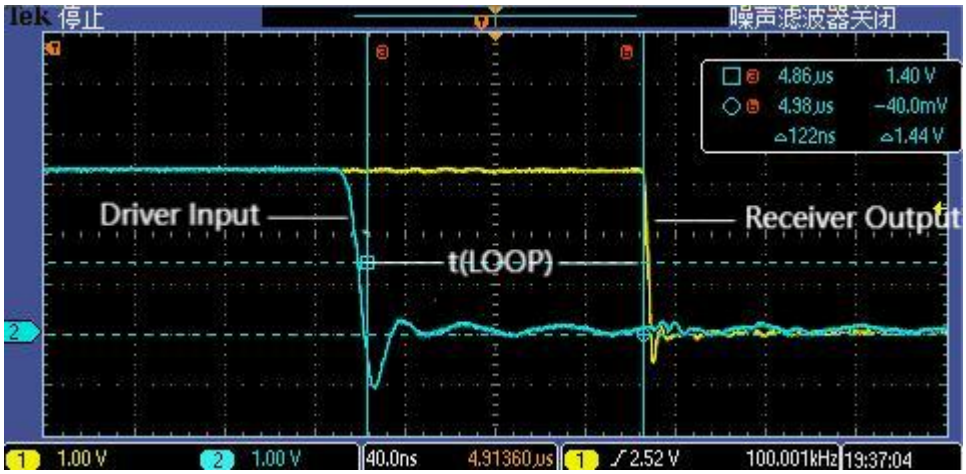


Figure 18. 122-ns Loop Delay Through the HG65HVD230 With Rs = 0

Bus Loading, Length and Number of Nodes

The ISO11898 Standard specifies up to 1Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CAN open, CAN kingdom, Device Net and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the HG65HVD230 CAN family. ISO11898-2 specifies the driver differential output with a 60 Ω load (two 120 Ω termination resistors in parallel) and the differential output must be greater than 1.5V. The HG65HVD230 devices are specified to meet the 1.5V requirement with a 60 Ω load, and additionally specified with a differential output Voltage minimum of 1.2V across a common mode range of –2V to 7V Via a 167 Ω coupling network. This network represents the bus loading of 120 HG65HVD230 transceivers based on their minimum differential input resistance of 40kΩ. Therefore, the HG65HVD230 supports up to 120 transceivers on a single bus segment with margin to the 1.2V minimum differential input Voltage requirement at each node. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loading, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO11898 standard of 40 meters by careful system design and data rate trade offs. For example, CAN open network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.This flexibility in CAN network design is one of the key strengths of the Various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design.

Detailed Design Procedure

The following system level considerations should be looked at when designing your application. There are trade- offs between the total number of nodes, the length of the bus, and the slope of the driver output that need to be evaluated when building up a system.

Transient Protection

Typical applications that use CAN will sometime require some form of ESD, burst, or surge protection performance at the system level. If these requirements are higher than those of the device some form of external protection may be needed to shield the transceiver against these high power transients that can cause damage. Transient Voltage suppressor (TVS) are Very commonly used and can help clamp the amount of energy that reaches the transceiver.

Transient Voltage Suppressors

Transient Voltage suppressors are the preferred protection components for CAN bus applications due to their low capacitance, fast response times and high peak power dissipation limits. The low bus capacitance allows these devices to be used at many, if not all, nodes on the network without having to reduce the data rate. The quick response times in the order of a few picoseconds enable these devices to clamp the energy of Very fast transients like ESD and EFT. Lastly, the high peak power ratings enable these devices to handle high energy surge pulses without being damaged.

Application Curve

Typical driver output wave forms from a pulse input signal with different slope control resistances are displayed in Figure 19. The top waveform show the typical differential signal when transitioning from a recessive level to a dominant level on the CAN bus with Rs tied to GND through a zero ohm resistor. The second waveform shows the same signal for the condition with a 100k ohm resistor tied from Rs to ground.

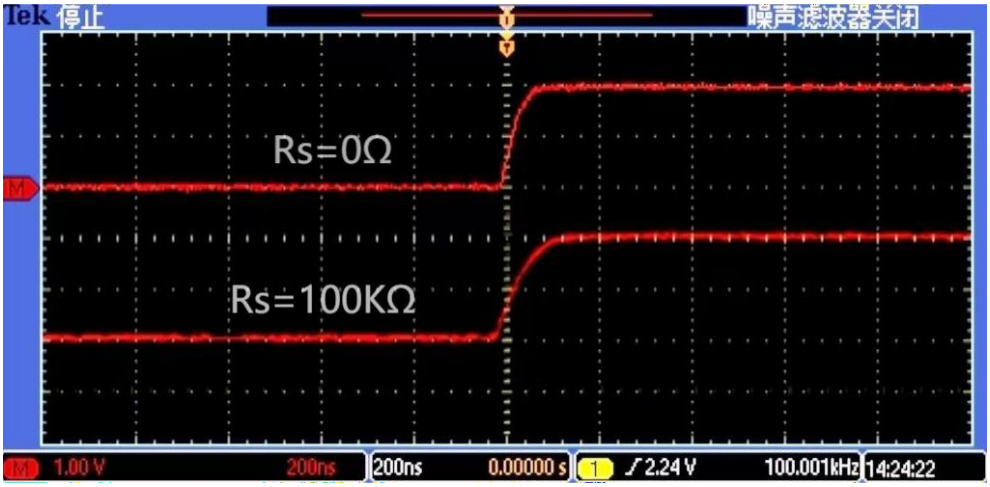


Figure 19. Typical HG65HVD230 200-kbps Output Pulse Wave forms With Slope Control

System Example

Introduction

Many users Value the low power consumption of operating their CAN transceivers from a 3.3V supply. However, some are concerned about the interoperability with 5V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the Voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this Voltage difference and outputs the bus state with a single-ended output signal.

The CAN driver creates the differential Voltage between CANH and CANL in the dominant state. The dominant differential output of the HG65HVD230 is greater than 1.5V and less than 3V across a 60 ohm load as defined by the ISO 11898 standard. These are the same limiting Values for 5V supplied CAN transceivers.

Typically, the bus termination resistors drive the bus back to the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state when less than 500 mV of differential Voltage exists on the bus, and a dominant state when more than 900mV of differential Voltage exists on the bus. The CAN receiver must do this with common-mode input Voltages from -2V to 7Volts per the ISO 11898-2 standard. The HG65HVD230 family receivers meet these same input specifications as 5V supplied receivers.

Common Mode Signal

A common-mode signal is an average Voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Since the bias Voltage of the recessive state of the device is dependent on V_{CC}, any noise present or Variation of V_{CC} will have an effect on this bias Voltage seen by the bus. The HG65HVD230 family has the recessive bias Voltage set higher than $0.5V_{CC}$ to comply with the ISO 11898-2 CAN standard which states that the recessive bias Voltage must be between 2V and 3V. The caveat to this is that the common mode Voltage will drop by a couple hundred milli volts when driving a dominant bit on the bus.

This means that there is a common mode shift between the dominant bit and recessive bit states of the device. While this is not ideal, this small Variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

Interoperability of 3.3V CAN in 5V CAN Systems

The 3.3V supplied HG65HVD230 family of CAN transceivers are fully compatible with 5V CAN transceivers. The differential output Voltage is the same, the recessive common mode output bias is the same, and the receivers have the same input specifications. The only difference is in the dominant common mode output Voltage is lower in 3.3V CAN transceivers than with 5V supplied transceiver (by a few hundred milli volts).

To help ensure the widest interoperability possible, the HG65HVD230 family has successfully passed the internationally recognized GIFT ICT conformance and interoperability testing for CAN transceivers which is shown in . Electrical interoperability does not always assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. This comes only with thorough equipment testing.

Power Supply Recommendations

The HG65HVD230 3.3V CAN transceivers provide the interface between the 3.3V μPs, MCUs and DSPs and the differential bus lines, and are designed to transmit data at signaling rates up to 1Mbps as defined by the ISO 11898 standard.

To ensure reliable operation at all data rates and supply Voltages, the VCC supply pin of each CAN transceiver should be decoupled with a 100nF ceramic capacitor located as close to the VCC and GND pins as possible.

Layout

Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors.Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use VCC and ground planes to provide low inductance. Note: high frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bi-directional diode or Varistor solution) and bus filter capacitors C8 and C9 are shown in .

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.Bus termination: Figure 20 shows split termination. This is where the termination is split into two resistors, R7 and R8, with the center or split tap of the termination connected to ground Via capacitor C7. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues of the bus is not properly terminated on both ends. See the application section for information on power ratings needed for the termination resistor(s).

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}).

Use at least two Vias for VCC and ground connections of bypass capacitors and protection devices to minimize trace and Via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4. Since the internal pull up and pull down biasing of the device is weak for floating pins, an external 1k to 10k ohm pull-up or down resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open drain host processor is used to drive the D pin of the device an external pull-up resistor between 1k and 10k ohms should be used to drive the recessive input state of the device (R1).

Pin 8: is shown assuming the mode pin, Rs, will be used. If the device will only be used in normal mode or slope control mode, R3 is not needed and the pads of C4 could be used for the pull down resistor to GND.

Pin 5 in is shown for the HG65HVD230 devices which have a Vref output Voltage reference. If used, this pin should be tied to the common mode point of the split termination. If this feature is not used, the pin can be left floating.

Layout Example

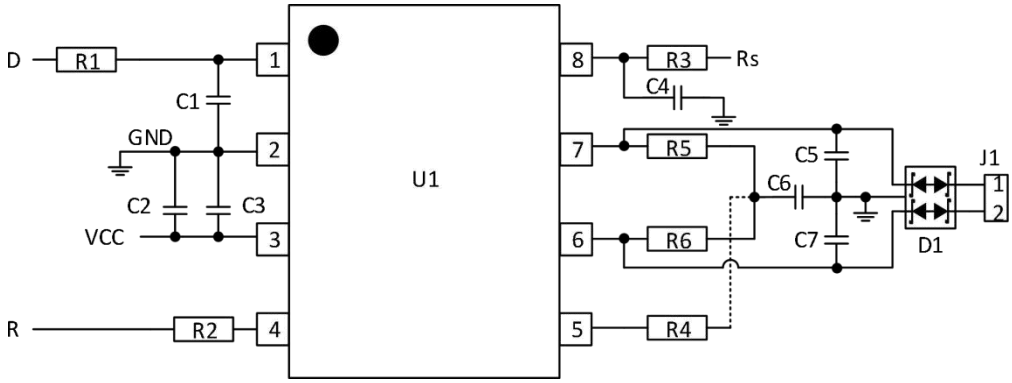
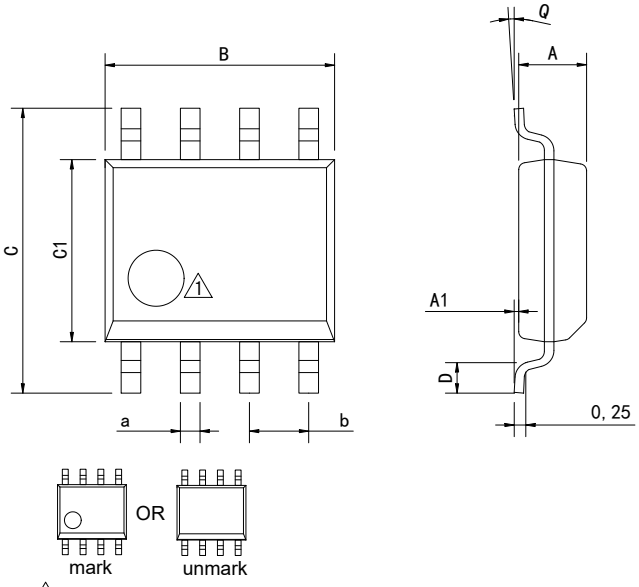


Figure 20. Layout Example Schematic

Physical Dimensions

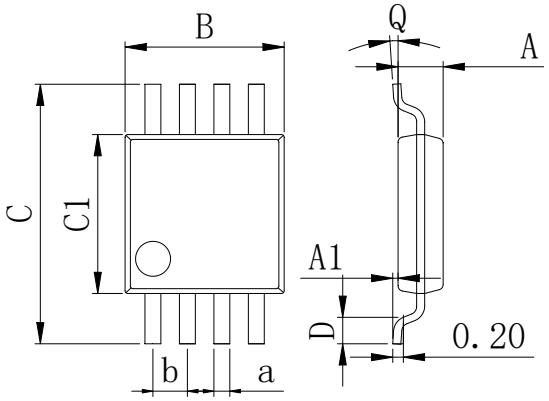
SOP-8 (150mil)



1 Package top mark may be in lower left corner or unmark

Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2017-4	New	1-26
V1.1	2025-1	Document Reformatting	1-23

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