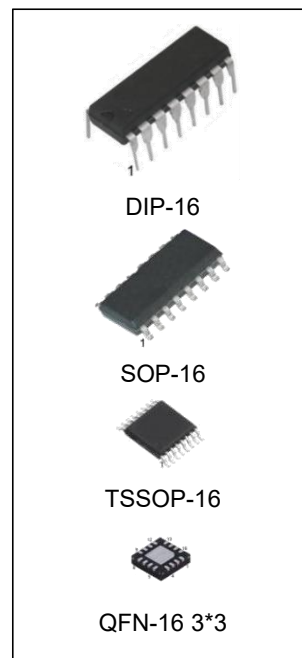


Dual Retriggerable Monostable Multivibrator with Reset

Features

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Specified from -40°C to +85°C
- Packaging information: DIP-16/SOP-16/TSSOP-16/QFN-16 3*3



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC123N	DIP-16	74HC123	TUBE	1000pcs/box
74HC123M/TR	SOP-16	74HC123	REEL	2500pcs/reel
74HC123MT/TR	TSSOP-16	HC123	REEL	2500pcs/reel
74HC123LQ/TR	QFN-16 3*3	HC123	REEL	5000pcs/reel

General Description

The 74HC123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($\overline{nA}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period ($nQ=HIGH$, $\overline{nQ}=LOW$) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{RD}$, which also inhibits the triggering.
3. An internal connection from $n\overline{RD}$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input $n\overline{RD}$.

Block Diagram And Pin Description

Block Diagram

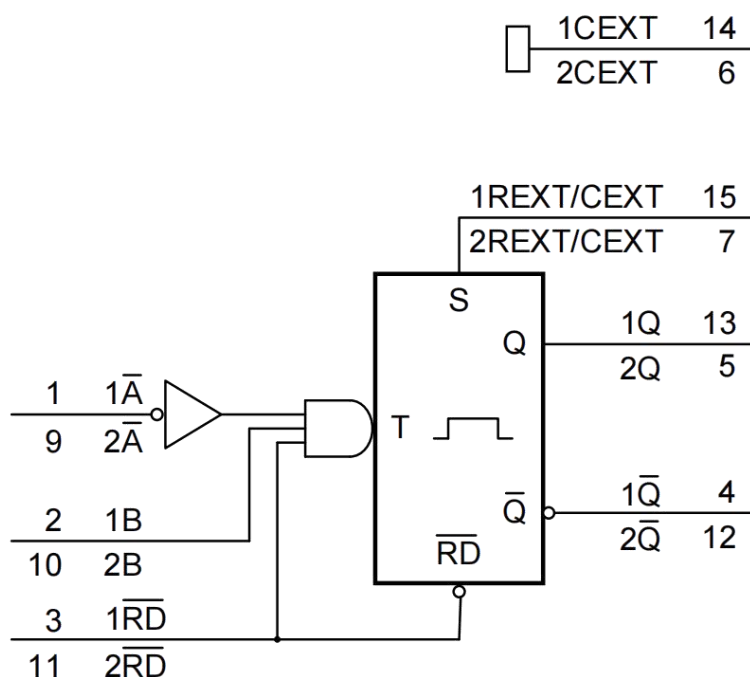


Figure 1. Logic symbol

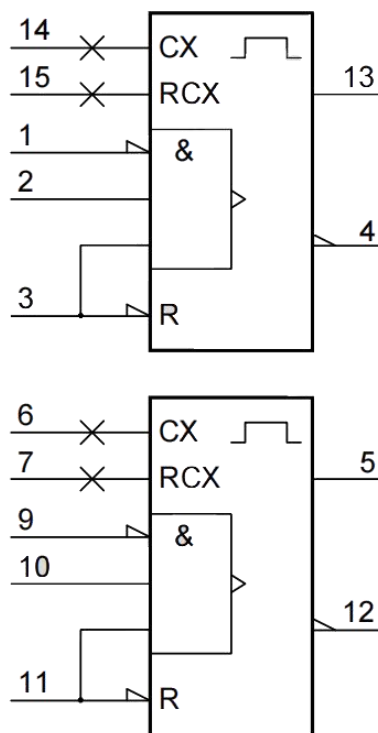


Figure 2. IEC logic symbol

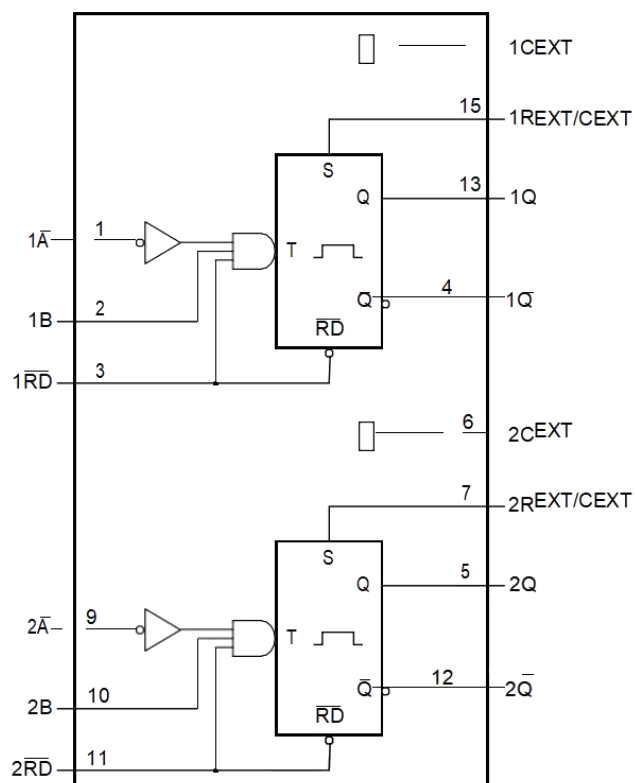


Figure 3. Functional diagram

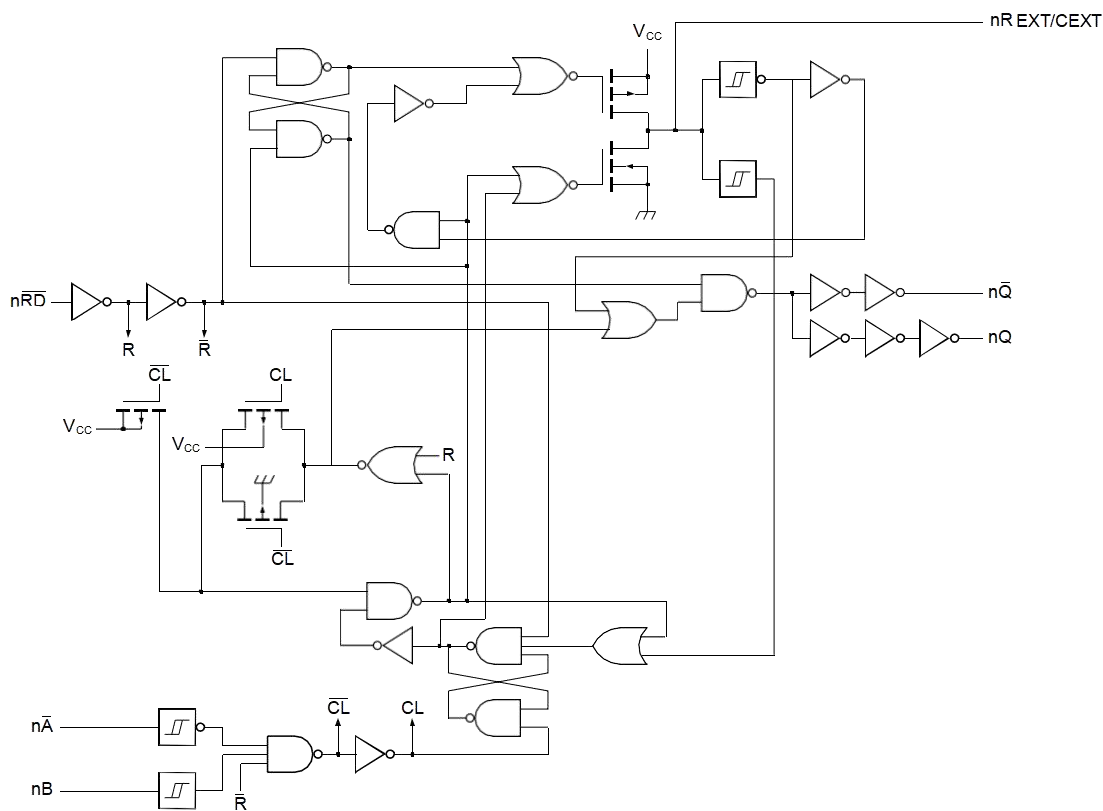
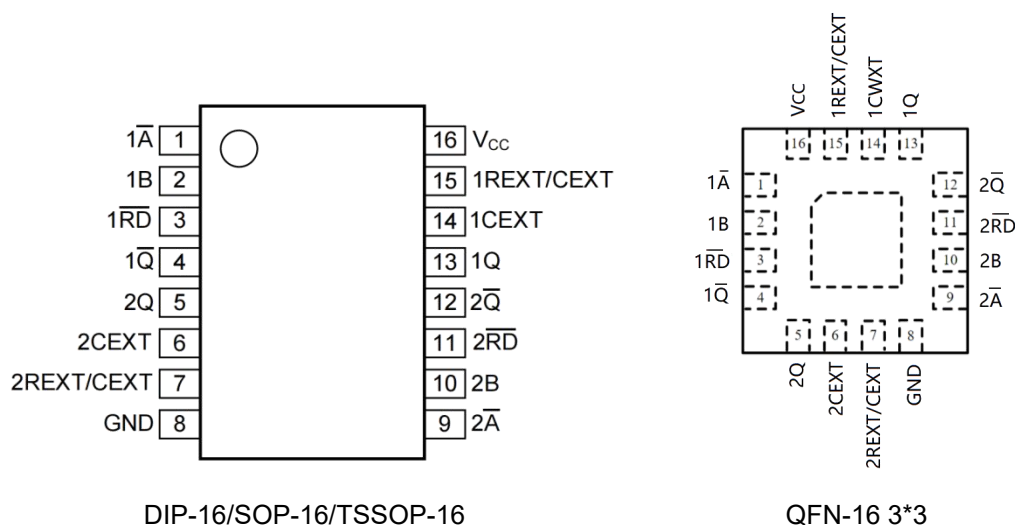


Figure 4. Logic diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	1 $\bar{A}$	negative-edge triggered input 1
2	1B	positive-edge triggered input 1
3	1 $\overline{RD}$	direct reset LOW and positive-edge triggered input 1
4	1 $\bar{Q}$	active LOW output 1
5	2Q	active HIGH output 2
6	2CEXT	external capacitor connection 2
7	2REXT/CEXT	external resistor and capacitor connection 2
8	GND	ground (0V)
9	2 $\bar{A}$	negative-edge triggered input 2
10	2B	positive-edge triggered input 2
11	2 $\overline{RD}$	direct reset LOW and positive-edge triggered input 2
12	2 $\bar{Q}$	active LOW output 2
13	1Q	active HIGH output 1
14	1CEXT	external capacitor connection 1
15	1REXT/CEXT	external resistor and capacitor connection 1
16	V _{CC}	supply voltage

Function Table

Input			Output	
$\overline{nRD}$	$\overline{nA}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

Note:

- 1.H=HIGH voltage level; L=LOW voltage level; X=don't care.
- 2.↑=LOW-to-HIGH transition; ↓=HIGH-to-LOW transition.
- 3.=one HIGH level output pulse; =one LOW level output pulse.
- 4.If the mono stable was triggered before this condition was established, the pulse will continue as programmed.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	±20	mA
output current	I_O	except for pins nREXT/CEXT; $V_O = -0.5V$ to $(V_{CC}+0.5V)$	-	±25	mA
supply current	I_{CC}	-	-	50	mA
ground current	I_{GND}	-	-	-50	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
soldering temperature	T_L	10s	260		°C

Note:5、Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

- 6、For DIP16 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.
- 7、For SOP16 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.
- 8、For (T)SSOP16 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K

Recommended Operating Conditions

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
supply voltage	V _{CC}	-		2.0	5.0	6.0	V
input voltage	V _I	-		0	-	V _{CC}	V
output voltage	V _O	-		0	-	V _{CC}	V
input transition rise and fall rate	Δt/ΔV	nRD ⁺ input	V _{CC} =2.0V	-	-	625	ns/V
			V _{CC} =4.5V	-	1.67	139	ns/V
			V _{CC} =6.0V	-	-	83	ns/V
ambient temperature	T _{amb}	-		-40	-	+85	°C

Electrical Characteristics

DC Characteristics 1 (T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	1.2	-	V
		V _{CC} =4.5V		3.15	2.4	-	V
		V _{CC} =6.0V		4.2	3.2	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	0.8	0.5	V
		V _{CC} =4.5V		-	2.1	1.35	V
		V _{CC} =6.0V		-	2.8	1.8	V
HIGH-level output voltage	V _{OH}	V _I =V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			I _O =-4mA; V _{CC} =4.5V	3.98	4.32	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.48	5.81	-	V
LOW-level output voltage	V _{OL}	V _I =V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			I _O =4mA; V _{CC} =4.5V	-	0.15	0.26	V
			I _O =5.2mA; V _{CC} =6.0V	-	0.16	0.26	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±0.1	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	8.0	uA
input capacitance	C _I	-		-	3.5	-	pF

DC Characteristics 2

(Tamb=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	VCC=2.0V		1.5	-	-	V
		VCC=4.5V		3.15	-	-	V
		VCC=6.0V		4.2	-	-	V
LOW-level input voltage	V _{IL}	VCC=2.0V		-	-	0.5	V
		VCC=4.5V		-	-	1.35	V
		VCC=6.0V		-	-	1.8	V
HIGH-level output voltage	V _{OH}	VI = VIH or VIL	IO=-20uA; VCC=2.0V	1.9	-	-	V
			IO=-20uA; VCC=4.5V	4.4	-	-	V
			IO=-20uA; VCC=6.0V	5.9	-	-	V
			IO=-4mA; VCC=4.5V	3.84	-	-	V
			IO=-5.2mA; VCC=6.0V	5.34	-	-	V
LOW-level output voltage	V _{OL}	VI = VIH or VIL	IO=20uA; VCC=2.0V	-	-	0.1	V
			IO=20uA; VCC=4.5V	-	-	0.1	V
			IO=20uA; VCC=6.0V	-	-	0.1	V
			IO=4mA; VCC=4.5V	-	-	0.33	V
			IO=5.2mA; VCC=6.0V	-	-	0.33	V
input leakage current	I _I	VI=VCC or GND; VCC=6.0V		-	-	±1.0	uA
supply current	I _{CC}	VI=VCC or GND; IO=0A; VCC=6.0V		-	-	80	uA

DC Characteristics 3

(Tamb=-40°C to +105°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	VIH	VCC=2.0V		1.5	-	-	V
		VCC=4.5V		3.15	-	-	V
		VCC=6.0V		4.2	-	-	V
LOW-level input voltage	VIL	VCC=2.0V		-	-	0.5	V
		VCC=4.5V		-	-	1.35	V
		VCC=6.0V		-	-	1.8	V
HIGH-level output voltage	VOH	VI = VIH or VIL	IO=-20uA; VCC=2.0V	1.9	-	-	V
			IO=-20uA; VCC=4.5V	4.4	-	-	V
			IO=-20uA; VCC=6.0V	5.9	-	-	V
			IO=-4mA; VCC=4.5V	3.7	-	-	V
			IO=-5.2mA; VCC=6.0V	5.2	-	-	V
LOW-level output voltage	VOL	VI = VIH or VIL	IO=20uA; VCC=2.0V	-	-	0.1	V
			IO=20uA; VCC=4.5V	-	-	0.1	V
			IO=20uA; VCC=6.0V	-	-	0.1	V
			IO=4mA; VCC=4.5V	-	-	0.4	V
			IO=5.2mA; VCC=6.0V	-	-	0.4	V
input leakage current	II	VI=VCC or GND; VCC=6.0V		-	-	±1.0	uA
supply current	ICC	VI=VCC or GND; IO=0A; VCC=6.0V		-	-	160	uA

AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V); $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	tpd	nRD, nA, nB to nQ or nQ; CEXT=0pF; REXT=5kΩ; see Figure 6[1]	VCC=2.0V	-	83	255	ns
			VCC=4.5V	-	30	51	ns
			VCC=5.0V; CL=15pF	-	26	-	ns
			VCC=6.0V	-	24	43	ns
		nRD(reset) to nQ or nQ; CEXT=0pF; REXT=5kΩ; see Figure 6	VCC=2.0V	-	66	215	ns
			VCC=4.5V	-	25	43	ns
			VCC=5.0V; CL=15pF	-	20	-	ns
			VCC=6.0V	-	19	37	ns
transition time	tt	see Figure 6[1]	VCC=2.0V	-	19	75	ns
			VCC=4.5V	-	7	15	ns
			VCC=6.0V	-	6	13	ns
pulse width	tw	nA LOW; see Figure 7	VCC=2.0V	100	8	-	ns
			VCC=4.5V	20	3	-	ns
			VCC=6.0V	17	2	-	ns
		nB HIGH; see Figure 7	VCC=2.0V	100	17	-	ns
			VCC=4.5V	20	6	-	ns
			VCC=6.0V	17	5	-	ns
		nRD LOW; see Figure 8	VCC=2.0V	100	14	-	ns
			VCC=4.5V	20	5	-	ns
			VCC=6.0V	17	4	-	ns
		nQ HIGH and nQ LOW; VCC=5.0V; see Figure 7, 8[2]	CEXT=100nF; REXT=10kΩ	-	450	-	us
			CEXT=0pF; REXT=5kΩ	-	75	-	ns
		retrigger time	trtrig	nA, nB; CEXT=0pF; REXT=5kΩ; VCC=5.0V; see Figure 7[3][4]		-	110
external timing resistor	REXT	see Figure 7	VCC=2.0V	10	-	1000	kΩ
			VCC=5.0V	2	-	1000	kΩ
external timing capacitor	CEXT	VCC=5.0V; see Figure 9[4]		-	-	-	pF
power dissipation capacitance	CPD	per monostable; VI=GND to VCC[5]		-	54	-	pF

Note:

- tpd is the same as t_{PLH} and t_{PHL} ; tt is the same as t_{THL} and t_{TLH}
- For other REXT and CEXT combinations see Figure 9. If $CEXT > 10\text{nF}$, the next formula is valid.
 $t_w = K \times R_{EXT} \times C_{EXT}$, where;
 t_w = typical output pulse width in ns;
REXT = external resistor in kΩ; CEXT = external capacitor in pF;
K = constant = 0.45 for VCC=5.0V and 0.55 for VCC=2.0V;
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7pF.

3. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT}>10pF, the next formula (at V_{CC}=5.0V) for the setup time of a retrigger pulse is valid:

$$t_{rtrig} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$$
, where:
 t_{rtrig} =retrigger time in ns;
C_{EXT}=external capacitor in pF; R_{EXT}=external resistor in kΩ.
The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is 7pF.
4. When the device is powered-up, initiate the device via a reset pulse, when C_{EXT}<50pF
5. CPD is used to determine the dynamic power dissipation (PD in uW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$$
 where:
f_i=input frequency in MHz; f_o=output frequency in MHz;
D=duty factor in %; C_L=output load capacitance in pF;
V_{CC}=supply voltage in V;
C_{EXT}=timing capacitance in pF;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

AC Characteristics 2

(T_{amb}=-40°C to +85°C, GND=0V; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t _{pd}	n $\overline{RD}$, n $\overline{A}$, nB to nQ or n $\overline{Q}$; C _{EXT} =0pF; R _{EXT} =5kΩ; see Figure 6[1]	V _{CC} =2.0V	-	-	320 ns
			V _{CC} =4.5V	-	-	64 ns
			V _{CC} =6.0V	-	-	54 ns
		n $\overline{RD}$ (reset) to nQ or n $\overline{Q}$; C _{EXT} =0pF; R _{EXT} =5kΩ; see Figure 6	V _{CC} =2.0V	-	-	270 ns
			V _{CC} =4.5V	-	-	54 ns
			V _{CC} =6.0V	-	-	46 ns
transition time	t _t	see Figure 6[1]	V _{CC} =2.0V	-	-	95 ns
			V _{CC} =4.5V	-	-	19 ns
			V _{CC} =6.0V	-	-	16 ns
pulse width	t _w	n $\overline{A}$ LOW; see Figure 7	V _{CC} =2.0V	125	-	- ns
			V _{CC} =4.5V	25	-	- ns
			V _{CC} =6.0V	21	-	- ns
		nB HIGH; see Figure 7	V _{CC} =2.0V	125	-	- ns
			V _{CC} =4.5V	25	-	- ns
			V _{CC} =6.0V	21	-	- ns
		n $\overline{RD}$ LOW; see Figure 8	V _{CC} =2.0V	125	-	- ns
			V _{CC} =4.5V	25	-	- ns
			V _{CC} =6.0V	21	-	- ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

AC Characteristics 3

($T_{amb} = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $GND = 0V$; $C_L = 50pF$, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	n $\overline{RD}$, n $\overline{A}$, nB to nQ or n $\overline{Q}$; C _{EXT} =0pF; R _{EXT} =5k Ω ; see Figure 6[1]	V _{CC} =2.0V	-	-	385	ns
			V _{CC} =4.5V	-	-	77	ns
			V _{CC} =6.0V	-	-	65	ns
		n $\overline{RD}$ (reset) to nQ or n $\overline{Q}$; C _{EXT} =0pF; R _{EXT} =5k Ω ; see Figure 6	V _{CC} =2.0V	-	-	325	ns
			V _{CC} =4.5V	-	-	65	ns
			V _{CC} =6.0V	-	-	55	ns
transition time	t_t	see Figure 6[1]	V _{CC} =2.0V	-	-	110	ns
			V _{CC} =4.5V	-	-	22	ns
			V _{CC} =6.0V	-	-	19	ns
pulse width	t_w	n $\overline{A}$ LOW; see Figure 7	V _{CC} =2.0V	150	-	-	ns
			V _{CC} =4.5V	30	-	-	ns
			V _{CC} =6.0V	26	-	-	ns
		nB HIGH;	V _{CC} =2.0V	150	-	-	ns
		see Figure 7	V _{CC} =4.5V	30	-	-	ns
			V _{CC} =6.0V	26	-	-	ns
		n $\overline{RD}$ LOW; see Figure 8	V _{CC} =2.0V	150	-	-	ns
			V _{CC} =4.5V	30	-	-	ns
			V _{CC} =6.0V	26	-	-	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_t is the same as t_{THL} and t_{TLH} .

Testing Circuit

AC Testing Circuit

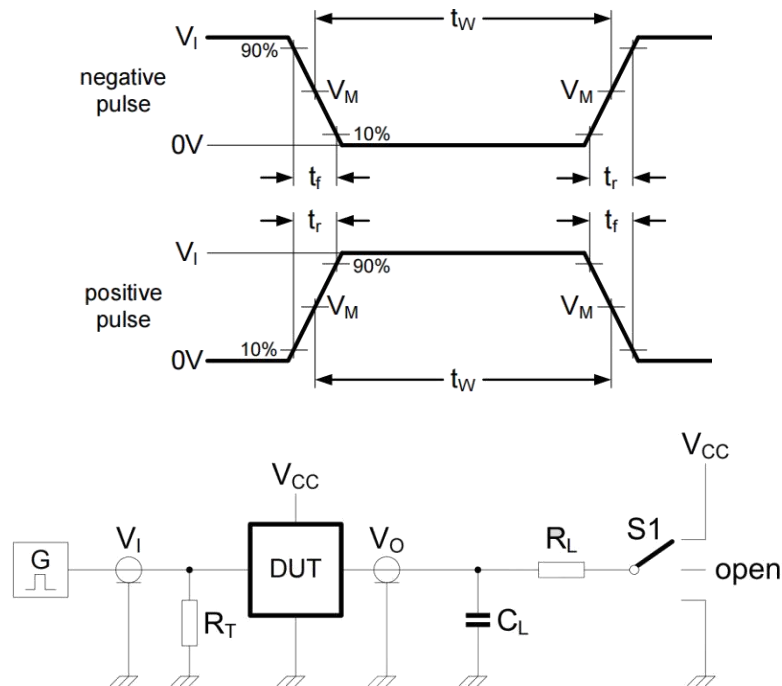


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulsegenerator.

S1=Test selection switch.

AC Testing Waveforms

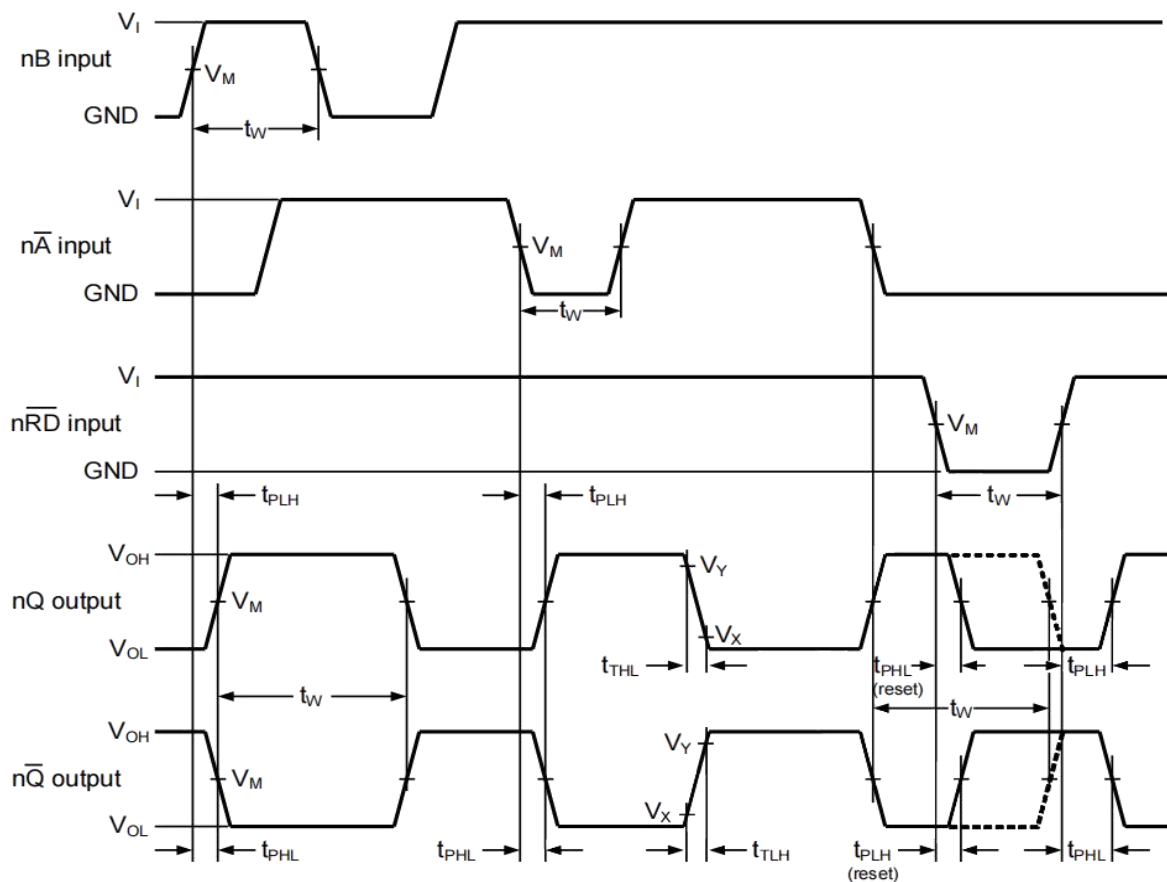


Figure 6. Propagation delays from inputs ($\overline{nA}$, nB , $\overline{nRD}$) to outputs (nQ , $\overline{nQ}$) and output transition times

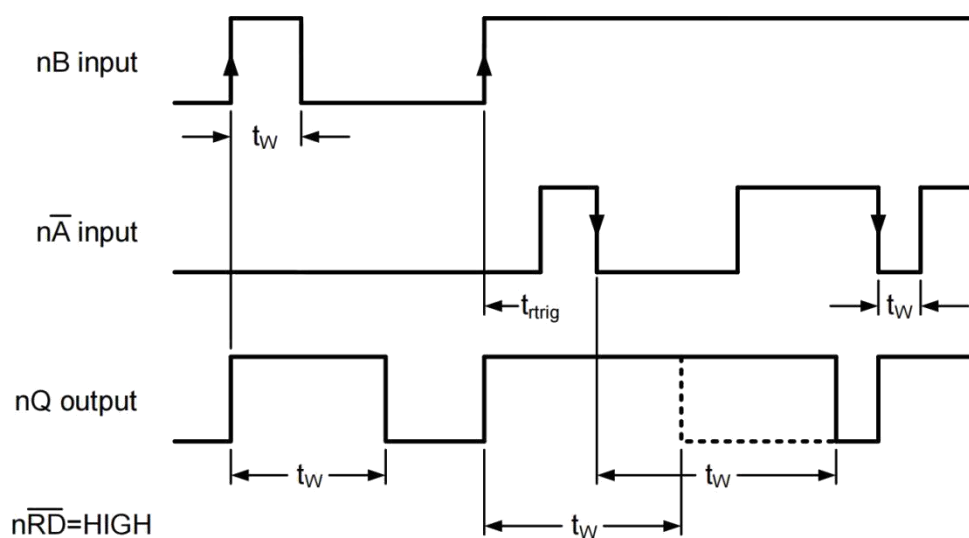


Figure 7. Output pulse control using retrigger pulse

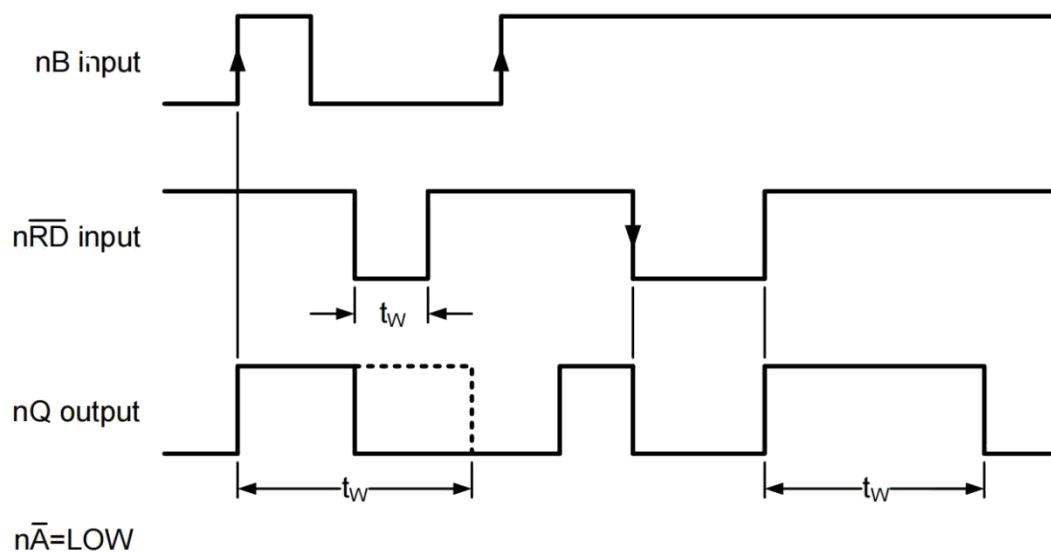
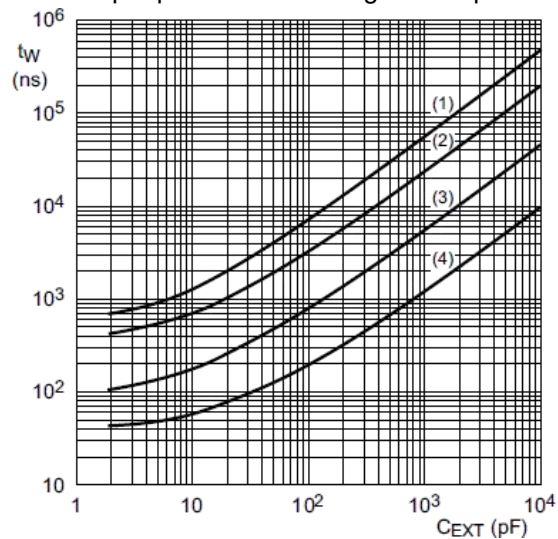


Figure 8. Output pulse control using reset input $\overline{nRD}$



$V_{CC}=5.0V$; $T_{amb}=25^\circ C$.

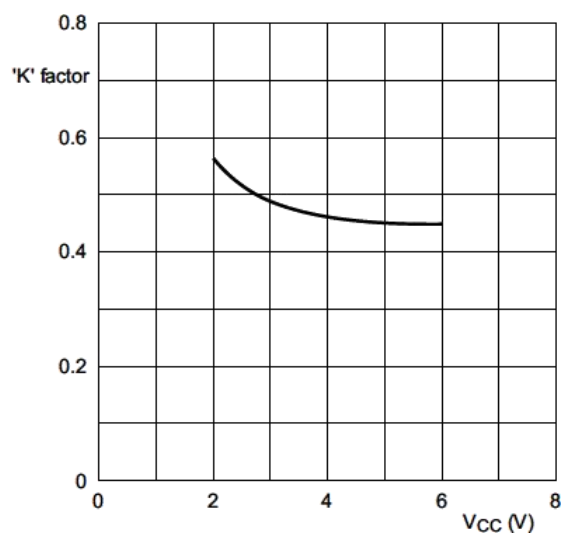
$R_{EXT}=100k\Omega$

$R_{EXT}=50k\Omega$

$R_{EXT}=10k\Omega$

$R_{EXT}=2k\Omega$

Figure 9. Typical output pulse width as a function of the external capacitor value



$C_{EXT}=10nF$; $R_{EXT}=10k\Omega$ to $100k\Omega$. $T_{amb}=25^{\circ}C$.

Figure 10. 74HC123 typical 'K' factor as function of VCC

Measurement Points

Type	Input	Output
	VM	VM
74HC123	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

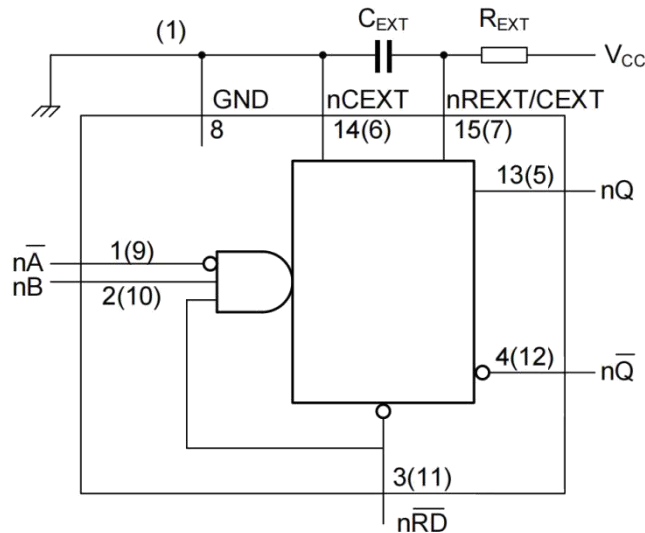
Test data

Type	Input		Load		S1 position
	V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}
74HC123	V_{CC}	6ns	15pF, 50pF	1k Ω	Open

Typical Application Circuit And Application Note

Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT} .



For minimum noise generation it is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

Figure 11. Timing component connections

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT} . This output pulse can be eliminated using the circuit shown in Figure 12.

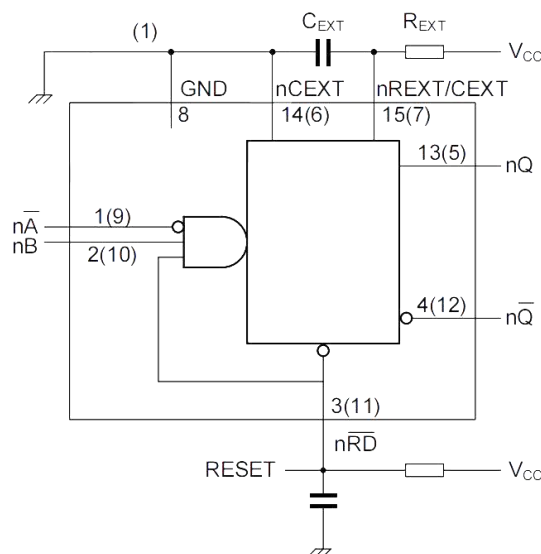


Figure 12. Power-up output pulse elimination circuit

Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 13.

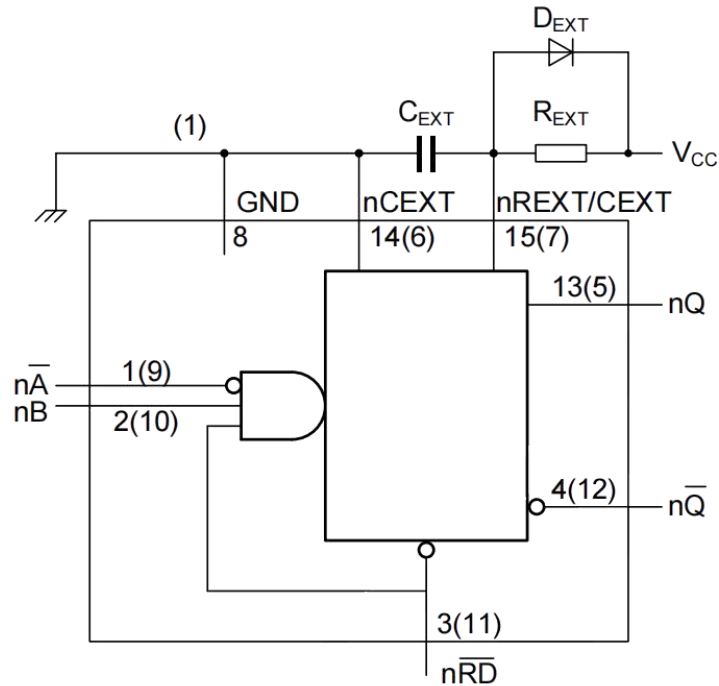
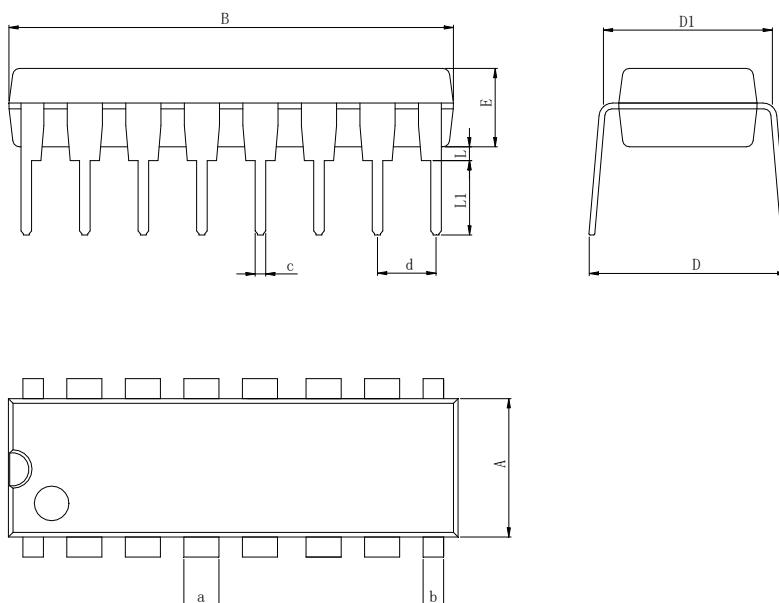


Figure 13. Power-down protection circuit

Physical Dimensions

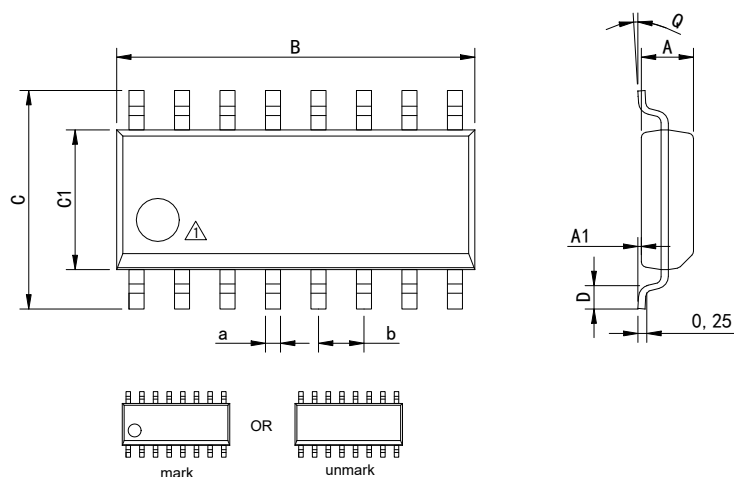
DIP-16



Dimensions In Millimeters(DIP-16)

Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP-16



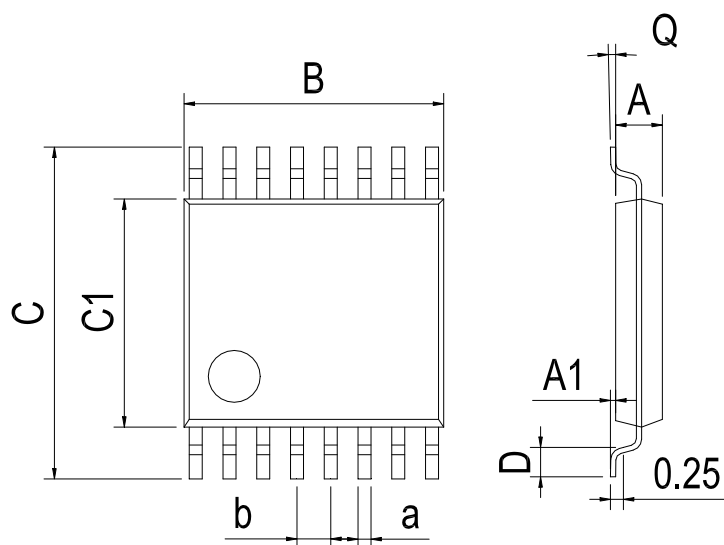
△ Package top mark may be in lower left corner or unmark

Dimensions In Millimeters(SOP-16)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

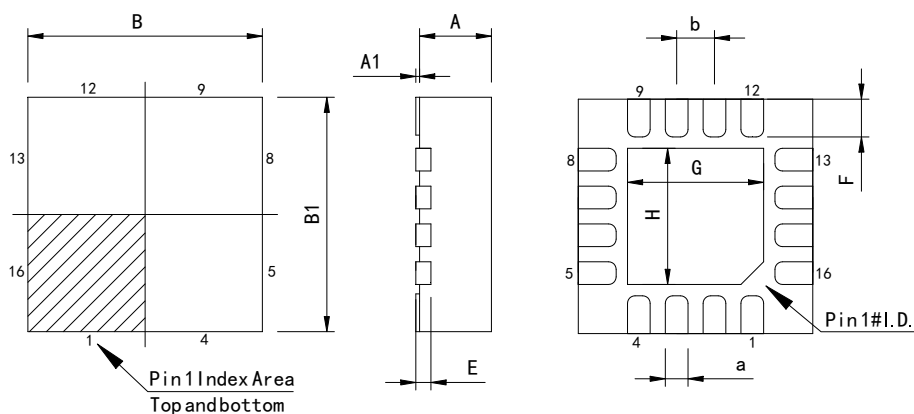
TSSOP-16



Dimensions In Millimeters(TSSOP-16)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

QFN-16 3*3



Dimensions In Millimeters(QFN-16 3*3)

Symbol:	A	A1	B	B1	E	F	G	H	a	b
Min:	0.85	0	2.90	2.90	0.15	0.25	1.45	1.45	0.18	0.50TYP
Max:	0.95	0.05	3.10	3.10	0.25	0.45	1.85	1.85	0.30	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V.10	2014-3	New	1-21
V1.1	2023-9	Modify the package dimension diagram TSSOP-16 、 Update encapsulation type、 Updated DIP-16 dimension	1、 18、 19
V1.2	2024-11	Add the QFN-16 package device、 Update Lead Temperature	1、 5
V1.3	2025-1	Update working temperature	6
V1.4	2025-9	Update important statements、 Update sop-16 Dimension drawing	18、 21
V1.5	2026-9	Update QFN-16 Dimension drawing	19

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