SA23003A

High-Efficiency, 5.5V, 3A, Single Synchronous Buck Converter

General Description

The SA23003A high-efficiency synchronous Buck converter can deliver 3A output current over an input voltage range from 2.8V to 5.5V. It uses built-in power MOSFETs to supply a resistor-configurable output voltage between 0.6V and V_{IN}. The fixed 2.35MHz switching frequency allows for small external inductor and capacitor values.

The SA23003A is available in a DFN1.4mm× 1.8mm-6 package.

Key Features

- 2.8V to 5.5V Input Voltage Range
- Up to 3A Output Current
- External Adjustable Voltage with ±1% Reference Accuracy
- 1μA Shutdown Current (Typical)
- Fixed 2.35MHz Switching Frequency Minimizes Required External Components
- Fixed Frequency PWM and PFM Operating Modes
- 100% Duty-Cycle Capable
- Cycle-by-Cycle Current-Limit Protection
- Hiccup-Mode Short-Circuit Protection
- Thermal Shutdown
- Package: DFN1.4mm×1.8mm-6
- Automotive AEC-Q100 Grade 1 Certified

Applications

- Automotive Infotainment and Cluster
- ADAS
- Automotive Display
- Other Electronic Equipment

Typical Application

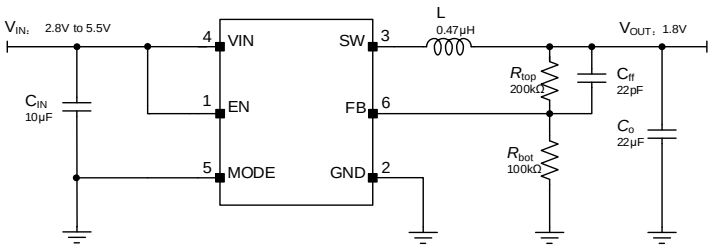


Figure 1. Schematic Diagram

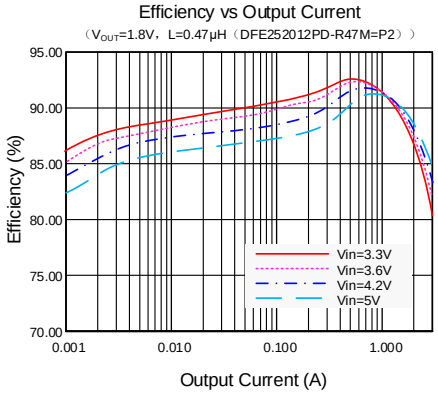


Figure 2. Efficiency vs Output Current

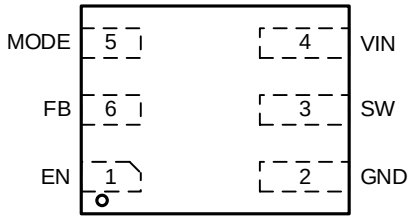
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Ordering Information

Ordering Part Number	Package Type	Top Mark
SA23003ATWD	DFN1.4×1.8-6 RoHS Compliant and Halogen Free	8r*xyz*

x=year code, y=week code, z= lot number code

Pinout (top view)



(DFN1.4×1.8-6)

Pin Description

Pin No	Pin Name	Pin Description
1	EN	Device enable pin, logic-high enable. There is no pulldown resistor inside. Do not leave floating.
2	GND	Ground
3	SW	Switching node
4	VIN	Power supply.
5	MODE	PFM/FCCM mode selection. When the MODE pin is high, the device is forced to operate in FCCM. When the pin is low, the device enters PFM in light-load operation. There is no pulldown resistor inside. Do not leave floating.
6	FB	Output voltage feedback pin. The output voltage reference is 0.6V.

Block Diagram

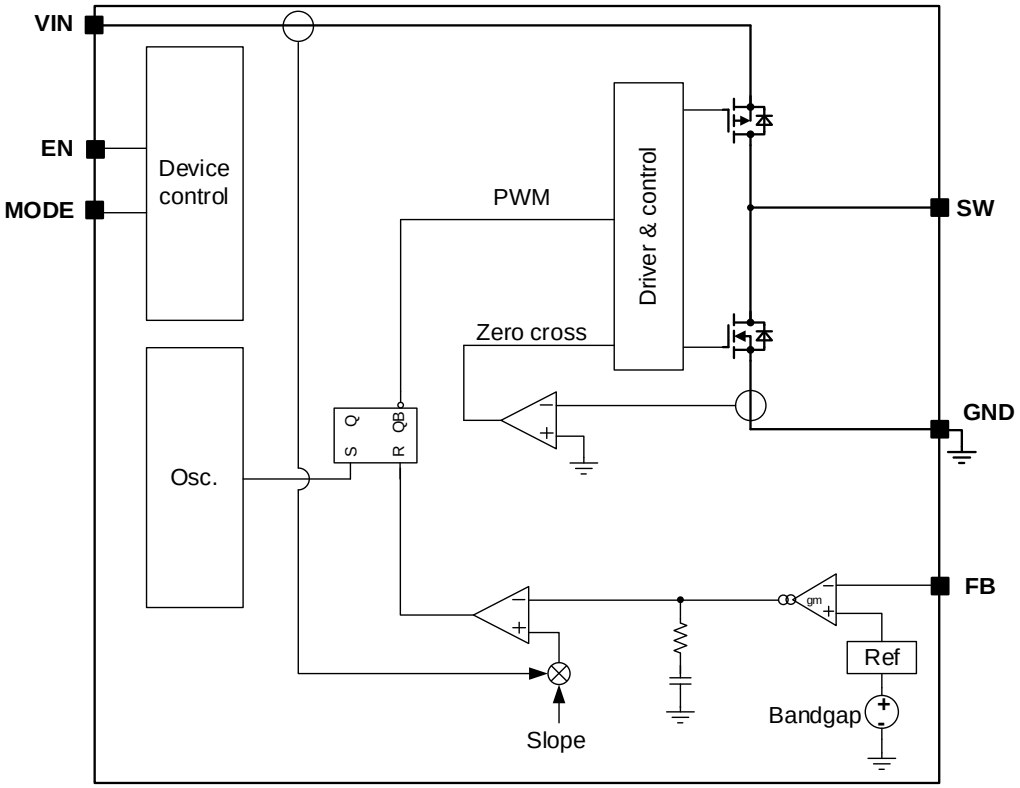


Figure 3. Functional Block Diagram

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Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	6.5	V
FB, EN, MODE	-0.3	V_{IN} + 0.3	
Dynamic SW to GND Voltage in 20ns Duration	-3	V_{IN} + 1.5	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Model)		2000	V
CDM (Charge Device Model) All Pins		500	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	125	°C/W
θ_{JB} Junction-to-Board Thermal Resistance	69	
θ_{JC_top} Junction-to-Case Top Thermal Resistance	29	
Ψ_{JT} Junction-to-Top Characterization Parameter	4	
Parameter (Note 3)	**Typ**	**Unit**
θ_{JA} Junction-to-Ambient Thermal Resistance	60	°C/W
θ_{JB} Junction-to-Board Thermal Resistance	31	
θ_{JC_top} Junction-to-Case Top Thermal Resistance	29	
Ψ_{JT} Junction-to-Top Characterization Parameter	3	

Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
V_{IN}	2.8	5.5	V
Ambient Temperature	-40	125	°C
Junction Temperature	-40	150	°C

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Electrical Characteristics

(2.8V ≤ V_{IN} ≤ 5.5V, -40°C ≤ T_J ≤ 125°C. typical values at V_{IN} = 5V and T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VIN	UVLO Rising Threshold	V_{UVLO_R}		2.6	2.7	2.8	V
	UVLO Falling Threshold	V_{UVLO_F}		2.45	2.55	2.65	
	Shutdown Current A	I_{SDA}	V_{EN} = 0V, T_J = 25°C		1	2	μA
	Shutdown Current B	I_{SDB}	V_{EN} = 0V, T_J = 125°C		6	12	
	Quiescent Current	I_Q	V_{MODE} = logic low, V_{EN} = logic high, no load		22	40	
EN	EN Logic 1 Threshold	V_{EN_H}		1.2			V
	EN Logic 0 Threshold	V_{EN_L}				0.4	
Power Stage	Switching Frequency	f_{sw}		2	2.35	2.7	MHz
	HS FET $R_{DS(ON)}$	$R_{DS(ON)_HS}$	V_{IN} = 5V		83		mΩ
	LS FET $R_{DS(ON)}$	$R_{DS(ON)_LS}$	V_{IN} = 5V		43		
	Discharge Resistor	$R_{DISCHARGE}$			200		Ω
Feedback and Soft-Start	Output Feedback Reference	V_{REF}		594	600	606	mV
	Soft-Start Time	t_{ss}		0.1	0.25	0.5	ms
Mode	Input Bias Current	I_{IN}			0.01	1	μA
	Logic 1 Threshold	V_{MODE_H}		1.2			V
	Logic 0 Threshold	V_{MODE_L}				0.4	
Thermal Shutdown	Thermal Shutdown Threshold	T_{SD}		150	165	180	°C
	Thermal Shutdown Hysteresis	T_{SDHYS}		10	15	20	
Current Limit	Peak Current Limit	I_{LIMIT_P}		4.0	5.0	6.0	A
	Valley Foldback Current Limit	I_{LIMIT_V}		2.3	3.5	4.5	
	Negative Valley Current Limit	I_{LIMIT_N}		1	1.6	2.2	
Short-Circuit Protection	Short-Circuit Threshold	V_{SCP}	V_{FB} as percent of V_{REF}	20	30	40	$\%V_{REF}$
	Short-Circuit Response Time	t_{SCP}	From V_{FB} < V_{SCP} to stop switching. No delay on the other side, V_{IN} = 5V.	5	10	20	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The parameters are measured in the natural convection at T_A = 25°C. Device mounted on 4-layer test board of JESD51-7 thermal measurement standard.

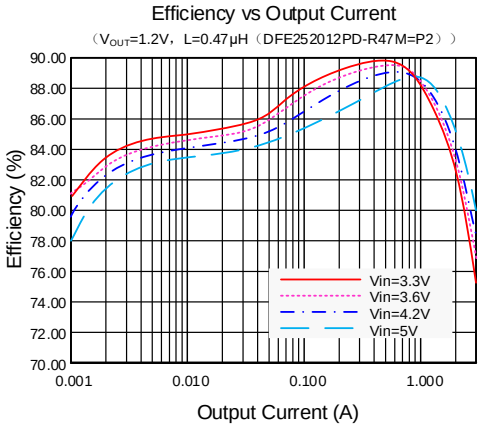
Note 3: The parameters are measured in the natural convection at T_A = 25°C. Device mounted on Silergy 4-layer, 6” x 6” FR-4 substrate PCB, 1oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

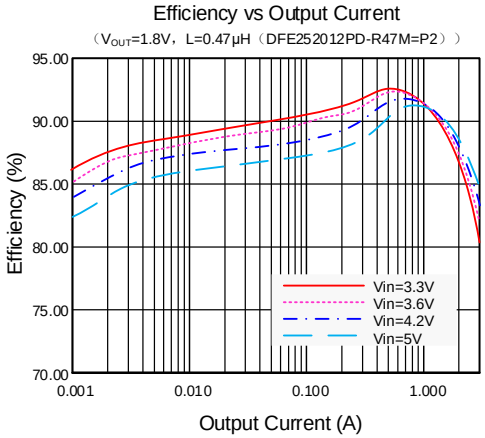
Note 4: The device is not guaranteed to electrical parameter outside its test conditions of EC Table.

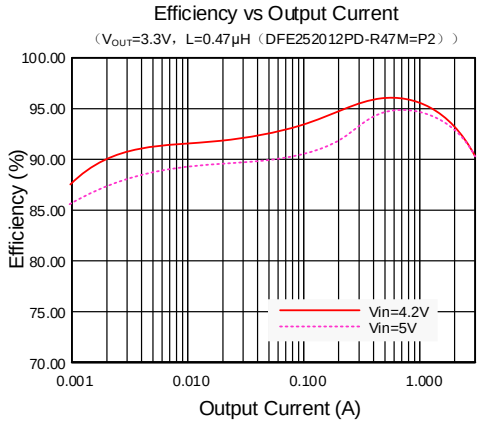
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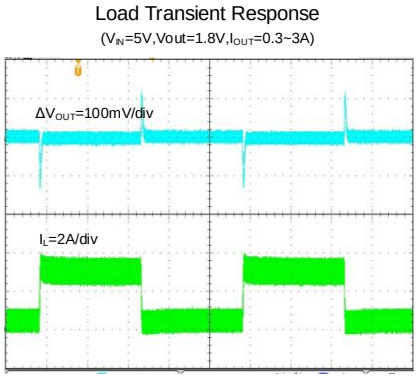
Typical Performance Characteristics

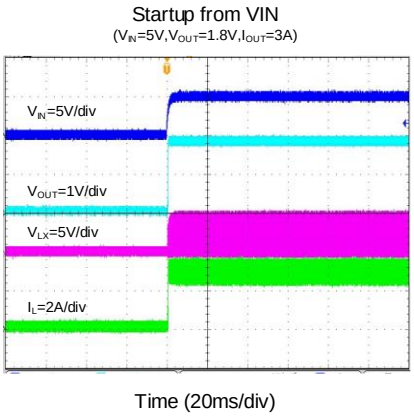
(T_A = 25°C, V_{IN} = 5V, V_{OUT} =1.8 V, L = 0.47µH, C_{OUT} = 22µF, unless otherwise noted)

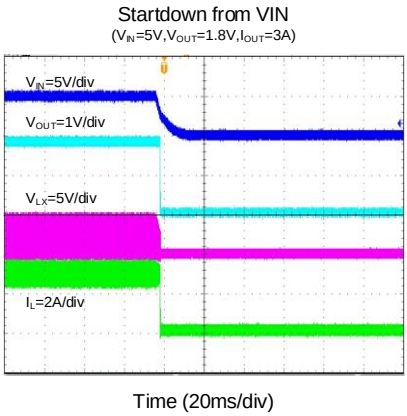








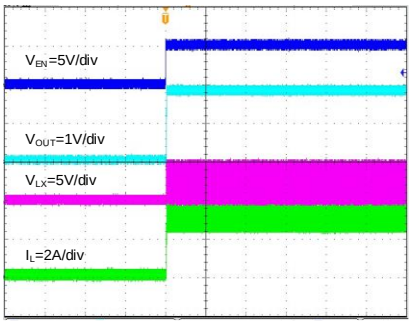




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Startup from VEN

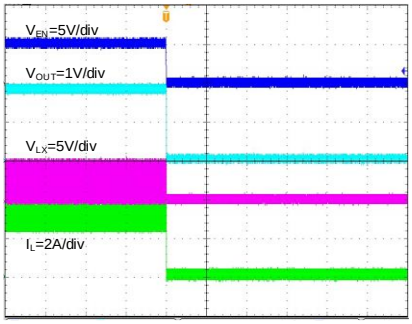
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=3A)



Time (10ms/div)

Startdown from VEN

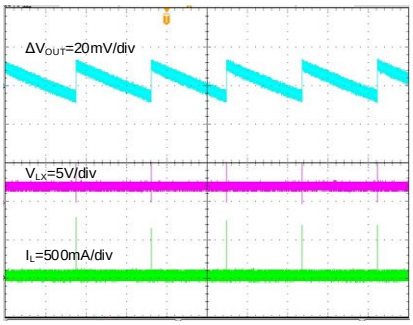
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=3A)



Time (10ms/div)

Output Ripple

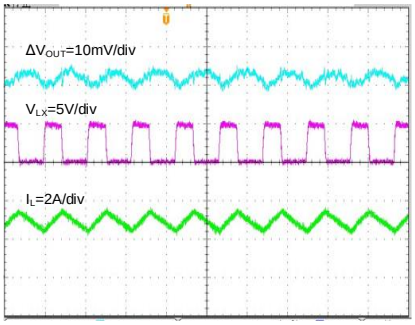
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=0A)



Time (40ms/div)

Output Ripple

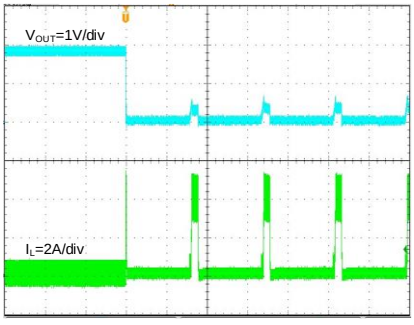
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=3A)



Time (400ns/div)

Output Short Circuit

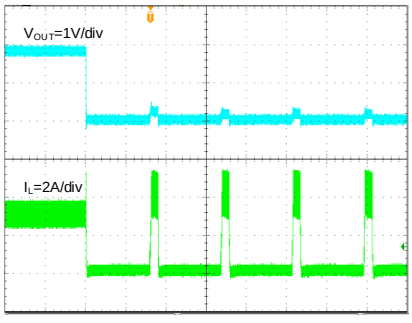
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=0A)



Time (2ms/div)

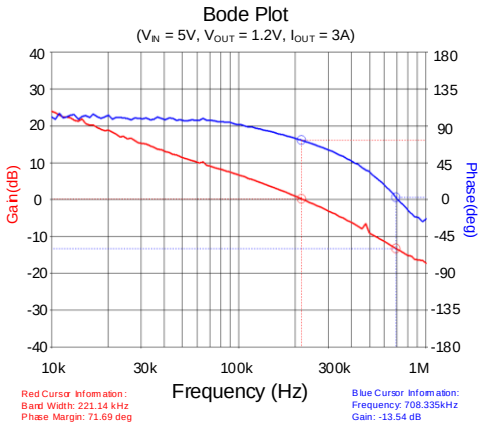
Output Short Circuit

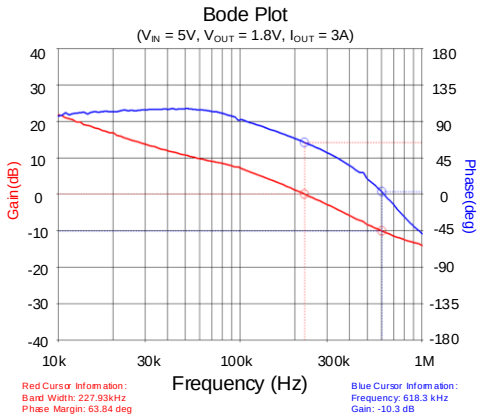
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=3A)

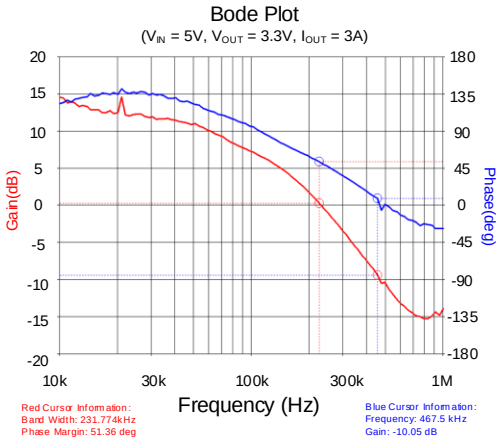


Time (2ms/div)

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Applications Information

The SA23003A high-efficiency synchronous Buck converter can deliver 3A output current over an input voltage range from 2.8V to 5.5V. It uses built-in power MOSFETs to supply a resistor-configurable output voltage between 0.6V and V_{IN}. The fixed 2.35MHz switching frequency allows for small external inductor and capacitor values.

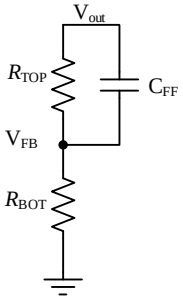
The selection process for the feedback resistors (R_{TOP} and R_{BOT}), output inductor L, input capacitor C_{IN}, and output capacitor C_{OUT} is described in the following sections.

Feedback Resistor Dividers R_{TOP} and R_{BOT}

Choose R_{TOP} and R_{BOT} to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R_{TOP} and R_{BOT} to minimize power consumption under light loads (refer to the Typical Application section for recommended feedback Resistor values).

The output voltage can be configured using the following equation:

$$V_{OUT} = (1 + \frac{R_{TOP}}{R_{BOT}}) \times V_{FB}$$



where V_{FB} has a value of 0.6V (typ).

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_s \times I_{OUT,MAX} \times 0.4}$$

Where f_S is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SA23003A has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT_MIN} > I_{OUT_MAX} + \frac{V_{OUT} \times (1\text{-}V_{OUT} / V_{IN_MAX})}{2 f_S \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency. Choose an inductor with smaller DCR to achieve a good overall efficiency.

Input Capacitor C_{IN}

The ripple current through the input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT_MAX} \times \sqrt{D \times (1 - D)}$$

The capacitance of the input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta V_{IN} \times F_s \times \eta \times V_{IN}^2}$$

where ΔV_{IN} is the maximum allowed input voltage ripple.

For reliable operation, place a typical X7R or better grade ceramic capacitor close to the VIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and the VIN/GND pins. A 10μF (0603) low-ESR ceramic capacitor is recommended in this case.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. It is recommended to use an X7R or better grade ceramic capacitor (refer to the Typical Application section for recommended capacitance values).

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Operation

Current Mode Control

The SA23003A uses a fixed frequency peak current mode control architecture. The peak current through the HS FET is added to the slope compensation ramp and fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier is fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch by using the switch logic block. This forces a high signal on the gate of HS FET and the HS FET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the HS FET turns off.

ON-OFF Sequence

When the device is enabled and the input voltage is above the UVLO threshold, the internal reference is activated and the analog circuits are settled. Afterwards, the soft-start is activated and the output voltage is ramped up.

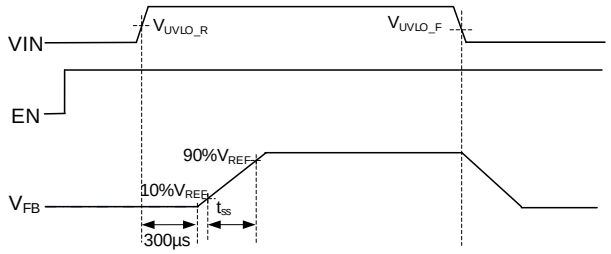


Figure 4. VIN ON/OFF Sequence

The device is enabled by setting the EN pin high. Once the EN pin is set high, the output voltage ramps up from 10% to 90% of nominal value with t_{ss} of 250µs (typical).

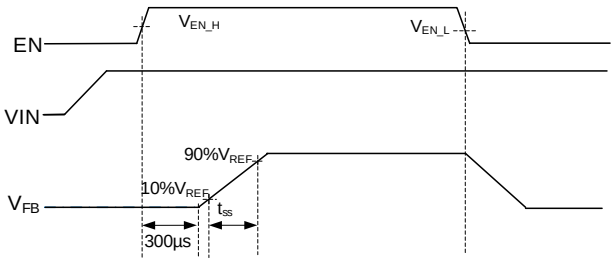


Figure 5. EN ON/OFF Sequence

Adaptive Frequency Fold-back at Min Toff Operation (Dropout)

The SA23003A provides adaptive frequency reduction during large-duty-cycle operation when minimum T_{OFF} is reached. Unlike conventional peak-current control, this approach ensures the stability of the circuit during dropout operation. When V_{IN} drops below the configured V_{OUT} voltage, the SA23003A will enter dropout mode, wherein its high-side FET will always be ON. Normal operation resumes when V_{IN} exceeds the target V_{OUT} level.

Light Load Operation

The SA23003A supports automatic PWM/PFM operation when the external MODE pin is set low. The converter operates in fixed-frequency PWM mode at medium to heavy loads, and in PFM mode during light loads, maintaining high efficiency over the entire load-current range.

Protection Features

The SA23003A provides integrated output short-circuit protection, output overcurrent protection, and thermal shutdown protection.

Table 1. Protection Features

Protection	Threshold	Deglitch Time	Operation
Thermal Shutdown	Rising: 165°C Falling: 150°C	-	Shutdown when temperature>165°C Restart when temperature<150°C
Cycle by Cycle Current Limit	5A		Peak limit = valley limit; Valley Foldback to 70% after 3 cycles.
Output SCP	V_{FB}<30%V_{REF}	10µs	Hiccup time 3.5ms.

Current Limit

The SA23003A features cycle-by-cycle current-limit protections. When the current-sense amplifier detects a voltage that exceeds the peak current limit, the power switch is turned off for the remainder of the cycle. See Figure 6.

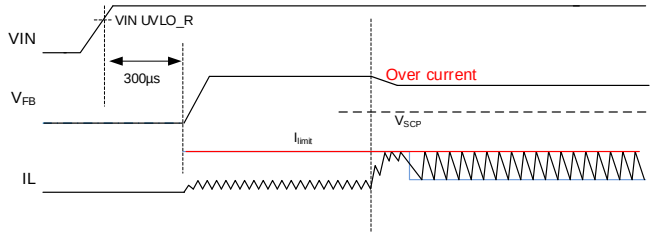


Figure 6. Cycle-by-Cycle Current Limit

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Short Circuit Protection

The SA23003A will attempt to protect the power MOSFET from damage in the event of a short circuit at the output. After the initial short-circuit blanking time t_{scp}, when the output voltage falls below the short-circuit threshold, the device will be turned off for the hiccup time and then go through the soft-start time t_{ss}. See Figure 7.

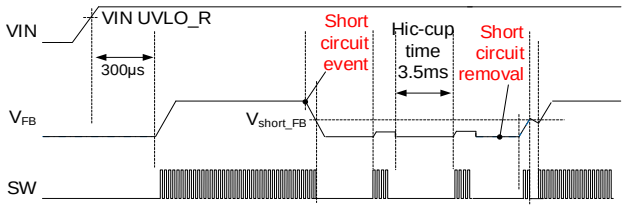


Figure 7. Short Circuit Protection

Overtemperature Protection

The SA23003A enters thermal shutdown when the junction temperature exceeds 165°C (typical). In this mode, the high-side switch and low-side switch are turned off. When the junction temperature falls below 150°C (typical), the Buck will automatically be re-enabled. See Figure 8.

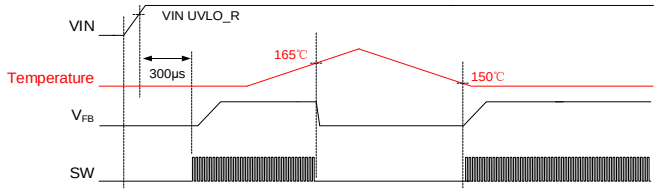
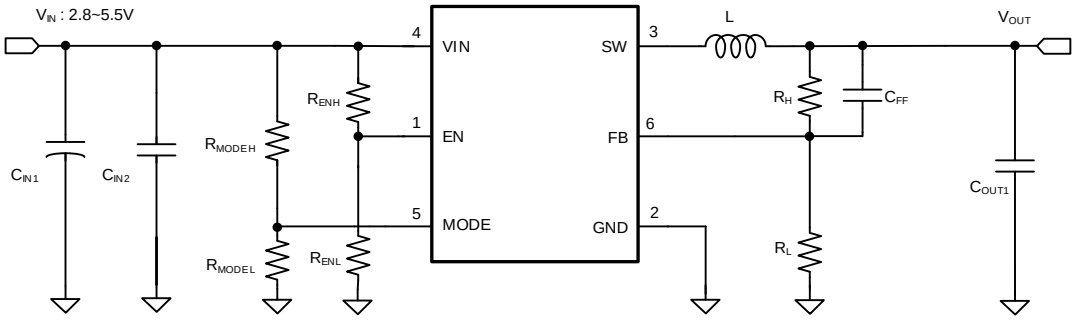


Figure 8. Overtemperature Protection

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Application Schematic (V_{OUT}=1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V Electrolytic Capacitor		
C_{IN2}	10μF/6.3V/X7T, 0603	GCM188D70J106ME36D	muRata
C_{OUT1}	22μF/6.3V/X7T, 0603	GRM188D70J226ME01D	muRata
L	0.47μH/inductor, 5.2A	DFE252012PD-R47M=P2	muRata
C_{FF}	22pF/50V/C0G, 0603		
R_H	200kΩ, 1%, 0603		
R_L	100kΩ, 1%, 0603		
R_{MODEH}	10kΩ, 1%, 0603		
R_{MODEL}	1MΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommend Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
0.6	0	NC	NC	0.47μH/DFE252012PD-R47M=P2	22μF*2/6.3V, 0603, X7T
0.85	49.9	120	47	0.47μH/DFE252012PD-R47M=P2	22μF/6.3V, 0603, X7T
1.2	100	100	22	0.47μH/DFE252012PD-R47M=P2	22μF/6.3V, 0603, X7T
1.8	200	100	22	0.47μH/DFE252012PD-R47M=P2	22μF/6.3V, 0603, X7T
3.3	270	60.4	47	0.47μH/DFE252012PD-R47M=P2	22μF/6.3V, 0603, X7T

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Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- Maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. Using a separate layer as a ground plane is highly recommended.
- To avoid EMI, minimize the PCB copper area associated with the SW pin.
- To avoid potential noise, ensure that the feedback components R_H and R_L, and the trace connecting to the FB pin, are **not** adjacent to the SW net on the PCB layout.

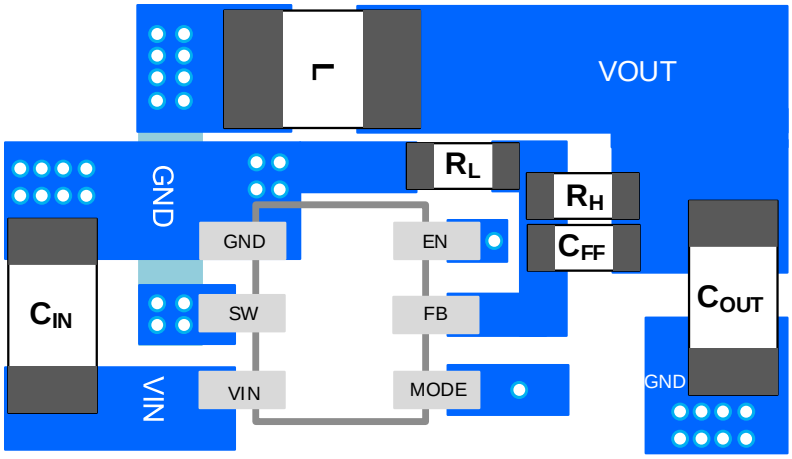
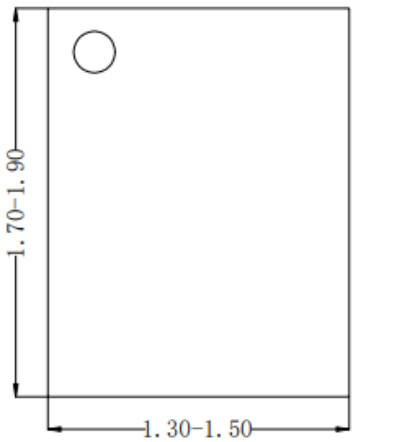


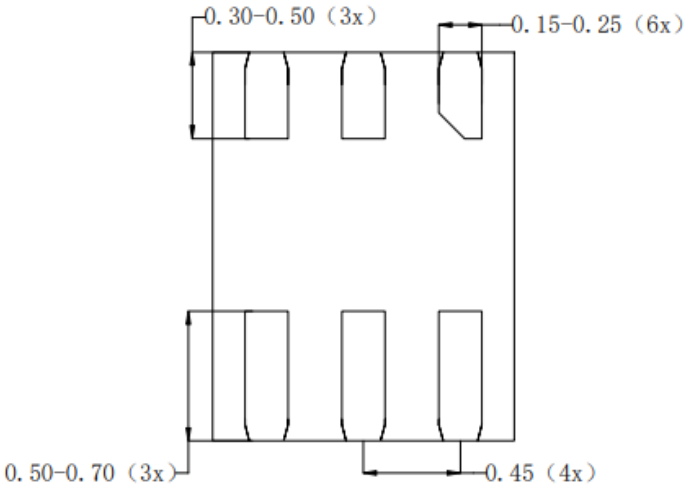
Figure 9. Layout Design Suggestion

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DFN1.4×1.8-6 Package Outline Drawing



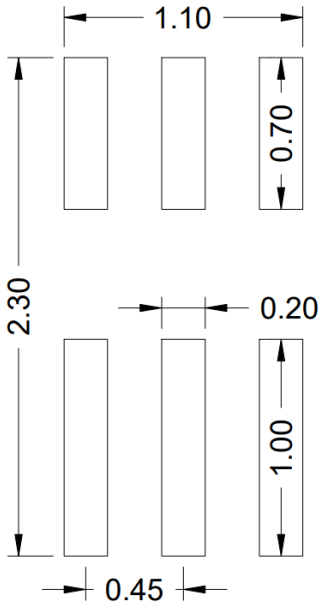
Top View



Bottom View



Side View



Recommended PCB Layout (Reference only)

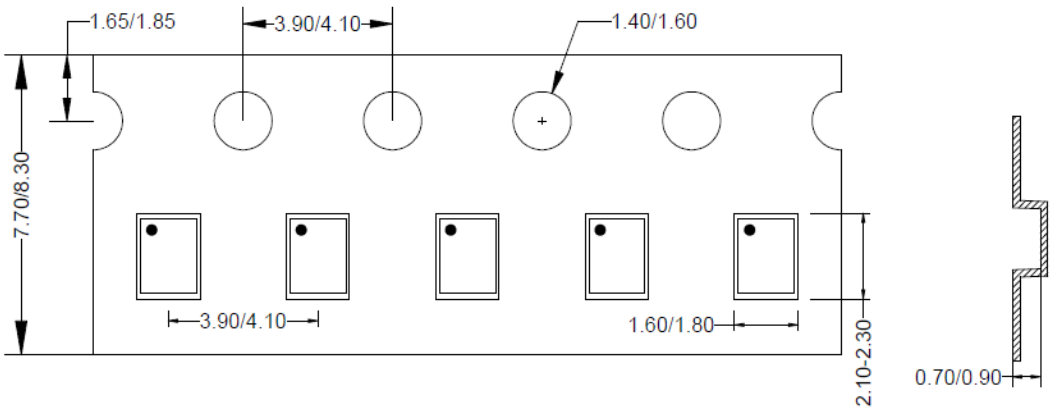
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

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Taping & Reel Specification

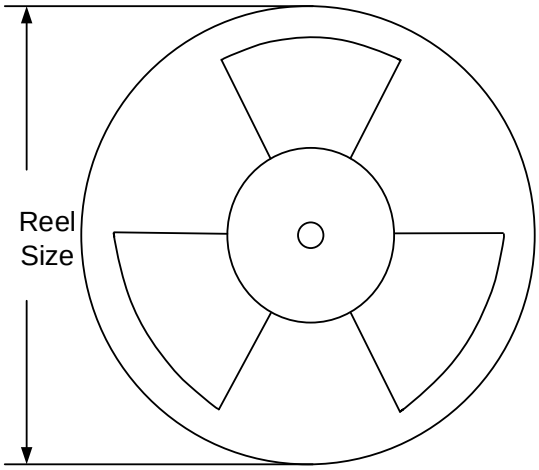
Taping Orientation

DFN1.4×1.8



Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.4×1.8	8	4	7"	400	400	3000

Others: NA

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages Changed
Dec. 29, 2023	Revision 1.0	Initial Release.	-
Feb. 27, 2024	Revision 1.0A	Add Recommended PCB Layout.	Page 13
		Update description of reference accuracy in Key Feature.	Page 1
		Delete description of Hiccup-Mode Overcurrent Protection in Key Feature.	
Jun. 24, 2024	Revision 1.0B	Reference voltage accuracy increased from ±1.5% to ±1%.	Page 1 and 4

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