



MK eMMC Product Family

eMMC 5.1 Specification Compatibility

Product List

MKEMJ032GM1M-C

32GB eMMC

<http://www.mkfounder.com>



Revision History

Version	Date	Description
Rev 1.0	2025/02/20	Released
Rev 1.1	2025/07/18	Modify CID value

Notice :

The datasheet is prepared and approved by MK Founder semiconductor co., LTD.

MK Founder reserves the right to change products or specifications without notice.

©2021 MK Founder semiconductor co., LTD. All rights reserved.



Table Of Contents

1 General Description.....	- 4 -
2 Product List	- 4 -
3 Key Features.....	- 4 -
4 Functional Block Diagram	- 6 -
5 eMMC Device and System	- 7 -
5.1 eMMC System Overview	- 7 -
5.2 eMMC Device Overview	- 7 -
6 eMMC 5.1 Feature Overview.....	- 9 -
6.1 Boot	- 9 -
6.2 Sleep (CMD5).....	- 9 -
6.3 Bus Modes.....	- 9 -
6.4 Reliable Write	- 11 -
6.5 Secure Erase.....	- 11 -
6.6 Secure Trim	- 11 -
6.7 Trim	- 12 -
6.8 Partition Management.....	- 12 -
6.9 High priority interrupt (HPI)	- 13 -
6.10 Background Operations	- 13 -
6.11 H/W Reset	- 13 -
6.12 Packed Commands	- 13 -
6.13 Cache	- 14 -
6.14 Discard	- 14 -
6.15 Sanitize.....	- 14 -
6.16 Dynamic Capacity Management	- 15 -
7 Product Specifications.....	- 15 -
7.1 Power Consumption	- 15 -
7.2 Performance	- 16 -
7.3 Operating Conditions	- 16 -
7.4 Physical Specification	- 17 -
8 Interface Description	- 19 -
8.1 eMMC Interface ball array.....	- 19 -
8.2 Pins and Signal Description	- 20 -
9 Device Registers	- 21 -
9.1 Operating Condition Resister (OCR).....	- 21 -
9.2 Card Identification Resister (CID)	- 22 -
9.3 Card Specific Data Resister (CSD)	- 22 -
9.4 Extended CSD Resister	- 24 -



1 General Description

MK Founder e-MMC is an embedded flash memory storage solution.

MK Founder e-MMC is a hybrid device combining an embedded flash controller include LDPC based ECC and flash memory, with JEDEC Standard e-MMC 5.1 interface.

The e-MMC controller include LDPC based ECC directs the Flash management, including ECC, wear-leveling, IOPS optimization and read sensing, significantly reducing the storage management burden of the host CPU.

e-MMC is an ideal storage solution for many electronics devices. e-MMC designed to cover a wide area of application such as smart phones, Tablet PCs, Mobile phones, PDAs, Handheld electronics, Digital video cameras, Multimedia equipment, etc. Not only used in consumer products, e-MMC is being adopted rapidly in embedded applications, such as many Computer on Module designs, because of its compact size, low power consumption and many enhanced feature.

The technology specifications of e-MMC are managed by JEDEC, the global leader in developing open standards for the microelectronics industry.

2 Product List

Part Number	Density	PackageType	Package size	Remark
MKEMJ032GM1M-C	32GB	FBGA153	8x8.5x0.9 (mm)	1 stack

3 Key Features

- Support JEDEC/ e-MMC 5.1 Compliant
- Support 3.3V/1.8V power supply
- Support 12 wire bus (CLK, CMD, Data Strobe, DAT[7:0] and hardware reset (RST_n))
- Up to 200MHz clock speed
- Support Single Data Rate(SDR) and Dual Data Rate(DDR)
- Support different Bus width : 1bit, 4bit, 8bit
- Support Original Boot and Alternative Boot modes
- Support Data Removal (Erase, Trim and Sanitize)
- Support Replay Protected Memory Block(RPMB)
- Support Multiple Partitions with enhanced attribute
- Support Lock/Unlock and Write Protection
- Support Data Protection for Power Failure



- Support Power Saving Sleep Mode
- Support High Priority Interrupt(HPI)
- Support Background Operation
- Support Packed Commands
- Support Sampling Tuning Sequence
- Support Dynamic Power Manager : standby and sleep modes
- Support Command Queuing
- Support Secure Write Protection
- Package size
 - 8.0mm x 8.5mm x 0.9mm
- Operating Voltage range
 - $V_{CC} = 2.7V \sim 3.6V$ (typical 3.3V)
 - $V_{CCQ} = 1.7V \sim 1.95V$ (typical 1.8V), $2.7V \sim 3.6V$ (typical 3.3V)
- Temperature
 - Operating : $-25^{\circ}C \sim 85^{\circ}C$
 - Storage : $-40^{\circ}C \sim 85^{\circ}C$

4 Functional Block Diagram

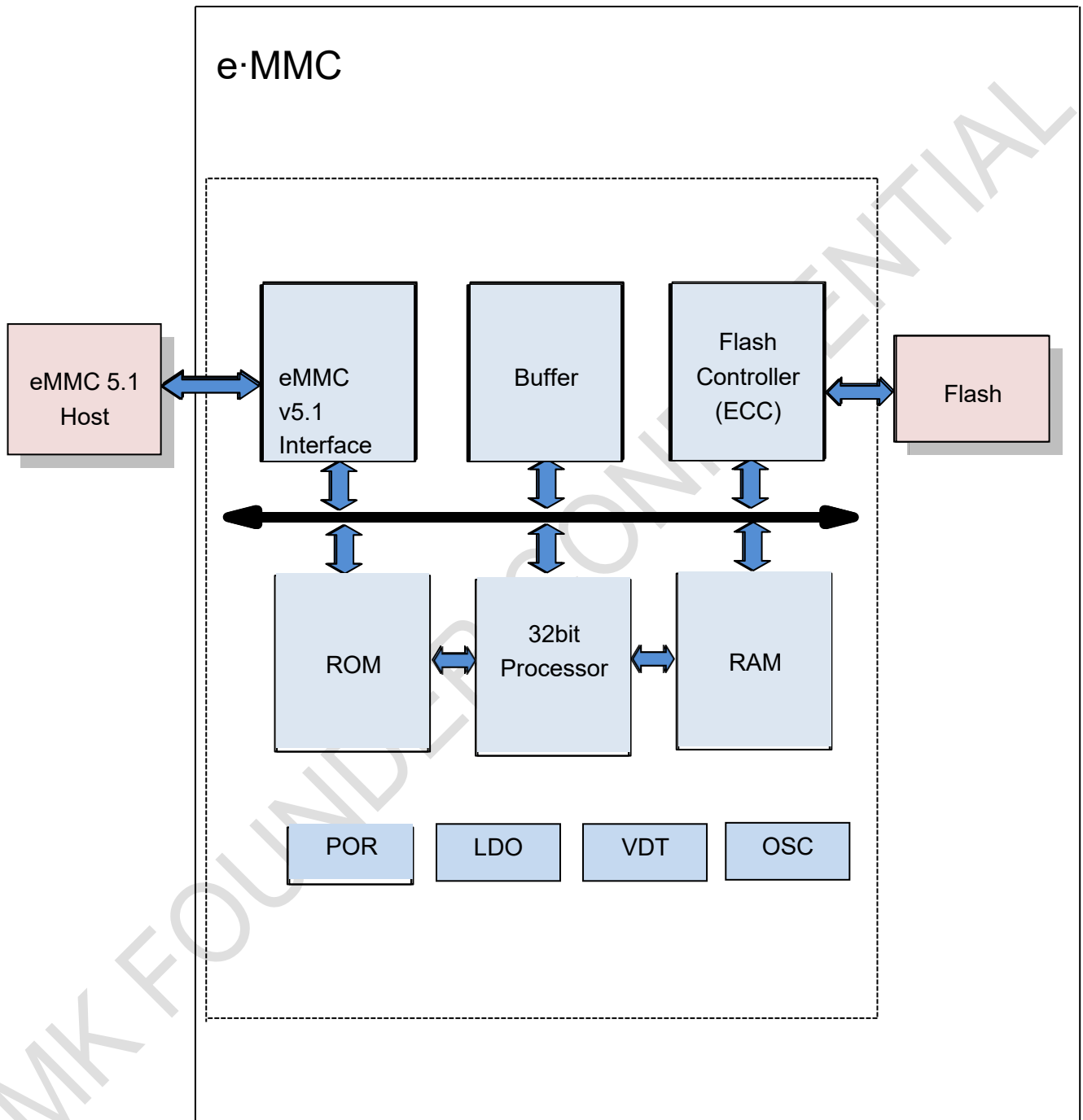


Figure 1 - e-MMC Block Diagram

5 e-MMC Device and System

5.1 e-MMC System Overview

The e-MMC specification covers the behavior of the interface and the device controller include BCH based ECC. AS part of this specification the existence of a host controller include BCH based ECC and a memory storage array are implied but the operation of these pieces is not fully specified

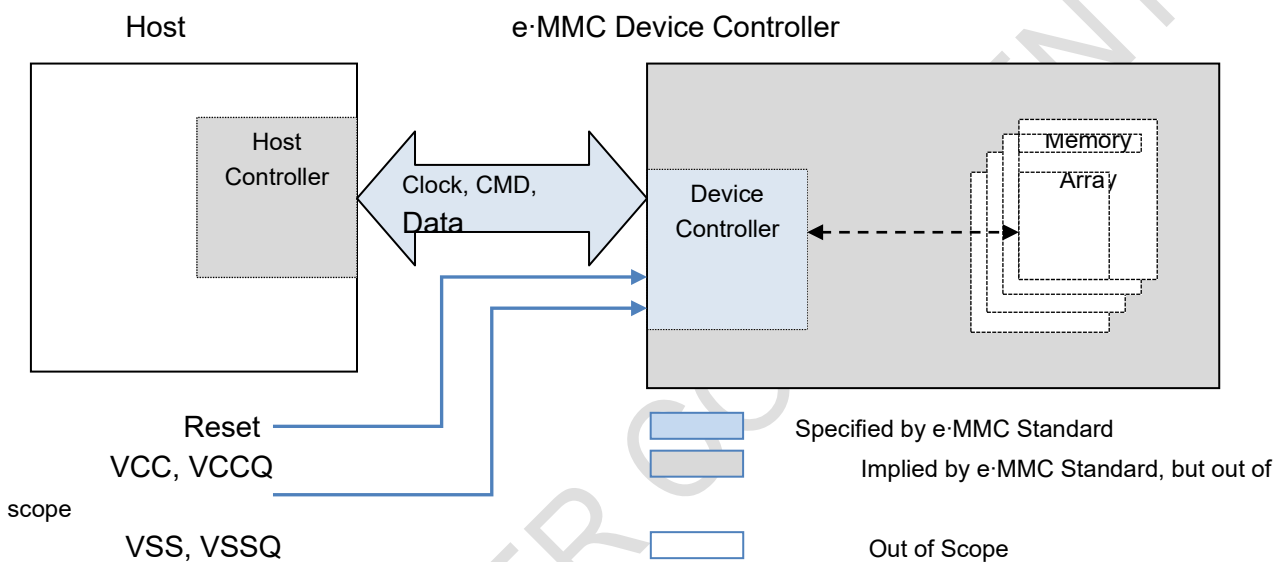


Figure 2 - e-MMC System Overview

5.2 e-MMC Device Overview

The e-MMC bus has the following communication and power lines

- CLK : Clock Input
- DS : Data strobe used for output in HS400 mode.
- CMD : Command is a bidirectional signal. The host and e-MMC operate in two modes, open drain and push-pull
- DAT0~DAT7 : Data lines are bidirectional signal. Host and e-MMC operate in push-pull mode.
- RST_n : Hardware Reset Input
- VCC : VCC is the power supply for core and flash IO.
- VCCQ : VCCQ is the power supply line for host interface
- VSS, VSSQ : Ground lines.

Name	Type	Description
CLK	I	Clock
DS	O/PP	Data Strobe
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
I: input, O: output, PP: push-pull, OD: open-drain, NC: Not connected, S: power supply		

Table 1 eMMC Interface

Name	Width (bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for Identification.	Mandatory
RCA	2	Relative Device Address, is the device system address, Dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver stage Resister, to configure the Device 's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation Conditions.	Mandatory
OCR	4	Operation Conditions Resister. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

Table 2 eMMC registers

6 e-MMC 5.1 Feature Overview

6.1 Boot

e-MMC supports JESD84-B51A boot operation mode, both mandatory as well as alternate mode are supported.

6.2 Sleep (CMD5)

A Device may be switched between a Sleep state and a Standby state by SLEEP/AWAKE(CMD5). In the Sleep State the power consumption of the memory device is minimized. In this state the memory device reacts only to the commands RESET(CMD0 with argument of either 0x00000000 or 0XF0F0F0F0 or H/W reset) and SLEEP/AWAKE(CMD5). All the other commands are ignored by the memory device.

The Vcc power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer JESD84-B51A.

6.3 Bus Modes

- **Boot mode**

The device will be in boot mode after power cycle, reception of CMD0 with argument of 0xF0F0F0F0 or the assertion of hardware reset signal.

- **Device identification mode**

The device will be in device identification mode after boot operation mode is finished or if host and/or device does not support boot operation mode. The device will be in this mode, until the SET_RCA command (CMD3) is received.

- **Interrupt mode**

Host and device enter and exit interrupt mode simultaneously. In interrupt mode there is no data transfer.

The only message allowed is an interrupt service request from the device or the host.

- Data transfer mode

The device will enter data transfer mode once an RCA is assigned to it. The host will enter data transfer mode after identifying the device on the bus

- Inactive mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid.

The device can also enter inactive mode with GO_INACTIVE_STATE command(CMD15). The device will reset to Pre-idle state with power cycle.

Device State	Operation mode	Bus mode
Inactive State	Inactive mode	Open-drain
Pre-Idle State	Boot mode	
Pre-Boot State		
Idle State	Device identification mode	
Identification State		
Stand-by State		
Sleep State	Data transfer mode	Push-pull
Transfer State		
Bus-Test State		
Sending-data State		
Receive-data State		
Programming State		
Disconnect State		
Boot State	Boot mode	
Wait-IRQ State	Interrupt mode	Open-drain

Table 3 Bus mode's overview



6.4 Reliable Write

eMMC supports 512B reliable write as defined in eMMC 5.1 spec.

Reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed.

This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing reliable write, data will remain valid even if a sudden power loss occurs during programming.

6.5 Secure Erase

In addition to the standard Erase command the eMMC support the optional Secure erase command. The Secure Erase command differs from the basic Erase command in that it requires the device and host to wait until the operation is complete before moving to the next device operation.

For additional information please refer JESD84-B51A.

The secure erase command requires device to perform a secure purge operation on the erase groups, and copy items identified for erase, in those erase groups.

A purge operation is defined as overwriting addressable location with a single character and the performing an erase.

This new command meets high security application requirements that once data has been erased, it can no longer be retrieved from device.

6.6 Secure Trim

The Secure Trim command is very similar to the Secure Erase command. The Secure Trim command performs a secure purge operation on write blocks instead of erase groups. To minimize the impact on the device's performance and reliability the Secure Trim operation is completed by executing two distinct steps.

For additional information please refer JESD84-B51A.

6.7 Trim

The Trim function is similar to the Erase command but applies the erase operation to write blocks instead of erase groups.

For additional information please refer JESD84-B51A.

6.8 Partition Management

The default area of the memory device consists of a User Data Area to store data, two possible boot area partitions for booting and the Replay Protected Memory Block Area Partition to manage data in an authenticated and replay protected manner. The memory configuration initially consists (before any partitioning operation) of the User Data Area and RPMB Area Partitions and Boot Area Partitions.

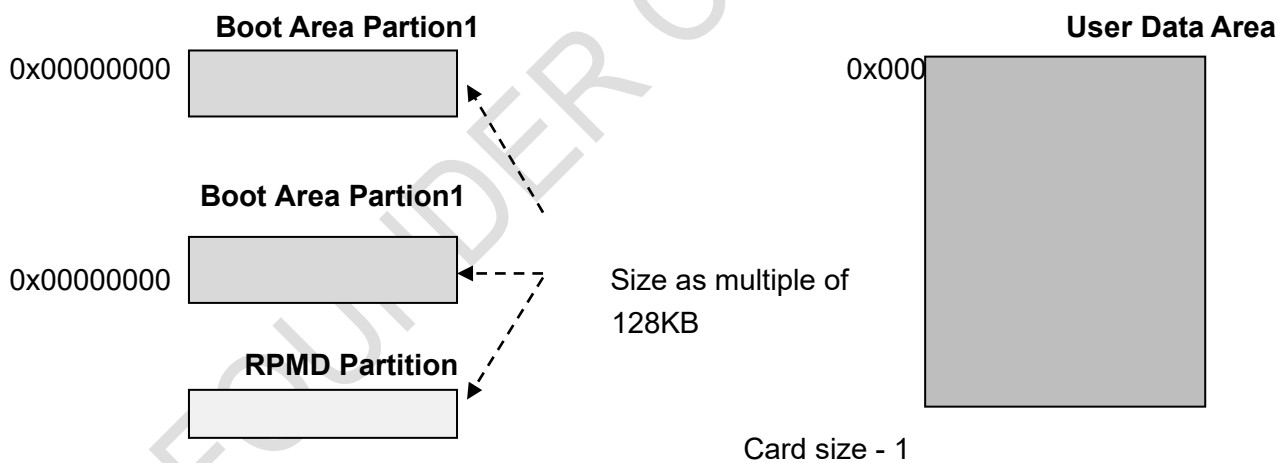


Figure 3 eMMC memory organization at time zero

For additional information please refer JESD84-B51A.

6.9 High priority interrupt (HPI)

Many operating systems use demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation, the request will be delayed until the completion of the write command which, in the worst case scenario, can take up to 350ms.

The high priority interrupt (HPI) as defined in JESD84-B51A enables low read latency operation by suspending a lower priority operation before it is actually completed. This mechanism can reduce read latency, in typical condition, to 5msec

For additional information please refer JESD84-B51A.

6.10 Background Operations

Devices have various maintenance operations that they need to perform internally, such as garbage collection, erase and compaction. In order to reduce latencies during time critical operations, it is better to execute maintenance operations when the device is not serving the host.

Operations are then separated into two types: foreground operations – such as read or write command, and background operations- operations that the device can execute when the host is not being served.

For additional information please refer JESD84-B51A.

6.11 H/W Reset

Hardware reset may be used by host to reset the device, moving the card to a Pre-Idle state and disabling the power-on period write protect on blocks that was set as power-on write protect before the reset was asserted.

For additional information please refer JESD84-B51A.

6.12 Packed Commands

Read and write commands can be packed in groups of commands (either all read or all write) that transfer the data for all commands in the group in one transfer on the bus to reduce overheads.

For additional information please refer JESD84-B51A.

6.13 Cache

Cache is temporary storage space in an e-MMC device. The cache should in typical case reduce the access time (compared to an access to the main non-volatile) for both write and read. The cache is not directly accessible by the host. This temporary storage space may be utilized also for some implementation specific operations like as an execution memory for the memory controller include BCH based ECC and/or as storage for an address mapping table etc but which definition is out of scope of this specification.

For additional information please refer JESD84-B51A.

6.14 Discard

The Discard is similar operation to TRIM. The Discard function allows the host to identify data that is no longer required so that the device can erase the data if necessary during background erase events. The contents of a write block where the discard function has been applied shall be 'don't care'. After discard operation, the original data may be remained partially or fully accessible to the host dependent on device. The portions of data that are no longer accessible by the host may be removed or unmapped just as in the case of TRIM. The device will decide the contents of discarded write block.

For additional information please refer JESD84-B51A.

6.15 Sanitize

The sanitize operation is a feature, in addition to TRIM and Erase that is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. A Sanitize operation is initiated by writing a value to the extended CSD[165] SANITIZE_START.

For additional information please refer JESD84-B51A.

6.16 Dynamic Capacity Management

Extensive memory usage and aging of Flash could result in bad block.

Dynamic Capacity Management provides a mechanism for the memory device to reduce its reported capacity and extend the device life time.

The mechanism to manipulate dynamic capacity is based on: memory array partitioning and the granularity of WP groups. Reducing the capacity is done by releasing of WP-groups anywhere within the address space of the user area. A released WP-Group will behave as a permanently write protected group and it shall not be read from: Writing to an address within a released WP-Group returns a WP error; Reading from an address within a released WP-Group is forbidden and may return an error; Checking write protection (using CMD30) and write protect type (using CMD31) shall report protected groups and permanent write protection accordingly.

For additional information please refer JESD84-B51A.

7 Product Specifications

7.1 Power Consumption

Power Consumption	32GB	Units
Standby(VCCQ & VCC on)	35	uA
Sleep (VCCQ on, VCC off)	76	uA
HS400 Read VCC	184	mA
HS400 Read VCCQ	182	mA
HS400 Write VCC	125	mA
HS400 Write VCCQ	100	mA

Table 4 Power Consumption (Ta=25°C@VCC=3.3V & VCCQ=1.8V)



7.2 Performance

HS400 Performance	32GB	Units
Sequential Read	315	MB/s
Sequential Write	142	MB/s
Random Read	18	MB/s
Random Write	8	MB/s

Table 5 Performance

7.3 Operating Conditions

	Temperature	Remark
Operating	-25°C ~ 85 °C	
Non-Operating	-40°C ~ 85 °C	

Table 6 Operating and Storage Temperature

7.4 Physical Specification

e-MMC is a 153pin, thin fine-pitched ball grid array.(BGA)

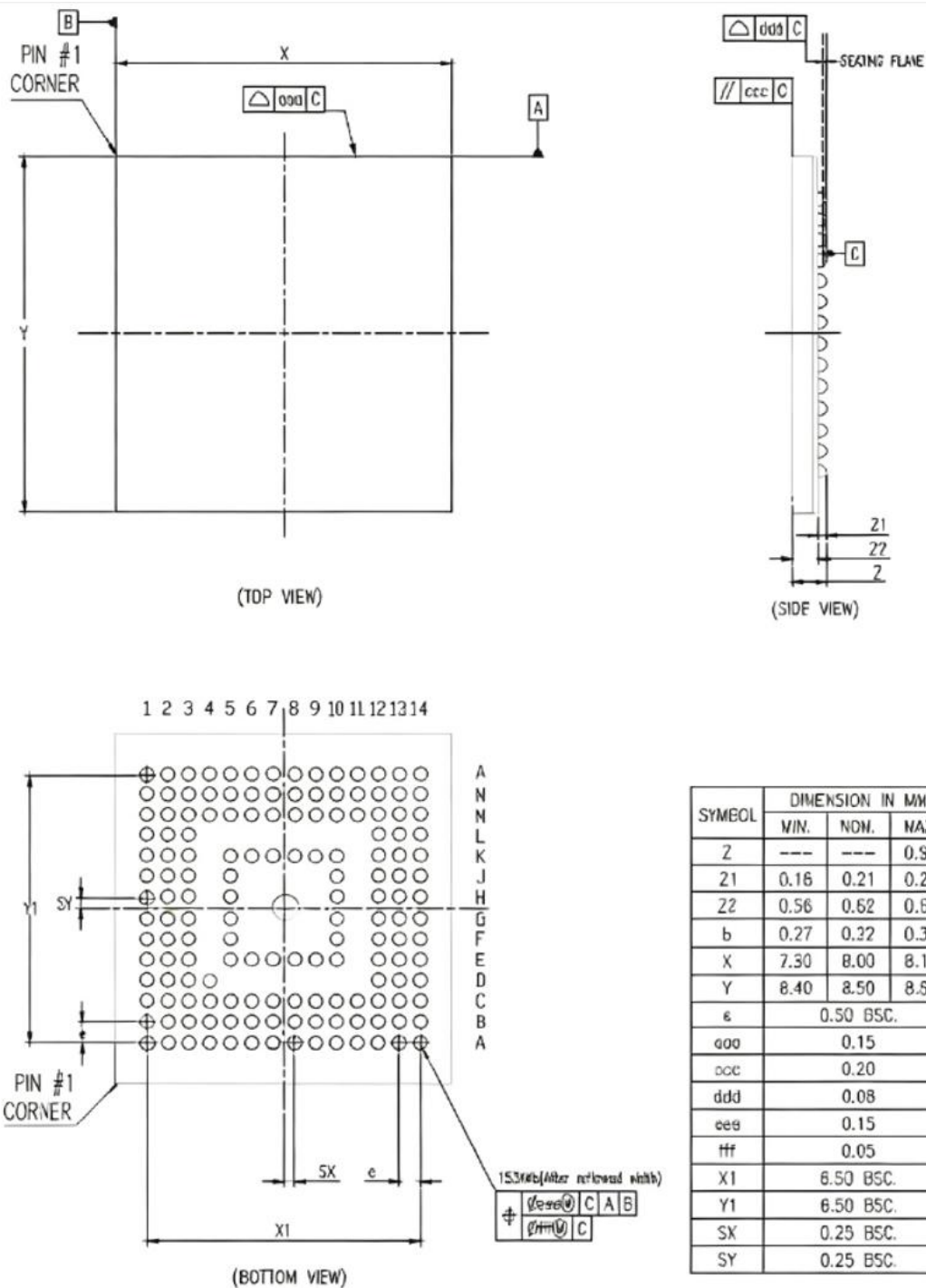


Figure 5 8 x8.5x 0.9mm Bottom & side View

8 Interface Description

8.1 e-MMC Interface ball array

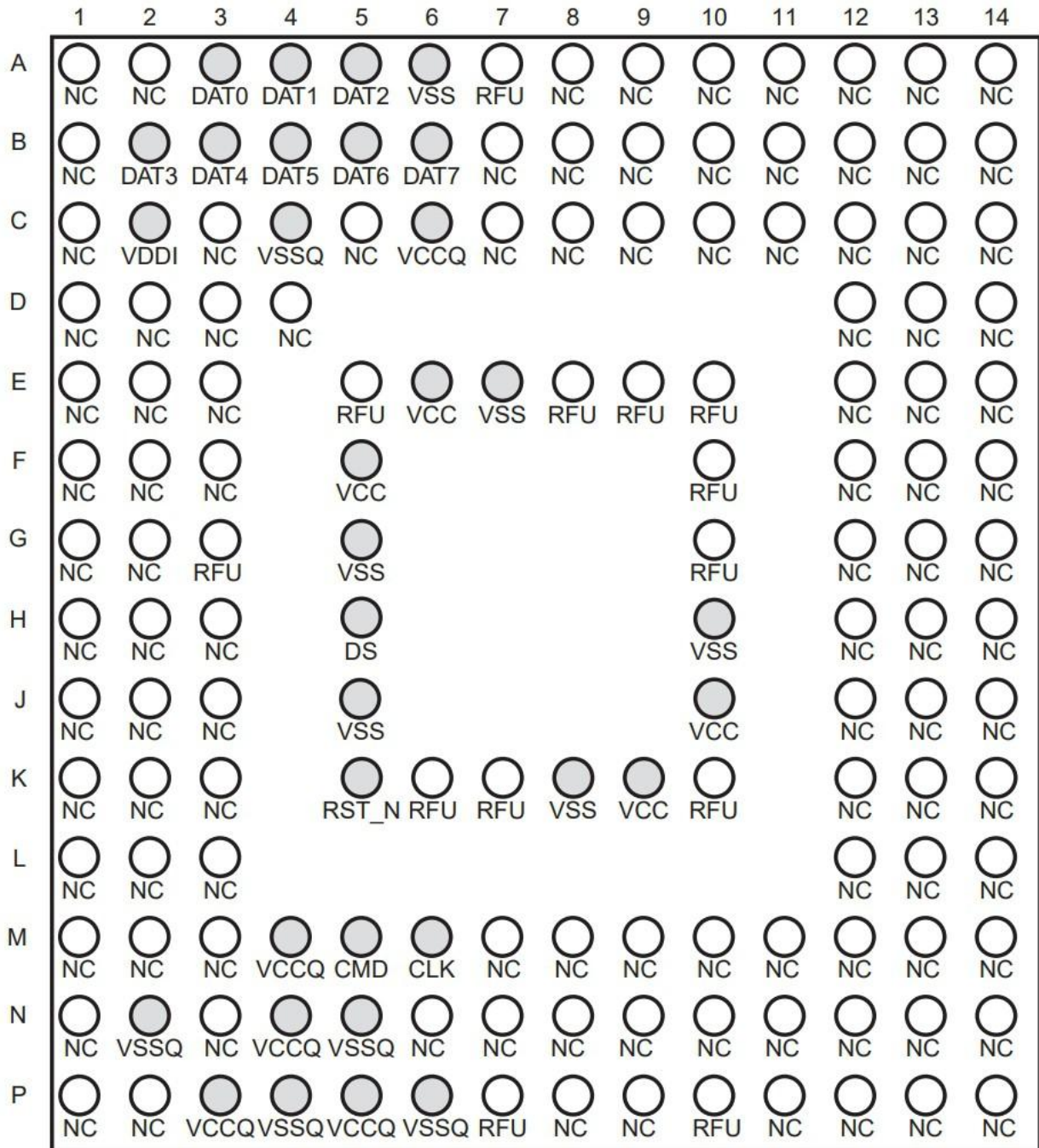


Figure 6 FBGA153 Package Connection (top view through package)

8.2 Pins and Signal Description

153-Ball Device	Symbol	Type	Ball Function
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
M5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfer. Command has two operating mode : 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
A3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
A4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
A5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
B2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
B3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
B4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
B5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
B6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
K5	RST_n	Input	Reset signal pin
E6, F5, J10, K9	VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
C6, M4, N4, P3, P5	VccQ	Supply	VccQ: Memory controller core and MMC interface I/O power supply.
A6, E7, G5, J5, H10, K8	VSS	Supply	Vss: Flash memory I/F and Flash memory ground connection.
C4, N2, N5, P4, P6	VssQ	Supply	VssQ
C2	VDDi		VDDi : Connect 1uF capacitor from VDDi to ground.
H5	DS		Data Strobe : Return clock signal used in HS400 mode

Table 7 Pin and signal Description

9 Device Resisters

9.1 Operating Condition Resister (OCR)

The 32-bit operation condition register(OCR) store the Vdd voltage profile of the e-MMC and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the e-MMC power up procedure has been finished. The OCR register shall be implemented by e-MMC.

OCR bit	Description	Value	Remark
[6:0]	Reserved	000 0000b	
[7]	1.70 ~ 1.95V	1b	
[14:8]	2.0 ~ 2.6V	000 0000b	
[23:15]	2.7 ~ 3.6V	1 1111 1111b	
[28:24]	Reserved	0 0000b	
[30:29]	Access mode	10b	
[31]	card power up status bit (busy) ¹		

¹)This bit is set to LOW if the Device has not finished the power up routine.

Table 8 OCR register definition

9.2 Card Identification Resister (CID)

The Card Identification(CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase(e-MMC protocol). Every individual flash or I/O Device shall have a unique identification number. Table 21 lists these identifiers.

The structure of the CID register is defined in the following section.

Name	Field	Width	CID-Slice	CID Value	Remark
Manufacture ID	MID	8	[127:120]	FFh	
Reserved		6	[119:114]		
Card / BGA	CBX	2	[113:112]	01h	BGA
OEM/Application ID	OID	8	[111:104]	FFh	Not fixed
Product name	PNM	48	[103:56]	MK032D	Not fixed
Product revision	PRV	8	[55:48]	FF	Not fixed
Product serial number	PSN	32	[47:16]	Random by Production	Not fixed
Manufacturing date	MDT	8	[15:8]	month, year	Not fixed
CRC7 checksum	CRC	7	[7:1]	0h	Not fixed
Not used, always '1'	-	1	[0:0]	0h	

Table 9 Card Identification register definition

9.3 Card Specific Data Resister (CSD)

The Device-specific Data (CSD) register provides information on how to access the Device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register(entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries below is coded as follows :

- R : Read only
- W : One time programmable and not readable.
- R/W : One time programmable and readable
- W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/C_P : Writeable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.



- R/W/E_P : Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- W/E_P : Multiple writable with value reset power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Width	Cell type	CSD Slice	CSD Value	Remark
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h	
System Specification version	SPEC_VERS	4	R	[125:122]	4h	
Reserved	-	2	R	[121:120]		
Data read access-time 1	TAAC	8	R	[119:112]	2Fh	20ms
Data read access-time 2in CLK cycle (NSAC*100)	NSAC	8	R	[111:104]	1h	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	2Ah	20MHz
Device command classes	CCC	12	R	[95:84]	5F5h	Class 0,2,4,5,6,7,8,10
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h	512B
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h	Not support
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h	Not support
Name	Field	Width	Cell type	CSD Slice	CSD Value	Remark
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h	Not support
DSR implemented	DSR_IMP	1	R	[76:76]	0h	Not support
Reserved		2	R	[75:74]		
Device size	C_SIZE	12	R	[73:62]	FFFh	
Max read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]	6h	
Max read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]	6h	
Max write current @VDD min	VDD_W_CURR_MIN	3	R	[53:53]	6h	
Max write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]	6h	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh	



Write protect group size	WP_GRP_SIZE	5	R	[36:32]	1Fh	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h	
Write speed factor	R2W_FACTOR	3	R	[28:26]	1h	
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h	512B
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	Not support
Reserved		4	R	[20:17]		
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h	Not support
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC code	ECC	2	R/W/E	[9:8]	0h	None
CRC	CRC	7	R/W/E	[7:1]	7h	
Not used, always '1'		1	-	[0:0]	1h	

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

Table 10 CSD Field

9.4 Extended CSD Resister

The Extended CSD register defines the Device properties and selected modes. It is 512bytes long. The most significant 320bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host means of the SWITCH command.

For details, refer to section 7.4 of the JEDEC Standard Specification No. JESD84-B51A.



Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark
Properties Segment					
Reserved1	RESERVED	TBD	[511:506]		
Extended Security Command Error	EXT_SECURITY_ERROR	R	[505]	0x00h	
Supported Command Sets	S_CMD_SET	R	[504]	0x01h	
HPI features	HPI_FEATURES	R	[503]	0x01h	
Background operations support	BKOPS_SUPPORT	R	[502]	0x01h	
Max packed read commands	MAX_PACKED_READS	R	[501]	0x20h	
Max packed write commands	MAX_PACKED_WRITES	R	[500]	0x20h	
Data Tag Support	DATA_TAG_SUPPORT	R	[499]	0x01h	
Tag Unit Size	TAG_UNIT_SIZE	R	[498]	0x00h	
Tag Resources Size	TAG_RES_SIZE	R	[497]	0x00h	
Context Management Capabilities	CONTEXT_CAPABILITIES	R	[496]	0x78h	
Large Unit Size	LARGE_UNIT_SIZE_M1	R	[495]	0x01h	
Extended partition Attribute Support	EXT_SUPPORT	R	[494]	0x03h	
Supported modes	SUPPORTED_MODES	R	[493]	0x01h	
FFU features	FFU_FEATURES	R	[492]	0x00h	
Operation codes timeout	OPERATION_CODE_TIMEOUT	R	[491]	0x17h	
FFU Argument	FFU_ARG	R	[490:487]	0xFFFFAFF0h	
Barrier support	BARRIER_SUPPORT	R	[486]	0x01h	
Reserved1		TBD	[485:309]		
CMD Queuing Support	CMDQ_SUPPORT	R	[308]	0x01h	
CMD Queuing Depth	CMDQ_DEPTH	R	[307]	0x1Fh	



MKEMJ032GM1M-C

Reserved1		TBD	[306]		
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	R	[305:302]	0x00000000 h	
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	R	[301:270]	0x00h	
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	R	[269]	0x01h	
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	R	[268]	0x01h	
Pre EOL information	PRE_EOL_INFO	R	[267]	0x01h	
Optimal read size	OPTIMAL_READ_SIZE	R	[266]	0x40h	
Optimal write size	OPTIMAL_WRITE_SIZE	R	[265]	0x40h	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	R	[264]	0x07h	
Device version	DEVICE_VERSION	R	[263:262]	0x4205 h	
Firmware version	FIRMWARE_VERSION	R	[261:254]	0x00000000000000001h	
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	R	[253]	0x00h	
Cache size	CACHE_SIZE	R	[252:249]	0x00000400h	
Generic CMD6 timeout	GENERIC_CMD5_TIME	R	[248]	0X05h	
Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark
Power off notification (long)timeout	POWER_OFF_LONG_TIME	R	[247]	0x64h	
Background operations status	BKOPS_STATUS	R	[246]	0x00h	
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	R	[245:242]	0x00000000h	
1st initialization time after partitioning	INI_TIMEOUT_AP	R	[241]	0x0Ah	
Cache Flushing Policy	CACHE_FLUSH_POLICY	R	[240]	0x01h	
Power class for 52MHz, DDR at VCC = 3.6V	PWR_CL_DDR_52_360	R	[239]	0x00h	
Power class for 52MHz, DDR at VCC = 1.95V	PWR_CL_DDR_52_195	R	[238]	0x00h	
Power class for 200MHz at VCCQ = 1.95V, VCC = 3.6V	PWR_CL_200_195	R	[237]	0x00h	
Power class for 200MHz at VCCQ = 1.3V, VCC = 3.6V	PWR_CL_200_130	R	[236]	0x00h	



MKEMJ032GM1M-C

Minimum Write Performance for 8bit At 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	R	[235]	0x00h	
Minimum Read Performance for 8bit At 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	R	[234]	00x00h	
Reserved ₁	RESERVED	TBD	[233]		
TRIM Multiplier	TRIM_MULT	R	[232]	0x02h	
Secure Feature support	SEC_FEATURE_SUPPORT	R	[231]	0x55h	
Secure Erase Multiplier	SEC_ERASE_MULT	R	[230]	0x19h	
Secure TRIM Multiplier	SEC_TRIM_MULT	R	[229]	0x0Ah	
Boot information	BOOT_INFO	R	[228]	0x07h	
Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark
Reserved ₁	RESERVED	TBD	[227]		
Boot partition size	BOOT_SIZE_MULT	R	[226]	0x20h	
Access size	ACC_SIZE	R	[225]	0x06h	
High-capacity erase unit size	HC_ERASE_GRP_SIZE	R	[224]	0x01h	
High-capacity erase timeout	ERASE_TIMEOUT_MULT	R	[223]	0x02h	
Reliable write sector count	REL_WR_SEC_C	R	[222]	0x01h	
High-capacity write protect group size	HC_WP_GRP_SIZE	R	[221]	0x10h	
Sleep current (VCC)	S_C_VCC	R	[220]	0x07h	
Sleep current(VCCQ)	S_C_VCCQ	R	[219]	0x07h	
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	R	[218]	0x17h	
Sleep/awake timeout	S_A_TIMEOUT	R	[217]	0x12h	
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	R	[216]	0x0Ch	
Sector Count	SEC_COUNT	R	[215:212]	0x03A40000h	
Secure Write Protect Information	SECURE_WP_INFO	TBD	[211]	0x01h	
Minimum Write Performance for 8bit At 52MHz	MIN_PERF_W_8_52	R	[210]	0x00h	
Minimum Read Performance for 8bit At 52MHz	MIN_PERF_R_8_52	R	[209]	0x00h	

**MKEMJ032GM1M-C**

Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	R	[208]	0x00h	
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	R	[207]	0x00h	
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	R	[206]	0x00h	
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_R_26	R	[205]	0x00h	
Reserved ₁	RESERVED	R	[204]	TBD	
Power class for 26MHz at 3.6V 1R	PWR_CL_26_360	R	[203]	0x00h	
Power class for 52MHz at 3.6V 1R	PWR_CL_52_360	R	[202]	0x00h	
Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark
Power class for 26MHz at 1.95V 1R	PWR_CL_26_195	R	[201]	0x00h	
Power class for 52MHz at 1.95V 1R	PWR_CL_52_195	R	[200]	0x00h	
Partition switching timing	PARTITION_SWITCH_H_TIME	R	[199]	0x04h	
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	R	[198]	0x0Ah	
I/O Driver Strength	DRIVER_STRENGTH	R	[197]	0x1Fh	
Device type	DEVICE_TYPE	R	[196]	0x57h	
Reserved ₁	RESERVED	TBD	[195]		
CSD structure	CSD_STRUCTURE	R	[194]	0x02h	
Reserved ₁	RESERVED	TBD	[193]		
Extend CSD revision	EXT_CSD_REV	R	[192]	0x08h	
Modes Segment					
Command set	CMD_SET	R/W/E_P	[191]	0x00h	
Reserved ₁	RESERVED	TBD	[190]		
Command set revision	CMD_SET_REV	R	[189]	0x00h	
Reserved ₁	RESERVED	TBD	[188]		
Power class	POWER_CLASS	R/W/E_P	[187]	0x00h	
Reserved ₁	RESERVED	TBD	[186]		
High-speed interface timing	HS_TIMING	R/W/E_P	[185]	0x00h	
Strobe Support	STROBE_SUPPORT	R	[184]	0x01h	

**MKEMJ032GM1M-C**

Bus width mode	BUS_WIDTH	W/E_P	[183]	0x00h	
Reserved ₁	RESERVED		[182]		
Erase memory content	ERASED_MEM_CONTENT	R	[181]	0x00h	
Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark
Reserved ₁	RESERVED	TBD	[180]		
Partition configuration	PARTITION_CONFIG	R/W/E & R/W/E_P	[179]	0x00h	
Boot config protection	BOOT_CONFIG_PROT	R/W/E & R/W/C_P	[178]	0x00h	
Boot bus Conditions	BOOT_BUS_CONDITIONS	R/W/E	[177]	0x00h	
Reserved ₁	RESERVED	TBD	[176]		
High-density erase group definition	ERASE_GROUP_DEF	R	[175]	0x00h	
Boot write protection status registers		TBD	[174]	0x00h	
Boot area write protection register	BOOT_WP	R/W/E & R/W/C_P	[173]	0x00h	
Reserved ₁	RESERVED	TBD	[172]		
User area write protection register	USER_WP	R/W, & R/W/C_P & R/W/E_P	[171]	0x00h	
Reserved ₁	RESERVED	TBD	[170]		
FW configuration	FW_CONFIG	R/W	[169]	0x00h	
RPMB Size	RPMB_SIZE_MULT	R	[168]	0x20h	
Write reliability setting register	WR_REL_SET	R/W	[167]	0x1Fh	
Write reliability parameter register	WR_REL_PARAM	R	[166]	0x15h	
Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark
Start Sanitize operation	SANITIZE_START	W/E_P	[165]	0x00h	
Manually start background operations	BKOPS_EN	W/E_P	[164]	0x00h	
Enable background operations handshake	BKOPS_EN	R/W	[163]	0x02h	
H/W reset function	RST_n_FUNCTION	R/W	[162]	0x00h	



MKEMJ032GM1M-C

HPI management	HPI_MGMT	R/W/ E_P	[161]	0x00h	
Partitioning Support	PARTITIONING_SUPPORT	R	[160]	0x07h	
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	R	[159:157]	0x0004DAh	
Partitions attribute	PARTITIONS_ATTRIBUTE	R/W	[156]	0x00h	
Partitioning Setting	PARTITION_SETTING_COMPLETED	R/W	[155]	0x00h	
General Purpose Partition Size	GP_SIZE_MULT	R/W	[154:143]	0x0000000000000000 000000000 h	
Enhanced User Data Area Size	ENH_SIZE_MULT	R/W	[142:140]	0x0000000h	
Enhanced User Data Start Address	ENH_START_ADDR	R/W	[139:136]	0x00000000 h	
Reserved ₁	RESERVED	TBD	[135]		
Bad Block Management mode	SEC_BAD_BLK_MGMT	R/W	[134]	0x00h	
Production state awareness	PRODUCTION_STATE_AWARENESS	R/W/E	[133]	0x00h	
Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark
Package Case Temperature is Controlled	TCASE_SUPPORT	W/E_P	[132]	0x00h	
Periodic Wake-up	PERIODIC_WAKEUP	R/W/E	[131]	0x00h	
Program CID/CSD in DDR mode Support	PROGRAM_CID_CSD_DDR_SUPPORT	R	[130]	0x01h	
Reserved ₁	RESERVED	TBD	[129:128]		
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD		[127:64]	0x0000000000000000 0000000000000000 0000000000000000 0000000000000000 0000000000000000 0000000000000000 0000000000000000 0000000000000000 280001400C8	
Native sector size	NATIVE_SECTOR_SIZE	R	[63]	0x01h	
Sector size emulation	USE_NATIVE_SECTOR	R/W	[62]	0x00h	
Sector size	DATA_SECTOR_SIZE	R	[61]	0x00h	
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	R	[60]	0x0Ah	
Class 6 commands control	CLASS_6_CTRL	R/W/E_P	[59]	0x00h	
Number of addressed group to be Released	DYNCAP_NEEDED	R	[58]	0x00h	



Exception event control	EXCEPTION_EVENTS_CTRL	R/W/E_P	[57:56]	0x0000h	
Exception event status	EXCEPTION_EVENTS_STATUS	R	[55:54]	0x0000 h	
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	R/W	[53:52]	0x0000 h	
Context configuration	CONTEXT_CONF	R/W/E_P	[51:37]	0x0000000000000000 0000000000000000 h	
Packed command status	PACKED_COMMAND_STATUS	R	[36]	0x00h	
Packed command failure index	PACKED_FAILURE_INDEX	R	[35]	0x00h	
Power Off Notification	POWER_OFF_NOTIFICATION	R/W/E_P	[34]	0x00h	
Control to turn the Cache ON/OFF	CACHE_CTRL	R/W/E_P	[33]	0x00h	
Flushing of the cache	FLUSH_CACHE	W/E_P	[32]	0x00h	
Control to turn the Barrier ON/OFF	BARRIER_CTRL	R/W	[31]	0x00h	
Mode config	MODE_CONFIG	R/W/E_P	[30]	0x00h	
Mode operation codes	MODE_OPERATION_CODES	W/E_P	[29]	0x00h	
Reserved1		TBD	[28:27]		
FFU status	FFU_STATUS	R	[26]	0x00h	
Pre loading data size	PRE_LOADING_DATA_SIZE	R/W/E_P	[25:22]	0x00000000 h	
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	R	[21:18]	0x01368000	
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	R/W/E & R	[17]	0x01h	
Secure Removal Type	SECURE_REMOVAL_TYPE	R/W/E & R	[16]	0x39h	
Command Queue Mode Enable	CMDQ_MODE_EN	R/W/E_P	[15]	0x00h	
Reserved1		TBD	[14:0]		
NOTE1. Reserved bits should read as “0” NOTE2. Obsolete values should be don't care					

Table 11 Extended CSD Field