

1 FEATURES

- Operates with a single 3.3V Supply
- Compatible With ISO 11898-2 Standard
- Low Power Replacement for the HMT1050 Footprint
- Bus Pin ESD Protection Exceeds $\pm 16\text{kV}$ HBM
- High Input Impedance Allows for Up to 120 nodes ($\leq 1\text{ Mbps}$)
- Data Rates up to 5Mbps
- Thermal Shutdown Protection
- Open Circuit Fail-Safe Design
- Glitch Free Power Up and Power Down Protection for Hot Plugging Applications
- Available in near chip scale DFN(2mmx2mm)

2 APPLICATIONS

- Industrial Automation, Sensors and Drive Systems
- Motor and Robotic Control
- Building and Climate Control (HVAC)
- Telecommunications and Base Station Control and Status
- CAN Bus Standards Such as CAN open

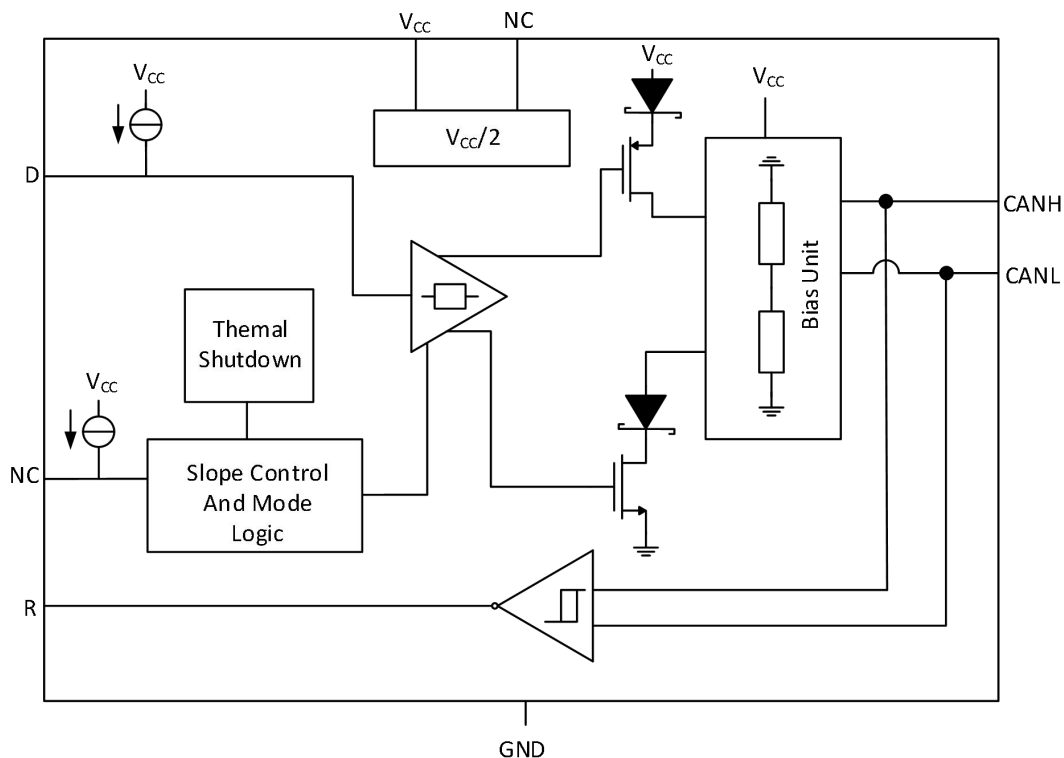
3 DESCRIPTION

The HMT232TK controller area network (CAN) transceiver is compatible to the specifications of the ISO 11898-2 High Speed CAN Physical Layer standard (transceiver). These devices are designed for data rates up to 5Mbps, and include many protection features providing device and CAN network robustness. The HMT232TK transceiver is designed for use with 3.3V μP , MCU and DSP with CAN controllers, or with equivalent protocol controller devices. The devices are intended for use in applications employing the CAN serial communication physical layer in accordance with the ISO 11898 standard.

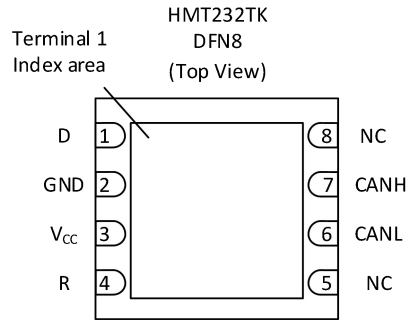
Designed for operation in especially harsh environments, these devices feature cross wire protection, loss of ground and over voltage protection, over temperature protection, as well as wide common mode range of operation.

The CAN transceiver is the CAN physical layer and interfaces the single ended host CAN protocol controller with the differential CAN bus found in industrial, building automation, and automotive applications. These devices operate over a -15V to 15V common mode range on the bus.

Block Diagram



4 Pin Configuration and Functions



Pin		Type	Description
Name	No.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
V _{CC}	3	Supply	Transceiver 3.3V supply Voltage
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
NC	5	NC	No Connect
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
NC	8		No Connect

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Supply Voltage, V _{CC}	-0.3	6	V
Voltage at any bus terminal (CANH or CANL)	-40	40	V
Digital Input and Output Voltage, V _I (D or R)	-0.5	V _{CC} + 0.5	V
Receiver output current, I _O	-11	11	mA
Storage temperature, T _{stg}	-40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All Voltage Values, except differential I/O bus Voltages, are with respect to network ground terminal.

5.2 ESD Ratings

			Value	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM)	CANH, CANL and GND	±16000	V
		All pins	±4000	
	Charged-device model (CDM)		±1000	

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}		3		3.6	V
Voltage at any bus terminal (common mode) V_{IC}		-15 ⁽¹⁾		15	V
High-level input Voltage, V_{IH}	D, R	2			V
Low-level input Voltage, V_{IL}	D, R			0.8	V
Differential input Voltage, V_{ID} (see Figure 5)		-20		20	V
High-level output current, I_{OH}	Driver	-40			mA
	Receiver	-8			
Low-level output current, I_{OL}	Driver			48	mA
	Receiver			8	
Thermal shutdown temperature			165		°C
Thermal shutdown hysteresis			10		
Operating free-air temperature, T_A		-40		125	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.4 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

Parameter			Test Conditions		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	Bus output Voltage	Dominant	$V_I = 0V$, See Figure 1 and Figure 3	CANH	2.45		V_{CC}	V
				CANL	0.5		1.0	
V_{OL}		Recessive	$V_I = 3V$, See Figure 1 and Figure 3	CANH		2.3		
				CANL		2.3		
$V_{OD(D)}$	Differential output Voltage	Dominant	$V_I = 0V$,	See Figure 1	1.5	2	3	V
			$V_I = 0V$,	See Figure 2	1.2	2	3	
$V_{OD(R)}$		Recessive	$V_I = 3V$,	See Figure 1	-120	0	12	mV
			$V_I = 3V$,	No load	-0.5	-0.2	0.05	V
I_{IH}	High-level input current	$V_I = 2V$			-10	-2.5	10	μA
I_{IL}	Low-level input current	$V_I = 0.8V$			-10	-6.0	15	μA
I_{OS}	Short-circuit output current	$V_{CANH} = -15V$			-250		250	mA
		$V_{CANL} = 15V$			-250		250	
C_o	Output capacitance	See receiver						
I_{CC}	Supply current	All devices	Dominant	$V_I = 0V$, No load	Dominant	1	2	mA
			Recessive	$V_I = V_{CC}$, No load	Recessive	1	2	

(1) All typical Values are at 25°C and with a 3.3V supply.

5.5 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold Voltage	See Table 1			800	900	mV
V _{IT-}	Negative-going input threshold Voltage			500	700		mV
V _{hys}	Hysteresis Voltage (V _{IT+} - V _{IT-})				100		
V _{OH}	High-level output Voltage	-20V ≤ V _{ID} ≤ 500mV, I _O = -8mA, See Figure 5		2.4			V
V _{OL}	Low-level output Voltage	900mV ≤ V _{ID} ≤ 20V, I _O = 8mA, See Figure 5				0.4	
I _I	Bus input current	V _{IH} = 10V	V _{CC} = 0V	Other input at 0V, D = 3V	100	350	μA
		V _{IH} = -10V			-350	-30	
		V _{IH} = -10V	V _{CC} = 0V		-350	-20	
R _{Diff}	Differential input resistance	Pin-to-pin	V _(D) = 3V	40	70	100	kΩ
R _I	CANH, CANL input resistance			20	35	50	kΩ

(1) All typical Values are at 25°C and with a 3.3V supply.

5.6 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	C _L = 50pF, See Figure 4		55	85	ns
t _{PHL}	Propagation delay time, high-to-low-level output			80	120	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			25		
t _r	Differential output signal rise time		25	50	100	
t _f	Differential output signal fall time		30	40	70	

5.7 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	See Figure 6		35	50	ns
t _{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})				10	ns
t _r	Output signal rise time				1.5	ns
t _f	Output signal fall time				1.5	ns

5.8 Switching Characteristics: Device

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
t _(LOOP1)	Total loop delay, driver input to receiver output, recessive to dominant	See Figure 7		90	130	ns
t _(LOOP2)	Total loop delay, driver input to receiver output, dominant to recessive	See Figure 7		120	170	ns

6 Parameter Measurement Information

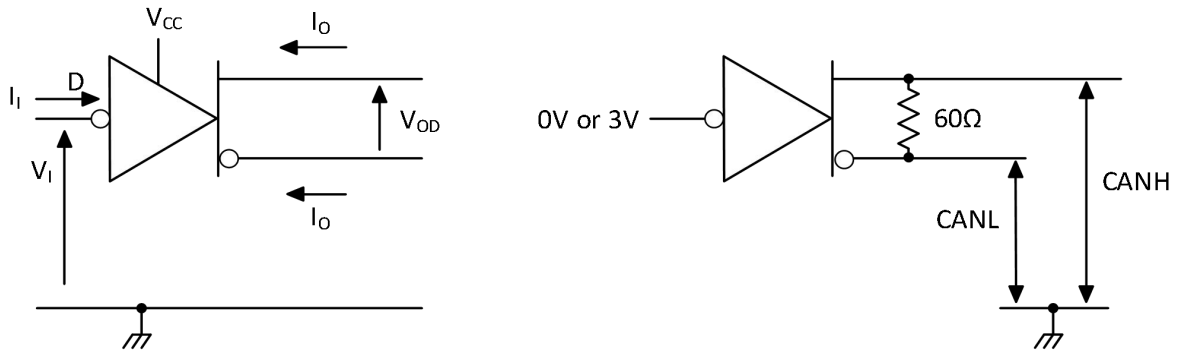


Figure1. Driver Voltage and Current Definitions

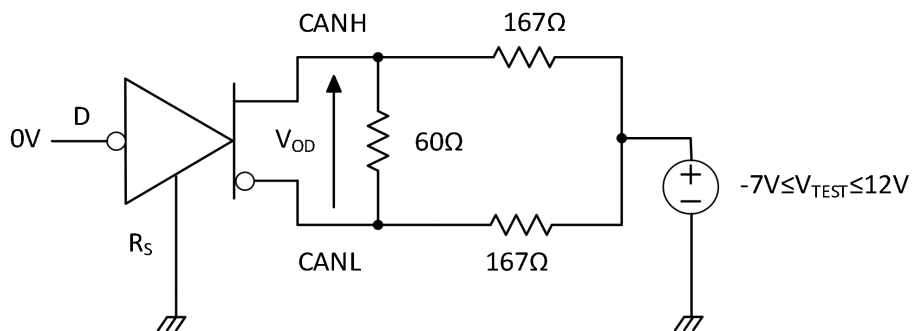


Figure2. Driver V_{OD}

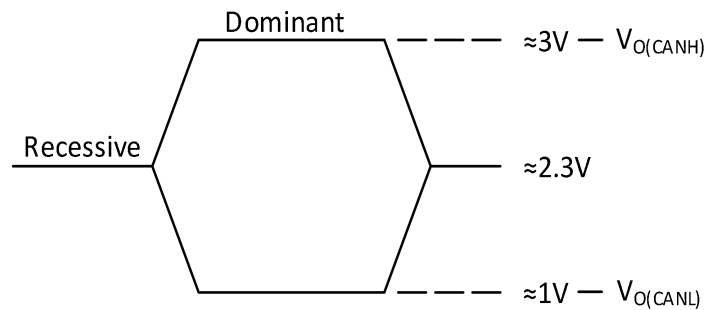
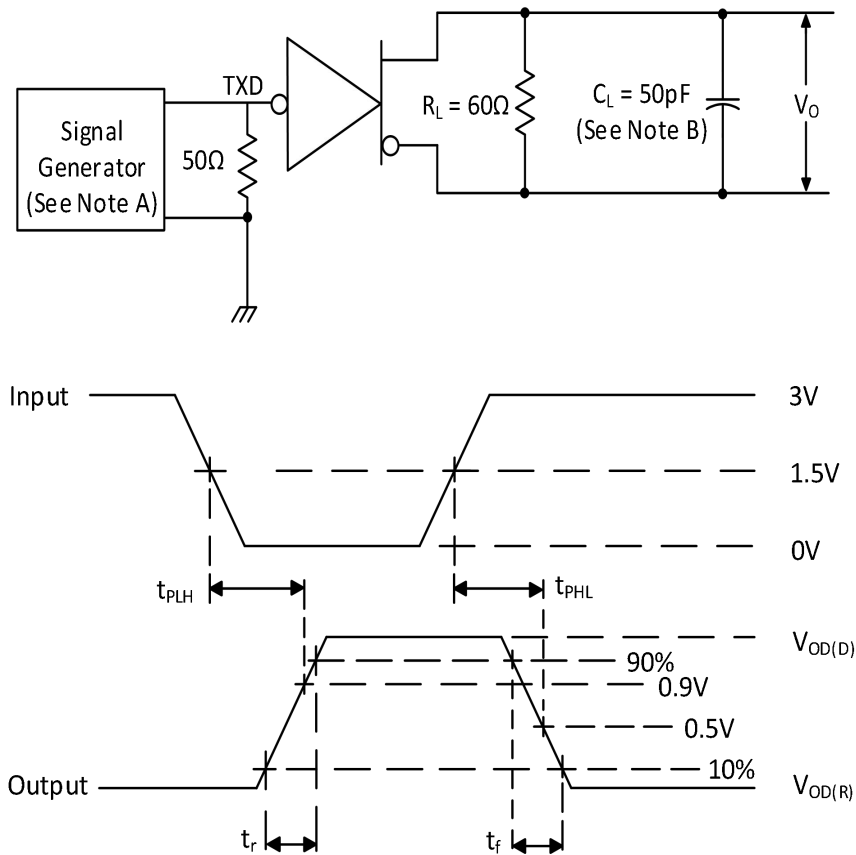


Figure3. Driver Output Voltage Definitions

Parameter Measurement Information(continued)



- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) $\leq 125\text{kHz}$, 50% duty cycle, $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$, $Z_o = 50\Omega$.
B. C_L includes fixture and instrumentation capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

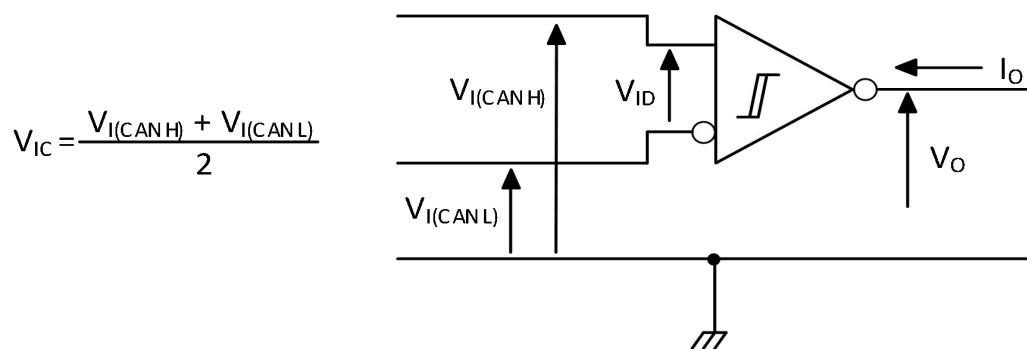
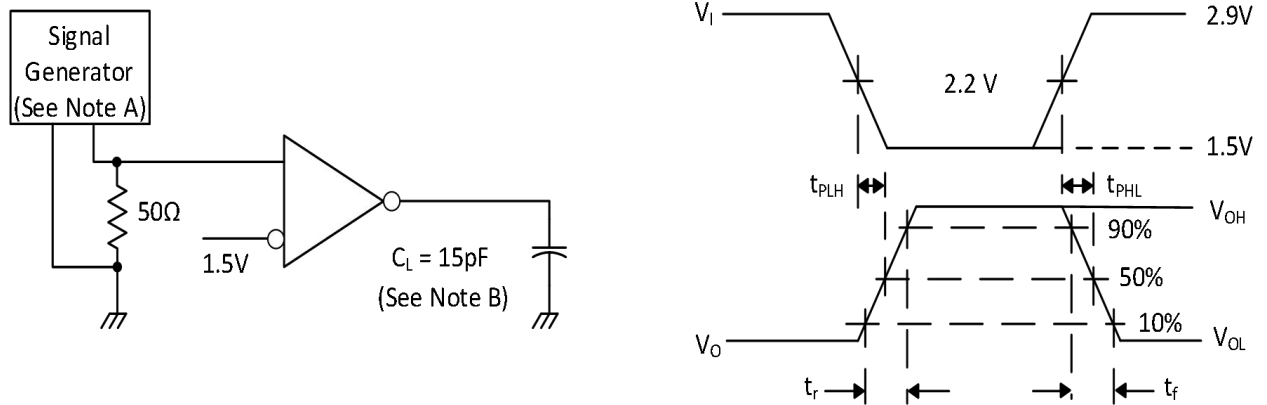


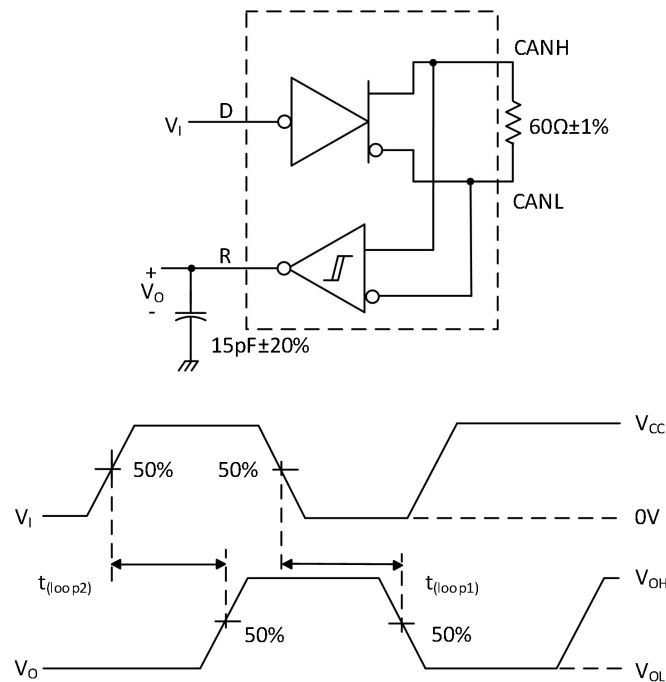
Figure 5. Receiver Voltage and Current Definitions

Parameter Measurement Information(continued)



- A. The Input pulse is supplied by a generator having the following characteristics: $PRR \leq 500 \text{ kHz}$, 50% duty cycle, $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$, $Z_o = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms



- A. All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6\text{ns}$, Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 7. $t_{(LOOP)}$ Test Circuit and Voltage Waveforms

Parameter Measurement Information(continued)

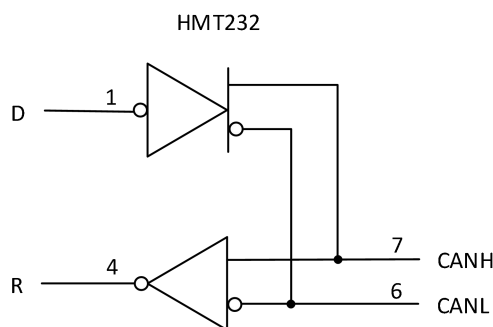


Figure 8. Logic Diagram (Positive Logic)

Table 1. Receiver Characteristics Over Common Mode

V_{IC}	V_{ID}	V_{CANH}	V_{CANL}	R OUTPUT	
-15V	900mV	-14.55V	-15.45V	L	V_{OL}
15V	900mV	15.45V	14.55V	L	
10V	20V	20V	0V	L	
12V	20V	22V	2V	L	
-15V	500mV	-14.75V	-15.25V	H	V_{OH}
15V	500mV	15.25V	14.75V	H	
-10V	-20V	-20V	0V	H	
-12V	-20V	-22V	-2V	H	
X	X	Open	Open	H	

Table 2. Receiver Functions

RECEIVER ⁽¹⁾	
DIFFERENTIAL INPUTS	OUTPUT R
$V_{ID} \geq 0.9V$	L
$0.5V < V_{ID} < 0.9V$	?
$V_{ID} \leq 0.5V$	H
Open	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

Table 3. Driver Functions

DRIVER ⁽¹⁾			
INPUT D	OUTPUTS		BUS STATE
	CANH	CANL	
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

(1) H = high level; L = low level; Z = high impedance

7 Application and Implementation

7.1 Application Information

This application section provides information concerning the implementation of the physical medium attachment layer in a CAN network according to the ISO 11898 standard. It presents a typical application circuit and test results, as well as discussions on total loop delay, and interoperability in 5V CAN systems.

7.2 CAN Bus States

The CAN bus has two states during powered operation of the device; dominant and recessive. A dominant bus state is when the bus is driven differently, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal resistors R_I and R_{Diff} of the receiver, corresponding to a logic high on the D and R pins. See [Figure 9](#) and [Figure 10](#).

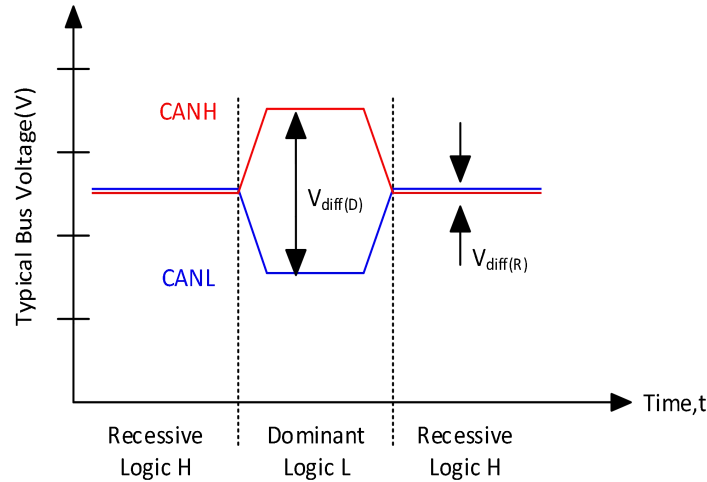


Figure 9. CAN Bus States (Physical Bit Representation)

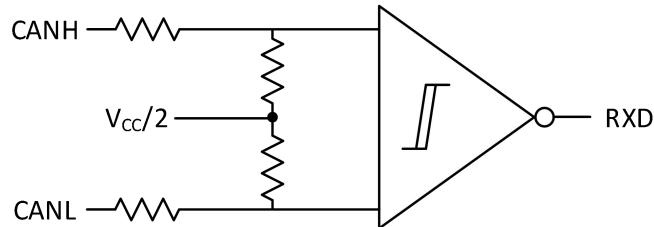


Figure 10. Simplified Recessive Common Mode Bias and Receiver

7.3 Typical Application

Figure 11 illustrates a typical application of the HMT232TK. The output of the host μP 's CAN controller (TXD) is connected to the transceivers driver input, pin D, and the transceivers receiver output, pin R, is connected to the input of the CAN controller (RXD). The transceiver is attached to the differential bus lines at pins CANH and CANL. Typically, the bus is a twisted pair of wires with a characteristic impedance of 120Ω , in the standard half-duplex multi point topology of Figure 12. Each end of the bus is terminated with 120Ω resistors in compliance with the standard to minimize signal reflections on the bus.

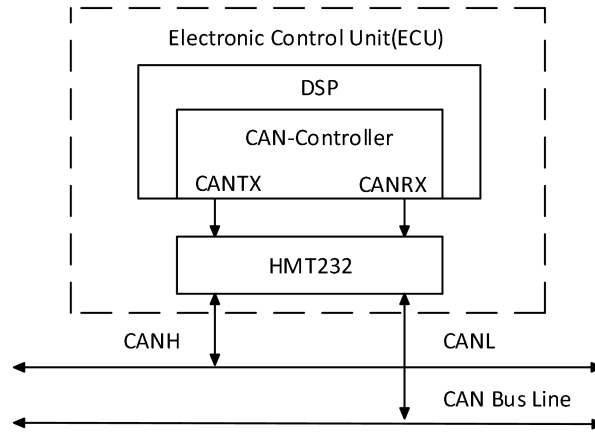


Figure 11. Details of a Typical CAN Node

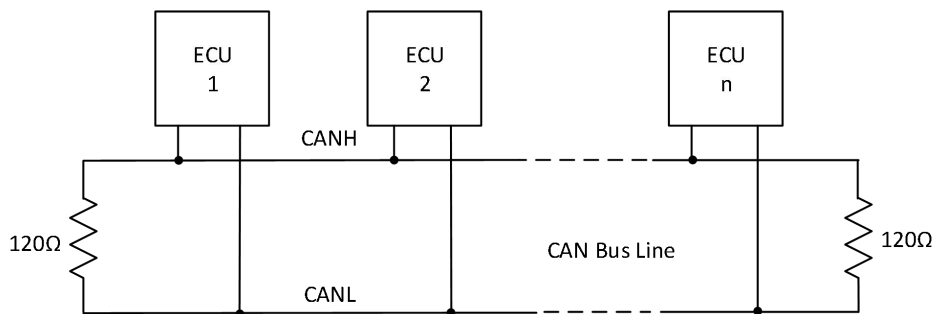


Figure 12. Typical CAN Network

7.3.1 CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_0). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

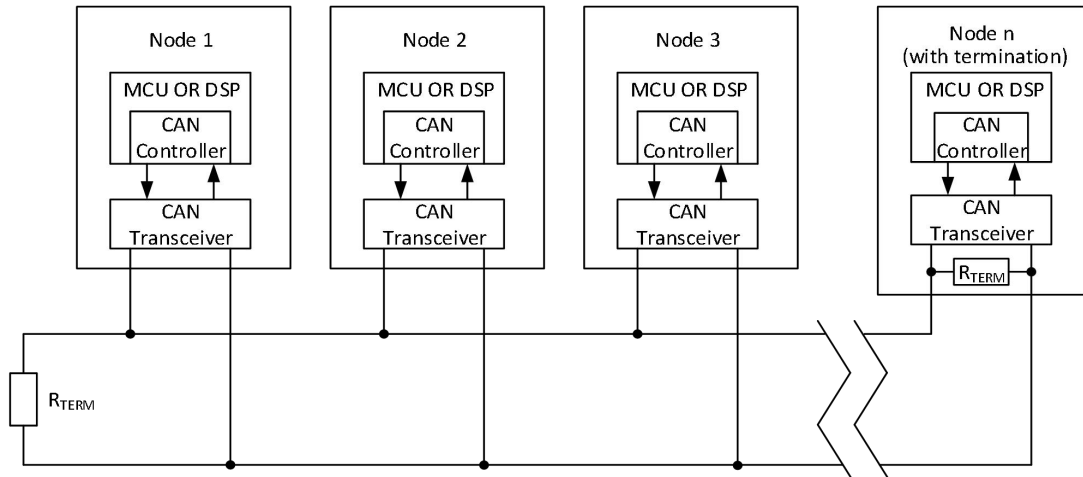


Figure 13. Typical CAN Bus

Termination is typically a 120 Ω resistor at each end of the bus. If filtering and stabilization of the common mode Voltage of the bus is desired, then split termination may be used (see Figure 14). Split termination utilizes two 60 Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode Voltages at the start and end of message transmissions. Care should be taken in the power ratings of the termination resistors used. Typically the worst case condition would be if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition would be much higher than the transceiver's current limit.

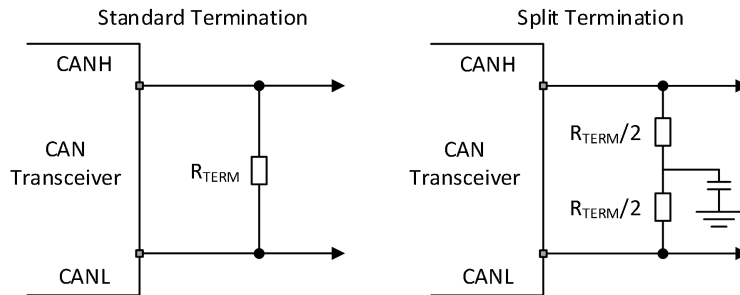


Figure 14. CAN Termination

7.3.2 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (D pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs (CANH and CANL) to its output (R pin). A typical loop delay for the HMT232TK transceiver is displayed in [Figure 15](#).

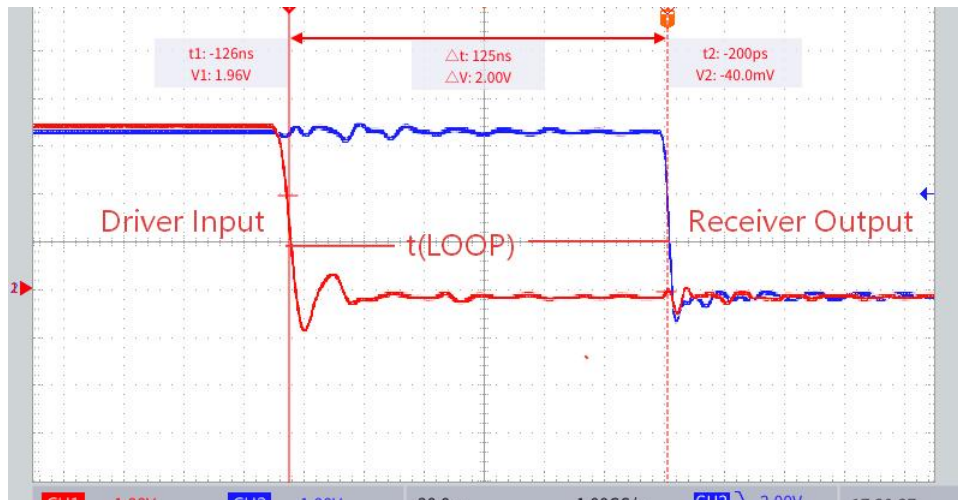


Figure 15. 122ns Loop Delay Through the HMT232TK

7.3.3 Bus Loading, Length and Number of Nodes

In classic CAN per ISO 11898-2, the bus supports up to 1 Mbps, with a maximum bus length of 40 m, a maximum stub length of 0.3 m and a maximum of 32 nodes. In CAN FD (data phase up to 5 Mbps), the bus length, stub length and node count must be derated due to the shorter bit time at 5 Mbps; see Section "Bus Loading, Length and Number of Nodes" for the FD limits. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CAN open, CAN kingdom, Device Net and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the HMT232TK. ISO11898-2 specifies the driver differential output with a 60Ω load (two 120Ω termination resistors in parallel) and the differential output must be greater than 1.5V. The HMT232TK device is specified to meet the 1.5V requirement with a 60Ω load, and additionally specified with a differential output Voltage minimum of 1.2V across a common mode range of -2V to 7V Via a 167 Ω coupling network. This network represents the bus loading of 120 HMT232TK transceivers based on their minimum differential input resistance of 40kΩ. Therefore, the HMT232TK supports up to 120 transceivers on a single bus segment with margin to the 1.2V minimum differential input Voltage requirement at each node. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loading, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO11898 standard of 40 meters by careful system design and data rate trade offs. For example, CAN open network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate. This flexibility in CAN network design is one of the key strengths of the Various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design.

7.3.4 Detailed Design Procedure

The following system level considerations should be looked at when designing your application. There are trade- offs between the total number of nodes, the length of the bus that need to be evaluated when building up a system.

7.3.5 Transient Protection

Typical applications that use CAN will sometime require some form of ESD, burst, or surge protection performance at the system level. If these requirements are higher than those of the device some form of external protection may be needed to shield the transceiver against these high power transients that can cause damage. Transient Voltage suppressor (TVS) are Very commonly used and can help clamp the amount of energy that reaches the transceiver.

7.3.6 Transient Voltage Suppressors

Transient Voltage suppressors are the preferred protection components for CAN bus applications due to their low capacitance, fast response times and high peak power dissipation limits. The low bus capacitance allows these devices to be used at many, if not all, nodes on the network without having to reduce the data rate. The quick response times in the order of a few picoseconds enable these devices to clamp the energy of Very fast transients like ESD and EFT. Lastly, the high peak power ratings enable these devices to handle high energy surge pulses without being damaged.

7.4 System Example

7.4.1 Introduction

Many users Value the low power consumption of operating their CAN transceivers from a 3.3V supply. However, some are concerned about the interoperability with 5V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

7.4.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the Voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this Voltage difference and outputs the bus state with a single-ended output signal.

The CAN driver creates the differential Voltage between CANH and CANL in the dominant state. The dominant differential output of the HMT232TK is greater than 1.5V and less than 3V across a 60 ohm load as defined by the ISO 11898 standard. These are the same limiting Values for 5V supplied CAN transceivers. Typically, the bus termination resistors drive the bus back to the recessive bus state and not the CAN driver. A CAN receiver is required to output a recessive state when less than 500mV of differential Voltage exists on the bus, and a dominant state when more than 900mV of differential Voltage exists on the bus. The CAN receiver must do this with common-mode input Voltages from -15V to 15Volts per the ISO 11898-2 standard. The HMT232TK receiver meets these same input specifications as 5V supplied receivers.

7.4.3 Common Mode Signal

A common-mode signal is an average Voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Since the bias Voltage of the recessive state of the device is dependent on V_{CC} , any noise present or Variation of V_{CC} will have an effect on this bias Voltage seen by the bus. The HMT232TK has the recessive bias Voltage set higher than $0.5V_{CC}$ to comply with the ISO 11898-2 CAN standard which states that the recessive bias Voltage must be between 2V and 3V. The caveat to this is that the common mode Voltage will drop by a couple hundred milli volts when driving a dominant bit on the bus. This means that there is a common mode shift between the dominant bit and recessive bit states of the device. While this is not ideal, this small Variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

7.4.4 Interoperability of 3.3V CAN in 5V CAN Systems

The 3.3V supplied HMT232TK CAN transceiver is fully compatibles with 5V CAN transceivers. The differential output Voltage is the same, the recessive common mode output bias is the same, and the receivers have the same input specifications. The only difference is in the dominant common mode output Voltage is lower in 3.3V CAN transceivers than with 5V supplied transceiver (by a few hundred milli volts).

To help ensure the widest interoperability possible, the HMT232TK has successfully passed the internationally recognized GIFT ICT conformance and interoperability testing for CAN transceivers which is shown in [Figure 13](#). Electrical interoperability does not always assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. This comes only with thorough equipment testing.

8 Power Supply Recommendations

The HMT232TK 3.3V CAN transceiver provides the interface between the 3.3V μ Ps, MCUs and DSPs and the differential bus lines, and are designed to transmit data at signaling rates up to 5Mbps backward compatible with classic CAN (≤ 1 Mbps) as defined by the ISO 11898-2 standard.

To ensure reliable operation at all data rates and supply Voltages, the V_{CC} supply pin of each CAN transceiver should be decoupled with a 100nF ceramic capacitor located as close to the V_{CC} and GND pins as possible.

9 Layout

9.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system. Use V_{CC} and ground planes to provide low inductance. Note: high frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bi-directional diode or Varistor solution) and bus filter capacitors C8 and C9 are shown in Figure 16.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 16 shows split termination. This is where the termination is split into two resistors, R7 and R8, with the center or split tap of the termination connected to ground Via capacitor C7. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues of the bus is not properly terminated on both ends. See the application section for information on power ratings needed for the termination resistor(s). Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}). Use at least two Vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and Via inductance. To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4. To filter noise on the digital I_O lines, a capacitor may be used close to the input side of the I_O as shown by C1 and C4. Since the internal pull up and pull down biasing of the device is weak for floating pins, an external 1k to 10k ohm pull-up or down resistor should be used to bias the state of the pin more strongly against noise during transient events. Pin 1: If an open drain host processor is used to drive the D pin of the device an external pull-up resistor between 1k and 10k ohms should be used to drive the recessive input state of the device (R1). For the HMT232TK, pins 5 and 8 are No Connect (NC). These pins are not internally connected and can be left floating. Do not connect any resistors or capacitors to these pins.

9.2 Layout Example

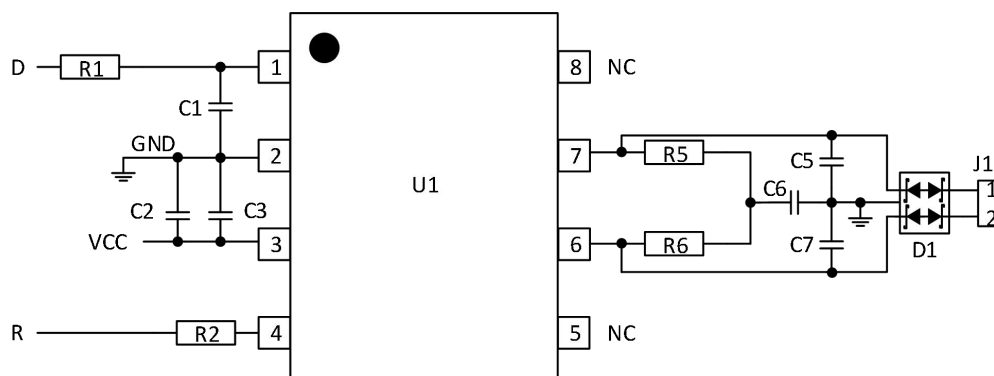
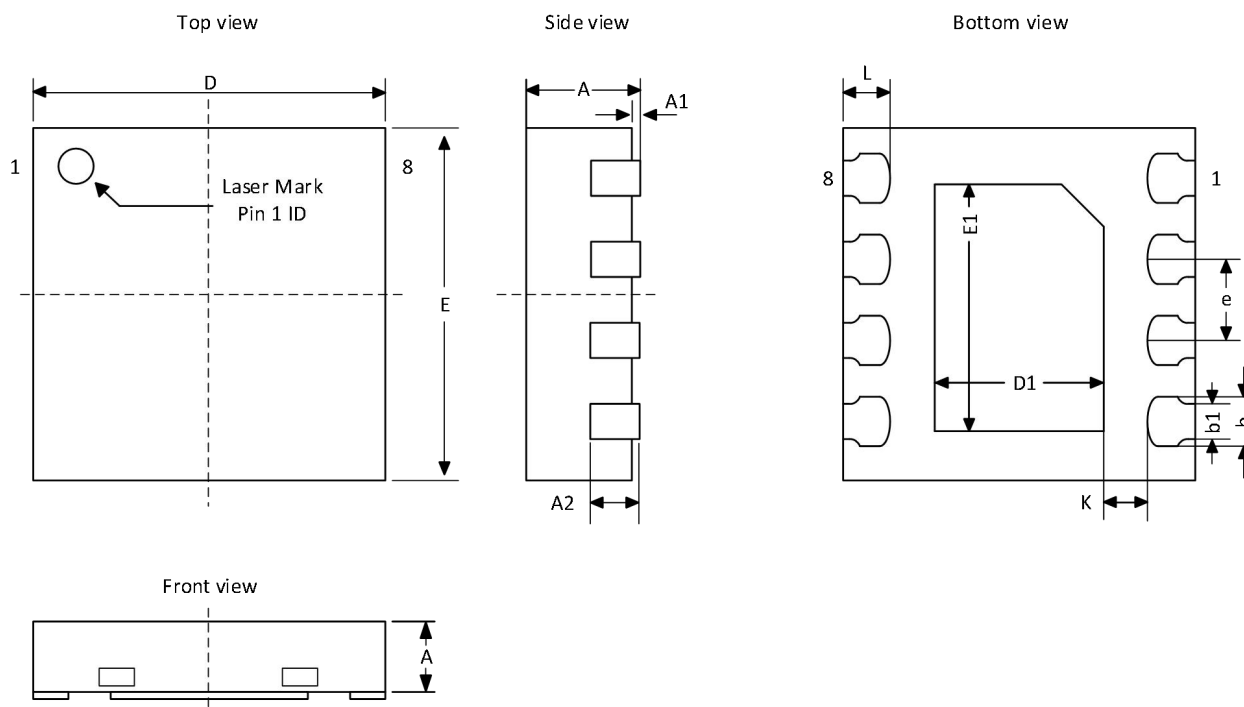


Figure 16. Layout Example Schematic

PACKAGING DIMENSION

DFN8-EP(2x2)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
b1	0.18 REF.		
D	1.90	2.00	2.10
D1	0.60	0.70	0.80
E	1.90	2.00	2.10
E1	1.10	1.20	1.30
e	0.50 BSC		
k	0.35 REF.		
L	0.20	0.30	0.40

Order Information

Order number	Package	Marking information	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
HMT232TK	DFN8-EP(2x2)	HMT232TK	-40 to 125°C	3	T&R, 3000	RoHs

VERSION MODIFICATION RECORD

VERSION	MODIFY THE DESCRIPTION	PAGE	TIME	MODIFY PERSONNEL
1.1	1.Original:HMT232TK_1.0 →HMT232TK_1.1		2026-10-16	KANG
	2.Updated the bus common-mode range:-2V to +7V → -15V to +15V.	1,3,4,13		
	3.modified the test conditions of V_{OH} , V_{OL} , I_L .	4		
	4.Updated the receiver functions table.	8		