MP2795

7-Cell to 16-Cell, High-Performance Battery Monitor and Protector with High-Side Driver

DESCRIPTION

The MP2795 is a robust battery management device, providing a complete analog front-end (AFE) monitoring and protection solution. It is designed for multiple-cell series battery management systems (BMS). The device can support I²C or SPI communication. It supports connections for 7-cell to 16-cell series battery packs, with an absolute voltage exceeding 80V on particular pins.

The MP2795 integrates two separate analog-to-digital converters (ADCs). The first ADC measures each channel's differential cell voltages (up to 16 channels), die temperature, and 4-channel temperatures via external NTC thermistors. The second ADC measures the charge/discharge current via an external current-sense resistor. The dual ADC architecture enables synchronous voltage and current measurements for pack impedance monitoring.

When paired with an MPF4279x fuel gauge, the MP2795 can achieve a state-of-charge (SOC) error to within 2%.

The MP2795 includes high-side MOSFET (HS-FET) drivers for charge and discharge control. The discharge (DSG) MOSFET driver includes a configurable soft start (SS) that provides a controlled turn-on, eliminating the need for an external pre-charge circuit. The MOSFET drivers also incorporate over-current protection (OCP), short-circuit protection (SCP), battery under-voltage protection (UVP), battery over-voltage protection (OVP), and high-/low-temperature protection. All of these protections have configurable thresholds.

Internal passive balancing MOSFETs can be used to equalize mismatched cells, supporting up to 58mA. There is also the option to drive external balancing transistors (MOSFET or BJT).

The MP2795 is available in a TQFP-48 (7mmx7mm) package.

FEATURES

- Incorporates Dual ADC Architecture:
  - <±2% State-of-Charge (SOC) Error with MPF4279x Fuel Gauge
  - Cell Voltage Measurement Error <5mV
  - Current/Coulomb Counter Error <±0.5%
  - Strictly Synchronized Current/Voltage Measurement for Impedance Sensing
- Includes High-Side N-Channel MOSFET Drivers for Charge and Discharge Control:
  - Supports MOSFET Soft-Start Discharge Control to Eliminate Pre-Charge Circuit
  - Drives Up to 100A DC with Parallel N-Channel MOSFETs
- Hardware-Configurable Protections:
  - Charge/Discharge OCP and SCP
  - Cell or Pack UVP and OVP
  - Cell Low-/High-Temperature Protection
  - Die High-Temperature Protection
- Passive Cell Balancing Up to 58mA/Cell:
  - Can Drive External Balancing Transistors
  - Automatic or Manual Control
- Additional Features:
  - Integrated 3.3V and 5V LDOs
  - Reduced Current Standby Mode
  - Load and Charger Plug-In Detection
  - Low-Voltage GPIOs
  - Dedicated Thermistor Inputs
  - Open-Wire Detection
  - Persistent Dead Battery Flag
  - Lockable Multiple-Time Programmable (MTP) Memory for Key Thresholds
- I²C Interface or SPI with 8-Bit CRC
- Random Cell Connection Tolerant
- Available in a TQFP-48 (7mmx7mm) Package

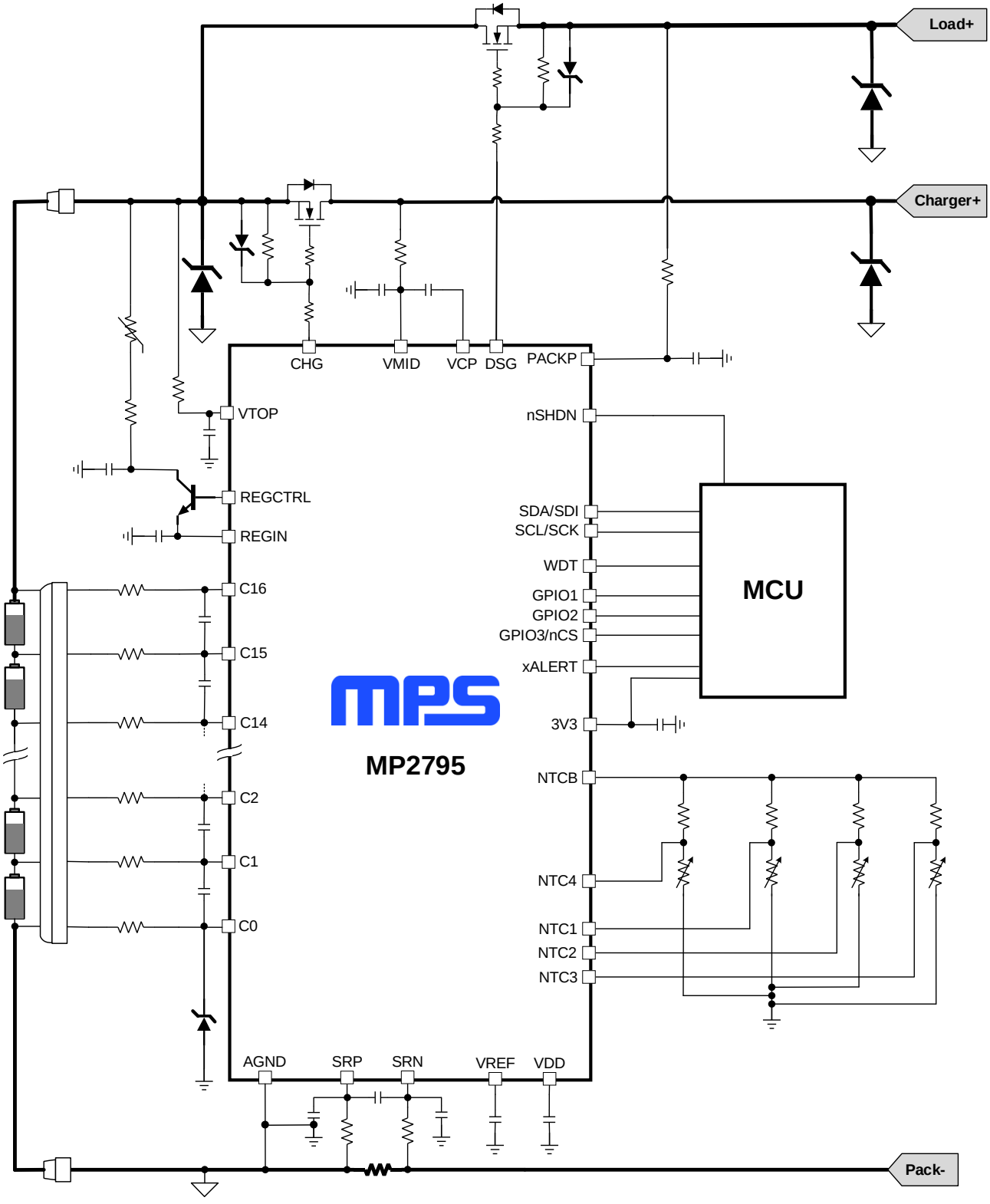
APPLICATIONS

- Energy Storage Systems (ESS)
- E-Bikes and E-Scooters
- Light Electric Vehicles (LEVs)
- Power and Gardening Tools
- Battery Backups and UPS

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating	Communication
MP2795DFP-xxxx**	TQFP-48 (7mmx7mm)	*See Below*	3	-
MP2795DFP-0000	TQFP-48 (7mmx7mm)	*See Below*	3	I^2C, CRC disabled
MP2795DFP-0001	TQFP-48 (7mmx7mm)	*See Below*	3	I^2C, CRC enabled
MP2795DFP-0002	TQFP-48 (7mmx7mm)	*See Below*	3	SPI, CRC disabled

* For Tray, add suffix -T (e.g. MP2795DFP-xxxx-T).

* For Tape & Reel, add suffix -Z (e.g. MP2795DFP-xxxx-Z).

** "xxxx" is the configuration code identifier for the register settings. Each "x" can be a hexadecimal value between 0 and F. The default codes are "0000", "0001", and "0002". Contact an MPS FAE to create this unique number.

TOP MARKING (MP2795)

MPSYYWW
MP2795
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2795: Part number
LLLLLLLLL: Lot number

EVALUATION KIT EVKT-MP2795-0000

EVKT-MP2795-0000 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2795-0000-FP-00A	MP2795DFP-0000 I^2C evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB-to-I^2C communication kit, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

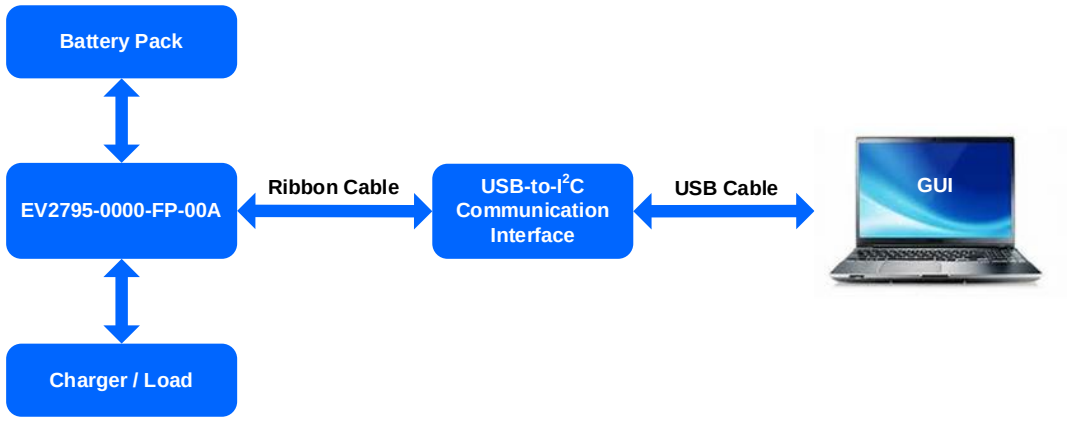
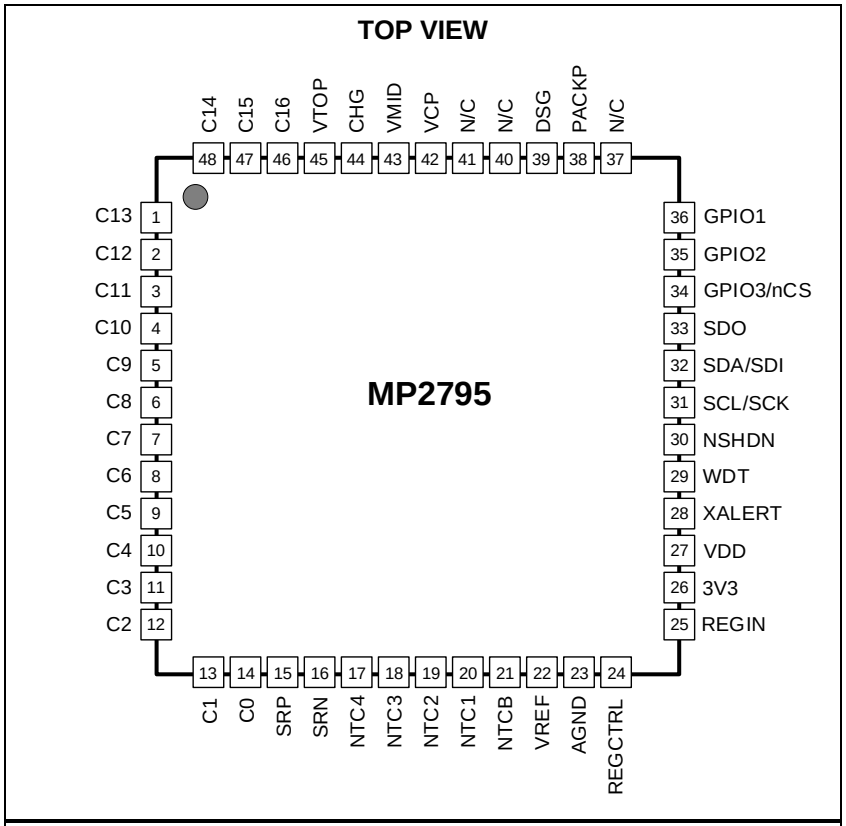


Figure 1: EV2795-0000-FP-00A Evaluation Kit Set-Up

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PACKAGE REFERENCE



TQFP-48 (7mmx7mm)

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PIN FUNCTIONS

Pin #	Name	Type	Description
26	3V3	P	**3.3V voltage output to drive external peripherals.** Bypass the 3V3 pin using an external 1µF capacitor.
23	AGND	P	**Ground.** Connect the AGND pin near the positive connection (SRP) of the low-side sense resistor.
45	VTOP	P	**Battery-side pack-sensing voltage and low-current positive supply.** The VTOP pin must be connected to the top of the battery stack, which is the highest positive voltage in the battery pack.
46	C16	I	**Connect to the positive pin of cell 16.**
47	C15	I	**Connect to the positive pin of cell 15.**
48	C14	I	**Connect to the positive pin of cell 14.**
1	C13	I	**Connect to the positive pin of cell 13.**
2	C12	I	**Connect to the positive pin of cell 12.**
3	C11	I	**Connect to the positive pin of cell 11.**
4	C10	I	**Connect to the positive pin of cell 10.**
5	C9	I	**Connect to the positive pin of cell 9.**
6	C8	I	**Connect to the positive pin of cell 8.**
7	C7	I	**Connect to the positive pin of cell 7.**
8	C6	I	**Connect to the positive pin of cell 6.**
9	C5	I	**Connect to the positive pin of cell 5.**
10	C4	I	**Connect to the positive pin of cell 4.**
11	C3	I	**Connect to the positive pin of cell 3.**
12	C2	I	**Connect to the positive pin of cell 2.**
13	C1	I	**Connect to the positive pin of cell 1.**
14	C0	I	**Connect to the negative pin of cell 1.**
44	CHG	O	**Charge MOSFET driver.**
39	DSG	O	**Discharge MOSFET driver.**
36	GPIO1	I/O	**General-purpose pin 1.**
35	GPIO2	I/O	**General-purpose pin 2.**
37	N/C		**Not connected.**
30	NSHDN	I	**Active-low shutdown input signal.**
20	NTC1	I	**Terminal of thermistor 1.**
19	NTC2	I	**Terminal of thermistor 2.**
18	NTC3	I	**Terminal of thermistor 3.**
17	NTC4	I	**Terminal of thermistor 4.**
21	NTCB	O	**Negative temperature coefficient (NTC) bias.**
40	N/C		**Not connected.**
38	PACKP	I/O	**Pack-sensing voltage (load side).**
24	REGCTRL	P	**Turn-on control for the external bipolar junction transistor (BJT) low-dropout (LDO) regulator.**
25	REGIN	P	**Internal regulator input.** Connect an external 3.3µF bypass capacitor between the REGIN and AGND pins.
41	N/C		**Not connected.**
29	WDT	I/O	**Watchdog timer.**
28	xALERT	O	**Interrupt alert output.**
16	SRN	I	**Negative sense.**
15	SRP	I	**Positive sense.**
42	VCP	P	**Charge pump regulated voltage.** Connect a 47nF capacitor between the VCP and VMID pins, then adjust the capacitance based on the number of parallel discharge (DSG) and charge (CHG) MOSFETs.
27	VDD	P	**1.8V rail for internal use.** Connect a 1µF bypass capacitor from VDD to AGND.
43	VMID	P	**Middle point of the protection MOSFET.**

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PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
22	VREF	P	**Analog-to-digital converter (ADC) reference voltage.**
34	GPIO3/nCS	I/O	**Multi-function pin.** This pin can be set as GPIO3, or it can be set for serial peripheral interface (SPI) cable selection.
31	SCL/SCK	I	**Multi-function pin.** This pin can be set as the I^2C interface clock or the SPI clock.
32	SDA/SDI	I/O	**Multi-function pin.** This pin can be set as the I^2C interface data or the SPI serial data input.
33	SDO	O	**SPI serial data output.**

ABSOLUTE MAXIMUM RATINGS (1)

CHG, DSG, VCP to AGND .....-0.3V to +100V
VTOP to AGND.....-0.3V to +86V
PACKP to AGND .....-0.5V to +86V
VMID to AGND.....-0.3V to +86V
Cx - C (x - 1) (x = 1 to 16) .....-0.3V to +9V
C16 to AGND .....-0.3V to +86V
Cn to AGND (n = 1 to 15) .....
..... -0.3V to (n - 1) x 5.375 +7V
C0 to AGND .....-0.5V to +5.7V
SRP, SRN to AGND.....-0.5V to +6V
VCP to VMID.....-0.3V to +20V
REGCTRL to AGND .....-0.3V to +15V
NSHDN to AGND.....-0.3V to +9V
VDD to AGND.....-0.3V to +2V
All other pins to AGND.....-0.3V to +6V
Junction temperature (T_J) .....150°C
Lead temperature.....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) (2)..... 1.5kV
Charged-device model (CDM) (3) 500V

Recommended Operating Conditions (4)

VTOP voltage.....18V to 75.2V
Cx - C (x - 1) (x = 1 to 16) (5) .....1V to 5V
C0 to AGND.....-0.25V to +0.3V
REGIN voltage.....4.5V to 5.5V
Operating temperature (T_J) ..... -40°C to +85°C
SRP to SRN.....-100mV to +100mV

Thermal Resistance (6)

Junction-to-ambient ($R_{\theta JA}$) ..... 46.6°C/W
Junction-to-case (top) ($R_{\theta JC_TOP}$)..... 14.5°C/W
Junction-to-board (top) ($R_{\theta JB_TOP}$) ..... 27.1°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Tested per ANSI/ESDA/JEDEC JS-001.
3) Tested per ANSI/ESDA/JEDEC JS-002.
4) The device is not guaranteed to function outside of its operating conditions.
5) The stack voltage must exceed 18V.
6) These values are provided using set-up conditions compliant with EIA/JESD51-2, 7, and 8.

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ELECTRICAL CHARACTERISTICS

16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
Supply Current and Leakage						
Total shutdown current	I_{VTOP_SHDN}	VTOP + REGIN current, NSHDN pin low, 3.3V off, T_A = 25°C		1		µA
		VTOP + REGIN current, NSHDN pin low, 3.3V off, T_A = -40°C to +85°C			2.5	µA
		VTOP + REGIN current, 3.3V on, NSHDN pin low, T_A = 25°C		13.5		µA
		VTOP + REGIN current, 3.3V on, NSHDN pin low, T_A = -40°C to +85°C			20	µA
Total safe state current	I_{VTOP_SAFE}	VTOP + REGIN current, communication interface enabled, safe state (all MOSFETs off), hardware monitoring off, plug-in detection disabled, T_A = 25°C		23		µA
		VTOP + REGIN current, communication interface enabled, safe state (all MOSFETs off), hardware monitoring off, plug-in detection disabled, T_A = -40°C to +85°C			30	µA
Cell leakage	I_{Cx_LEAK}	T_A = 25°C	-200		+200	nA
		T_A = -40°C to +85°C	-600		+600	nA
Supported Series Cells						
Supported cell number (7)	N_{CELL}		7		16	
VTOP supply voltage range	V_{TOP_SUPPLY}	T_A = -40°C to +85°C	18		75.2	V
VTOP under-voltage lockout (UVLO) threshold	V_{TOP_UVLO}	Falling edge, T_A = -40°C to +85°C	14.6	15.8	17	V
VTOP under-voltage (UV) hysteresis	$V_{TOP_UVLO_HYST}$	T_A = 25°C		1.15		V
		T_A = -40°C to +85°C	0.78		1.5	V
Current Sense						
Current analog-to-digital converter (ADC) conversion time	t_{IADC}	16 bits (15 bits + sign)		2		ms
SRP and SRN current ADC measurement range	$V_{SRP-SRN}$	T_A = -40°C to +85°C	-100		+100	mV
Current ADC measurement gain error	$I_{ADC_GAIN_ERR}$	16-bit conversion, FSR = 100mV, SRP and SRN common mode: +300mV to -125mV from ground, T_A = 25°C	-0.75		+0.75	%
		16-bit conversion, FSR = 100mV, SRP and SRN common mode: +300mV to -125mV from ground, T_A = -40°C to +85°C	-1		+1	%

Note:

7) Guaranteed by design.

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ELECTRICAL CHARACTERISTICS *(continued)*

16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
Current-sense offset (8)	$V_{IADC_ACC_OFFSET}$	SRP - SRN = 0V, SRP and SRN common mode: +300mV to -125mV from ground, T_A = -40°C to +85°C	-12		+12	µV
SRP and SRN leakage	I_{SRPN_LEAK}	I_{ADC} not running, T_A = -40°C to +85°C	-500		+500	nA
SRP and SRN differential input current	I_{SRPN_DIFF}	I_{ADC} running, |SRP - SRN| = 100mV, absolute value, T_A = -40°C to +85°C		0.5		µA
		I_{ADC} running, |SRP - SRN| < 5mV, T_A = -40°C to +85°C		50		nA
Analog-to-Digital Converter (ADC) Sigma Delta Voltage						
ADC voltage conversion time	t_{VADC}	15 bits, T_A = 25°C		2		ms
Cell Voltage Measurement						
ADC cell measurement range	V_{CELL}	T_A = -20°C to +65°C	1		5	V
Total cell measurement error (9)	V_{CELL_ERR}	V_{CELL} = 1V to 4.5V, T_A = 25°C	-5		+5	mV
		V_{CELL} = 1V to 4.5V, T_A = -20°C to +65°C	-10		+10	mV
C0 to AGND voltage	$V_{C0_TO_AGND}$	C0 to AGND voltage drop resulting in less than 15mV error on cell 1, T_A = -20°C to +65°C	-0.25			V
ADC cell input current	$I_{IN_CELL_CONV}$	Input current during ADC conversion when V_{CELL} = 5V and T_A = 25°C, cell 1 is measured by the C1 to C0 voltage		1.2		µA
Die Temperature						
Die temperature operating range	T_{DIE}		-40		+85	°C
Over-temperature (OT) analog shutdown threshold	T_{DIE_OTSD}			140	155	°C
Negative Temperature Coefficient (NTC) Temperature Measurement						
NTC voltage measurement range	V_{NTC}	Nominal NTC range within a percentage of NTCB, T_A = 25°C	0		100	%
NTC total measurement error	V_{NTC_ERR}	15-bit conversion, NTCB = 3.3V, T_A = -40°C to +85°C	-55		+55	LSB

Notes:

8) The current measurement offset error is specified after completion of post-PCB assembly calibration. Contact an MPS FAE for the related application note.
9) No calibration required. The error can be further reduced by post-PCB assembly calibration. Contact an MPS FAE for the related application note.

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ELECTRICAL CHARACTERISTICS *(continued)*

16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
NTCx input leakage	$I_{NTC_IN_LEAK}$	ADC off, on each NTC pin, T_A = -40°C to +85°C			250	nA
NTCx input leakage with ADC on	$I_{NTC_LEAK_CONV}$	ADC converting NTCx, on each NTC pin, T_A = 25°C			250	nA
VTOP Measurement						
VTOP measurement range	V_{TOP}	T_A = -40°C to +85°C	18		75.2	V
VTOP total measurement error	V_{TOP_ERR}	15-bit conversion (positive range), T_A = -40°C to +85°C	-250		+250	mV
PACKP Measurement						
Pack measurement range	V_{PACKP}	T_A = -40°C to +85°C	2.5		75.2	V
Pack total measurement error	V_{PACKP_ERR}	15-bit conversion (positive range), T_A = -40°C to +85°C	-250		+250	mV
GPIO Measurement						
GPIO measurement range	V_{GPIO}	T_A = 25°C	0		3.3	V
GPIO total measurement error	V_{GPIO_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
GPIO input current during ADC reading	$I_{GPIO_CONV_IN}$	Input current of the GPIO pins during ADC conversion, T_A = -40°C to +85°C		1		µA
Regulators Measurements						
REGIN measurement error	V_{REGIN_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
3V3 total measurement error	V_{3V3_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
VDD total measurement error	V_{VDD_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
Hardware Protection						
Cell over-voltage (OV) and UV steps	$V_{CELL_TH_STEP}$			19.5		mV
Cell OV/UV step accuracy	$V_{CELL_TH_ACC}$	V_{CELL} = 2V to 4.5V, T_A = 0°C to 60°C	-19.5		+19.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-40		+40	mV

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ELECTRICAL CHARACTERISTICS *(continued)*

16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
Pack OV/UV steps	$V_{PACK_TH_STEP}$			19.5		mV
Deep discharge steps	V_{DEEPTH_STEP}			19.5		mV
Deep discharge step accuracy	$V_{DEEPTH_STEP_ACC}$	V_{CELL} = 2V to 4.5V, T_A = 0°C to 60°C	-19.5		+19.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-40		+40	mV
Short circuit fastest detection time	$t_{SC_DGL_MIN}$	Fastest deglitch setting and latency, T_A = -40°C to +85°C			120	µs
Discharge over-current protection (OCP) threshold 1 (OC1) discharge full-scale range (FSR) value	$V_{OC1_DSG_FSR_1X}$	Range and least significant bit (LSB) selector = 0 (1x), FSR (max setting), T_A = 25°C		80		mV
OC1 discharge FSR accuracy	$V_{OC1_DSG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
OC1 discharge offset	$V_{OC1_DSG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on LSB, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC1 discharge FSR value	$V_{OC1_DSG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = 25°C		240		mV
OC1 discharge FSR accuracy	$V_{OC1_DSG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
OC1 discharge offset	$V_{OC1_DSG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
Discharge OCP threshold 2 (OC2) discharge FSR value	$V_{OC2_DSG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = 25°C		80		mV
OC2 discharge FSR accuracy	$V_{OC2_DSG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
OC2 discharge offset	$V_{OC2_DSG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC2 discharge FSR value	$V_{OC2_DSG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		240		mV
OC2 discharge FSR accuracy	$V_{OC2_DSG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
OC2 discharge offset	$V_{OC2_DSG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC charge FSR value	$V_{OC_CHG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = 25°C		51.2		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
Over-current (OC) charge FSR accuracy	$V_{OC_CHG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
OC charge offset	$V_{OC_CHG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC charge FSR value	$V_{OC_CHG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = 25°C		153		mV
OC charge FSR accuracy	$V_{OC_CHG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
OC charge offset	$V_{OC_CHG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
Short-circuit discharge FSR value	$V_{SC_DSG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = 25°C		176		mV
Short-circuit discharge FSR accuracy	$V_{SC_DSG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
Short-circuit discharge offset	$V_{SC_DSG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
Short-circuit discharge FSR value	$V_{SC_DSG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = 25°C		528		mV
Short-circuit discharge full-scale accuracy	$V_{SC_DSG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
Short-circuit discharge offset	$V_{SC_DSG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-2		+2	mV
Short-circuit charge FSR value	$V_{SC_CHG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = 25°C		80		mV
Short-circuit charge FSR accuracy	$V_{SC_CHG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%
Short-circuit charge offset	$V_{SC_CHG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
Short-circuit charge FSR value	$V_{SC_CHG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = 25°C		240		mV
Short-circuit charge FSR accuracy	$V_{SC_CHG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (maximum setting), T_A = -40°C to +85°C	-15		+15	%

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ELECTRICAL CHARACTERISTICS *(continued)*

16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
Short-circuit charge offset	$V_{SC_CHG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
Cell-Balancing						
On resistance for the balancing MOSFET	$R_{DS(ON)_BAL_FET}$	T_A = 25°C		28		Ω
Open-Wire Detection						
Open-wire pull-up current	I_{OW_PUP}	T_A = 25°C		100		µA
Open-wire pull-down current	I_{OW_PD}	T_A = 25°C		100		µA
Low-Dropout (LDO) Regulator Supply and References						
REGCTRL output voltage	$V_{REGCTRL}$	V_{TOP} = 18V to 75.2V, REGCTRL load current = 0mA to 1mA, T_A = -40°C to +85°C	5.45	5.6	5.75	V
REGIN voltage (10)	V_{REGIN}	With external REGIN bipolar junction transistor (BJT) (FZT853TA), V_{TOP} = 18V to 75.2V, load current = 1mA to 50mA, T_A = -40°C to +85°C	4.65	5.1	5.4	V
REGIN analog UV	V_{REGIN_UV}	External power to REGIN, falling edge, V_{TOP} = 18V to 75.2V, T_A = -40°C to +85°C	4.16	4.3	4.44	V
3V3 nominal voltage	V_{3V3}	T_A = 25°C		3.3		V
3V3 output accuracy	V_{3V3_ACC}	T_A = -40°C to +85°C	-5		+5	%
3V3 short-circuit current	I_{3V3_EFET}	External power to REGIN, T_A = -40°C to +85°C	55	68	80	mA
VDD output voltage	V_{DD}	T_A = 25°C		1.8		V
Reference voltage	V_{REF}	T_A = 25°C		3.3		V
NTCB pull-up voltage	V_{NTCB}	NTCB enabled, no load, T_A = 25°C		3.3		V
NTCB load	$I_{NTCB_MAXLOAD}$	NTCB enabled, maximum load, T_A = 25°C		4		mA
		NTCB enabled, maximum load, T_A = -40°C to +85°C	3.2		4.8	mA
3V3 analog UV	V_{3V3_UV}	Falling edge		2.85		V
GPIO						
GPIO input voltage (high)	V_{IH_GPIO}	Voltage high (V_H) = 3.3V or 5V, T_A = -40°C to +85°C	0.8 x V_H		V_H	V
GPIO input voltage (low)	V_{IL_GPIO}	V_H = 3.3V or 5V, T_A = -40°C to +85°C	0		0.2 x V_H	V
GPIO output voltage (high)	V_{OH_GPIO}	V_H = 3.3V or 5V, I_{SOURCE} = 1.5mA, T_A = -40°C to +85°C	V_H - 0.5		V_H	V

Note:

10) Guaranteed by design. The REGIN pin voltage (V_{REGIN}) is limited by the REGCTRL output voltage ($V_{REGCTRL}$) and is equal to the difference between $V_{REGCTRL}$ and the voltage between base and emitter of the BJT (V_{BE_ON}).

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ELECTRICAL CHARACTERISTICS *(continued)*

16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
GPIO low output voltage	V_{OL_GPIO}	V_H = 3.3V or 5V, I_{SINK} = 1.5mA, T_A = -40°C to +85°C	0		0.4	V
GPIO push-pull resistor (pull-up)	R_{GPIO_PUP}	GPIO high voltage = 3.3V, external power to REGIN		430		Ω
GPIO push-pull resistor (pull-down)	R_{GPIO_PDOWN}	GPIO low voltage = 0V		110	200	Ω
GPIO pull-up mode	$R_{GPIO_WEAK_PUP}$			17		kΩ
NSHDN Pin						
NSHDN internal pull-down	R_{SHDN_PD}	NSHDN = 0V to 5V		5		MΩ
NSHDN configuring voltage	V_{NSHDN_PROG}		7.5	7.6	7.7	V
NSHDN deglitch to enter shutdown	$t_{NSHDN_DGL_ENTER}$	T_A = 25°C, IC remains in safe mode for longer than $t_{NSHDN_DGL_ACTIVE}$		8		ms
NSHDN deglitch active time	$t_{NSHDN_DGL_ACTIVE}$	T_A = 25°C		4		ms
NSHDN falling threshold	V_{NSHDN_FALL}			1		V
NSHDN rising threshold	V_{NSHDN_RISE}	3V3 enabled in shutdown mode		2.65		V
		3V3 disabled in shutdown mode		2		V
WDT Pin						
Reset pulse length	$t_{WDT_RSTPULSE_LEN}$			10		ms
High-Side MOSFET (HS-FET) Drive						
CHG gate drive voltage	V_{CHG}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 75.2V, V_{GS} = 10V, T_A = 25°C		10		V
CHG gate drive voltage accuracy	V_{CHG_ACC}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 75.2V, 10V selected, T_A = -40°C to +85°C	9.3		10.7	V
CHG gate drive turn-on resistance	R_{CHG_ON}	MOSFET drive turned on, PACKP = V_{TOP}, T_A = 25°C		2600		Ω
CHG gate driver turn-off resistance	R_{CHG_OFF}	MOSFET driver turned off, PACKP = V_{TOP}, T_A = 25°C		840		Ω
DSG gate drive voltage	V_{DSG}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 75.2V, V_{GS} = 10V, T_A = 25°C		10		V
DSG gate driver voltage accuracy	V_{DSG_ACC}	C_{LOAD} = 80nF, static value at completed transition, V_{TOP} = 18V to 75.2V, 10V selected, T_A = -40°C to +85°C	9.3		10.7	V
DSG gate driver turn-on resistance	R_{DSG_ON}	MOSFET driver turned on, PACKP = V_{TOP}, T_A = 25°C		2600		Ω
DSG gate driver turn-off resistance	R_{DSG_OFF}	MOSFET driver turned off, PACKP = V_{TOP}, DSG = PACKP + 5V, T_A = 25°C		600		Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
Charge Pump						
Charge pump output voltage	V_{CP}	Gate driver voltage = 10V, regular control mode, T_A = 25°C		14.7		V
Charge pump output voltage accuracy	V_{CP_ACC}	Accuracy of selected VCP average value, T_A = -40°C to +85°C	-1		+1	V
Charge pump turn-on time	t_{CP_TON}	VCP - AGND transition from V_{TOP} to V_{TOP} + V_{CP}, 10nF capacitor on VCP, V_{TOP} = 21V, for both low-power mode (LPM) and regular control mode, T_A = -40 to +85°C			2	ms
Pull-Up Comparators						
PACKP charge	I_{PACKP_PUP}	V_{TOP} = 18V to 75.2V, T_A = 25°C		250		µA
PACKP discharge	I_{PACKP_PDOWN}	V_{TOP} = 18V to 75.2V, T_A = 25°C		250		µA
PACKP exceeds V_{TOP}	$V_{PACKP_HGR_VTOP}$	V_{TOP} = 18V to 75.2V, T_A = 25°C		280		mV
PACKP is below V_{TOP}	$V_{PACKP_LWR_VTOP}$	V_{TOP} = 18V to 75.2V, T_A = 25°C		-1.77		V
Standby comparator accuracy	$V_{SBY_COMP_ACCU}$	Offset on the smallest setting, T_A = 25°C	-125		+125	µV
PACKP short recovery threshold	$V_{PACKP_SCOC_REC_TH}$	T_A = 25°C		110		mV
Short recovery current source accuracy	I_{SCOC_PUP}	Offset on the smallest setting, T_A = 25°C	-50		+50	µA
Internal Clock						
Internal clock frequency	f_{2M_CLOCK}	V_{TOP} = 18V to 75.2V, T_A = 25°C		2		MHz
		V_{TOP} = 18V to 75.2V, T_A = -40°C to +85°C	1.85	2	2.15	MHz
Low-frequency internal clock	f_{32K_CLOCK}	V_{TOP} = 18V to 75.2V, T_A = 25°C	31.2	32	32.8	kHz
		V_{TOP} = 18V to 75.2V, T_A = -40°C to +85°C	30.7		33.3	kHz
I^2C Communication Interface						
I^2C clock frequency	f_{I2C}	T_A = 25°C			400	kHz
SCL or SDA low input voltage	V_{ILOW}	T_A = -40°C to +85°C			0.25 x 3V3	V
SCL or SDA high input voltage	V_{IHIGH}	T_A = -40°C to +85°C	0.7 x 3V3			V
SCL or SDA input hysteresis	V_{IHYST}	T_A = -40°C to +85°C		0.2 x 3V3		V

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ELECTRICAL CHARACTERISTICS *(continued)*

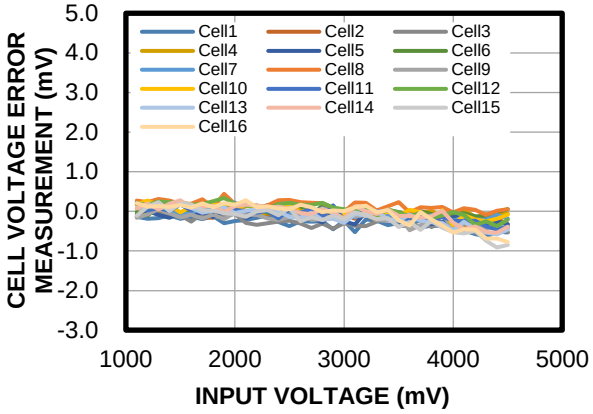
16 connected cells, where each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Conditions	Min	Typ	Max	Units
SPI Communication Interface						
SPI clock frequency	f_{SPI}	T_A = 25°C			1.0	MHz
SPI input low	$V_{SPI_IN_LOW}$	SDI, CLK, T_A = -40°C to +85°C			0.25 x 3V3	V
SPI input high	$V_{SPI_IN_HIGH}$	SDI, CLK, T_A = -40°C to +85°C	0.7 x 3V3			V
SDO high-side (HS) on resistance	$R_{SDS(ON)_SDO_DRV_HI}$	I_{SOURCE} = 1.5mA, T_A = -40°C to +85°C	75	100	125	Ω
SDO low-side (LS) on resistance	$R_{DS(ON)_SDO_DRV_LOW}$	I_{SINK} = 1.5mA, T_A = -40°C to +85°C	38	52	66	Ω

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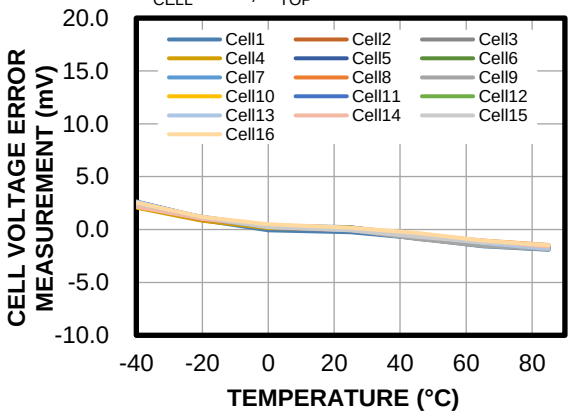
TYPICAL CHARACTERISTICS

Cell Voltage Error Measurement at 25°C vs. Input Voltage



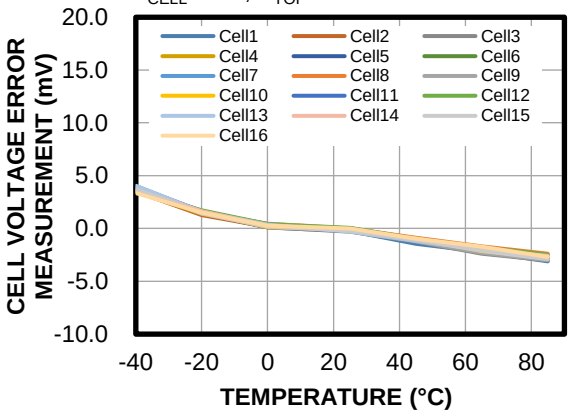
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 2V, V_{TOP} = 32V



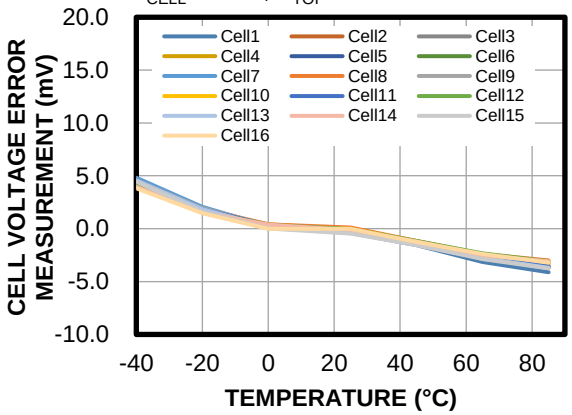
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 3V, V_{TOP} = 48V



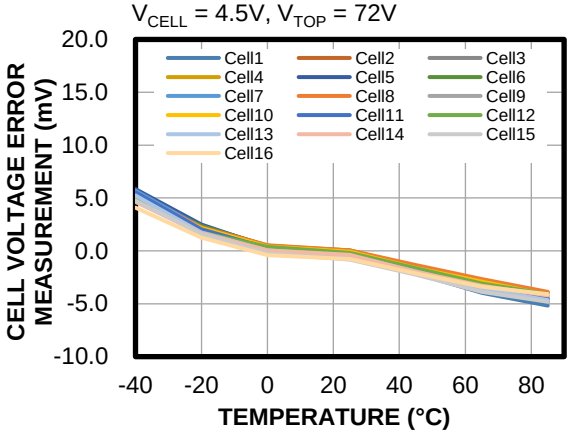
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 3.7V, V_{TOP} = 59.2V



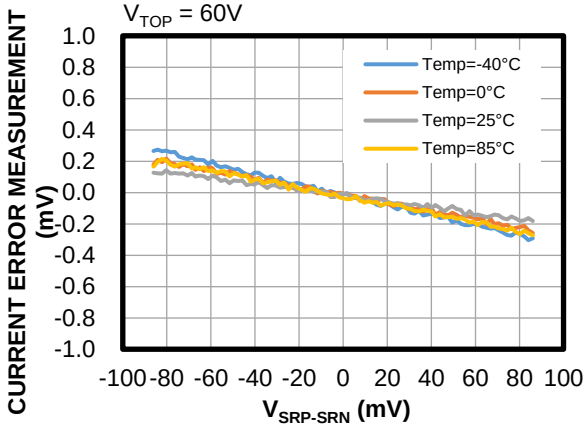
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 4.5V, V_{TOP} = 72V



Current Error Measurement vs. $V_{SRP-SRN}$

V_{TOP} = 60V



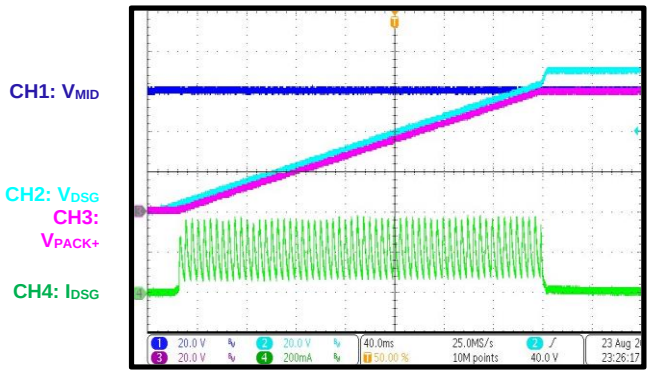
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TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

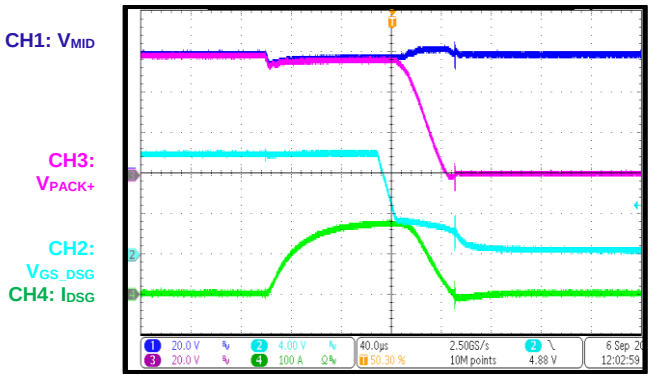
DSG Soft Start

PACK+ is connected to a 1mF capacitor, the DSG slope is 0.2V/ms



DSG Fast-Off during Short Circuit

$R_{SRP-SRN}$ = 1mΩ, short-circuit threshold is 99mV, deglitch off, 4 paralleled AM90N08-04BA devices act as the DSG N-channel MOSFETs, which has a typical C_{ISS} of 9924pF



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TYPICAL PERFORMANCE WHEN PAIRED WITH MPF4279X FUEL GAUGE

The MP2795 battery monitor includes strictly synchronized cell and pack voltage as well as current measurements for the purpose of maximizing state-of-charge (SOC) determination. MPS's MPF4279x family of fuel gauges are designed to take advantage of this feature. This section illustrates the SOC accuracy of the MP2795 battery monitor when combined with MPS's MPF4279x fuel gauge family.

Constant-Current/Constant-Voltage (CC/CV) Charge and Dynamic Discharge Cycle

The next scenarios consist of charging a 10S1P (11) battery using the typical CC/CV method, followed by a highly dynamic discharge at different ambient temperatures. The charge constant current rate is 1C, while the charge termination current in this example is 0.1C. The highly dynamic discharge corresponds to a typical e-bike's current profile, with an average current of 1C and maximum peak currents up to 2.8C. Figure 2 shows the current profile of the complete cycle at 25°C.

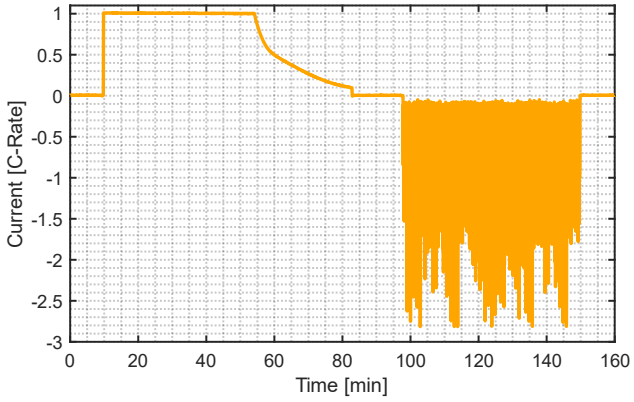


Figure 2: CC/CV Charge and Dynamic Discharge Current Profile

Figure 3 shows the performance of the combined MP2795 and MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 25°C. During charge, the root-mean-squared (RMS) (12) and maximum pack SOC error are 0.61% and 1.03%, respectively. During discharge, the RMS and pack SOC error are 0.78% and 1.94%, respectively.

Notes:

11) 10S1P refers to the battery configuration. There are 10 groups of 1 parallel cell connected in series.

12) The RMS error is equal to $\sqrt{\frac{\sum_{n=1}^{N}(\theta_n-\hat{\theta}_n)^2}{N}}$, where θ is the actual SOC, $\hat{\theta}$ is the estimated SOC, and *N* is the number of samples.

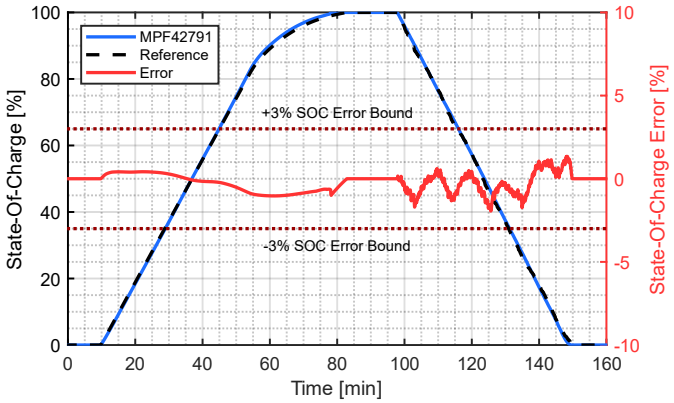


Figure 3: Combined MP2795 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 25°C)

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Figure 4 shows the performance of the combined MP2795 and MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 0°C. During charge, the RMS and maximum pack SOC error are 0.68% and 1.22%, respectively. During discharge, the RMS and pack SOC error are 1.15% and 2.97%, respectively.

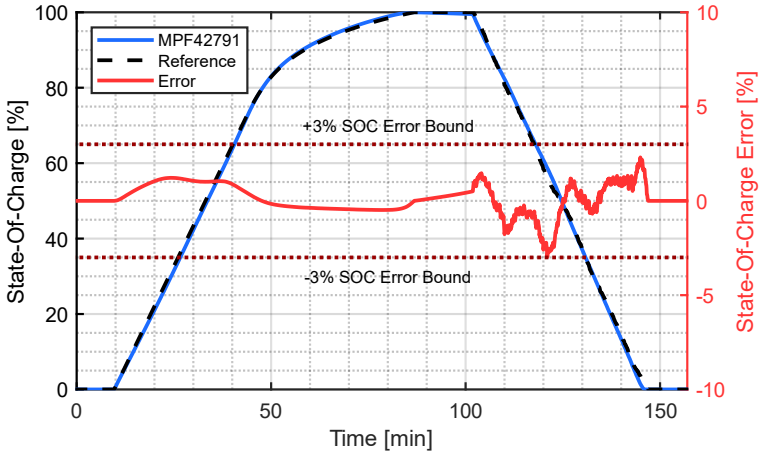


Figure 4: Combined MP2795 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 0°C)

Figure 5 shows the performance of the combined MP2795 and MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 40°C. During charge, the RMS and maximum pack SOC error are 0.40% and 0.60%, respectively. During discharge, the RMS and pack SOC error are 0.77% and 1.89%, respectively.

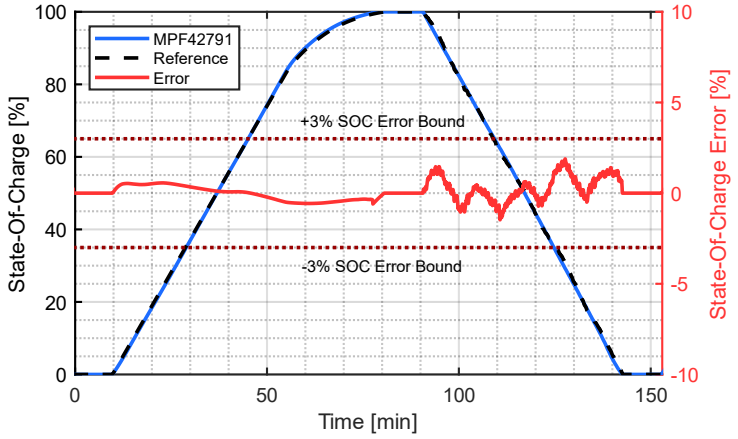


Figure 5: Combined MP2795 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 40°C)

Performance Summary

This section provides a summary of the combined MP2795 and MPF42791's real-world performance. Table 1 shows a summary of the pack SOC performance metrics for a 10S1P battery.

Table 1: MPF42791 SOC Root-Mean-Squared (and Maximum) Error

Test Case	0°C	25°C	40°C
CC/CV charge	0.68% (1.22%)	0.61% (1.03%)	0.4% (0.6%)
Dynamic discharge	1.15% (2.97%)	0.78% (1.94%)	0.77% (1.89%)

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FUNCTIONAL BLOCK DIAGRAM

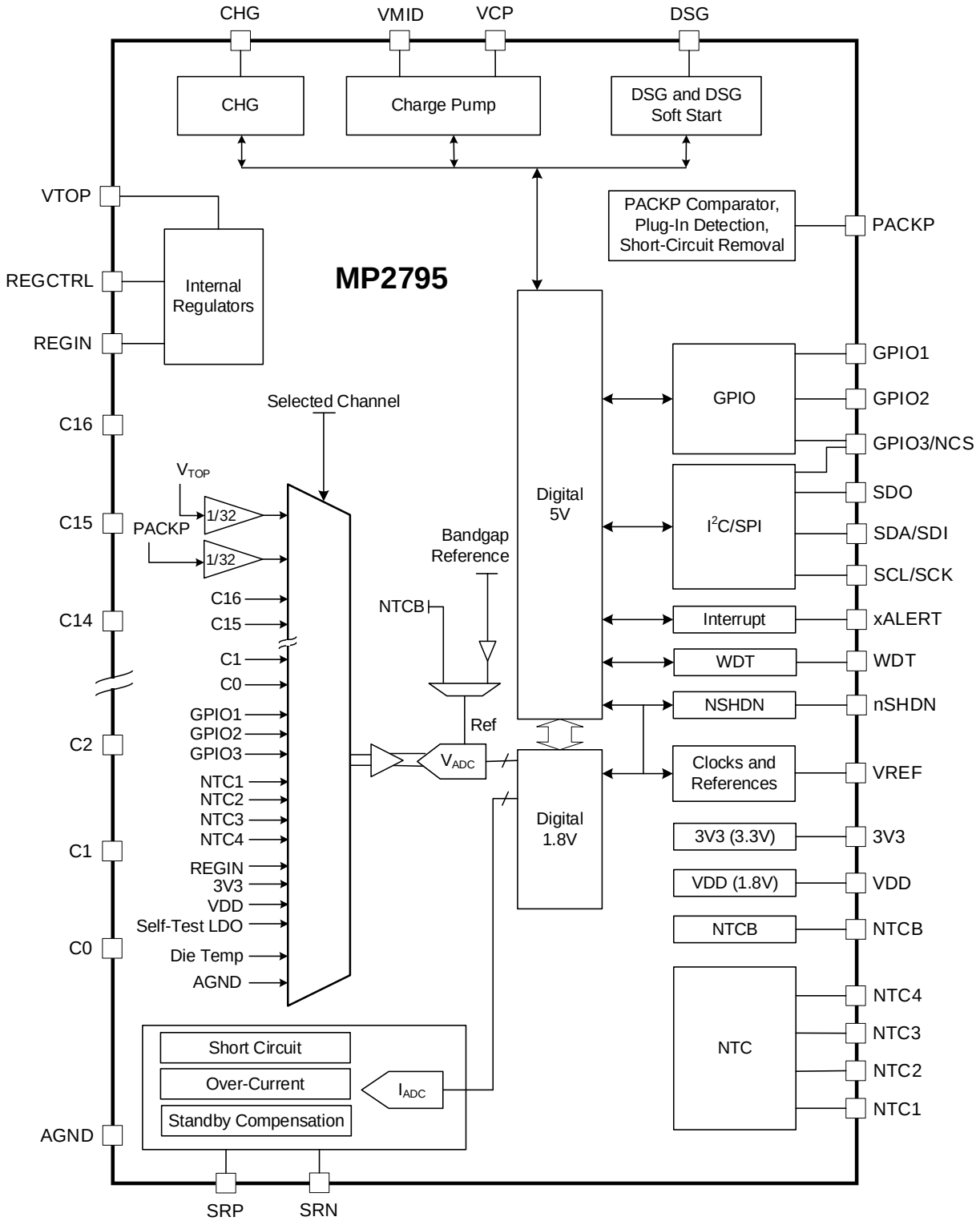


Figure 6: Functional Block Diagram

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OPERATION

Main Modes

The MP2795's main modes are listed and described below (see Figure 7).

Shutdown Mode

It is vital to preserve a battery's capacity. Shutdown mode minimizes the amount of leakage from the battery pack, which extends the battery pack's shelf storage life.

In shutdown mode, the communication interface is unavailable and REGIN is loosely regulated, which means its voltage is below the normal voltage without any load capacity. However, it is possible to keep 3.3V active in shutdown mode with a slight margin for current consumption.

Pull the NSHDN pin to ground to enter shutdown mode.

Safe Mode

To enter safe mode from shutdown mode, pull up the NSHDN pin and wait at least 5ms before issuing an I²C or SPI command. If any functional commands are required in safe mode (e.g. high-resolution voltage scanning, Coulomb counting, turning on the MOSFETs, voltage protection monitoring, open wire detection, cell-balancing), then the I²C or SPI bus must be idle for at least 200µs after the functional command is enabled.

Safe mode is characterized by the following conditions:

- The protection MOSFETs turn off.
- The over-voltage (OV) and under-voltage (UV) hardware autonomous protection state machine is disabled, unless it is forcibly enabled.
- The communication interface is enabled.

To exit safe mode, see the Protection MOSFET Enable Control section on page 22.
In safe mode, it is possible to enable protection monitoring (cell OV, cell UV, and current monitoring).

Active Mode

In active mode, the high-side drivers turn on, and the battery management system (BMS) can be powered or be charged by a downstream system through the charge (CHG) and discharge (DSG) N-channel MOSFETs.

Standby Mode

Standby mode reduces current consumption. To enter this mode, standby mode must be enabled, and the current must be below the standby current threshold.

In standby mode, the time between the analog-to-digital converter (ADC) voltage conversions used for protection monitoring can be independently lengthened via the STBY_MONITOR_CFG bits (06h, bits[5:4]). This reduces the average current consumption.

Fault Mode

In fault mode, both the CHG and DSG MOSFET drivers turn off in response to a fault event. Protection monitoring remains enabled during a fault.

Fault mode can be cleared manually or through automatic fault recovery, depending on the configuration.

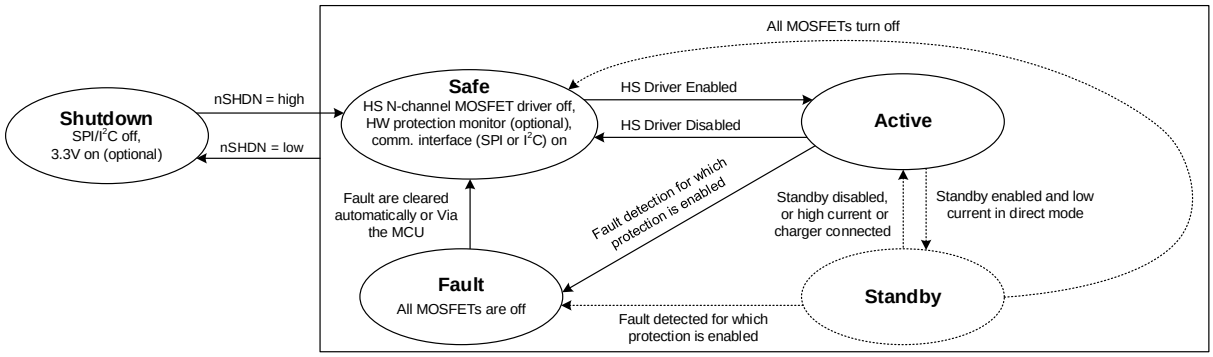


Figure 7: Main States Diagram

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Registers (Default and Lock)

Most of the configuration settings and options have a configurable default value. Certain registers can be configured independently, or they can be locked in read-only mode. This prevents critical safety features from being changed.

Protection MOSFET Enable Control

The MP2795 can exit safe mode and enter active mode via pin control or register control. Only one control method can be selected at a time. The FET_SRC bit (05h, bit[0]) can be set either via the ACT_CFG (05h) command or GPIO1/GPIO2 pin to determine whether the device should remain in safe mode or active mode.

Two different control strategies can be selected via the FET_CFG bit (05h, bit[1]): simple mode or direct mode. Table 2 shows the BMS behavior in simple mode, where a single control is offered for both the CHG and the DSG driver. The system internally handles the MOSFETs' turn-on and turn-off sequences.

Table 2: Protection MOSFETs (Simple Mode)

Configuration: FET_SRC = GPIO			
MOSFET	**GPIO1 = Low**	**GPIO1 = High**	**GPIO1 = High**
		Fault	**No Fault**
CHG N-channel MOSFET	Off	Off	On
DSG N-channel MOSFET	Off	Off	On

Table 3 shows the BMS behavior in direct mode, where each driver (the CHG MOSFET driver and DSG MOSFET driver) can be directly controlled.

Table 3: Protection MOSFETs (Direct Mode)

Configuration: FET_SRC = GPIO					
MOSFET	**GPIO1 = Low GPIO2 = Low**	**Fault**	**No Fault**		
			GPIO1 = High GPIO2 = Low	**GPIO1 = Low GPIO2 = High**	**GPIO1 = High GPIO2 = High**
CHG N-channel MOSFET	Off	Off	Off	On	On
DSG N-channel MOSFET	Off	Off	On	Off	On

MOSFET Driving Ability

The high-side MOSFET (HS-FET) driver can drive multiple DSG or CHG MOSFETs in parallel. The VCP pin capacitance (C_{VCP}) must be increased, depending on the number of parallel MOSFETs in the application.

Soft Start (SS) of the Discharge (DSG) MOSFET (13)

One of the biggest challenges when designing a BMS with HS-FETs is limiting the inrush current and protecting the DSG MOSFET from exceeding its safe operating area (SOA) when it turns on with a large capacitive load present.

To address this issue, most system designers add what is commonly referred to as a pre-charge or pre-biased external circuit. This type of external circuit requires additional MOSFETs and physically large power resistors, which limit the discharge current while the load capacitance is charging. To reduce the significant size and cost of this circuit, the MP2795's DSG N-channel MOSFET driver includes an innovative soft start (SS) discharge MOSFET control circuit.

SS controls the rising slope of the DSG voltage by setting the DSG_SOFTON_DV bits (14h, bits[2:0]), and thereby reducing the discharging current. To ensure that the DSG MOSFET does not exceeds its SOA during SS, the MP2795 uses three separate over-current (OC) comparators.

Note:

13) For detailed design guidelines on how to configure the SS settings of the DSG MOSFET, contact an MPS FAE for the related application note.

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GPIO Pins

The GPIO pins can be directly controlled by the microcontroller unit (MCU) via the registers, or they can be assigned to special functions. The GPIO pins have the following functions:

- Push-pull output: The pull-up voltage can be configured to REGIN or 3V3.
- Pull-up capability: Connect a 20kΩ pull-up resistor to REGIN or 3V3.
- Digital input.
- Analog input: Can act as a buffered ADC input with a 0V to 3.3V range.

In addition to the GPIO functions, the GPIO1 and GPIO2 pins can also enable certain protections (see the Protection MOSFET Enable Control section on page 22).

The GPIO3 pin can be configured to initiate automatic cell-balancing (as an input) or indicate the fault status (as an output).

WDT Pin

The WDT pin is controlled by the watchdog timer and provides the following functions:

- Toggles with a high pulse when a watchdog event occurs to reset an external IC (e.g. the host MCU).
- Triggers a self-reset to the IC by bringing the device back to its default values.
- Can be pulled high externally to reset the device.

Alert (xALERT Pin)

The xALERT pin can be configured to be an active high (3.3V) or active low interrupt pin. When set to active low, xALERT goes low if there is a pending interrupt. When set to active high, this pin goes high if there is a pending interrupt.

Protections and other events trigger the xALERT pin, but certain bits must be enabled to ensure that only the relevant sources generate an interrupt.

Protections, Interrupts, and Faults

Hardware protections can trigger both interrupt and faults independently (see Figure 8).

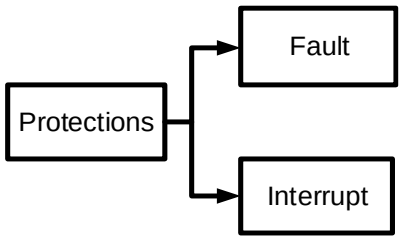


Figure 8: General Faults and Interrupts Architecture

Current Protections

Over-Current Protection (OCP)

All over-current protection (OCP) monitoring is performed with the same over-current (OC) analog comparator. Two possible range (RNG) levels are available for each threshold.

The threshold limit and deglitch are available with the multiple-time programmable (MTP) memory, meaning the value can be customized during battery pack assembly for different projects. OC1_DCHG_EN_CTRL (23h, bit[0]), OC2_DCHG_EN_CTRL (23h, bit[1]), and OC_CHG_EN_CTRL (23h, bit[2]) are the enable bits for discharge OCP threshold 1 (OC1), discharge OCP threshold 2 (OC2), and charge OC monitoring.

Once enabled, the monitoring function starts during the transition from safe mode to active mode, then remains running in active mode. Use the SAFE_SCOC_EN bit (07h, bit[1]) to enable monitoring in safe mode.

The enable bits for OC monitoring can be permanently locked in read-only mode, preventing the MCU from performing further changes. Once OC monitoring is enabled, the interrupt and fault rules can be set.

When only the CHG or DSG MOSFET turns on, the OC limits are set to whichever value is smaller between the configured value and 17.5mV. Meanwhile, the deglitch filter is the smaller value between the configured value and 16ms.

Discharge Over-Current Protection (OCP)

Two independent thresholds are available for discharge OCP: OC1 and OC2.

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Table 4 shows the resolution and ranges for OC1 and OC2.

Table 4: OC1 and OC2

Threshold	RNG = 0	RNG = 1 (3x)
LSB (mV)	2.5	7.5
FSR (mV)	80	240

Each limit has its own configurable deglitch time ($t_{OC1_DSG_DGL}$ and $t_{OC2_DSG_DGL}$) with two configurable ranges (see Table 5). In standby mode, OC1 and OC2 are set to 2.5mV and the deglitch filter is the shorter value between the configured value and 1ms.

Table 5: OC1 and OC2 Deglitch Times

Deglitch Range	$t_{OCx_DSG_DGL}$ RNG = 0	$t_{OCx_DSG_DGL}$ RNG = 1
LSB (ms)	5	40
FSR (ms)	315	2520

Charge Over-Current Protection (OCP)

Table 6 shows the resolution and range for charge OCP.

Table 6: Charge OCP

Threshold	RNG = 0	RNG = 1 (3x)
LSB (mV)	1.6	4.8
FSR (mV)	51.2	153.6

The charge OC limit has its own configurable deglitch time ($t_{OC_CHG_DGL}$) with two configurable ranges (see Table 7).

Table 7: Charge OC Deglitch Time

Deglitch Range	$t_{OC_CHG_DGL}$ RNG = 0	$t_{OC_CHG_DGL}$ RNG = 1
LSB (ms)	5	40
FSR (ms)	315	2520

Short-Circuit Protection (SCP)

All short-circuit protection (SCP) monitoring is performed on a single short-circuit analog comparator. Each limit has a configurable deglitch time between 100µs and 25.5ms.

SC_DCHG_EN_CTRL (2Ah, bit[0]) and SC_CHG_EN_CTRL (2Ah, bit[1]) are the enable bits for discharge short-circuit and charge short-circuit monitoring, respectively. Once monitoring is enabled and the MP2795 transitions from safe mode to active mode, the IC begins monitoring.

The SAFE_SCOC_EN bit can enable monitoring in safe mode.

Once short-circuit current monitoring is enabled, the interrupt and fault rules can be set.

Discharge Short Circuit

Table 8 shows the resolution and range for the discharge short-circuit current limit.

Table 8: Discharge Short-Circuit (DSC) Current Limit

DSC Threshold	Limit		Deglitch Range
	RNG = 0	RNG = 1	
LSB	5.5mV	16.5mV	200µs
FSR	176mV	528mV	25.4ms

Charge Short Circuit

Table 9 shows the resolution and range for the charge short-circuit current limit.

Table 9: Charge Short-Circuit (CSC) Current Limit

CSC Threshold	Limit		Deglitch Range
	RNG = 0	RNG = 1	
LSB	2.5mV	7.5mV	200µs
FSR	80mV	240mV	25.4ms

Voltage Protections

When enabled, all voltage protections are automatically monitored without requiring an MCU to schedule ADC conversion.

An autonomous hardware state machine periodically schedules the conversion for all relevant channels, and the results are internally checked and compared to the limits.

The deglitch filters refer to the number of consecutive readings during which the relevant channel exceeds its thresholds. The interval between readings is typically 254ms, though this value depends on the device's state (e.g. active mode or standby mode) and the configuration of the hardware monitoring (e.g. the ACTIVE_MONITOR_CFG bit set via 07h, bit[3] for active mode and the STBY_MONITOR_CFG bits for standby mode).

Cell Under-Voltage (UV) and Over-Voltage (OV) Thresholds

When fewer than 16 cells are used, only the cells enabled by CELL_S_CTRL (00h, bits[3:0]) are monitored for under-voltage (UV) and over-voltage (OV) conditions.

These thresholds are available in the MTP, meaning they can be customized during battery

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pack assembly for different projects. Table 10 shows the cell OV and UV thresholds.

Table 10: Cell OV and UV Thresholds

Cell OV/UV	Limit	Hysteresis	Deglitch
LSB	19.5mV	19.5mV	1 reading
FSR	4.98V	292.5mV	16

Pack Under-Voltage (UV) and Over-Voltage (OV) Thresholds

The pack OV and UV thresholds are monitored by the VTOP pin. These thresholds are available in the MTP, meaning they can be customized during battery pack assembly for different projects (see Table 11).

Table 11: Pack OV and UV Thresholds

Pack OV/UV	Limit	Hysteresis	Deglitch
LSB	19.5mV	78mV	1 reading
FSR	80V	4.922V	16

Negative Temperature Coefficient (NTC) Temperature

The negative temperature coefficient (NTC) voltages are checked during the automatic hardware monitoring sequence.

Figure 9 shows the block diagram of the NTC-sensing architecture.

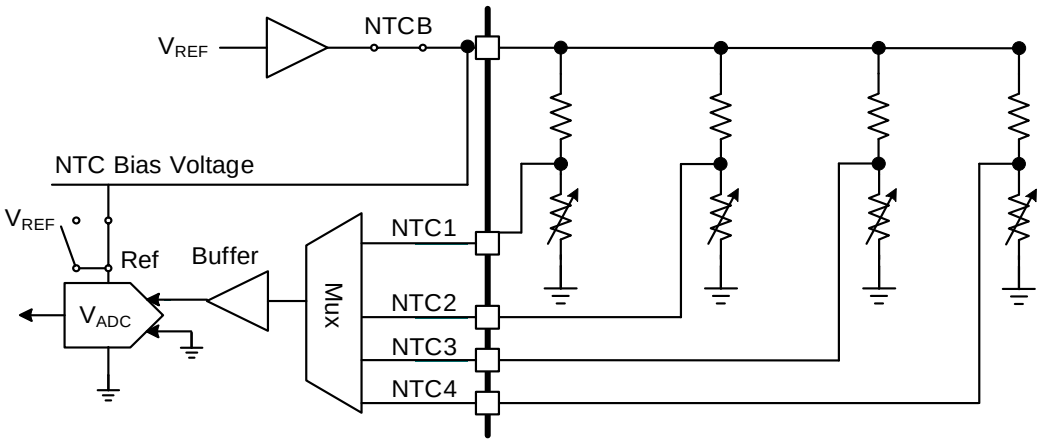


Figure 9: Architecture for NTC ADC Acquisition

All NTC channels are monitored in a ratiometric conversion, where the ADC reference is switched to NTCB for the NTC channels. In this scenario, all effects related to NTCB drifts due to the temperature and operating conditions being removed from the reading.

NTC1, NTC2, NTC3, and NTC4 have limits that can be set according to two modes:

1. Cell monitor mode: The NTC monitors the temperature of the lithium cell in the pack. The MP2795 provides independent cell temperature limits (hot and cold) for the charging and discharging currents.

   These thresholds are available in the MTP, and can be customized during battery pack assembly for different projects.

2. PCB monitor mode: The NTC monitors the PCB or the protection MOSFET's temperature. A standard hot temperature limit is provided for both the charge and discharge current.

Using NTCs results in a lower voltage threshold for over-temperature (OT) or hot conditions and a higher voltage threshold for under-temperature or cold conditions.

Die Temperature

The die temperature alarm has two thresholds. The first is a digital threshold that can be configured between 70°C and 120°C. With this threshold, the comparator's output can force the IC to enter fault mode. The second is an analog threshold that forces the device to shut down at 140°C.

The digital die temperature threshold is typically used as an early warning since the analog threshold forces the IC to shut down. Until the analog OT condition is resolved, the IC remains in a forced shutdown state, and the communication interface is unavailable.

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Dead Cells

The pack is monitored at a cell level for dead cells. A dead cell is defined as any cell with a voltage that falls below the manufacturer's specified final discharge voltage, in which case, continued charging should be avoided. If dead cell detection is enabled, the MP2795 checks whether any cell is below the configurable threshold (CELL_DEAD_LIMIT, set via 3Ch, bits[6:0]), which is typically much lower than the cell's UV threshold.

Once a dead cell condition is detected, the persistent dead cell flag (CELL_DEAD_LOG_STS, set via 34h, bit[14]) is set to 1. When the default values for the CELL_DEAD_EN bit (34h, bit[8]) and the CELL_DEAD_FAULT_EN bit (34h, bit[9]) are enabled via the one-time programmable (OTP) memory, this flag remains at 1, even if the device enters and exits shutdown mode. This flag can be cleared by the CELL_DEAD_DET_CLEAR bit (34h, bit[15]).

Mismatched Cells

Excessively mismatched or unbalanced cells can be detected by monitoring the maximum and minimum cell voltages.

If the difference between the maximum cell voltage and the minimum cell voltage exceeds a defined threshold, then a cell mismatch status is triggered. The mismatched cell with the higher voltage is reported as an individual flag. The cell with the minimum voltage is reported in the CELL_MSMT_LOWER bits (33h, bits[13:10]).

Diagnostics and Integrity

Low-Dropout (LDO) (REGIN, 3.3V, and 1.8V) Rail Monitoring

The low-dropout (LDO) UV threshold is provided for the REGIN, 3.3V and 1.8V rails. This UV threshold is compared to the ADC readings with the same refresh interval as the other voltage monitors, ensuring that it measures the nominal rail voltage rather than detecting voltage spikes.

Analog-to-Digital Converter (ADC) Self-Test Conversion

The ADC converts a known voltage and determines whether the conversion result is within a predefined window that accounts for tolerance and temperature shifts.

One-Time Programmable (OTP) Cyclic Redundancy Check (CRC)

A one-time programmable (OTP) cyclic redundancy check (CRC) is executed when the device exits shutdown mode. If CRC fails, the device can be configured to enter fault mode, preventing the BMS from turning on the protection MOSFETs.

Communication Cyclic Redundancy Check (CRC)

Typically, the CRC detects errors in exchanged data. The MP2795 supports CRC for exchanged data. When this functionality is enabled, the following is possible:

- Write a transaction to one register (2 bytes) to append a 1-byte CRC. A correct CRC is required for a successful write transaction.
- Read a transaction for one register (2 bytes) to append a 1-byte CRC.
- The read transaction length can be temporarily increased to 126 bytes using a dedicated register. The CRC is appended at the end of the transaction.

CRC is implemented by the CRC-8 algorithm, where it can detect 1 incorrect bit. However, all CRC techniques encounter limitations when there are more incorrect bits.

If more than 1 bit is corrupted, the error detection depends on the specific pattern. Statistically, the detection can occur, but it is not guaranteed. In general, the ability to detect errors decreases when there is more data to check. For more details, see the I²C Read section on page 38 and the SPI Read section to page 40.

Watchdog Timer

The watchdog timer monitors communication with the I²C interface or serial peripheral interface (SPI). If there is no write to the WDT_RST bit (0Fh, bit[0]) within a set interval, then the timer is triggered. The watchdog has a bark-bite style.

The bark notifies the device when the MCU has failed to clear the watchdog timer. This results in a bark timeout, which can be configured to trigger the alert pin. The watchdog timer bark counter setting is 25ms per least significant bit (LSB), with a maximum up to 3.2s.

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After a bite timeout, there is an optional feature to reset the device's registers to the default values. The watchdog timer bite counter setting is 25ms per LSB, with a maximum up to 3.2s.

Using the bidirectional, configurable watchdog timer, it is possible to set up the IC to self-reset and/or to reset an external IC if its reset trigger is connected to the WDT pin.

Interrupts

Interrupt statuses are split between two commands: RD_INT0 (15h) and RD_INT1 (16h). Each interrupt source has a matching enable bit and a dedicated clear bit to clear the interrupt. Table 12 shows the main interrupts, and Table 13 on page 28 shows additional interrupts.

Table 12: Main Interrupts (RD_INT0)

Condition	Flag	Description	Related Status Register(s)
Cell over-voltage (OV)	CELL_OV_INT_ STS (15h, bit[0])	Unified flag for cell OV conditions. The related register reports each cell's OV flag, which is checked to determine which cell is generating the interrupt.	Flags in address, RD_CELL_OV (2Eh)
Cell under-voltage (UV)	CELL_UV_INT_ STS (15h, bit[1])	Unified flag for cell UV conditions. The related register reports each cell's UV flag, which is checked to determine which cell is generating the interrupt.	Flags in address, RD_CELL_UV (2Dh)
VTOP pack OV	VTOP_OV_INT_ STS (15h, bit[3])	Dedicated flag for battery pack OV conditions detected on the VTOP pin.	-
VTOP pack UV	VTOP_UV_INT_ STS (15h, bit[2])	Dedicated flag for battery pack UV conditions detected on the VTOP pin. This is unrelated to the VTOP UV analog threshold.	-
Over-current (OC)	OVER_CURR_ INT_STS (15h, bit[4])	OC interrupt for charge, discharge 1, and discharge 2.	OC1_DCHG_STS (20h, bit[0]), OC2_DCHG_STS (20h, bit[1]), OC_CHG_STS (20h, bit[2])
Short-circuit protection (SCP)	SHORT_CURR_ INT_STS (15h, bit[5])	Short-circuit interrupt for both charge and discharge.	SC_CHG_STS (27h, bit[1]), SC_DCHG_STS (27h, bit[0])
Negative temperature coefficient (NTC) cold	NTC_COLD_INT_ STS (15h, bit[6])	Unified flag for NTC cold conditions for all NTC channels configured in cell mode. To identify which NTC is the source of the interrupt, the additional individual flags should be checked.	NTC1_CELL_COLD_ STS (3Eh, bit[4]), NTC2_CELL_COLD_ STS (3Eh, bit[5]), NTC3_CELL_COLD_ STS (3Eh, bit[6]), NTC4_CELL_COLD_ STS (3Eh, bit[7])
NTC hot	NTC_HOT_INT_ STS (15h, bit[7])	Unified flag for NTC hot conditions for all NTC channels configured in cell mode. To identify which NTC is the source of the interrupt, the additional individual flags should be checked.	NTC1_CELL_HOT_ STS (3Eh, bit[0]), NTC2_CELL_HOT_ STS (3Eh, bit[1]), NTC3_CELL_HOT_ STS (3Eh, bit[2]), NTC4_CELL_HOT_ STS (3Eh, bit[3])

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Watchdog interrupt	WDT_INT_STS (15h, bit[8])	Notification for either a bite or bark event from the communication watchdog timer.	WDT_BARKED (0Eh, bit[0]), WDT_BITE (0Eh, bit[1])
Fault recovered	RECOVERED_ INT_STS (15h, bit[9])	Notification that the system has recovered from a fault state, including both automatic fault recovery and manual MCU clearing.	-
Analog front-end (AFE) mode change	AFE_MODE_ CHANGE_INT_ STS (15h, bit[10])	The AFE has changed states (e.g. safe mode, active mode, fault mode, standby mode).	PWR_STATE (01h, bits[4:0])
Scan complete	VSCAN_DONE_ INT_STS	Notification that the high-resolution voltage analog-to-digital converter (ADC) scan has finished converting all the channels on its list.	-
Coulomb counting done	CC_ACC_INT_ STS (15h, bit[12])	Flag reporting that a new Coulomb counting accumulation value has been updated to CC_ACC_LSBS (65h, bits[15:0]) and CC_ACC_MSBS (66h, bits[9:0]).	-
Plug-in detection	CONN_DET_INT_ STS (15h, bit[13])	The plug-in detection logic reports that either a device (capacitive load or charger) has been connected, or the detection cannot be successfully complete.	LD_IN (03h, bit[14]), CHG_IN (03h, bit[15]), CHGDET_FAIL (03h, bit[13]), LDDET_FAIL (03h, bit[12])
Pack current	PACK_ CURRENT_INT_ STS (15h, bit[14])	Interrupt indicating a change in the battery pack current range (discharge, standby, or charge).	PACK_CURRENT_ STATUS (01h, bits[9:7])

Table 13: Additional Interrupts (RD_INT1)

Name	Flag	Description	Related Status Register(s)
MOSFET driver	FET_DRIVER_ INT_STS (16h, bit[13])	Reports a MOSFET driver issue such as the following: • MOSFET timeout: The DSG or CHG driver does not reach its final voltage within the timeout interval • A lower level OC condition occurs during CHG or DSG soft start • A short circuit is issued before DSG turns on	FET_TIMEOUT (11h, bit[3])
PACKP voltage	PACKP_V_INT_ STS (16h, bit[12])	The voltage on the PACKP node changes compared to VTOP. The PACKP comparator is invalid when disabled or during short-circuit removal, but still reports to the interrupt.	PACKP_COMP_STS (02h, bits[10:8])
Balancing complete	BAL_DONE_INT_ STS (16h, bit[11])	Balancing has been completed.	Flags in address, BAL_STS (A4h)
Self-test fail	SELF_TEST_INT_ STS (16h, bit[10])	The ADC fails its self-diagnostic test and/or the conversion of this value is outside the specified boundaries.	SELF_TEST_STS_OV (4Eh, bit[1]), SELF_TEST_STS_UV (4Eh, bit[0]),

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Scheduler error	FSM_ERROR_ INT_STS (16h, bit[9])	The scheduler is busy when a new feature command is requested, and concurrent operation is not supported. For example, the device may report that an MCU conversion command is ignored since open-wire detection is running, or it may report that a cell-balancing command is ignored since open-wire detection is running.	-
PCB temperature hot	PCB_MNTR_ HOT_INT_STS (16h, bit[8])	Unified flag for NTC hot conditions for all NTC channels configured in PCB mode. To identify which NTC is the source of the interrupt, the individual flags should be checked.	NTC1_PCB_MNTR_ HOT_STS (3Eh, bit[8]), NTC2_PCB_MNTR_ HOT_STS (3Eh, bit[9]), NTC3_PCB_ MNTR_HOT_STS (3Eh, bit[10]), NTC4_PCB_ MNTR_HOT_STS (3Eh, bit[11])
Die temperature	DIE_TEMP_INT_ STS (16h, bit[7])	The die temperature is too high. The temperature is reported by the digital die temperature check.	-
Mismatched cells	CELL_ MISMATCH_INT_ STS (16h, bit[6])	The voltage difference between cells is too great.	Flags in address, RD_CELL_MSMT (2Fh)
Dead cell	CELL_DEAD_ INT_STS (16h, bit[5])	The dead cell threshold is reached.	Flags in address, RD_CELL_DEAD (30h)
Open wire	OPEN_WIRE_ INT_STS (16h, bit[4])	Open-wire detection is complete. The open-wire interrupt status register must be checked to identify if there are any disconnected wires.	Flags in address, RD_OPENH, RD_OPENL
VDD	VDD_INT_STS (16h, bit[3])	The VDD rail is below the defined UV threshold.	-
3V3	3V3_INT_STS (16h, bit[2])	The 3.3V rail is below the defined UV threshold.	-
REGIN	REGIN_INT_STS (16h, bit[1])	The REGIN rail is below the defined UV threshold.	-
OTP CRC	OTP_CRC_ EVENT_INT_STS (16h, bit[0])	The cyclic redundancy check (CRC) stored in the one-time programmable (OTP) memory does not match the computed CRC value from OTP memory readback. The manual CRC check is completed.	-

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The interrupt source can be configured using a TYPE selector. Depending on the interrupt, the TYPE selector provides a few options:

- Level (high)
- Rising edge
- Falling edge
- Rising and falling edge

Each interrupt that is related to a protection flag follows the processes described above.

Fault

In fault mode, both discharge and charge N-channel MOSFETs (DSG N-channel MOSFETs and CHG N-channel MOSFETs, respectively) are turned off. Faults can be cleared either by automatic recovery or manual MCU clearing. The fault enable control bit for each fault has a configurable default value, as well as the option to permanently lock the register in read-only mode. Table 14 shows certain faults and their recovery methods. Table 15 on page 31 shows additional faults and their recovery methods.

Table 14: Fault and Recovery Management (Part I)

Fault	Enable Control	Can Be Read-Only?	Recovery Method(s)
Cell OV	CELL_OV_FAULT_EN (35h, bit[5])	Yes	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear bit (CELL_OV_FAULT_CLR) (5Fh, bit[1]) • Automatic recovery: This method is enabled with CELL_OV_REC (61h, bit[11]). An additional recovery logic option is available via CELL_OV_LOGIC_SEL (61h, bit[9])
Cell UV	CELL_UV_FAULT_EN (35h, bit[2])	Yes	Configurable for manual or automatic recovery. If the battery pack current status is charging, then the cell UV fault is blocked, but the status is still reported when the cell voltage (V_{CELL}) is below the cell UV threshold. • Manual recovery: The host MCU writes to the fault clear bit (CELL_UV_FAULT_CLR) (5Fh, bit[0]) • Automatic recovery: This method is enabled with CELL_UV_REC (61h, bit[7]). An additional recovery logic option is available via CELL_UV_LOGIC_SEL (61h, bit[5])
Dead cell	CELL_DEAD_FAULT_EN (34h, bit[9])	Yes	The host MCU writes to the fault clear command (CELL_DEAD_FAULT_CLR) (5Fh, bit[2]). CELL_DEAD_LOG_STS (34h, bit[14]) prevents the IC from entering active mode, which can only be cleared by CELL_DEAD_DET_CLEAR (34h, bit[15]).
Cell mismatch	CELL_MSMT_FAULT_EN (34h, bit[12])	Yes	The host MCU writes to CELL_MSMT_FAULT_CLR (5Fh, bit[3]).
Open wire	OPEN_WIRE_FAULT_EN (56h, bit[9])	Yes	The host MCU writes to OPEN_WIRE_FAULT_CLR (5Fh, bit[4]).
VTOP OV	VTOP_OV_FAULT_EN_CTRL (34h, bit[5])	Yes	The host MCU writes to VTOP_OV_FAULT_CLR (5Fh, bit[6]).
VTOP UV	VTOP_UV_FAULT_EN_CTRL (34h, bit[1])	Yes	The host MCU writes to VTOP_UV_FAULT_CLR (5Fh, bit[5]).

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Cell NTC too hot (discharge)	NTC_CELL_HOT_FAULT_EN (47h, bit[13])	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_HOT_FAULT_CLR) (5Fh, bit[8]) • Automatic mode: The device recovers when the NTC voltage (V_{NTC}) exceeds the sum of the hot discharge threshold and hysteresis. This method is enabled with NTC_CELL_DCHG_REC (60h, bit[1])
Cell NTC too cold (discharge)	NTC_CELL_COLD_FAULT_EN (47h, bit[14])	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_COLD_FAULT_CLR) (5Fh, bit[9]) • Automatic mode: The device recovers when V_{NTC} falls below the difference between cold discharge threshold and hysteresis. This method is enabled with NTC_CELL_DCHG_REC
Cell NTC too hot (charge)	NTC_CELL_HOT_FAULT_EN (47h, bit[13])	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_HOT_FAULT_CLR) • Automatic recovery: The device recovers when V_{NTC} exceeds the sum of the hot charge threshold and hysteresis. This method is enabled with NTC_CELL_CHG_REC (60h, bit[2]). An additional recovery logic option is available via NTC_CHG_REC_MODE (60h, bit[3])
Cell NTC too cold (charge)	NTC_CELL_COLD_FAULT_EN (47h, bit[14])	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_COLD_FAULT_CLR) • Automatic recovery: The device recovers when V_{NTC} falls below the difference between the cold charge threshold and hysteresis. This method is enabled via NTC_CELL_CHG_REC. An additional recovery logic option is available via NTC_CHG_REC_MODE

Table 15: Fault and Recovery Management (Part II)

Fault	Enable Control	Can Be Read-Only?	Recovery Method(s)
Pack OC discharge 1	OC1_DCHG_FAULT_EN (23h, bit[6])	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when OC_DCHG_RECOVERY_FAILED (5Eh, bit[12]) has issued a report. • Manual recovery: The host MCU writes to the fault clear command (OC1_DCHG_FAULT_CLR) (5Fh, bit[10]) • Automatic recovery: Enabled with OC1_DCHG_REC (60h, bit[6]). This device tries to turn on the MOSFETs to check whether the condition is removed. If removed, the device automatically clears the fault status and returns to safe mode. If the condition is not removed within the time set by OC1_DCHG_RETRY, then the device reports to OC_DCHG_RECOVERY_FAILED. Once the pack drops below 110mV, the device reports to OC_DCHG_RECOVERY_FAILED directly.

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Pack OC discharge 2	OC2_DCHG_ FAULT_EN (23h, bit[7])	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when OC_DCHG_RECOVERY_FAILED has issued a report. • Manual recovery: The host MCU writes to the fault clear bit (OC2_DCHG_FAULT_CLR) (5Fh, bit[11]) • Automatic recovery: Enabled with OC2_DCHG_REC (60h, bit[7]). This device tries to turn on the MOSFETs to check whether the condition is removed. If removed, the device automatically clears the fault status and returns to safe mode. If the condition is not removed within the time set by OC2_DCHG_RETRY (63h, bits[7:6]), then the device reports to OC_DCHG_RECOVERY_FAILED. Once the pack drops below 110mV, the device reports to OC_DCHG_RECOVERY_FAILED directly.
Pack OC charge	OC_CHG_ FAULT_EN (23h, bit[8])	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when OC_CHG_RECOVERY_FAILED (5Eh, bit[11]) has issued a report. • Manual recovery: The host MCU writes to the fault clear bit (OC_CHG_FAULT_CLR) (5Fh, bit[12]) • Automatic recovery: Enabled with OC_CHG_REC (60h, bit[8]). This device tries to turn on the MOSFETs to check whether the condition is removed. If removed, the device automatically clears the fault status and returns to safe mode. If the condition is not removed within the time set by OC_CHG_RETRY (63h, bits[11:10], then the device reports to OC_CHG_RECOVERY_FAILED.
Pack short-circuit current discharge	SC_DCHG_ FAULT_EN (2Ah, bit[4])	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when SC_DCHG_RECOVERY_FAILED (5Eh, bit[10]) has issued a report. • Manual recovery: The host MCU writes to the fault clear bit (SC_DCHG_FAULT_CLR) (5Fh, bit[13]) • Automatic recovery: Enabled with SC_DCHG_REC (60h, bit[9]). The device monitors the PACKP voltage to check whether it rises to 110mV. If this condition is not removed by SC_PUP_RETRY_N (62h, bits[14:13]), then the device reports to SC_DCHG_RECOVERY_FAILED.
Pack short-circuit current charge	SC_CHG_ FAULT_EN (2Ah, bit54])	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when SC_CHG_RECOVERY_FAILED (5Eh, bit[9]) has issued a report. • Manual recovery: The host MCU writes to the fault clear bit (SC_CHG_FAULT_CLR) (5Fh, bit[14]) • Automatic recovery: Enabled with SC_CHG_REC (60h, bit[10]). The device monitors the PACKP voltage to check whether it falls below the sum of the VTOP pin voltage (V_{TOP}) and 270mV. If this condition is not removed within the time set by SC_PUP_RETRY_N, then the device reports to SC_CHG_RECOVERY_FAILED.

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3.3V or VDD UV	3V3_VDD_FAULT_EN	Yes	Manual recovery only. The host MCU writes to the fault clear command (3V3_VDD_FAULT_CLR) (60h, bit[15]).
PCB monitor too hot	PCB_MNTR_FAULT_EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (PCB_MNTR_FAULT_CLR) (5Fh, bit[7]) • Automatic recovery: The device recovers when V_{NTC} exceeds the sum of the monitor hot threshold and hysteresis. This method is enabled with PCB_MNTR_REC (60h, bit[4]).
Die too hot digital	DIE_TEMP_DIG_FAULT_EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (DIE_TEMP_FAULT_CLR) (5Fh, bit[15]) • Automatic recovery: The device waits for the die temperature to drop below the difference between the digital temperature threshold and hysteresis. This method is enabled with DIE_TEMP_FAULT_REC (60h, bit[12]).
Die too hot analog	N/A (hardcoded enable)	N/A	The IC returns to safe mode from shutdown mode once the die temperature drops below the difference between the analog temperature threshold and hysteresis.
Driver turn-on failure	N/A (hardcoded enable)	N/A	Manual recovery only. The host MCU writes to the fault clear command (DRIVER_FAULT_CLR) (60h, bit[13]).

Regulators and Power Domains

There are three main power rails, described below:

- REGIN (5V): Supplies power to the analog front-end (AFE) analog circuitry
- 3V3 (3.3V): Powers an external MCU
- VDD (1.8V): For internal use only. Powers the digital domain

The 3.3V rail can be configured to be on or off in shutdown mode.

Open-Wire Detection

The open wire state machine automatically controls the pull-up and pull-down currents sources during open-wire detection, and detects the voltage changes on each cell. The cells that are detected can be set by the CELLS_CTRL (00h) command.

The open-wire detection current uses a pair of 100µA pull-up/-down currents. The interval can be configured to be between 1ms and 16ms, with a 1ms resolution. The default is 8ms.

The threshold that determines how much change can be accepted for an open circuit is a configurable voltage threshold ranging between 39.06mV and 625mV, with 39.06mV steps. The default is 195mV. The host MCU can trigger open-wire detection with a dedicated command register. If multiple open wires are present simultaneously, then the detection logic reports at least one open wire, which tells the device to avoid using the overall battery pack (see Figure 10).

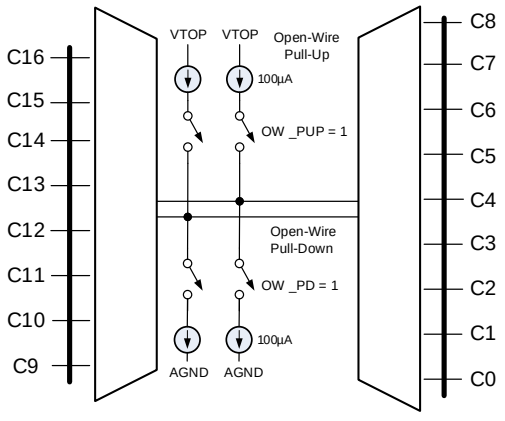


Figure 10: Open-Wire Detection Architecture

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Cell-Balancing

The battery reaches its end of life (EOL) when the capacity of the weakest cell is too low to be usable. Unbalanced cells yield the same effect, with one cell at a higher SOC, and another at a lower SOC. To reduce the effects of this issue, it is critical to balance lithium cells.

Unbalanced cells can be caused by cell temperature differences, different self-discharge rates, and general production tolerances that affect cell chemistry and alter aging rates among strings of parallel cells.

Cell-balancing can extend the usable life of the battery pack by keeping the voltage of each cell within the defined SOA.

Internal MOSFET Balancing

The MP2795 supports direct cell balancing, without the use of external MOSFETs or BJTs, for currents up to about 58mA (with a 4V cell voltage). The balance current for each cell is determined by the combined filter resistor and the on resistance of the internal balancing MOSFET ($R_{(DS)ON}$). The MP2795 can simultaneously balance only even or odd cells. Internal logic handles the sequencing between even and odd cells.

External Balancing

A balancing current exceeding 58mA can be achieved by adding external balancing MOSFETs or BJTs. This balancing current is limited by board thermals and the wiring resistance. For external MOSFETs, it is also limited by the MOSFETs' $R_{(DS)ON}$ at the appropriate gate voltage (V_{GS}). For external BJTs, it may be limited by the DC current gain (h_{FE}). For external MOSFETs, a minimum gate voltage threshold of 1.8V is required (assuming a 4.2V lithium cell) to turn on the balancing MOSFETs.

Manual Cell-Balancing

The cells that must be balanced are manually marked by writing to the appropriate register set via the BAL_LIST (A5h) command.

The balancing time for marked cells can be configured via BAL_REPETITION (A7h, bits[7:3]), with 0 to 31 repetitions. When the BAL_REPETITION bits are set to 0, there is only one 30ms execution.

The host MCU should periodically read the AFE die temperature to ensure it is within the operating range, as an excessive temperature can lead to OT shutdown.

Automatic Cell-Balancing

Automatic cell-balancing offers the following configurations:

1. Enable automatic cell balancing by setting BALANCE_MODE_REG (A7h, bit[1]) to 1.
2. Configure the method for initiating automatic cell-balancing via the register BALANCE_MODE_CTRL (A7h, bit[0]). The MP2795 can be configured to use register control (BALANCE_GO, set via A6h, bit[0]) or GPIO3 control to initiate automatic cell-balancing.
3. Disable constant automatic balancing by setting AUTO_BAL_ALWAYS (A7h, bit[2]) to 0.
4. Set ABAL_ON_CHARGE (A8h, bit[6]) to 1 to enable automatic cell-balancing when the current is in charge mode. Set ABAL_ON_STBY (A8h, bit[7]) to 1 to enable automatic cell-balancing when the current is in standby mode.
5. The BAL_REPETITION bits set the number of cell-balancing iterations. The cell-balancing repetition number is ignored if AUTO_BAL_ALWAYS is set to 1, the device constantly balances the cells until AUTO_BAL_ALWAYS is set to 0, or until the balancing list is empty.
6. Set the balancing threshold via BAL_MSM_TH (A8h, bits[12:10]). This is the minimum voltage difference between the current cell voltage and the lowest cell voltage to be eligible for cell balancing. This value ranges between 19.5mV and 87.855mV, with 9.765mV steps.
7. Set the minimum balancing voltage via CELL_BAL_MIN (A8h, bits[5:0]). This is the minimum cell voltage for a cell to be eligible for balancing. This value ranges from 2500mV to 4961mV with 39mV steps.

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If the state of the current is in discharge mode, automatic cell-balancing is skipped.

The die temperature threshold can be used to prevent or suspend balancing. The MP2795 can be configured to suspend constant automatic cell-balancing (AUTO_BAL_ALWAYS = 1), when it exceeds the die temperature threshold (see the STOP_ON_HOT bit description in the BAL_THR (A8h) section on page 136). Once the OT condition is removed, constant automatic cell-balancing resumes.

Figure 11 shows the cell-balancing list update for automatic cell-balancing. Figure 12 shows the cell-balancing sequence for the cell-balancing list.

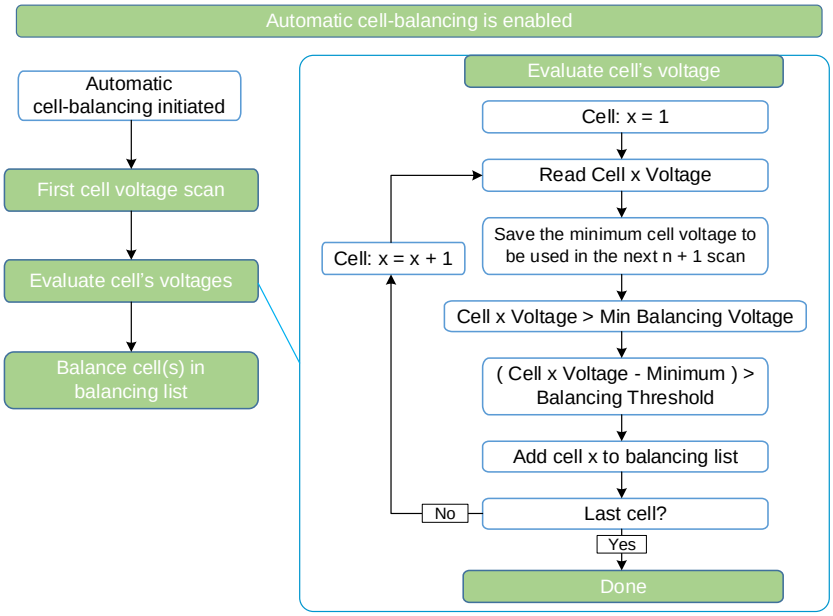


Figure 11: Automatic Cell-Balancing (Cell Voltage Evaluation)

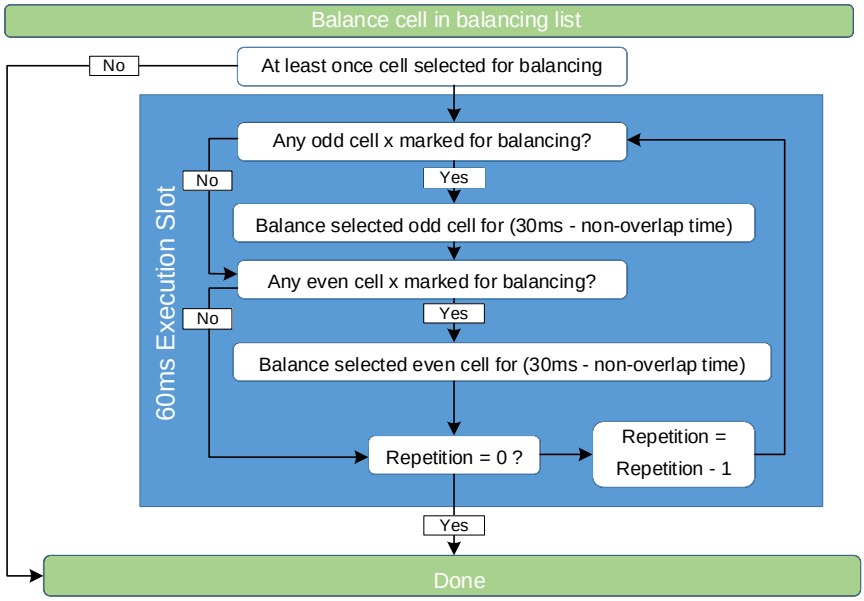


Figure 12: Execute Balancing for Cell in Balancing List

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Supported Concurrency

Table 16 shows which concurrent features can be enabled once a feature is active. When multiple features are enabled simultaneously, some remaining features can still be activated.

It is possible to use a high-resolution voltage scan during cell-balancing, but care should be taken, as voltage readings on the cell being balanced and adjacent cells are affected.

Table 16: Supported Concurrencies

Active Task	Triggered By	Concurrent Features
High-resolution voltage scan	ADC_SCAN_GO	• Cell-balancing • Coulomb counter
Cell-balancing	BALANCE_GO	• High-resolution voltage scan • Coulomb counter
Open wire	OPEN_WIRE_GO	N/A
Coulomb counter	CC_EN	• High-resolution voltage scan • Cell-balancing

The command sequence to the MP2795 should be controlled in the following manner:

- During high-resolution voltage scanning, wait to set ADC_SCAN_GO (99h, bit[0]) to 0 until SCAN_DONE_STS (99h, bit[1]) or SCAN_ERROR_STS (99h, bit[2]) updates to 1.
- During cell-balancing, wait to set BALANCE_GO to 0 until BAL_DONE_STS (A6h, bit[1]) or BAL_ERROR_STS (A6h, bit[2]) updates to 1. To stop automatic cell-balancing, set AUTO_BAL_ALWAYS to 0, wait until BAL_DONE_STS or BAL_ERROR_STS updates to 1, and then set BALANCE_GO to 0.
- When conducting open wire checks, wait to set OPEN_WIRE_GO (55h, bit[8]) to 0 until OPEN_WIRE_DONE_STS (55h, bit[9]) or OPEN_WIRE_ERR_STS (55h, bit[10]) updates to 1.
- For Coulomb counting, wait to set CC_EN (9Ah, bit[0]) to 0 until CC_DONE (9Ah, bit[4]) or CC_ERROR_STS (9Ah, bit[5]) updates to 1. To stop the back-to-back Coulomb counter, set CC_B2B_ACC_CTRL (9Ah, bit[14]) to 0. Wait until CC_DONE or CC_ERROR_STS updates to 1, then set CC_EN to 0.

For these command sequences, the status can be determined via polling or via the interrupts bits, VSCAN_DONE_INT_STS (15h, bit[11]), BAL_DONE_INT_STS (16h, bit[11]), OPEN_WIRE_INT_STS (16h, bit[4]), and CC_ACC_INT_STS (15h, bit[12]). See the Interrupts section on page 27 for more details.

Coulomb Counter

The MP2795 can accumulate up to 2s worth of the current ADC reading.

When the accumulation is complete, the value is stored in the lower 2 bytes of CC_ACC_LSBS (65h, bits[15:0]) and the upper 2 bytes of CC_ACC_MSBS (66h, bits[9:0]) for MCU readback, and an interrupt is triggered. The sequence below provides the typical steps to handle a Coulomb counting conversion:

1. Set CC_B2B_ACC_CTRL to enable back-to-back conversions, and set CC_ACC_INT_EN (19h, bit[12]) to enable interrupt.
2. Set CC_EN to enable starting the conversion.
3. Accumulation reaches the amount specified in CC_INT_CNT (9Ah, bits[13:8]).
4. CC_ACC_LSBS and CC_ACC_MSBS are updated to the values reported in CC_RT_ACC_LSBS (67h, bits[15:0]) and CC_RT_ACC_MSBS (68h, bits[9:0]).
5. CC_ACC_INT_STS reports a detected interrupt.
6. When back-to-back Coulomb counting accumulation is disabled, the CC_DONE flag can be checked to verify that accumulation has been completed. Readings are available in CC_ACC_LSBS and CC_ACC_MSBS.
7. If back-to-back conversion is enabled, the CC_RT_ACC_xSBS bits are automatically cleared and Coulomb counting restarts. The integrated value for completed accumulation can be read from CC_ACC_xSBS. If CC_ACC_INT_EN is enabled, a Coulomb

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counting done interrupt is triggered when CC_ACC_xSBS updates.

8. If back-to-back Coulomb counting accumulation is disabled, CC_EN can be set to disable clearing CC_DONE. To stop Coulomb counting if back-to-back conversions are enabled, the back-to-back flag should be cleared so that the ongoing conversion does not trigger a new conversion.
9. If an CC_ACC_INT_STS interrupt is detected, it should be cleared using CC_ACC_STS_INT_CLEAR (17h, bit[12]).

High-Resolution Voltage Analog-to-Digital Converter (ADC) Scan for the Microcontroller Unit (MCU)

A voltage scan can convert the following classes of inputs:

- Die temperature voltage
- NTC1, NTC2, NTC3, and NTC4 voltages
- Cell voltages
- VTOP pin voltage
- PACKP pin voltage
- GPIO voltages (GPIO1, GPIO2, and GPIO3)
- Regulators (VDD 1.8V, 3V3, and REGIN)

If a class of inputs is not enabled, the scan skips to the next class. Control bits are provided to enable individual channels in each class. The device is notified when the scan is complete, and the results are available for readback.

Synchronized Voltage and Current Reading

For pack voltages, the exact, synchronized current readings can be read in dedicated registers paired with the matching voltage reading. Synchronous current readings can be enabled via VTOP_SYNC_EN (9Ch, bit[9]).

The synchronized voltage and current reading can be requested concurrently with Coulomb counting monitoring.

Non-Volatile Memory (NVM) Configuration

The default values of most registers can be configured through the non-volatile memory (NVM). Some registers are one-time programmable (OTP), while others are multiple-time programmable (MTP). The MTP registers can be configured up to three times. These values can be locked, meaning the same version of the IC can be adjusted for similar projects with minor differences.

To configure the MTP, apply 7.5V to the NSHDN pin and follow the steps below:

1. Ensure that the NSHDN pin is set to 7.5V.
2. Write the appropriate value to the register that enables MTP.
3. Prior to the store command, write the following command access code: 0xA5B6 (B9h, bits[15:0] = 0xA5B6).
4. Send the command to store the register's current value to the NVM by writing 1 to STORE_NVM_CMD (B8h, bit[3]).
5. Wait for STORE_IN_PROGRESS (B8h, bit[15]) to return to 0.
6. Recover the NSHDN pin to 3.3V.

I²C Interface

The MP2795 can use an I²C interface to flexibly set parameters and report device statuses instantaneously. The I²C is a two-wire serial interface with two bus lines: a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are open drains, and they must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a target device that receives control inputs from the initiator device, such as a MCU. The SCL is always driven by the initiator device. The I²C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the initiator. A start command is defined as a high-to-low transition on the SDA while the SCL is high. A stop command is defined as a low-to-high transition on the SDA while the SCL is high (see Figure 13).

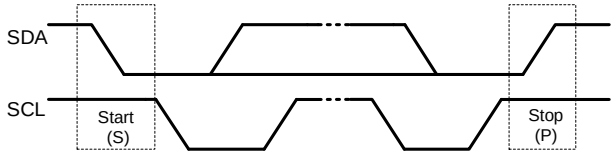


Figure 13: Start and Stop Commands

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For data validity, the data on the SDA must be stable during the clock's high period. The SDA's high or low state can only change when the clock signal on the SCL is low (see Figure 14).

Every byte on the SDA must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

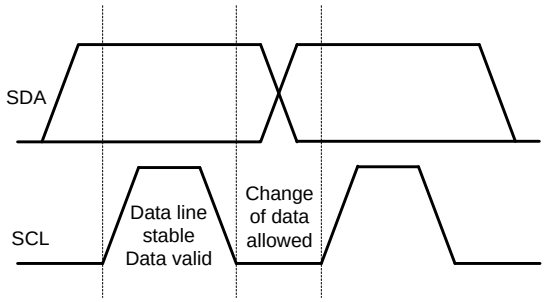


Figure 14: Bit Transfer on the I²C Bus

Each byte must be followed by an acknowledge (ACK) bit, which is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal occurs when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low. The SDA line remains low during the 9th clock pulse's high period.

If the SDA line is high during the 9th clock pulse, this is defined as a not acknowledge (NACK) signal. The initiator can then generate either a stop command to abort the transfer, or a repeated start (Sr) command to initiate a new transfer.

After the start command, a target address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 15 shows the address bit arrangement.

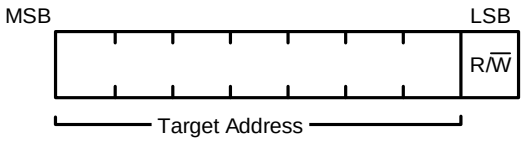


Figure 15: 7-Bit Address

Figure 16 shows a data transfer on the I²C bus.

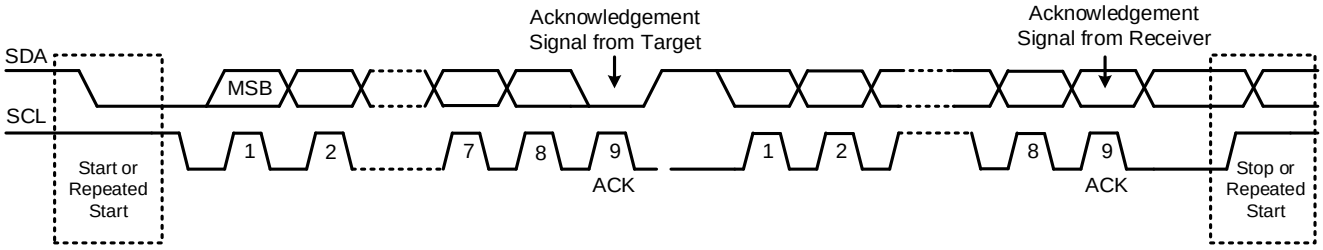


Figure 16: Data Transfer on the I²C Bus

I²C Read

When CRC is enabled, the payload is limited to 2 bytes by default (see Figure 17 on page 39). This value can be increased to 63 words (126 bytes) using XFR_NUM_RD_WORDS (A0h, bits[5:0]). Since the XFR_NUM_RD_WORDS bits retain the new value only for the next transaction, ensure that the next transaction uses the increased payload count.

Cyclic Redundancy Check (CRC) in an I²C Read Transaction

After completing the request for a read transaction, the host MCU must ensure that the CRC matches the value provided in the read transaction to confirm that no bits were corrupted during the transmission.

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes, following the order in which the bytes are transmitted or received. If the algorithm is applied bit-wise, the MSB is processed first in each byte. An example of this sequence is shown below:

1. Target address byte + write (02h)
2. Register address byte (00h)
3. Target address byte + read (03h)
4. Register address byte (00h)
5. Word 1 - byte 1 / 0x7C (lower 8 bits)
6. Word 1 - byte 2 / 0x00 (higher 8 bits)

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This sequence results in CRC = 0x36 being appended as the last CRC byte.

Although this byte of the fourth sequence does not exist in the actual read sequence, it must be added in the CRC calculation.

I²C Write

Figure 18 on page 40 shows how the byte is ordered in a write transaction. When CRC is enabled, the targeted register address is modified according to the payload, only if the CRC results match.

Cyclic Redundancy Check (CRC) in an I²C Write Transaction

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes following the order in which they are transmitted or received. If the algorithm is applied bit-wise, the MSB is processed first in each byte. An example of this sequence is shown below:

1. Target address byte + write (02h)
2. Register address byte (00h)
3. Word 1 - byte 1 / 0x7C (lower 8 bits)
4. Word 1 - byte 2 / 0x00 (higher 8 bits)

This sequence results in CRC = 0x72, which the host MCU should append as the last CRC byte to ensure a successful transaction.

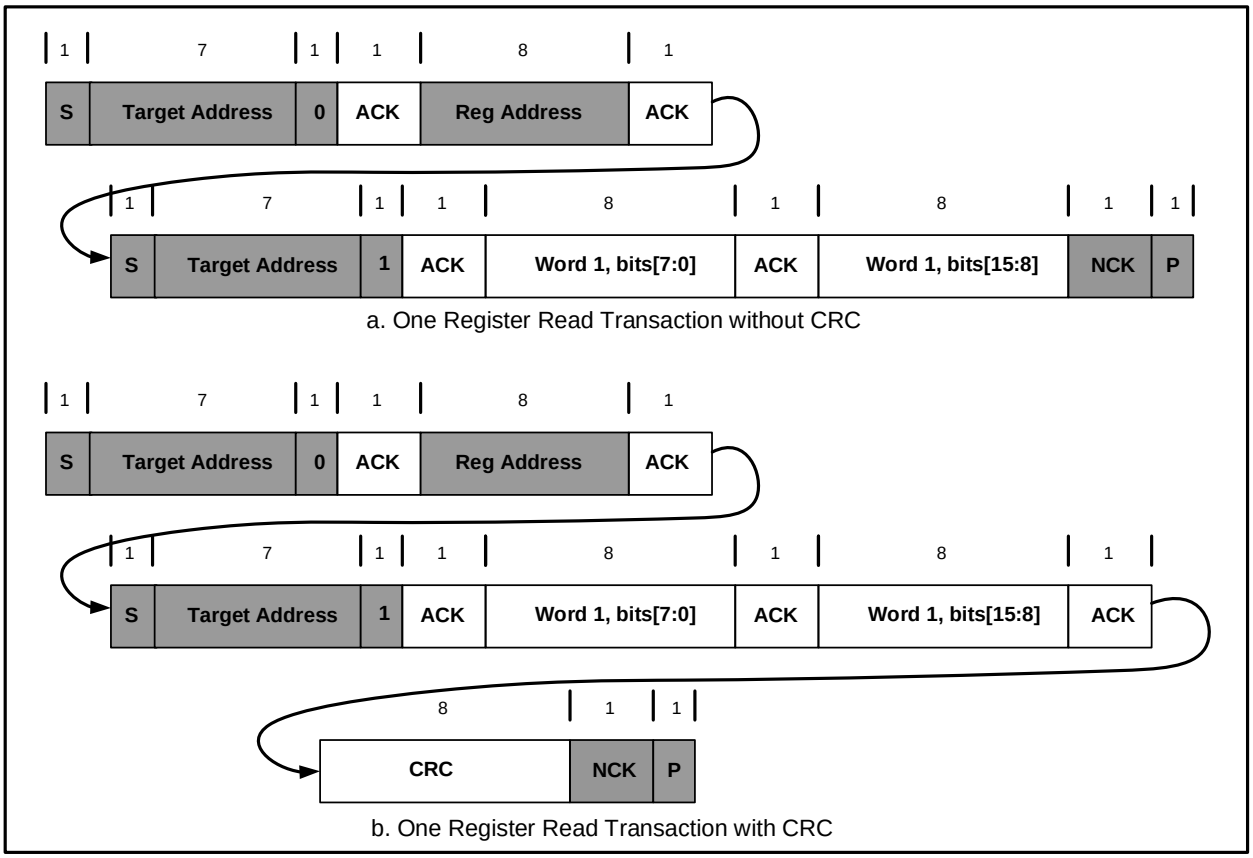


Figure 17: I²C Single Address Read

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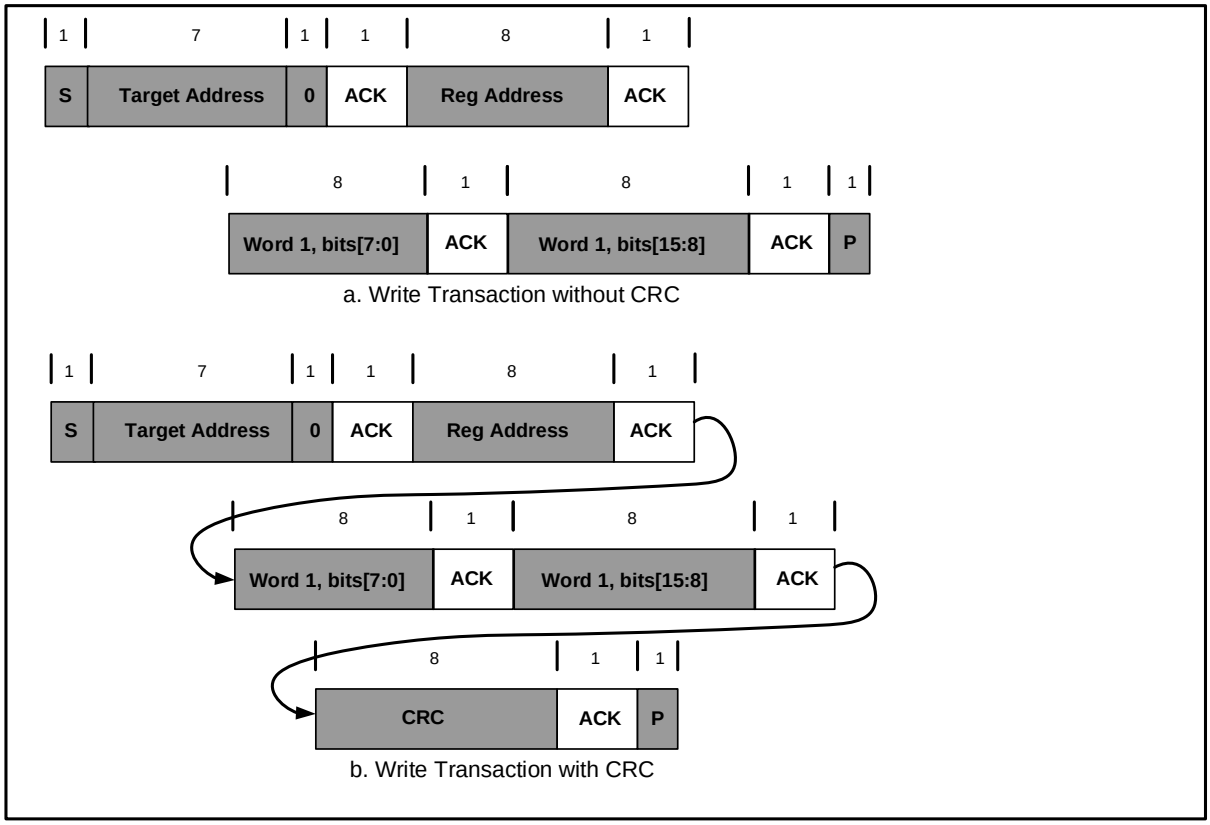


Figure 18: I²C Write Transaction

Serial Peripheral Interface (SPI)

The MP2795 has an interface that is compatible with serial peripheral interfaces (SPIs). This interface is configured to operate by setting the clock phase (CPHA) to 1 and by setting the clock polarity (CPOL) to 1. Consequently, data on SDI must be stable during SCK's rising edge. Words are transferred with the MSB first.

During a write transaction, the data value on SDI is latched to the device on SCK's rising edge. During a read transaction, the bit stream is presented on SDO with the MSB first and is valid during SCK's rising edge, while the SDO transitions on SCK's falling edge.

nCS must remain low for the entire command sequence duration, including the time between the command byte and subsequent data. During a write command, data is latched on nCS's rising edge (see Figure 19 on page 41).

SPI Data Protocol

For a successful SPI transaction, nCS must go low, and there must be a successful match between the transaction target address and the internally configured target address (located in DEVICE_ADD, set via A3h, bits[14:8]). The MP2795's SPI requires a specific transaction structure.

SPI Read

Read transactions should have the fields arranged with a matching order for the target address, read bit, register address, and data payload (see Figure 20 on page 42).

When CRC is enabled, the payload is limited to 2 bytes by default. This value can be increased to 63 words (126 bytes) using the XFR_NUM_RD_WORDS bits. Since the XFR_NUM_RD_WORDS bits retain the new value only for the next transaction, ensure that the next transaction uses the increased payload count.

Cyclic Redundancy Check (CRC) in an SPI Read Transaction

After completing the request for a read transaction, the host MCU must ensure that the CRC matches the value provided in the read transaction to confirm that no bits were corrupted during the transmission.

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The CRC-8 algorithm follows the polynomial (1 + $x^1 + x^2 + x^8$), and is applied byte-wise to the bytes, following the order in which bytes are transmitted or received. If the algorithm is applied bit-wise, the MSB is processed first in each byte. An example of this sequence is shown below:

1. Target address byte + read (03h)
2. Register address byte (00h)
3. Word 1 - byte 1 / 0x7C (lower 8 bits)
4. Word 1 - byte 2 / 0x00 (higher 8 bits)

This sequence results in CRC = 0x64 being appended as the last CRC byte.

SPI Write

Write transactions should have the fields arranged with a target address, write bit, register address, and data payload (see Figure 21 on page 42). When CRC is enabled, the SPI write payload is limited to 2 bytes, and targeted register addresses are modified according to the payload only if the CRC matches.

Cyclic Redundancy Check (CRC) in an SPI Write Transaction

The CRC-8 algorithm follows the polynomial (1 + $x^1 + x^2 + x^8$), and is applied byte-wise to the bytes following the order in which they are transmitted or received. If the algorithm is applied bit-wise, the MSB is processed first in each byte. An example of this sequence is shown below:

1. Target address byte + write (02h)
2. Register address byte (00h)
3. Word 1 - byte 1 / 0x7C (lower 8 bits)
4. Word 1 - byte 2 / 0x00 (higher 8 bits)

This sequence results in CRC = 0x72, which the host MCU should append as the last CRC byte to ensure a successful transaction.

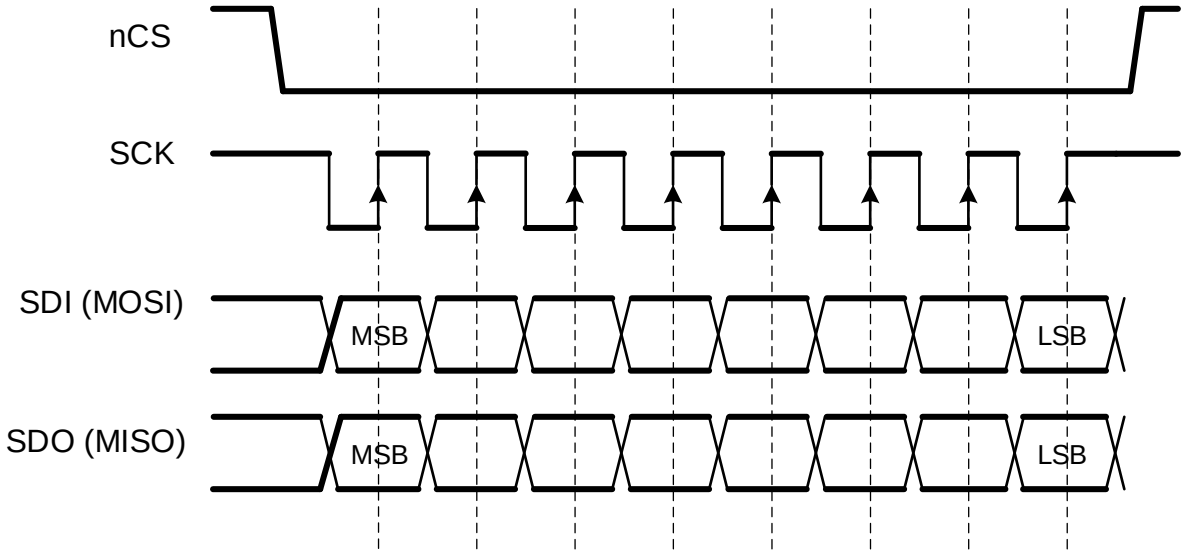
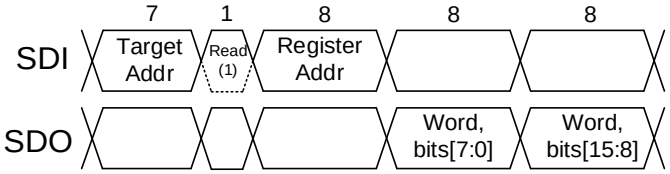


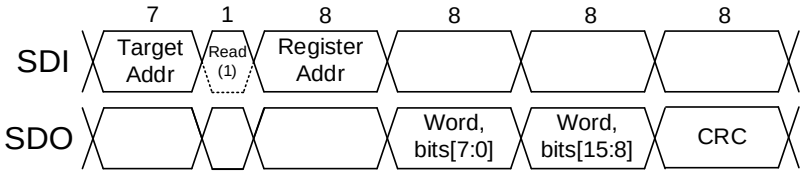
Figure 19: SPI Signal Sequencing

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SPI Read without CRC: 1 Word (2 Bytes)



SPI Read with CRC: 1 Word (2 Bytes) Payload



SPI Read with CRC: 2 Words (4 Bytes) Payload

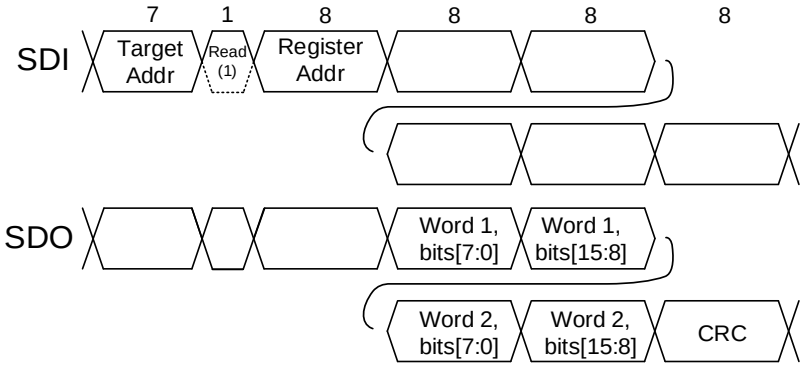
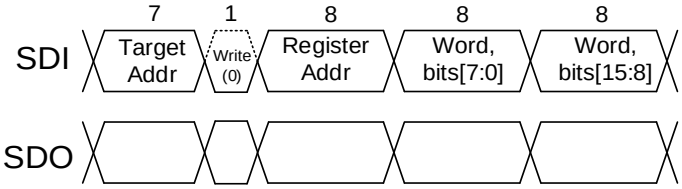


Figure 20: SPI Read Transaction

SPI Write without CRC: 1 Word (2 Bytes)



SPI Write with CRC: 1 Word (2 Bytes)

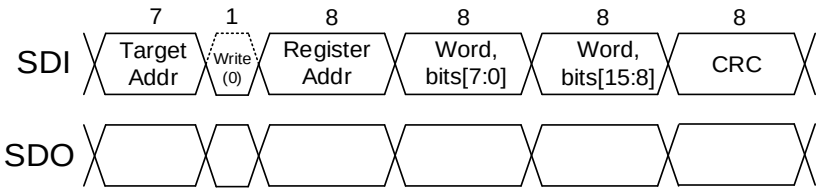


Figure 21: SPI Write Transaction

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REGISTER MAP

The default target address is 01h. The address can be configured by modifying DEVICE_ADD (A3h, bits[14:8]). Once the value is changed, the next communication should use the new address. The default address may be different for chips with varying -xxxx suffixes.

All the bits in an address that are not populated by a register should be treated as reserved bits. Their values should not be modified during write operations that are meant to change bits in the same address.

Refer to the MP279x User Guide for register details and more details on how to configure and control the MP2795.

CELLS_CTRL (00h)

Format: Unsigned binary

The CELLS_CTRL command controls the number of stacked cells in use.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3:0	R/W (can lock to read-only)	CELL_S_CTRL	4'b 1111	Sets the number of stacked cells in use. 0x0: Cell 7 to Cell 1 enabled 0x1: Cell 7 to Cell 1 enabled 0x2: Cell 7 to Cell 1 enabled 0x3: Cell 7 to Cell 1 enabled 0x4: Cell 7 to Cell 1 enabled 0x5: Cell 7 to Cell 1 enabled 0x6: Cell 7 to Cell 1 enabled 0x7: Cell 8 to Cell 1 enabled 0x8: Cell 9 to Cell 1 enabled 0x9: Cell 10 to Cell 1 enabled 0xA: Cell 11 to Cell 1 enabled 0xB: Cell 12 to Cell 1 enabled 0xC: Cell 13 to Cell 1 enabled 0xD: Cell 14 to Cell 1 enabled 0xE: Cell 15 to Cell 1 enabled 0xF: Cell 16 to Cell 1 enabled These bits allow the multiple-time programmable (MTP) memory.

PWR_STATUS (01h)

Format: Unsigned binary

The PWR_STATUS command reports the pack current status and the power state status.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:7	R	PACK_CURRENT_STATUS	3'b 010	Returns the pack current status. 0x1: The battery pack current is discharging 0x2: The battery pack current is in standby range, meaning it is within ±STBY_CUR_TH (06h, bits[2:1]) 0x4: The battery pack current is charging
6:5	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
4:0	R	PWR_STATE	5'b 00001	Returns the power state status. 0x01: Safe 0x02: Standby 0x04: Active 0x08: Fault mode 0x10: Recovery mode

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STB_STATUS (02h)

Format: Unsigned binary

The STB_STATUS command reports the voltage comparison result between the PACKP pin voltage (V_{PACKP}) and the VTOP pin voltage (V_{TOP}). It also reports the on/off setting for standby mode.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
10:8	R	PACKP_COMP_STS	3'b 000	Reports the voltage comparison result between V_{PACKP} and V_{TOP}. The exact voltage level for the transition can be slightly different based on the direction of the transition and the applied hysteresis. 0x4: $V_{PACKP} > V_{TOP}$ + 270mV 0x3: The PACKP comparator is invalid 0x2: V_{TOP} + 160mV > $V_{PACKP} > V_{TOP}$ - 1V 0x1: $V_{PACKP} < V_{TOP}$ - 1.6V 0x0: The comparison result is not available
7:1	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
0	R	STBY_STATE	1'b 0	Reports the on/off setting for standby mode. If turned off, the analog front-end (AFE) does not transition to standby mode from active mode, regardless of whether the current level is within the standby mode range. 0: Off 1: On

LOAD_CHARGER_STATUS (03h)

Format: Unsigned binary

The LOAD_CHARGER_STATUS command reports the charger/load plug-in detection process and result.

Bits	Access	Bit Name	Default	Description
15	R	CHG_IN	1'b 0	Reports the detected/not detected charger plug-in event. This bit can be cleared by writing 0 to CHG_LD_CLR (09h, bit[0]). 0: Not detected 1: Detected
14	R	LD_IN	1'b 0	Reports the detected/not detected load plug-in event. This bit can be cleared by writing 0 to CHG_LD_CLR. 0: Not detected 1: Detected
13	R	CHGDET_FAIL	1'b 0	Reports the outcome of PACKP detection pre-bias. When true, the charger plug-in detection could not pre-charge V_{PACKP} to V_{TOP} in the allocated time, meaning there is no engagement. When false, detection is in a different state. 0: False 1: True
12	R	LDDET_FAIL	1'b 0	Reports the outcome of PACKP detection pre-bias. When true, the load plug-in detection could not pre-charge V_{PACKP} to V_{TOP} in the allocated time, meaning there is no engagement. When false, detection is in a different state. 0: False 1: True
11:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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5	R	CHGDET_ENGAGED	1'b 0	Reports the status of PACKP detection pre-bias. When true, V_{PACKP} has reached V_{TOP} and is waiting to detect a plug-in. The state machine for charger plug-in detection is enabled, and the current source/sink is enabled. When false, detection is ineffective. 0: False 1: True
4	R	LDDET_ENGAGED	1'b 0	Reports the status of PACKP detection pre-bias. When true, V_{PACKP} has reached V_{TOP} and is waiting to detect a plug-in. The state machine for load plug-in detection is enabled, and the current source/sink is enabled. When false, detection is ineffective. 0: False 1: True
3	R	CHG_SETTLING	1'b 0	Reports the status of PACKP detection pre-charging. When true, V_{PACKP} is approaching V_{TOP} but has not reached it. The state machine for charger plug-in detection is enabled, and the current source/sink is enabled. When false, detection is in a different state. 0: False 1: True
2	R	LD_SETTLING	1'b 0	Reports the status of PACKP detection pre-charging. When true, V_{PACKP} is approaching V_{TOP} but has not reached it. The state machine for load plug-in detection is enabled, and the current source/sink is enabled. When false, detection is in a different state. 0: False 1: True
1	R	CHCONN_EN	1'b 0	Reports whether charger plug-in detection is enabled. 0: Disabled 1: Enabled
0	R	LDDET_EN	1'b 0	Reports whether load plug-in detection is enabled. 0: Disabled 1: Enabled

ACT_CFG (05h)

Format: Unsigned binary

The ACT_CFG command configures the MOSFET transition method, turn-on/-off command, control logic, and control method.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9	R/W (can lock to read-only)	FT_STATE_SEL	1'b 0	When this bit is set to 0, the MOSFETs' transition to start-up via a control source (depending on FET_SRC, set via bit[0] of this command), which is disabled then enabled. When this bit is set to 1, the MOSFETs start up depending on the control source status. 0: Rising edge 1: Level This bit allows one-time programmable (OTP) memory.
8:5	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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4:3	R/W	ACTIVE_CTRL	2'b 00	When FET_SRC is set to 0, and FET_CFG (bit[1] of this command) is set to 0: 0x0: All MOSFETs are off 0x1: The charge (CHG) and discharge (DSG) MOSFETs turn on 0x2: All MOSFETs are off 0x3: The CHG and DSG MOSFETs turn on When FET_SRC is set to 0, and FET_CFG is set to 1: 0x0: All MOSFETs are off 0x1: The DSG MOSFET turns on 0x2: The CHG MOSFET turns on 0x3: The CHG and DSG MOSFETs turn on These bits allow OTP.
2	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
1	R/W (can lock to read-only)	FET_CFG	1'b 1	Selects the CHG and DSG MOSFET control logic. 0: Simple mode. The internal logic automatically determines the turn-on/-off sequencing 1: Direct mode. In direct mode with pin control, GPIO1 controls the DSG MOSFET and GPIO2 controls the CHG MOSFET. When direct mode is selected and faults are enabled, the IC still uses the internal logic to turn off the MOSFETs This bit allows OTP.
0	R/W (can lock to read-only)	FET_SRC	1'b 0	Defines the source that enables the MOSFETs and switches to enter normal mode. The CHG and DSG MOSFETs are controlled by the host MCU, via either register or pin. 0: Register control 1: GPIOx pin control (GPIO1 or GPIO1 and GPIO2 depending on FET_CFG) This bit allows OTP.

STB_CFG (06h)

Format: Unsigned binary

The STB_CFG command enables standby mode and the standby current hysteresis. It also configures the standby current threshold and the refresh interval for voltage protection reading in standby or safe mode.

Bits	Access	Bit Name	Default	Description
15:6	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
5:4	R/W (can lock to read-only)	STBY_MONITOR_CFG	2'b 10	Selects the interval used for voltage protection monitoring to refresh the analog-to-digital converter (ADC) reading while in standby or safe mode. 0x0: Voltage protection readings are refreshed every 254ms 0x1: Voltage protection readings are refreshed every 492ms 0x2: Voltage protection readings are refreshed every 968ms 0x3: Disabled These bits allow OTP.
3	R/W	STBY_HYS	1'b 0	Enables digital hysteresis on the standby current comparator. 0: Disabled 1: Enabled This bit allows OTP.

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2:1	R/W	STBY_CUR_TH	2'b 01	Sets the standby comparator current threshold. 0x0: 250μV 0x1: 375μV 0x2: 500μV 0x3: 625μV These bits allow OTP.
0	R/W (can lock to read-only)	STBY_STATE_EN	1'b 0	Enables standby mode. When disabled, the device cannot enter standby mode. 0: Disabled 1: Enabled This bit allows OTP.

SAFE_CFG (07h)

Format: Unsigned binary

The SAFE_CFG command enables over-current (OC), short-circuit, and voltage protection monitoring in safe mode. It also configures the refresh interval for voltage protection reading in normal mode.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3	R/W	ACTIVE_MONITOR_CFG	1'b 0	Selects the interval used for voltage protection monitoring to refresh the ADC reading in active mode or fault mode. 0x0: Voltage protection readings are refreshed every 254ms 0x1: Voltage protection readings are refreshed every 135ms
2	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
1	R/W	SAFE_SCOC_EN	1'b 0	Enables short-circuit and OC monitoring, even in safe mode. This function is disabled by default since the MOSFETs are disabled in safe mode. If enabled, current consumption increases. 0: Disabled 1: Enabled
0	R/W	PROTECT_IN_SAFE_CFG	1'b 0	Enables voltage protection monitoring in safe mode. 0: Disabled 1: Enabled This bit allows OTP.

RGL_CFG (08h)

Format: Unsigned binary

The RGL_CFG command enables 3V3 in shutdown mode and reports its status.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
3	R	V3P3_SHOFF_STS	1'b 1	Reports the internal enable or disable control for the 3.3V regulator in shutdown mode. When enabled, the 3.3V rails remain on even in shutdown mode. 0: Off 1: On
2	R/W (can lock to read-only)	V3D3_SHDN_EN	1'b 1	Enables the 3.3V regulator during shutdown mode. 0: Disabled 1: Enabled This bit allows OTP.

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1:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

LOAD_CHARGER_CFG (09h)

Format: Unsigned binary

The LOAD_CHARGER_CFG command enables charger and load plug-in detection, the PACKP and TOP voltage comparator, and charger detection in standby mode. This command configures the PACKP pre-charging time and reports the load/charger plug-in detection, in addition to clearing the charger/load detection status and reporting whether load/charger detection is complete.

Bits	Access	Bit Name	Default	Description
15	R/W	PACKP_CMP_EN	1'b 0	Enables the PACKP vs. TOP voltage comparator. When disabled, the comparator can still be internally enabled for other functions, such as plug-in detection. 0: Disabled 1: Enabled This bit allows OTP.
14:11	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
10:8	R/W	T_PLUGIN_ PRECHARGE_MAX	3'b 101	Selects the PACKP pre-charging expiration timer. 0x0: 0.2s 0x1: 0.4s 0x2: 0.8s 0x3: 1.6s 0x4: 3.2s 0x5: 6.4s 0x6: 12s 0x7: 24s These bits allow OTP.
7:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
5	R/W (can lock to read-only)	CH_CONN_P_SBY	1’b 0	Enables charger detection in standby mode. 0: Disabled 1: Enabled This bit allows OTP.
4	R	LD_DET_DONE_STS	1'b 0	Indicates whether load plug-in detection is complete. 0: Not completed 1: Completed
3	R	CHG_DET_DONE_ STS	1'b 0	Indicates whether charger plug-in detection is complete. 0: Not completed 1: Completed
2	R/W (can lock to read-only)	LD_PLUGIN_DET_ EN	1'b 0	Enables load plug-in detection. If this detection is re-enabled, this bit must be written to 0 and then written to 1 again. 0: Disabled 1: Enabled This bit allows OTP.
1	R/W (can lock to read-only)	CH_PLUGIN_DET_ EN	1'b 0	Enables charger plug-in detection. If this detection is re-enabled, this bit must be written to 0 and then written to 1 again. 0: Disabled 1: Enabled This bit allows OTP.

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0	W	CHG_LD_CLR	1'b 0	Write to this bit to clear the detection function status bits. This bit clears itself. This command does not clear the interrupt function, meaning CONN_DET_INT_CLEAR (17h, bit[13]) must be used.

GPIO_STATUS (0Ah)

Format: Unsigned binary

The GPIO_STATUS command reports the GPIO status (high/low).

Bits	Access	Bit Name	Default	Description
15:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R	GPIO3	1'b 0	Reports the GPIO3 pin status. 0: Low 1: High
1	R	GPIO2	1'b 0	Reports the GPIO2 pin status. 0: Low 1: High
0	R	GPIO1	1'b 0	Reports the GPIO1 pin status. 0: Low 1: High

GPIO_OUT (0Bh)

Format: Unsigned binary

The GPIO_OUT command controls the output level for GPIO.

Bits	Access	Bit Name	Default	Description
15:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R/W (can lock to read-only)	GPIO3_O	1'b 0	Sets the target output level for GPIO3 (high or low). This bit is effective only when GPIO3 is used as a digital output (GPIO3_IO is set to the output). 0: Low 1: High This bit allows OTP.
1	R/W	GPIO2_O	1'b 0	Sets the target output level for GPIO2 (high or low). This bit is effective only when GPIO2 is used as a digital output (GPIO2_IO is set to output). 0: Low 1: High This bit allows OTP.
0	R/W	GPIO1_O	1'b 0	Sets the target output level for GPIO1 (high or low). This bit is effective only when GPIO1 is used as a digital output (GPIO1_IO is set to output). 0: Low 1: High This bit allows OTP.

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GPIO_CFG (0Ch)

Format: Unsigned binary

The GPIO_CFG command enables the pull-up capability of GPIO1 to GPIO3. This command also defines the direction and the type of input for GPIO1 to GPIO3.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11	R/W (can lock to read-only)	GPIO3_FSEL	1'b 0	Defines the function of GPIO3. 0: GPIO 1: Fault indicator. Valid when GPIO3 is set to be an output This bit allows OTP.
10	R/W (can lock to read-only)	GPIO3_PUP	1'b 0	Enables the GPIO3 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO3. 0: Disabled 1: Enabled This bit allows OTP.
9	R/W (can lock to read-only)	GPIO3_TYPE	1'b 0	Defines the type of input for GPIO3. 0: Digital input 1: Buffered ADC input with 3.3V range This bit allows OTP.
8	R/W (can lock to read-only)	GPIO3_IO	1'b 0	Defines the direction for GPIO3. 0: Output 1: Input This bit allows OTP.
7	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
6	R/W (can lock to read-only)	GPIO2_PUP	1'b 0	Enables the GPIO2 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO2. 0: Disabled 1: Enabled This bit allows OTP.
5	R/W (can lock to read-only)	GPIO2_TYPE	1'b 0	Defines the type of input for GPIO2. 0: Digital input 1: Buffered ADC input with 3.3V range This bit allows OTP.
4	R/W (can lock to read-only)	GPIO2_IO	1'b 0	Defines the direction for GPIO2. 0: Output 1: Input This bit allows OTP.
3	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
2	R/W (can lock to read-only)	GPIO1_PUP	1'b 0	Enables the GPIO1 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO1. 0: Disabled 1: Enabled This bit allows OTP.

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1	R/W (can lock to read-only)	GPIO1_TYPE	1'b 0	Defines the type of input for GPIO1. 0: Digital input 1: Buffered ADC input with 3.3V range This bit allows OTP.
0	R/W (can lock to read-only)	GPIO1_IO	1'b 0	Defines the direction for GPIO1. 0: Output 1: Input This bit allows OTP.

PINS_CFG (0Dh)

Format: Unsigned binary

The PINS_CFG command defines the pull-up voltage of GPIO1 to GPIO3. This command also sets the behavior of the WDT pin and xALERT pin.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
8	R/W (can lock to read-only)	GPIO_LV_CFG	1'b 0	Sets the GPIO1 to GPIO3 pull-up voltage. 0: 3V3 1: REGIN This bit allows OTP.
7	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
6	R/W (can lock to read-only)	WDT_RST_EN	1'b 1	Enables the WDT pin to reset the MP2797A back to its factory settings. When disabled, a watchdog timer pulse caused by a watchdog bite does not trigger a reset. 0: Disabled 1: Enabled This bit allows OTP.
5	R/W (can lock to read-only)	WDT_RPT	1'b 1	Enables a watchdog bite event triggers the WDT pin to toggle a high pulse. 0: Disabled 1: Enabled This bit allows OTP.
4:1	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
0	R/W (can lock to read-only)	ALERT_POL	1'b 1	Sets the polarity of the xALERT pin when the interrupt is pending. 0: Active low. xALERT goes low when an interrupt is pending 1: Active high. xALERT goes high when an interrupt is pending This bit allows OTP.

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WDT_STATUS (0Eh)

Format: Unsigned binary

The WDT_STATUS command reports the watchdog timer status.

Bits	Access	Bit Name	Default	Description
15:2	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
1	R	WDT_BITE	1'b 0	Indicates whether the bite timer has expired and a bite event has occurred. This event toggles the WDT pin if WDT_RPT (0Dh, bit[5]) is enabled. 0: False 1: True
0	R	WDT_BARKED	1'b 0	Indicates whether the bark timer has expired and a bark event has occurred. 0: False 1: True

WDT_RST (0Fh)

Format: Unsigned binary

The WDT_RST command controls the reset of the watchdog timer.

Bits	Access	Bit Name	Default	Description
15:1	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
0	W	WDT_RST	1'b 0	Writing 1 to this bit resets the watchdog timer counter and clears WDT_BITE (0Eh, bit[1]) and WDT_BARKED (0Eh, bit[0]). This is a self-clearing register.

WDT_CFG (10h)

Format: Unsigned binary

The WDT_CFG command enables watchdog timer communication and configures the watchdog timer bite and bark timeout.

Bits	Access	Bit Name	Default	Description
15:9	R/W (can lock to read-only)	WDT_BITE_CFG	7'b 1011110	Configures the watchdog bite timeout. The bite setting defines the delay from the bark to the bite. Least significant bit (LSB): 25ms Offset: 25ms Range: 25ms to 3200ms Value (ms) = Setting x 25 + 25 These bits allow OTP.
8:2	R/W (can lock to read-only)	WDT_BARK_CFG	7'b 0110110	Configures the watchdog bark timeout. The bark setting defines the delay from the last watchdog reset to the bark. LSB: 25ms Offset: 25ms Range: 25ms to 3200ms Value (ms) = Setting x 25 + 25 These bits allow OTP.
1	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
0	R/W (can lock to read-only)	WDT_COM_CTRL	1'b 0	Enables watchdog communication. 0: Disabled 1: Enabled This bit allows OTP.

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FET_STATUS (11h)

Format: Unsigned binary

The FET_STATUS reports the status of the DSG driver, CHG driver, and charge pump.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11	R	CP_STS	1'b 0	Indicates the charge pump's status. 0: Off 1: On
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
9	R	DSG_DRV_TRANS	1'b 0	Reports whether the DSG driver is changing states. 0: The DSG driver is settled (off or at its target voltage) 1: The DSG driver is changing states
8	R	CHG_DRV_TRANS	1'b 0	Reports whether the CHG driver is changing states. 0: The CHG driver is settled (off or at its target voltage) 1: The CHG driver is changing states
7:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3	R	FET_TIMEOUT	1'b 0	When true, an issue was detected during the latest turn-on attempt. 0: False 1: True
2	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
1	R	DSG_DRV	1'b 0	Reports whether the DSG driver is on or off. 0: Off 1: On
0	R	CHG_DRV	1'b 0	Reports whether the CHG driver is on or off. 0: Off 1: On

FET_MODE (13h)

Format: Unsigned binary

The FET_MODE configures soft start (SS) for the CHG and DSG MOSFETs.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11	R/W (can lock to read-only)	CHG_SOFTON_ OC_LIM	1'b 0	Sets the OC threshold that is only applicable when the CHG MOSFET enters SS. 0: 3.6mV 1: 4.8mV This bit allows OTP.
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
9	R/W (can lock to read-only)	TURNON_ TIMEOUT_FAULT	1'b 0	Enables the driver’s fault report for the turn-on timeout. 0: Disabled 1: Enabled This bit allows OTP.

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8	R/W (can lock to read-only)	CHG_TURNON_TIMER	1'b 1	Sets the CHG MOSFET's SS timeout. 0: 25ms 1: 50ms This bit allows OTP.
7:5	R/W	TURNON_TIMEOUT	3'b 000	Sets the MOSFET turn-on timeout delay. Applies to both the CHG and DSG MOSFETs. This function is paused during SS. LSB: 20ms Offset: 40ms Range: 40ms to 180ms Value (ms) = Setting x 20 + 40 These bits allow OTP.
4	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
3	R/W (can lock to read-only)	FET_ON_RUN_SC_DET_EN	1'b 1	Enables the short-circuit detection sequence prior to the MOSFET turning on. If detection is enabled and the device detects that PACKP is shorted to ground, then a MOSFET driver fault is generated. The associated MOSFET driver bit can be manually cleared with DRIVER_FAULT_CLR (60h, bit[13]). 0: Disabled 1: Enabled This bit allows OTP.
1:2	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
0	R/W (can lock to read-only)	DSG_SOFTON_EN	1'b 1	Enables SS for the DSG MOSFET driver. 0: Disabled 1: Enabled This bit allows OTP.

FET_CFG (14h)

Format: Unsigned binary

The FET_CFG command configures the driver voltages and SS of the CHG and DSG MOSFET.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:12	R/W (can lock to read-only)	FET_DRV_LVL	3'b 110	Defines the gate-source voltage (V_{GS}) for the CHG and DSG MOSFETs. 0x0: 7V 0x1: 8V 0x2: 9V 0x3: 10V 0x4: 11V 0x5: 12V 0x6: 12V 0x7: 12V These bits allow OTP.
11:9	R/W (can lock to read-only)	CHG_SOFTON_PUP	3'b 100	Sets the pull-up current during the CHG MOSFET's SS. LSB: 1μA Offset: 3μA Range: 3μA to 10μA Value (μA) = Setting + 3 These bits allow MTP.

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8:6	R/W	RAMP_UP_SC_GF	3'b 011	Sets the deglitch filter for the standby comparator current threshold when the DSG N-channel MOSFET is ramping up during SS. 3'b000: 100µs 3'b001: 200µs 3'b010: 400µs 3'b011: 800µs 3'b100: 1200µs 3'b101: 2400µs 3'b110: 2400µs 3'b111: 2400µs These bits allow OTP.
5:4	R/W	STBY_SC_CUR_TH	2'b 11	Sets the standby comparator current threshold, which functions as a protection against excessive current while the DSG N-channel MOSFET ramps up during SS. 0x0: 250µV 0x1: 375µV 0x2: 500µV 0x3: 625µV These bits allow OTP.
3	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
2:0	R/W (can lock to read-only)	DSG_SOFTON_DV	3'b 000	Sets the discharge MOSFET turn-on slope. 3'b000: 0.1V/ms 3'b001: 0.2V/ms 3'b010: 0.4V/ms 3'b011: 0.6V/ms 3'b100: 0.8V/ms 3'b101: 1.0V/ms 3'b110: 1.2V/ms 3'b111: 1.6V/ms These bits allow MTP.

RD_INT0 (15h)

Format: Unsigned binary

The RD_INT0 command reports interrupts, such as current status changes, charger/load detection, Coulomb counting, ADC, AFE status changes, fault recovery, watchdog, cell negative temperature coefficient (NTC) hot, cell NTC cold, short-circuit, over-current (OC), pack over-voltage (OV), pack under-voltage (UV), cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14	R	PACK_CURRENT_INT_STS	1'b 0	Reports whether an interrupt related to a battery pack current change has been detected. The pack current changes when switching between discharge, standby, and charge mode, which is reported in PACK_CURRENT_STATUS (01h, bits[9:7]). 0: Not detected 1: Detected
13	R	CONN_DET_INT_STS	1'b 0	Reports whether an interrupt related to charger or load plug-in detection has been detected. 0: Not detected 1: Detected

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12	R	CC_ACC_INT_STS	1'b 0	Reports whether an interrupt related a new Coulomb counting accumulation value has occurred, and updated CC_ACC_LSBS (65h, bits[15:0]) and CC_ACC_MSBS (66h, bits[9:0]). 0: Not detected 1: Detected
11	R	VSCAN_DONE_ INT_STS	1'b 0	Reports whether an interrupt related to a high-resolution voltage scan has been detected. 0: Not detected 1: Detected
10	R	AFE_MODE_ CHANGE_INT_STS	1'b 0	Reports whether an interrupt related to an AFE mode change has been detected. A mode change is defined as a change between any of the modes (e.g. safe, normal A/B/C, standby). 0: Not detected 1: Detected
9	R	RECOVERED_INT_ STS	1'b 0	Reports whether an interrupt related to a fault recovery event from normal C state has been detected. 0: Not detected 1: Detected
8	R	WDT_INT_STS	1'b 0	Reports whether an interrupt related to watchdog communication has been detected. A watchdog bark and a watchdog bite event can both trigger a watchdog event interrupt. 0: Not detected 1: Detected
7	R	NTC_HOT_INT_STS	1'b 0	Reports whether an interrupt related to a cell NTC hot event has been detected. This signal is generated by combining interrupt detection for all four NTC channels. NTC1_VALUE (42h, bits[9:0]), NTC2_VALUE (41h, bits[9:0]), NTC3_VALUE (40h, bits[9:0]), and NTC4_VALUE (3Fh, bits[9:0]) can be read to identify the source of the interrupt. 0: Not detected 1: Detected
6	R	NTC_COLD_INT_ STS	1'b 0	Reports whether an interrupt related to a cell NTC cold event has been detected. This signal is generated by combining interrupt detection for all four NTC channels. NTC1_VALUE, NTC2_VALUE, NTC3_VALUE, and NTC4_VALUE can be read to identify the source of the interrupt. 0: Not detected 1: Detected
5	R	SHORT_CURR_INT_ STS	1'b 0	Reports whether an interrupt related to a short-circuit event has been detected. This signal is generated by combining interrupt detection for discharge short-circuit and charge short-circuit. SC_CHG_STS (27h, bit[1]) and SC_DCHG_STS (27h, bit[0]) should be checked to identify the source of the interrupt. 0: Not detected 1: Detected
4	R	OVER_CURR_INT_ STS	1'b 0	Reports whether an interrupt related to an OC event has been detected. This signal is generated by combining interrupt detection for discharge OC and charge OC. OC1_DCHG_STS (20h, bit[0]), OC2_DCHG_STS (20h, bit[1]), and OC_CHG_STS (20h, bit[2]) should be checked to identify the source of the interrupt. 0: Not detected 1: Detected

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3	R	VTOP_OV_INT_STS	1'b 0	Reports whether an OV interrupt related to the battery stack positive terminal (VTOP to AGND) has been detected. 0: Not detected 1: Detected
2	R	VTOP_UV_INT_STS	1'b 0	Reports whether a UV interrupt related to the battery stack positive terminal (VTOP to AGND) has been detected. 0: Not detected 1: Detected
1	R	CELL_UV_INT_STS	1'b 0	Reports whether an interrupt related to a cell UV event has been detected. The flags located in the RD_CELL_UV (2Dh) command should be checked to identify which cell caused the interrupt. 0: Not detected 1: Detected
0	R	CELL_OV_INT_STS	1'b 0	Reports whether an interrupt related to a cell OV event has been detected. The flags located in the RD_CELL_OV (2Eh) command should be checked to identify which cell caused the interrupt. 0: Not detected 1: Detected

RD_INT1 (16h)

Format: Unsigned binary

The RD_INT1 command reports interrupts, such as driver error, pack voltage changes, balancing done, ADC self-diagnostics, scheduler errors, NTC hot PCB monitoring, a digital die temperature, cell mismatch, dead cell, open-wire detection, VDD UV, 3V3 UV, REGIN UV, and one-time programmable (OTP) cyclic redundancy check (CRC) events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
13	R	FET_DRIVER_INT_STS	1'b 0	Reports whether an interrupt related to a MOSFET driver error has been detected. MOSFET driver errors cover the following conditions: • MOSFET timeout • An issue during CHG or DSG SS, such as a short-circuit or OC condition 0: Not detected 1: Detected
12	R	PACKP_V_INT_STS	1'b 0	Reports whether an interrupt related to a V_{PACKP} change event has been detected. 0: Not detected 1: Detected
11	R	BAL_DONE_INT_STS	1'b 0	Reports whether an interrupt related to a cell-balancing done event has been detected. 0: Not detected 1: Detected
10	R	SELF_TEST_INT_STS	1'b 0	Reports whether an interrupt related to an ADC self-diagnostic event has been detected. The SELF_TEST_STS_OV (4Eh, bit[1]) and SELF_TEST_STS_UV (4Eh, bit[0]) flags should be checked to identify the cause of the interrupt. 0: Not detected 1: Detected

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9	R	FSM_ERROR_INT_STS	1'b 0	Reports whether an interrupt related to a scheduler error event has been detected. 0: Not detected 1: Detected
8	R	PCB_MNTR_HOT_INT_STS	1'b 0	Reports whether an interrupt related to the NTC hot PCB monitor has been detected. NTC1_PCB_MNTR_HOT_STS (3Eh, bit[8]), NTC2_PCB_MNTR_HOT_STS (3Eh, bit[9]), NTC3_PCB_MNTR_HOT_STS (3Eh, bit[10]), and NTC4_PCB_MNTR_HOT_STS (3Eh, bit[11]) should be checked to identify which NTC caused the interrupt. 0: Not detected 1: Detected
7	R	DIE_TEMP_INT_STS	1'b 0	Reports whether an interrupt related to a digital die temperature event has been detected. 0: Not detected 1: Detected
6	R	CELL_MISMATCH_INT_STS	1'b 0	Reports whether an interrupt related to a cell mismatch has been detected. Flags in the RD_CELL_MSMT (2Fh) command and CELL_MSMT_LOWER (33h, bits[13:10]) should be read to identify the cells triggering the event. 0: Not detected 1: Detected
5	R	CELL_DEAD_INT_STS	1'b 0	Reports whether an interrupt related to a dead cell has been detected. 0: Not detected 1: Detected
4	R	OPEN_WIRE_INT_STS	1'b 0	Reports whether an interrupt related to an open-wire event has been detected. The open wire status registers (located in the RD_OPENH (53h) and RD_OPENL (54h) commands) must be checked to determine whether there are disconnected wires. 0: Not detected 1: Detected
3	R	VDD_INT_STS	1'b 0	Reports whether an interrupt related to a UV condition on VDD has been detected. A VDD UV event can be triggered by either ADC voltage monitoring or the VDD UV comparator. The VDD analog comparator is always enabled, meaning when VDD_INT_EN (1Ah, bit[3]) is enabled, it can trigger an interrupt even if VDD_EN (56h, bit[2]) is disabled. 0: Not detected 1: Detected
2	R	3V3_INT_STS	1'b 0	Reports whether an interrupt related to a UV condition on 3V3 has been detected. This is triggered by monitoring the 3V3 ADC or the 3.3V analog comparator. The 3.3V UV analog comparator is always enabled, meaning when 3V3_INT_EN (1Ah, bit[2]) is enabled, it can trigger an interrupt even if 3V3_EN (56h, bit[1]) is disabled. 0: Not detected 1: Detected

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1	R	REGIN_INT_STS	1'b 0	Reports whether an interrupt related to a UV condition on REGIN has been detected. 0: Not detected 1: Detected
0	R	OTP_CRC_EVENT_INT_STS	1'b 0	Reports whether an interrupt related to an OTP memory CRC fault has been detected. When enabled, this interrupt can be triggered by the following conditions: The OTP CRC calculation fails while restoring the OTP. OTP CRC is manually triggered using NVM_CRC_DO (55h, bit[0]). In this scenario, an interrupt event is generated when CRC is completed (for either passing or failing). 0: Not detected 1: Detected

INT0_CLR (17h)

Format: Unsigned binary

The INT0_CLR command clears the interrupts, such as pack current change, charger/load connection, CC done, ADC done, AFE mode change, fault recovery, watchdog, cell NTC hot, cell NTC cold, short-circuit, over-current, pack OV, pack UV, cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14	W	PACK_CURRENT_INT_CLEAR	1'b 0	Write 1 to this bit to clear a battery pack current change interrupt. This is a self-clearing register.
13	W	CONN_DET_INT_CLEAR	1'b 0	Write 1 to this bit to clear a charger/load connection interrupt. This is a self-clearing register.
12	W	CC_ACC_STS_INT_CLEAR	1'b 0	Write 1 to this bit to clear a CC done interrupt. This is a self-clearing register.
11	W	VSCAN_DONE_INT_CLEAR	1'b 0	Write 1 to this bit to clear a completed high-resolution voltage scan interrupt. This is a self-clearing register.
10	W	AFE_MODE_CHANGE_INT_CLEAR	1'b 0	Write 1 to this bit to clear an AFE mode change interrupt. This is a self-clearing register.
9	W	RECOVERED_INT_CLEAR	1'b 0	Write 1 to this bit to clear a fault recovery interrupt. This is a self-clearing register.
8	W	WDT_INT_CLEAR	1'b 0	Write 1 to this bit to clear a watchdog event interrupt. This is a self-clearing register.
7	W	NTC_HOT_INT_CLEAR	1'b 0	Write 1 to this bit to clear a cell NTC hot monitor interrupt. This is a self-clearing register.
6	W	NTC_COLD_INT_CLEAR	1'b 0	Write 1 to this bit to clear a cell NTC cold monitor interrupt. This is a self-clearing register.
5	W	SHORT_CURR_INT_CLEAR	1'b 0	Write 1 to this bit to clear a short-circuit interrupt. This is a self-clearing register.
4	W	OVER_CURR_INT_CLEAR	1'b 0	Write 1 to this bit to clear an OC interrupt. This is a self-clearing register.
3	W	VTOP_OV_INT_CLEAR	1'b 0	Write 1 to this bit to clear a battery pack OV interrupt. This is a self-clearing register.
2	W	VTOP_UV_INT_CLEAR	1'b 0	Write 1 to this bit to clear a battery pack UV interrupt. This is a self-clearing register.
1	W	CELL_UV_INT_CLEAR	1'b 0	Write 1 to this bit to clear a cell UV interrupt. This is a self-clearing register.

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0	W	CELL_OV_INT_ CLEAR	1'b 0	Write 1 to this bit to clear a cell OV interrupt. This is a self-clearing register.

INT1_CLR (18h)

Format: Unsigned binary

The INT1_CLR command clears the interrupts, such as driver error, pack voltage change, balancing done, ADC self-diagnostic, scheduler error, NTC hot PCB monitor, cell mismatch, dead cell, open-wire detection, VDD UV, 3V3 UV, REGIN UV, and OTP CRC events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
13	W	FET_DRIVER_INT_ CLEAR	1'b 0	Write 1 to this bit to clear a MOSFET driver event interrupt. This is a self-clearing register.
12	W	PACKP_V_INT_ CLEAR	1'b 0	Write 1 to this bit to clear a V_{PACKP} change interrupt. This is a self-clearing register.
11	W	BAL_DONE_INT_ CLEAR	1'b 0	Write 1 to this bit to clear a balancing done interrupt. This is a self-clearing register.
10	W	SELF_TEST_INT_ CLEAR	1'b 0	Write 1 to this bit to clear a self-diagnostic interrupt. This is a self-clearing register.
9	W	FSM_ERROR_INT_ CLEAR	1'b 0	Write 1 to this bit to clear a schedule error interrupt. This is a self-clearing register.
8	W	PCB_MNTR_TEMP_ INT_CLEAR	1'b 0	Write 1 to this bit to clear an NTC hot PCB monitor interrupt. This is a self-clearing register.
7	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
6	W	CELL_MISMATCH_ INT_CLEAR	1'b 0	Write 1 to this bit to clear a mismatched cell interrupt. This is a self-clearing register.
5	W	CELL_DEAD_INT_ CLEAR	1'b 0	Write 1 to this bit to clear a dead cell interrupt. This is a self-clearing register.
4	W	OPEN_WIRE_INT_ CLEAR	1'b 0	Write 1 to this bit to clear an open wire interrupt. This is a self-clearing register.
3	W	VDD_INT_CLEAR	1'b 0	Write 1 to this bit to clear a VDD UV interrupt. This is a self-clearing register.
2	W	3V3_INT_CLEAR	1'b 0	Write 1 to this bit to clear a 3V3 UV interrupt. This is a self-clearing register.
1	W	REGIN_INT_CLEAR	1'b 0	Write 1 to this bit to clear a REGIN interrupt. This is a self-clearing register.
0	W	OTP_CRC_EVENT_ INT_CLEAR	1'b 0	Write 1 to this bit to clear an OTP CRC interrupt. This is a self-clearing register.

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INT0_EN (19h)

Format: Unsigned binary

The INT0_EN command enables the interrupts, such as interrupt reports to xALERT, pack current direction changes, charger/load connection, Coulomb counting accumulation, ADC voltage scan completion, AFE mode change, fault recovery, watchdog communication, cell NTC hot and cold monitoring, short-circuit, OC, pack OV, pack UV, cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	R/W (can lock to read-only)	INT_ALERT_CTRL	1'b 1	Enables interrupt reporting to the xALERT pin. 0: Disabled 1: Enabled This bit allows OTP.
14	R/W	PACK_CURRENT_INT_EN	1'b 0	Enables interrupt reporting for battery pack current direction changes. 0: Disabled 1: Enabled
13	R/W	CONN_DET_INT_EN	1'b 0	Enables interrupt reporting for charger/load connection. 0: Disabled 1: Enabled
12	R/W	CC_ACC_INT_EN	1'b 0	Enables interrupt reporting for Coulomb counting accumulation. 0: Disabled 1: Enabled
11	R/W	VSCAN_DONE_INT_EN	1'b 0	Enables interrupt reporting for high-resolution ADC voltage scan completion. 0: Disabled 1: Enabled
10	R/W	AFE_MODE_CHANGE_INT_EN	1'b 0	Enables interrupt reporting an AFE mode change. 0: Disabled 1: Enabled
9	R/W	RECOVERED_INT_EN	1'b 0	Enables interrupt reporting for fault recovery. 0: Disabled 1: Enabled
8	R/W	WDT_INT_EN	1'b 0	Enables interrupt reporting for watchdog communication. 0: Disabled 1: Enabled
7	R/W	NTC_HOT_INT_EN	1'b 0	Enables interrupt reporting for cell NTC hot monitoring conditions. 0: Disabled 1: Enabled
6	R/W	NTC_COLD_INT_EN	1'b 0	Enables interrupt reporting for cell NTC cold monitoring conditions. 0: Disabled 1: Enabled
5	R/W	SHORT_CURR_INT_EN	1'b 0	Enables interrupt reporting for short-circuit conditions. There are individual enable/disable control bits: SC_CHG_INT_EN (2Ah, bit[3]) and SC_DCHG_INT_EN (2Ah, bit[2]). This bit functions as a master enabler, meaning it must be enabled for the charger and discharge interrupt to work. 0: Disabled 1: Enabled

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4	R/W	OVER_CURR_INT_EN	1'b 0	Enables interrupt reporting for OC conditions. There are individual enable/disable control bits: OC_CHG_INT_EN (23h, bit[5]), OC2_DCHG_INT_EN (23h, bit[4]), and OC1_DCHG_INT_EN (23h, bit[3]). This bit functions as a master enabler, meaning it must be enabled for the charger and discharge interrupt to work. 0: Disabled 1: Enabled
3	R/W	VTOP_OV_INT_EN	1'b 0	Enables interrupt reporting for battery pack OV conditions. 0: Disabled 1: Enabled
2	R/W	VTOP_UV_INT_EN	1'b 0	Enables interrupt reporting for battery pack UV conditions. 0: Disabled 1: Enabled
1	R/W	CELL_UV_INT_EN	1'b 0	Enables interrupt reporting for cell UV conditions. 0: Disabled 1: Enabled
0	R/W	CELL_OV_INT_EN	1'b 0	Enables interrupt reporting for cell OV conditions. 0: Disabled 1: Enabled

INT1_EN (1Ah)

Format: Unsigned binary

The INT1_EN command enables the interrupts, such as MOSFET driver issues, V_{PACKP} changes, completed cell-balancing, ADC self-diagnostics for OV/UV conditions, scheduled errors, NTC hot PCB, die over-temperature, cell mismatch, dead cell, open-wire detection, VDD UV, 3V3 UV, REGIN UV, and OTP CRC events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
13	R/W	FET_DRIVER_INT_EN	1'b 0	Enables interrupt reporting for MOSFET driver issues. 0: Disabled 1: Enabled
12	R/W	PACKP_V_INT_EN	1'b 0	Enables interrupt reporting for V_{PACKP} changes. 0: Disabled 1: Enabled
11	R/W	BAL_DONE_INT_EN	1'b 0	Enables interrupt reporting for completed cell-balancing. 0: Disabled 1: Enabled
10	R/W	SELF_TEST_INT_EN	1'b 0	Enables interrupt reporting for ADC self-diagnostics OV/UV conditions. 0: Disabled 1: Enabled
9	R/W	FSM_ERROR_INT_EN	1'b 0	Enables interrupt reporting for a scheduled error. 0: Disabled 1: Enabled
8	R/W	PCB_MNTR_TEMP_INT_EN	1'b 0	Enables interrupt reporting for an NTC hot PCB condition. 0: Disabled 1: Enabled

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7	R/W	DIE_TEMP_INT_EN	1'b 0	Enables interrupt reporting for a die over-temperature (OT) event. 0: Disabled 1: Enabled
6	R/W	CELL_MISMATCH_ INT_EN	1'b 0	Enables interrupt reporting for a cell mismatch condition. 0: Disabled 1: Enabled
5	R/W	CELL_DEAD_INT_EN	1'b 0	Enables interrupt reporting for a dead cell condition. 0: Disabled 1: Enabled
4	R/W	OPEN_WIRE_INT_ EN	1'b 0	Enables interrupt reporting for completed open-wire detection. 0: Disabled 1: Enabled
3	R/W	VDD_INT_EN	1'b 0	Enables interrupt reporting for a VDD UV event. 0: Disabled 1: Enabled
2	R/W	3V3_INT_EN	1'b 0	Enables interrupt reporting for a 3V3 UV event. 0: Disabled 1: Enabled
1	R/W	REGIN_INT_EN	1'b 0	Enables interrupt reporting for a REGIN UV event. 0: Disabled 1: Enabled
0	R/W	OTP_CRC_EVENT_ INT_EN	1'b 1	Enables interrupt reporting for an OTP CRC event. 0: Disabled 1: Enabled

INT_TYPE0 (1Bh)

Format: Unsigned binary

The INT_TYPE0 command controls the triggering logic for the interrupts, such as cell NTC hot, cell NTC cold, pack OV, and pack UV events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
7:6	R/W	NTC_HOT_INT_ TYPE	2'b 00	Controls the triggering logic for a cell NTC hot interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
5:4	R/W	NTC_COLD_INT_ TYPE	2'b 00	Controls the triggering logic for a cell NTC cold interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

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3:2	R/W	VTOP_OV_INT_TYPE	2'b 00	Controls the triggering logic for a battery pack OV interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
1:0	R/W	VTOP_UV_INT_TYPE	2'b 00	Controls the triggering logic for a battery pack UV interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

INT_TYPE1 (1Ch)

Format: Unsigned binary

The INT_TYPE1 command controls the triggering logic for the interrupts, such as VDD UV, 3V3 UV, and REGIN UV interrupts.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change this register value.
13:12	R/W	VDD_INT_TYPE	2'b 00	Controls the triggering logic for a VDD UV interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
11:10	R/W	3V3_INT_TYPE	2'b 00	Controls the triggering logic for a 3V3 interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
9:8	R/W	REGIN_INT_TYPE	2'b 00	Controls the triggering logic for a REGIN interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
7:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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INT_TYPE2 (1Dh)

Format: Unsigned binary

The INT_TYPE2 command controls the triggering logic for interrupts including self-diagnostic, NTC hot PCB monitor, die temperature, cell mismatch, and dead cell events.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11:10	R/W	SELF_TEST_INT_TYPE	2'b 00	Controls the triggering logic for a self-diagnostic interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
9:8	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
7:6	R/W	PCB_MNTR_TEMP_INT_TYPE	2'b 00	Controls the triggering logic for an NTC hot PCB monitor interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
5:4	R/W	DIE_TEMP_INT_TYPE	2'b 00	Controls the triggering logic for a die temperature interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
3:2	R/W	CELL_MISMATCH_INT_TYPE	2'b 00	Controls the triggering logic for a mismatched cell interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
1:0	R/W	CELL_DEAD_INT_TYPE	2'b 00	Controls the triggering logic for a dead cell interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

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MASK_INT0 (1Eh)

Format: Unsigned binary

The MASK_INT0 command masks the triggering interrupts, such as cell NTC hot and cold, short-circuit, OC, VTOP OV and UV, and cell OV and UV events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
7	R/W	NTCS_CELL_HOT_MASK	1'b 0	Enables clearing the cell NTC hot interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
6	R/W	NTCS_CELL_COLD_MASK	1'b 0	Enables clearing the cell NTC cold interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
5	R/W	SC_MASK	1'b 0	Enables clearing the short-circuit interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
4	R/W	OVER_CURR_MASK	1'b 0	Enables clearing the OC interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
3	R/W	VTOP_OV_MASK	1'b 0	Enables clearing the VTOP OV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
2	R/W	VTOP_UV_MASK	1'b 0	Enables clearing the VTOP UV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
1	R/W	CELL_UV_MASK	1'b 0	Enables clearing the cell UV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
0	R/W	CELL_OV_MASK	1'b 0	Enables clearing the cell OV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled

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MASK_INT1 (1Fh)

Format: Unsigned binary

The MASK_INT1 command masks the triggering interrupts, such as NTC hot PCB monitor, die hot temperature, cell mismatch, VDD under-voltage, 3V3 UV, REGIN UV, and self-test events.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
8	R/W	PCB_MNTR_HOT_MASK	1'b 0	Enables clearing the NTC hot PCB monitor interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
7	R/W	DIE_TEMP_DIG_MASK	1'b 0	Enables clearing the die temperature interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
6	R/W	CELL_MSMT_MASK	1'b 0	Enables clearing the mismatched cell interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
5:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3	R/W	VDD_MASK	1'b 0	Enables clearing the VDD interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
2	R/W	3V3_MASK	1'b 0	Enables clearing the 3V3 interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
1	R/W	REGIN_MASK	1'b 0	Enables clearing the REGIN interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
0	R/W	SELF_TEST_MASK	1'b 0	Enables clearing the self-test interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled

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OC_STATUS (20h)

Format: Unsigned binary

The OC_STATUS command reports both the real-time and latched status of charge OC, discharge over-current protection (OCP) threshold 1 (OC1), and discharge OCP threshold 2 (OC2) events.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
10	R	OC_CHG_RT_STS	1'b 0	Reports in real time whether a charge OC limit is detected. 0: Not detected 1: Detected
9	R	OC2_DCHG_RT_STS	1'b 0	Reports in real time whether an OC2 limit is detected. 0: Not detected 1: Detected
8	R	OC1_DCHG_RT_STS	1'b 0	Reports in real time whether an OC1 limit is detected. 0: Not detected 1: Detected
7:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R	OC_CHG_STS	1'b 0	Indicates the latched charge OC limit interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). • For a rising edge type, the bit is set to 1 if a rising edge is detected • For a falling edge type, the bit is set to 1 if a falling edge is detected • For a rising and falling edge type, the bit is set to 1 if either edge is detected • For a level, the bit is set to 1 if the source signal is high. The type is defined by OC_CHG_INT_TYPE (23h, bits[15:14]). These status bits can be cleared with OVER_CURR_INT_CLEAR (17h, bit[4]). 0: Not detected 1: Detected
1	R	OC2_DCHG_STS	1'b 0	Indicates the latched OC2 limit interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). • For a rising edge type, the bit is set to 1 if a rising edge is detected. • For a falling edge type, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge type, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. The type is defined by OC_DCHG_INT_TYPE (23h, bits[13:12]), with the type selection being common for both OC1 and OC2 limit interrupts. This status bit can be cleared with OVER_CURR_INT_CLEAR. 0: Not detected 1: Detected

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0	R	OC1_DCHG_STS	1'b 0	Indicates the latched OC1 limit interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). • For a rising edge type, the bit is set to 1 if a rising edge is detected. • For a falling edge type, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge type, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. The type is defined by OC_DCHG_INT_TYPE, with the type selection being common for both OC1 and OC2 limit interrupts. This status bit can be cleared with OVER_CURR_INT_CLEAR. 0: Not detected 1: Detected

OCFT_CTRL (23h)

Format: Unsigned binary

The OCFT_CTRL command controls the triggering logic for interrupts of charge OC, discharge OCP threshold 1 (OC1), and discharge OCP threshold 2 (OC2) events. It also enables interrupts, faults, and monitoring for charge OC, OC1, and OC2 events.

Bits	Access	Bit Name	Default	Description
15:14	R/W	OC_CHG_INT_TYPE	2'b 00	Controls the triggering logic for a charge OC interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
13:12	R/W	OC_DCHG_INT_ TYPE	2'b 00	Controls the triggering logic for OC1 and OC2 interrupts. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
11:9	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
8	R/W (can lock to read-only)	OC_CHG_FAULT_EN	1'b 1	Enables a charge OC event to turn off the CHG driver. When enabled, this charge OC event turns off the CHG MOSFET. 0: Disabled 1: Enabled This bit allows OTP.
7	R/W (can lock to read-only)	OC2_DCHG_FAULT_ EN	1'b 1	Enables an OC2 event to turn off the DSG driver. When enabled, this OC2 event turns off the DSG MOSFET. 0: Disabled 1: Enabled This bit allows OTP.

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6	R/W (can lock to read-only)	OC1_DCHG_FAULT_EN	1'b 1	Enables an OC1 event to turn off the DSG driver. When enabled, this OC1 event turns off the DSG MOSFET. 0: Disabled 1: Enabled This bit allows OTP.
5	R/W	OC_CHG_INT_EN	1'b 0	Enables bit-level control for a charge OC interrupt. OVER_CURR_INT_EN (19h, bit[4]) must be enabled for this bit to be effective. 0: Disabled 1: Enabled
4	R/W	OC2_DCHG_INT_EN	1'b 0	Enables bit-level control for an OC2 interrupt. OVER_CURR_INT_EN must be enabled for this bit to be effective. 0: Disabled 1: Enabled
3	R/W	OC1_DCHG_INT_EN	1'b 0	Enables bit-level control for an OC1 interrupt. OVER_CURR_INT_EN must be enabled for this bit to be effective. 0: Disabled 1: Enabled
2	R/W (can lock to read-only)	OC_CHG_EN_CTRL	1'b 1	Enables charge OC limit monitoring. When disabled, a charge OC limit event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled. 0: Disabled 1: Enabled This bit allows MTP.
1	R/W (can lock to read-only)	OC2_DCHG_EN_CTRL	1'b 1	Enables OC2 limit monitoring. When disabled, an OC2 limit event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled. 0: Disabled 1: Enabled This bit allows MTP.
0	R/W (can lock to read-only)	OC1_DCHG_EN_CTRL	1'b 1	Enables OC1 limit monitoring. When disabled, an OC1 limit event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled. 0: Disabled 1: Enabled This bit allows MTP.

DSGOC_LIM (24h)

Format: Unsigned binary

The DSGOC_LIM command configures the threshold and threshold range for discharge OCP threshold 1 (OC1) and discharge OCP threshold 2 (OC2) events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
13	R/W (can lock to read-only)	OC2_DCHG_RNG	1'b 1	Selects the range and LSB for the OC2 threshold. 0: 2.5mV/ LSB, 80mV full-scale range (FSR) 1: 7.5mV/ LSB, 240mV FSR This bit allows MTP.

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12:8	R/W (can lock to read-only)	OC2_DCHG_LIM	5'b 01001	Sets the OC2 threshold. With a 1x range (bit[13] of this command = 0): LSB: 2.5mV Offset: 2.5mV Range: 2.5mV to 80mV Value (mV) = Setting x 2.5 + 2.5. With a 3x range (bit[13] of this command = 1): LSB: 7.5mV Offset: 7.5mV Range: 7.5mV to 240mV Value (mV) = Setting x 7.5 + 7.5. These bits allow MTP.
7:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
5	R/W (can lock to read-only)	OC1_DCHG_RNG	1'b 0	Selects the range and LSB for the OC1 threshold. 0: 2.5mV/ LSB, 80mV FSR 1: 7.5mV/ LSB, 240mV FSR This bit allows MTP.
4:0	R/W (can lock to read-only)	OC1_DCHG_LIM	5'b 10000	Sets the OC1 threshold. With a 1x range (bit[5] of this command = 0): LSB: 2.5mV Offset: 2.5mV Range: 2.5mV to 80mV Value (mV) = Setting x 2.5 + 2.5. With a 3x range (bit[5] of this command = 1): LSB: 7.5mV Offset: 7.5mV Range: 7.5mV to 240mV Value (mV) = Setting x 7.5 + 7.5. These bits allow MTP.

DSGOC_DEG (25h)

Format: Unsigned binary

The DSGOC_DEG command configures the deglitch and deglitch range for discharge OCP threshold 1 (OC1) and discharge OCP threshold 2 (OC2) events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14	R/W (can lock to read-only)	OC2_DCHG_DGL_RNG	1'b 0	Sets the OC2 deglitch bit weight and selects the range for bits[13:8] of this command. 0: 5ms LSB / 315ms FSR 1: 40ms LSB / 2520ms FSR This bit allows MTP.

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13:8	R/W (can lock to read-only)	OC2_DCHG_DGL	6'b 000100	Sets the OC2 deglitch value. When these bits are set to 0x00, there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 60µs. When bit[14] of this command is set to 0x0: LSB: 5ms Range: 0ms to 315ms Value (ms) = Setting x 5 When bit[14] of this command is set to 0x1: LSB: 40ms Range: 0ms to 2520ms Value (ms) = Setting x 40 These bits allow MTP.
7	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
6	R/W (can lock to read-only)	OC1_DCHG_DGL_RNG	1'b 0	Sets the OC1 deglitch bit weight and selects the range for bits[5:0] of this command. 0: 5ms LSB / 315ms FSR 1: 40ms LSB / 2520ms FSR This bit allows MTP.
5:0	R/W (can lock to read-only)	OC1_DCHG_DGL	6'b 010100	Sets the OC1 deglitch value. When these bits are set to 0x00, there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 60µs. When bit[6] of this command is set to 0x0: LSB: 5ms Range: 0ms to 315ms Value (ms) = Setting x 5 When bit[6] of this command is set to 0x1: LSB: 40ms Range: 0ms to 2520ms Value (ms) = Setting x 40 These bits allow MTP.

CHGOC_DEG (26h)

Format: Unsigned binary

The CHGOC_DEG command configures the deglitch, deglitch range, threshold, and threshold range for charge OC events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14	R/W (can lock to read-only)	OC_CHG_DGL_RNG	1'b 0	Sets the charge OC deglitch bit weight and selects the range for bits[13:8] of this command. 0: 5ms LSB / 315ms FSR 1: 40ms LSB / 2520ms FSR This bit allows MTP.

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13:8	R/W (can lock to read-only)	OC_CHG_DG	6'b 000100	Sets the charge OC deglitch value. When these bits are set to 0x00, there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 60µs. When bit[14] of this command is set to 0x0: LSB: 5ms Range: 0ms to 315ms Value (ms) = Setting x 5 When OC2_DCHG_DGL_RNG (25h, bit[14]) is set to 0x1: LSB: 40ms Range: 0ms to 2520ms Value (ms) = Setting x 40 These bits allow MTP.
7:6	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
5	R/W (can lock to read-only)	OC_CHG_RNG	1'b 0	Selects the range and LSB for the charge OC threshold (set via bits[4:0] of this command). 0: 1.6mV/ LSB, 51.2mV FSR 1: 4.8mV/ LSB, 153.6mV FSR This bit allows MTP.
4:0	R/W (can lock to read-only)	OC_CHG_LIM	5'b 10000	Sets the charge OC threshold. With a 1x range (bit[5] of this command is set to 0): LSB: 1.6mV Offset: 1.6mV Range: 1.6mV to 51.2mV Value (mV) = Setting x 1.6 + 1.6 With a 3x range (bit[5] of this command is set to 1): LSB: 4.8mV Offset: 4.8mV Range: 4.8mV to 153.6mV Value (mV) = Setting x 4.8 + 4.8 These bits allow MTP.

SC_STATUS (27h)

Format: Unsigned binary

The SC_STATUS command reports both the real-time and latched status of charge and discharge short-circuit events.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9	R	SC_CHG_RT_STS	1'b 0	Reports whether a charge short-circuit event has been detected in real time. 0: Not detected 1: Detected
8	R	SC_DCHG_RT_STS	1'b 0	Reports whether a discharge short-circuit event has been detected in real time. 0: Not detected 1: Detected
7:2	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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1	R	SC_CHG_STS	1'b 0	Reports whether a latched charge short-circuit event has been detected. This status bit can be cleared with SHORT_CURR_INT_CLEAR (17h, bit[5]). 0: Not detected 1: Detected
0	R	SC_DCHG_STS	1'b 0	Reports whether a latched discharge short-circuit event has been detected. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling) selected by SC_DCHG_INT_TYPE (2Ah, bits[13:12]). • For a rising edge type, the bit is set to 1 if a rising edge is detected. • For a falling edge type, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge type, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. This status bit can be cleared with SHORT_CURR_INT_CLEAR. 0: Not detected 1: Detected

SCFT_CTRL (2Ah)

Format: Unsigned binary

The SCFT_CTRL command controls the triggering logic for the interrupts of charge and discharge short-circuit events. It also enables the fault protection, interrupt, and monitoring of charge and discharge short-circuit events.

Bits	Access	Bit Name	Default	Description
15:14	R/W	SC_CHG_INT_TYPE	2'b 00	Controls the triggering logic for a charge OC interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
13:12	R/W	SC_DCHG_INT_ TYPE	2'b 00	Controls the triggering logic for charge and discharge short-circuit interrupts. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
11:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
5	R/W (can lock to read-only)	SC_CHG_FAULT_EN	1'b 1	Enables a charge short-circuit event to provide a fault protection by turning off the CHG MOSFET. For this bit to be effective, SC_CHG_EN_CTRL must be enabled. 0: Disabled 1: Enabled This bit allows OTP

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4	R/W (can lock to read-only)	SC_DCHG_FAULT_EN	1'b 1	Enables a discharge short-circuit event to provide a fault protection by turn off CHG MOSFET. For this bit to be effective, SC_DCHG_EN_CTRL must be enabled. 0: Disabled 1: Enabled This bit allows OTP
3	R/W	SC_CHG_INT_EN	1'b 0	Enables the interrupt for a charge short-circuit current. For this bit to be effective, bit[1] of this command must be enabled. 0: Disabled 1: Enabled
2	R/W	SC_DCHG_INT_EN	1'b 0	Enables the interrupt for a discharge short-circuit current. For this bit to be effective, bit[0] of this command must be enabled. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	SC_CHG_EN_CTRL	1'b 1	Enables charge short-circuit monitoring. When disabled, this fault does not trigger an interrupt or a fault, regardless of whether the fault and interrupt enable bits are enabled. 0: Disabled 1: Enabled This bit allows MTP.
0	R/W (can lock to read-only)	SC_DCHG_EN_CTRL	1'b 1	Enables discharge short-circuit monitoring. When disabled, this fault does not trigger an interrupt or a fault, regardless of whether the fault and interrupt enable bits are enabled. 0: Disabled 1: Enabled This bit allows MTP.

DSGSC_CFG (2Bh)

Format: Unsigned binary

The DSGSC_CFG command configures the deglitch, threshold, and threshold range for discharge short-circuit events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:8	R/W (can lock to read-only)	SC_DCHG_DG	7'b 0000001	Configures the discharge short-circuit deglitch time. When these bits are to 0x00, there is no deglitch, meaning a short-circuit event is flagged as soon as it is detected. The response time is about 60µs. LSB: 0.2ms Range: 0ms to 25.4ms Value (ms) = Setting x 0.2 These bits allow MTP.
7:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
5	R/W (can lock to read-only)	SC_DCHG_RNG	1'b 0	Selects the range and LSB for the discharge short-circuit threshold (set via bits[4:0] of this command). 0: 5.5mV/ LSB, 176mV FSR 1: 16.5mV/ LSB, 528mV FSR This bit allows MTP.

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4:0	R/W (can lock to read-only)	SC_DCHG_LIM	5'b 10001	Configures the short-circuit discharge threshold. With a 1x range (bit[5] of this command is set to 0): LSB: 5.5mV Offset: 5.5mV Range: 5.5mV to 176mV Value (mV) = Setting x 5.5 + 5.5 With a 3x range (bit[5] of this command is set to 1): LSB: 16.5mV Offset: 16.5mV Range: 16.5mV to 528mV Value (mV) = Setting x 16.5 + 16.5 These bits allow MTP.

CHGSC_CFG (2Ch)

Format: Unsigned binary

The CHGSC_CFG command configures the deglitch, threshold, and threshold range for charge short-circuit events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:8	R/W (can lock to read-only)	SC_CHG_DG	7'b 0001000	Configures the charge short-circuit deglitch time. When these bits are set to 0x00, there is no deglitch, meaning a short-circuit event is flagged as soon as it is detected. The response time is about 60µs. LSB: 0.2ms Range: 0ms to 25.4ms Value (ms) = Setting x 0.2 These bits allow MTP.
7:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
5	R/W (can lock to read-only)	SC_CHG_RNG	1'b 0	Selects the range and LSB for the charge short-circuit threshold (set via bits[4:0] of this command). 0: 2.5mV/ LSB, 80mV FSR 1: 7.5mV/ LSB, 240mV FSR This bit allows MTP.
4:0	R/W (can lock to read-only)	SC_CHG_LIM	5'b 10001	Configures the charge short-circuit threshold. With a 1x range (bit[5] of this command is set to 0): LSB: 2.5mV Offset: 2.5mV Range: 2.5mV to 80mV Value (mV) = Setting x 2.5 + 2.5 With a 3x range (bit[5] of this command is set to 1): LSB: 7.5mV Offset: 7.5mV Range: 7.5mV to 240mV Value (mV) = Setting x 7.5 + 7.5 These bits allow MTP.

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RD_CELL_UV (2Dh)

Format: Unsigned binary

The RD_CELL_UV command reports whether under-voltage (UV) conditions have been detected on cell 1 to cell 16.

Bits	Access	Bit Name	Default	Description
15	R	CELL_16_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 16. If CELL_UV_STS_SEL (35h, bit[11]) = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
14	R	CELL_15_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 15. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
13	R	CELL_14_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 14. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
12	R	CELL_13_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 13. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
11	R	CELL_12_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 12. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
10	R	CELL_11_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 11. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
9	R	CELL_10_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 10. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
8	R	CELL_9_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 9. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is not under UV conditions
7	R	CELL_8_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 8. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions

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6	R	CELL_7_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 7. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
5	R	CELL_6_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 6. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
4	R	CELL_5_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 5. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
3	R	CELL_4_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 4. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
2	R	CELL_3_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 3. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
1	R	CELL_2_UV_STS	1'b 0	Reports whether an UV condition has been detected on cell 2. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under UV conditions 1: This cell is under UV conditions
0	R	CELL_1_UV_STS	1'b 0	Reports whether an under-voltage (UV) condition has been detected on cell 1. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not UV conditions 1: This cell is under UV conditions

RD_CELL_OV (2Eh)

Format: Unsigned binary

The RD_CELL_OV command reports whether over-voltage (OV) conditions have been detected on cell 1 to cell 16.

Bits	Access	Bit Name	Default	Description
15	R	CELL_16_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 16. If CELL_OV_STS_SEL (35h, bit[12]) = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions

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14	R	CELL_15_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 15. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
13	R	CELL_14_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 14. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
12	R	CELL_13_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 13. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
11	R	CELL_12_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 12. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
10	R	CELL_11_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 11. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
9	R	CELL_10_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 10. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
8	R	CELL_9_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 9. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
7	R	CELL_8_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 8. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
6	R	CELL_7_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 7. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
5	R	CELL_6_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 6. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions

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4	R	CELL_5_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 5. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
3	R	CELL_4_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 4. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
2	R	CELL_3_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 3. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
1	R	CELL_2_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 2. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions
0	R	CELL_1_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 1. Send an interrupt OV clear to clear this bit. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not under OV conditions 1: This cell is under OV conditions

RD_CELL_MSMT (2Fh)

Format: Unsigned binary

The RD_CELL_MSMT command reports cell 1 to cell 16 mismatch (MSMT) interrupt status.

Bits	Access	Bit Name	Default	Description
15	R	CELL_16_MSMT_STS	1'b 0	Reports cell 16's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR (18h, bit[6]). 0: No mismatch has been detected 1: A mismatch has been detected
14	R	CELL_15_MSMT_STS	1'b 0	Reports cell 15's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
13	R	CELL_14_MSMT_STS	1'b 0	Reports cell 14's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
12	R	CELL_13_MSMT_STS	1'b 0	Reports cell 13's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected

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11	R	CELL_12_MSMT_STS	1'b 0	Reports cell 12's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
10	R	CELL_11_MSMT_STS	1'b 0	Reports cell 11's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
9	R	CELL_10_MSMT_STS	1'b 0	Reports cell 10's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
8	R	CELL_9_MSMT_STS	1'b 0	Reports cell 9's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
7	R	CELL_8_MSMT_STS	1'b 0	Reports cell 8's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
6	R	CELL_7_MSMT_STS	1'b 0	Reports cell 7's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
5	R	CELL_6_MSMT_STS	1'b 0	Reports cell 6's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
4	R	CELL_5_MSMT_STS	1'b 0	Reports cell 5's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
3	R	CELL_4_MSMT_STS	1'b 0	Reports cell 4's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
2	R	CELL_3_MSMT_STS	1'b 0	Reports cell 3's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
1	R	CELL_2_MSMT_STS	1'b 0	Reports cell 2's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
0	R	CELL_1_MSMT_STS	1'b 0	Reports cell 1's mismatch interrupt status, and clears a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected

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RD_CELL_DEAD (30h)

Format: Unsigned binary

The RD_CELL_DEAD command reports whether dead cell conditions have been detected on cell 1 to cell 16.

Bits	Access	Bit Name	Default	Description
15	R	CELL_16_DEAD_STS	1'b 0	Reports cell 16's dead interrupt status. If CELL_DEAD_STS_SEL (34h, bit[10]) = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
14	R	CELL_15_DEAD_STS	1'b 0	Reports cell 15's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
13	R	CELL_14_DEAD_STS	1'b 0	Reports cell 14's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
12	R	CELL_13_DEAD_STS	1'b 0	Reports cell 13's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
11	R	CELL_12_DEAD_STS	1'b 0	Reports cell 12's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
10	R	CELL_11_DEAD_STS	1'b 0	Reports cell 11's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
9	R	CELL_10_DEAD_STS	1'b 0	Reports cell 10's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
8	R	CELL_9_DEAD_STS	1'b 0	Reports cell 9's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
7	R	CELL_8_DEAD_STS	1'b 0	Reports cell 8's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead

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6	R	CELL_7_DEAD_STS	1'b 0	Reports cell 7's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
5	R	CELL_6_DEAD_STS	1'b 0	Reports cell 6's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
4	R	CELL_5_DEAD_STS	1'b 0	Reports cell 5's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
3	R	CELL_4_DEAD_STS	1'b 0	Reports cell 4's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
2	R	CELL_3_DEAD_STS	1'b 0	Reports cell 3's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
1	R	CELL_2_DEAD_STS	1'b 0	Reports cell 2's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead
0	R	CELL_1_DEAD_STS	1'b 0	Reports cell 1's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: The cell is not dead 1: The cell is dead

CELL_MSMT_STS (33h)

Format: Unsigned binary

The CELL_MSMT_STS command reports the real-time cell mismatch status, the cell with the lowest voltage, and the voltage difference between the cell with the lowest voltage and the cell with the highest voltage.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14	R	CELL_MSMT_RT_STS	1'b 0	Reports the real-time cell mismatch status. 0: No mismatch has been detected 1: A mismatch has been detected

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13:10	R	CELL_MSMT_ LOWER	4'b 0000	Reports the cell with the lowest voltage. If the interrupt is disabled, this bit indicates the real-time status; otherwise, this bit is latched at the interrupt and returns to the real-time status after being cleared. 0x0: Cell 1 0x1: Cell 2 ... 0xF: Cell 16
9:0	R	CELL_MSMT_DELTA	10'b 0000000 000	Reports the voltage difference between the cell with the lowest voltage and the cell with the highest voltage. If the interrupt is disabled, this bit indicates the real-time status; otherwise, this bit is latched at the interrupt and returns to the real-time status after being cleared. LSB: 4.8828mV Range: 0mV to 4995.1044mV Value (mV) = Setting x 4.8828

PACKFT_CTRL (34h)

Format: Unsigned binary

The PACKFT_CTRL command enables the monitoring and fault protection of cell mismatch (MSMT), cell dead, and VTOP over-voltage (OV) or under-voltage (UV) events. It also reports the real-time or latched interrupt dead cell status and whether a dead cell event has been detected.

Bits	Access	Bit Name	Default	Description
15	W	CELL_DEAD_DET_ CLEAR	1'b 0	Write this bit to 1 to clear the dead cell status. This is a self-clearing bit.
14	R	CELL_DEAD_LOG_ STS	1'b 0	Reports whether a dead cell event has been detected. This status is not cleared by shutting down. It can be cleared by bit[15] of this command, watchdog timer reset, or the fully powered down. 0: Not detected 1: Detected
13	R	RESERVED	N/A	Reserved. Do not change the bit of this .
12	R/W (can lock to read-only)	CELL_MSMT_ FAULT_EN	1'b 0	Enables a cell mismatch event to provide fault protection. When enabled, this cell mismatch event provides fault protection. 0: Disabled 1: Enabled This bit allows OTP.
11	R/W	CELL_MSMT_EN	1'b 0	Enables cell mismatch monitoring protection. This bit must be enabled to trigger cell mismatch faults or interrupts (which have their respective enable controls). 0: Disabled 1: Enabled This bit allows OTP.
10	R/W	CELL_DEAD_STS_ SEL	1'b 0	Selects what each of the CELL_x_DEAD_STS bits (set via the RD_CELL_DEAD (30h) command) (where x = 1 to 16) report. 0: Reports the latched cell x status going to the interrupt controller 1: Reports the latest outcome of the cell x dead check
9	R/W (can lock to read-only)	CELL_DEAD_ FAULT_EN	1'b 0	Enables a cell dead event to provide fault protection. When enabled, this cell dead event provides fault protection. 0: Disabled 1: Enabled This bit allows OTP.

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8	R/W (can lock to read-only)	CELL_DEAD_EN	1'b 0	Enables dead cell protection. This bit must be enabled to trigger dead cell faults or interrupts (which have their respective enable controls). 0: Disabled 1: Enabled This bit allows OTP.
7:6	R	RESERVED	N/A	Reserved. Do not change the values of these bits.
5	R/W (can lock to read-only)	VTOP_OV_FAULT_EN_CTRL	1'b 0	Enables battery pack OVP to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
4	R/W	VTOP_OV_EN_CTRL	1'b 0	Enables the monitoring for battery pack (VTOP to AGND) OVP. 0: Disabled 1: Enabled This bit allows OTP
3:2	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
1	R/W (can lock to read-only)	VTOP_UV_FAULT_EN_CTRL	1'b 0	Enables battery pack UVP to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP
0	R/W	VTOP_UV_EN_CTRL	1'b 0	Enables the monitoring for battery pack (VTOP to AGND) UVP. 0: Disabled 1: Enabled This bit allows OTP.

CELLFT_CTRL (35h)

Format: Unsigned binary

The CELLFT_CTRL command enables monitoring and fault protection for cell over-voltage (OV) or under-voltage (UV) events. It also controls the triggering logic for cell OV and cell UV events.

Bits	Access	Bit Name	Default	Description
15:13	R	RESERVED	N/A	Reserved. Do not change this register value.
12	R/W	CELL_OV_STS_SEL	1'b 0	Selects what each of the CELL_x_OV_STS bits (set via the RD_CELL_OV (2Eh) command) (where x = 1 to 16) report. 0: Reports the latched cell x status going to the interrupt controller 1: Reports the latest outcome of the cell x OV check
11	R/W	CELL_UV_STS_SEL	1'b 0	Selects what each of the CELL_x_UV_STS bits (set via the RD_CELL_UV (2Dh) command) (where x = 1 to 16) report. 0: Reports the latched cell x status going to the interrupt controller 1: Reports the latest outcome of the cell x UV check
10:9	R/W	CELL_OV_INT_TYPE	2'b 01	Controls the triggering logic for a cell OV interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

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8:7	R/W	CELL_UV_INT_TYPE	2'b 01	Controls the triggering logic for a cell UV interrupt. 0x0: An interrupt is generated on the high input status signal 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
6	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
5	R/W (can lock to read-only)	CELL_OV_FAULT_EN	1'b 0	Enables a cell OV event to provide fault protection. When enabled, this cell OV event provides fault protection 0: Disabled 1: Enabled This bit allows OTP.
4	R/W (can lock to read-only)	CELL_OV_EN_CTRL	1'b 0	Enables cell OVP. This bit must be enabled for OV faults or interrupts to be triggered. 0: Disabled 1: Enabled This bit allows OTP.
3	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
2	R/W (can lock to read-only)	CELL_UV_FAULT_EN	1'b 0	Enables a cell UV event to provide fault protection. When enabled, this cell UV event provides fault protection. 0: Disabled 1: Enabled This bit allows OTP.
1	R/W (can lock to read-only)	CELL_UV_EN_CTRL	1'b 0	Enables cell UVP. This bit must be enabled for UV faults or interrupts to be triggered. 0: Disabled 1: Enabled This bit allows OTP.
0	R/W	SYNC_RT_STATUS	1'b 0	When this bit is turned on, it synchronizes the status bit to allow the ADC voltage monitoring input status to be cleared after the status bit has been disabled. 0: Off 1: On

CELL_HYST (36h)

Format: Unsigned binary

The CELL_HYST command configures the cell over-voltage (OV) and cell under-voltage (UV) threshold hysteresis.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11:8	R/W	CELL_OV_HYST	4’b 1010	Sets the cell OV threshold hysteresis. LSB: 19.5mV Range: 0mV to 292.5mV Value (mV) = Setting x 19.5 These bits allow OTP.

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7:4	R/W	CELL_UV_HYST	4’b 1010	Sets the cell UV threshold hysteresis. LSB: 19.5mV Range: 0mV to 292.5mV Value (mV) = Setting x 19.5 These bits allow OTP.
3:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

PACK_UV_OV (37h)

Format: Unsigned binary

The PACK_UV_OV command configures the V_{TOP} over-voltage (OV) and under-voltage (UV) threshold hysteresis. It also reports the real-time V_{TOP} OV and UV statuses.

Bits	Access	Bit Name	Default	Description
15:10	R/W	VTOP_OV_HYST	6'b 100000	Sets the battery pack OV threshold hysteresis. LSB: 78.125mV Range: 0mV to 4921.875mV Value (mV) = Setting x 78.125 These bits allow MTP.
9	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
8	R	VTOP_OV_RT_STS	1'b 0	Reports the real-time result of the stack top voltage (V_{TOP_AGND}) vs. OV threshold comparison. Depending on the settings, a hysteresis may be applied to the threshold for comparison. 0: $V_{TOP_AGND} \leq$ OV threshold 1: $V_{TOP_AGND} >$ OV threshold
7:2	R/W	VTOP_UV_HYST	6'b 100000	Sets the battery pack UV threshold hysteresis. LSB: 78.125mV Range: 0mV to 4921.875mV Value (mV) = Setting x 78.125 These bits allow MTP.
1	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
0	R	VTOP_UV_RT_STS	1'b 0	Reports the real-time result of V_{TOP_AGND} vs. UV threshold comparison. Depending on the settings, a hysteresis may be applied to the threshold for comparison. 0: $V_{TOP_AGND} \geq$ UV threshold 1: $V_{TOP_AGND} <$ UV threshold

CELL_UV (38h)

Format: Unsigned binary

The CELL_UV command configures the cell under-voltage (UV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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11:8	R/W (can lock to read-only)	CELL_UV_DG	4'b 0000	Sets the cell UV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: An UV condition is reported as soon as the UV threshold is reached 0x1: An UV condition is reported when the current and previous protection readings violate the cell UV threshold ... 0xF: An UV condition is reported when a total of 16 protection cycles violate the cell UV threshold These bits allow OTP.
7:0	R/W (can lock to read-only)	CELL_UV	8'b 10011000	Configures the cell UV threshold. LSB: 19.53mV Range: 0mV to 4980.15mV Value (mV) = Setting x 19.53 These bits allow MTP.

CELL_OV (39h)

Format: Unsigned binary

The CELL_OV command configures the cell over-voltage (OV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11:8	R/W (can lock to read-only)	CELL_OV_DG	4'b 0000	Sets the cell OV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: An OV condition is reported as soon as the OV threshold is reached 0x1: An OV condition is reported when the current and previous protection readings violate the cell OV threshold ... 0xF: An OV condition is reported when a total of 16 protection cycles violate the cell OV threshold These bits allow OTP.
7:0	R/W (can lock to read-only)	CELL_OV	8'b 11010111	Configures the cell OV threshold. LSB: 19.53mV Range: 0mV to 4980.15mV Value (mV) = Setting x 19.53 These bits allow MTP.

PACK_UV (3Ah)

Format: Unsigned binary

The PACK_UV command configures the V_{TOP} under-voltage (UV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R/W	VTOP_UV_DG	4'b 0000	Sets the V_{TOP} UV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: An UV condition is reported as soon as the UV threshold is reached 0x1: An UV condition is reported when the current and previous protection readings violate the V_{TOP} UV threshold ... 0xF: An UV condition is reported when a total of 16 protection cycles violate the V_{TOP} UV threshold These bits allow OTP.

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11:0	R/W	VTOP_UV_LIMIT	12'b 1001010 01000	Configures the battery pack UV threshold. LSB: 19.531mV Range: 0mV to 79979.445mV Value (mV) = Setting x 19.531 These bits allow MTP.

PACK_OV (3Bh)

Format: Unsigned binary

The PACK_OV command configures the V_{TOP} over-voltage (OV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R/W	VTOP_OV_DG	4'b 0000	Sets the V_{TOP} OV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: An OV condition is reported as soon as the OV threshold is reached 0x1: An OV condition is reported when the current and previous protection readings violate the V_{TOP} OV threshold ... 0xF: An OV condition is reported when a total of 16 protection cycles violate the V_{TOP} OV threshold These bits allow OTP.
11:0	R/W	VTOP_OV_LIMIT	12'b 1101011 10001	Configures the battery pack OV threshold. LSB: 19.531mV Range: 0mV to 79979.445mV Value (mV) = Setting x 19.531 These bits allow MTP.

CELL_DEAD_THR (3Ch)

Format: Unsigned binary

The CELL_DEAD_THR command configures the dead cell threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
10:7	R/W	CELL_DEAD_DGL_N	4'b 0000	Sets the dead cell deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: A dead cell condition is reported as soon as the dead cell threshold is reached 0x1: A dead cell condition is reported when the current and previous protection readings violate the dead cell threshold ... 0xF: A dead cell condition is reported when a total of 16 protection cycles violate the dead cell threshold These bits allow OTP.
6:0	R/W	CELL_DEAD_LIMIT	7'b 1101000	Configuration for dead cell threshold. LSB: 19.53mV Range: 0mV to 2480.31mV Value (mV) = Setting x 19.53 These bits allow MTP.

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CELL_MSMT (3Dh)

Format: Unsigned binary

The CELL_MSMT command configures the cell mismatch (MSMT) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
8:5	R/W	CELL_MSMT_DGL_N	4'b 0000	Sets the mismatched cell deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: A mismatched cell condition is reported as soon as the mismatched cell threshold is reached 0x1: A mismatched cell condition is reported when the current and previous protection readings violate the mismatched cell threshold ... 0xF: A mismatched cell condition is reported when a total of 16 protection cycles violate the mismatched cell threshold These bits allow OTP.
4:0	R/W	MSMT_TH	5'b 00010	Sets the mismatched cell threshold. LSB: 39.06mV Range: 0mV to 1210.86mV Value (mV) = Setting x 39.06 These bits allow OTP.

RD_NTC_DIE (3Eh)

Format: Unsigned binary

The RD_NTC_DIE command reports the NTC PCB hot, NTC cell hot, and NTC cell cold statuses. It also reports the die's temperature in real time, as well as its interrupt status.

Bits	Access	Bit Name	Default	Description
15	R	DIE_TEMP_ ANA_EVENT	1'b 0	Obtains the status from analog circuit recordings after a hot die temperature event. This bit cannot be read in real time since the digital logic is shut down when this event occurs. This bit is cleared by DIE_TEMP_ANA_CLEAR (44h, bit[15]). 0: The die temperature is within its normal range 1: The analog die temperature is too hot
14	R	DIE_TEMP_DIG_STS	1'b 0	Reports the die temperature interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. This bit is cleared by DIE_TEMP_DIG_CLEAR (44h, bit[14]). 0: No digital die temperature event has been detected 1: The digital die temperature event has been detected
13	R	DIE_TEMP_DIG_ RT_STS	1'b 0	Reports the real-time digital die temperature status, based on the result of the latest comparison between the digital die temperature reading and the associated hot threshold. 0: The die temperature is within its normal range 1: The digital die temperature is too hot
12	R	RESERVED	N/A	Reserved. Do not change the value of this bit.

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11	R	NTC4_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC4 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL (44h, bit[2]), this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC4 PCB temperature is within its normal range 1: The NTC4 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected
10	R	NTC3_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC3 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC3 PCB temperature is within its normal range 1: The NTC3 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected
9	R	NTC2_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC2 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC2 PCB temperature is within its normal range 1: The NTC2 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected

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8	R	NTC1_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC1 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC1 PCB temperature is within its normal range 1: The NTC1 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected
7	R	NTC4_CELL_COLD_STS	1'b 0	Reports the NTC4 cell cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected
6	R	NTC3_CELL_COLD_STS	1'b 0	Reports the NTC3 cell cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected
5	R	NTC2_CELL_COLD_STS	1'b 0	Reports the NTC2 cell cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected

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4	R	NTC1_CELL_COLD_STS	1'b 0	Reports the NTC1 cell cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected
3	R	NTC4_CELL_HOT_STS	1'b 0	Reports the NTC4 cell hot interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected
2	R	NTC3_CELL_HOT_STS	1'b 0	Reports the NTC3 cell hot interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected
1	R	NTC2_CELL_HOT_STS	1'b 0	Reports the NTC2 cell hot interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected
0	R	NTC1_CELL_HOT_STS	1'b 0	Reports the NTC1 cell charging hot interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling): • For a rising edge, the bit is set to 1 if a rising edge is detected. • For a falling edge, the bit is set to 1 if a falling edge is detected. • For a rising and falling edge, the bit is set to 1 if either edge is detected. • For a level, the bit is set to 1 if the source signal is high. 0: No interrupt has been detected 1: An interrupt has been detected

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RD_V_NTC4_LR (3Fh)

Format: Unsigned binary

The RD_V_NTC4_LR command reports the NTC1 to NTC 4 cell's cold real-time status. It also reports the NTC4 protection ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	NTC4_CELL_COLD_RT_STS	1'b 0	Reports the NTC4 cell's cold real-time status. 0: NTC4 is within its normal temperature range 1: NTC4 exceeds the discharging temperature range
14	R	NTC3_CELL_COLD_RT_STS	1'b 0	Reports the NTC3 cell's cold real-time status. 0: NTC3 is within its normal temperature range 1: NTC3 exceeds the discharging temperature range
13	R	NTC2_CELL_COLD_RT_STS	1'b 0	Reports the NTC2 cell's cold real-time status. 0: NTC2 is within its normal temperature range 1: NTC2 exceeds the discharging temperature range
12	R	NTC1_CELL_COLD_RT_STS	1'b 0	Reports the NTC1 cell's cold real-time status. 0: NTC1 is within its normal temperature range 1: NTC1 exceeds the discharging temperature range
11:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	NTC4_VALUE	10'b 0000000000	Reports the NTC4 protection ADC reading. NTC4 monitoring is controlled by NTC4_EN (47h, bit[6]), meaning these bits update when protection monitoring is requested and NTC4_EN is enabled. The NTC4 value can be calculated with the following equation: Value = Reading x 0.09766 (in %)

RD_V_NTC3_LR (40h)

Format: Unsigned binary

The RD_V_NTC3_LR command reports the NTC1 to NTC4 cell's hot real-time status. It also reports the NTC3 protection ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	NTC4_CELL_HOT_RT_STS	1'b 0	Reports the NTC4 cell's hot real-time status. 0: NTC4 is within its normal temperature range 1: NTC4 exceeds the charging temperature range
14	R	NTC3_CELL_HOT_RT_STS	1'b 0	Reports the NTC3 cell's hot real-time status. 0: NTC3 is within its normal temperature range 1: NTC3 exceeds the charging temperature range
13	R	NTC2_CELL_HOT_RT_STS	1'b 0	Reports the NTC2 cell's hot real-time status. 0: NTC2 is within its normal temperature range 1: NTC2 exceeds the charging temperature range
12	R	NTC1_CELL_HOT_RT_STS	1'b 0	Reports the NTC1 cell's hot real-time status. 0: NTC1 is within its normal temperature range 1: NTC1 exceeds the charging temperature range
11:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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9:0	R	NTC3_VALUE	10'b 0000000 000	Reports the NTC3 protection ADC reading. NTC3 monitoring is controlled by NTC3_EN (47h, bit[4]), meaning these bits update when protection monitoring is requested and NTC3_EN is enabled. The NTC3 value can be calculated with the following equation: Value = Reading x 0.09766 (in %)

RD_V_NTC2_LR (41h)

Format: Unsigned binary

The RD_V_NTC2_LR command reports the NTC2 protection ADC reading.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	NTC2_VALUE	10'b 0000000 000	Reports the NTC2 protection ADC reading. NTC2 monitoring is controlled by NTC2_EN (47h, bit[2]), meaning these bits update when protection monitoring is requested and NTC2_EN is enabled. The NTC2 value can be calculated with the following equation: Value = Reading x 0.09766 (in %)

RD_V_NTC1_LR (42h)

Format: Unsigned binary

The RD_V_NTC1_LR command reports the NTC1 protection ADC reading.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the values of these bits.
9:0	R	NTC1_VALUE	10'b 0000000 000	Reports the NTC1 protection ADC reading. NTC1 monitoring is controlled by NTC1_EN (47h, bit[0]), meaning these bits update when protection monitoring is requested and NTC1_EN is enabled. The NTC1 value can be calculated with the following equation: Value = Reading x 0.09766 (in %)

RD_T_DIE (43h)

Format: Unsigned binary

The RD_T_DIE command reports the die's temperature ADC reading.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	DIE_TEMP_V	10'b 0000000 000	Reports the die temperature, which can be calculated with the following equation: T = Reading x 0.474 - 269.12°C

NTC_CLR (44h)

Format: Unsigned binary

The NTC_CLR command controls the clearing of an event when the digital die is too hot. It also controls reporting the real-time or latched NTC PCB status.

Bits	Access	Bit Name	Default	Description
15	W	DIE_TEMP_ ANA_CLEAR	1'b 0	Write 1 to clear an analog die too hot event. This bit is a self-clearing register.

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14	W	DIE_TEMP_DIG_ CLEAR	1'b 0	Write 1 to clear a digital die too hot event. This bit is a self-clearing register.
13:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R/W	PCB_MNTR_STS_ SEL	1'b 0	Controls the NTCx_PCB_MNTR_bit (set via the RD_NTC_DIE (3Eh) command) (where x = 1 to 4). 0: Shows the latched status going to the interrupt controller 1: Shows the real-time status
1:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

DIE_CFG (46h)

Format: Unsigned binary

The DIE_CFG command enables digital die temperature monitoring and fault protection.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3	R/W (can lock to read-only)	DIE_TEMP_DIG_ FAULT_EN	1'b 0	Enables a die temperature hot event to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
2	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
1	R/W (can lock to read-only)	DIE_TEMP_DIG_EN	1'b 1	Enables digital die temperature monitoring. This bit must be enabled for die temperature hot faults or interrupts to be triggered. 0: Disabled 1: Enabled This bit allows OTP.
0	R	RESERVED	N/A	Reserved. Do not change the value of this bit.

NTC_CFG (47h)

Format: Unsigned binary

The NTC_CFG command configures NTC fault protection and monitoring.

Bits	Access	Bit Name	Default	Description
15	R/W (can lock to read-only)	PCB_MNTR_FAULT_ EN	1'b 0	Enables the PCB NTC hot event to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
14	R/W (can lock to read-only)	NTC_CELL_COLD_ FAULT_EN	1'b 0	Enables the NTC cell cold event to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
13	R/W (can lock to read-only)	NTC_CELL_HOT_ FAULT_EN	1'b 0	Enables the NTC cell hot event to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
12:11	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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10	R/W (can lock to read-only)	NTCB_DYNAMIC_ON	1'b 1	Enables dynamic bias on the NTCB pin during ADC conversions of NTC channels. When disabled, NTCB is always enabled, which increases current consumption. 0: Always remains on 1. Dynamic turn-on This bit allows OTP.
9	R/W (can lock to read-only)	NTC4_PD_EN	1'b 0	Enables the internal pull-down function on NTC3. 0: Disabled 1: Enabled This bit allows OTP.
8	R/W (can lock to read-only)	NTC3_PD_EN	1'b 0	Enables the internal pull-down function on NTC4. 0: Disabled 1: Enabled This bit allows OTP.
7	R/W (can lock to read-only)	NTC4_TYPE_SEL	1'b 1	Configures the NTC4 monitor type. 0: Cell monitor 1: PCB monitor This bit allows OTP.
6	R/W (can lock to read-only)	NTC4_EN	1'b 0	Enables protection monitoring for NTC4 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG (07h, bit[0]). 0: Disabled 1: Enabled This bit allows OTP.
5	R/W (can lock to read-only)	NTC3_TYPE_SEL	1'b 0	Configures the NTC3 monitor type. 0: Cell monitor 1: PCB monitor This bit allows OTP.
4	R/W (can lock to read-only)	NTC3_EN	1'b 0	Enables protection monitoring for NTC3 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG. 0: Disabled 1: Enabled This bit allows OTP.
3	R/W (can lock to read-only)	NTC2_TYPE_SEL	1'b 0	Configures the NTC2 monitor type. 0: Cell monitor 1: PCB monitor This bit allows OTP.
2	R/W (can lock to read-only)	NTC2_EN	1'b 0	Enables protection monitoring for NTC2 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG. 0: Disabled 1: Enabled This bit allows OTP.

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1	R/W (can lock to read-only)	NTC1_TYPE_SEL	1'b 0	Configures the NTC1 monitor type. 0: Cell monitor 1: PCB monitor This bit allows OTP.
0	R/W (can lock to read-only)	NTC1_EN	1'b 0	Enables protection monitoring for NTC1 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG. 0: Disabled 1: Enabled This bit allows OTP.

NTCC_OTHR_DSG (48h)

Format: Unsigned binary

The NTCC_OTHR_DSG command configures the discharge NTC hot cell's monitor voltage threshold.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R/W (can lock to read-only)	NTC_CELL_HOT_DISCH	10'b 0100101110	Sets the discharge NTC hot cell's monitor voltage threshold. The limit is triggered if the value is equal to or below the set threshold. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766 These bits allow MTP.

NTCC_UTHR_DSG (49h)

Format: Unsigned binary

The NTCC_UTHR_DSG command configures the discharge NTC cold cell's monitor voltage threshold.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R/W (can lock to read-only)	NTC_CELL_COLD_DISCH	10'b 1010010100	Sets the discharge NTC cold cell's monitor voltage threshold. The limit is triggered if the value exceeds the set threshold. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766 These bits allow MTP.

NTCC_OTHR_CHG (4Ah)

Format: Unsigned binary

The NTCC_OTHR_CHG command configures the charge NTC hot cell's monitor voltage threshold.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R/W (can lock to read-only)	NTC_CELL_HOT_CHG	10'b 0100101110	Sets the charge NTC hot cell's monitor voltage threshold. The limit is triggered if the value is equal to or below the set threshold. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766 These bits allow MTP.

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NTCC_UTHR_CHG (4Bh)

Format: Unsigned binary

The NTCC_UTHR_CHG command configures the charge NTC cold cell's monitor voltage threshold and NTC cell monitor hysteresis.

Bits	Access	Bit Name	Default	Description
15:11	R/W (can lock to read-only)	NTC_CELL_HYST	5'b 10001	Sets the NTC cell's monitor hysteresis. LSB: 0.1953% Range: 0% to 6.0543% Value (%) = Setting x 0.1953 These bits allow OTP.
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
9:0	R/W (can lock to read-only)	NTC_CELL_COLD_CHG	10'b 1010010100	Sets the charge NTC cold cell's monitor voltage threshold. The limit is triggered if the value exceeds the set threshold. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766 These bits allow MTP.

NTCM_OTHR (4Ch)

Format: Unsigned binary

The NTCM_OTHR command configures the NTC hot PCB's monitor threshold and hysteresis.

Bits	Access	Bit Name	Default	Description
15:11	R/W	PCB_MNTR_HYST	5'b 10000	Sets the NTC hot PCB's monitor hysteresis. LSB: 0.1953% Range: 0% to 6.0543% Value (%) = Setting x 0.1953 These bits allow OTP.
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
9:0	R/W	PCB_MNTR_HOT	10'b 0011101011	Sets the NTC hot PCB's monitor voltage threshold. The limit is triggered if the NTC reading is equal to or below the set threshold. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766 These bits allow OTP.

DIE_OT (4Dh)

Format: Unsigned binary

The DIE_OT command configures the digital die temperature threshold and hysteresis.

Bits	Access	Bit Name	Default	Description
15:11	R/W	DIE_TEMP_HYST	5'b 10101	Sets the digital die temperature hysteresis. LSB: 0.474°C Range: 0°C to 14.694°C Value (°C) = Setting x 0.474 These bits allow OTP.
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.

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9:0	R/W	DIE_TEMP_HOT	10'b 1011101 100	Sets the digital die temperature threshold. LSB: 0.474°C Offset: -269.12°C Range: -269.12°C to +215.782°C Value (°C) = Setting x 0.474 - 269.12 These bits allow OTP.

SELF_STS (4Eh)

Format: Unsigned binary

The SELF_STS command reports the NVM CRC check outcome, VDD under-voltage (UV), 3V3 UV, and REGIN UV detection results, as well as the ADC self-test OV or UV detection results.

Bits	Access	Bit Name	Default	Description
15:7	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
6	R	NVM_CRC_ OUTCOME	1'b 0	Reports the errors in the outcome NVM CRC check. The result of the previous check is retained until NVM_CRC_DO (55h, bit[0]) is set from 0 to 1. Then this bit remains at 0 until the check is completed and a new result is available. 0: No errors are detected 1: One or more error(s) are detected
5	R	NVMCHK_DONE_ STS	1'b 0	When true, NVM CRC check is complete. This bit can be cleared by setting NVM_CRC_DO to 0. 0: False 1: True
4	R	VDD_STS	1'b 0	Reports whether VDD UV has been detected. 0: Not detected 1: Detected
3	R	3V3_STS	1'b 0	Reports whether 3V3 UV has been detected. 0: Not detected 1: Detected
2	R	REGIN_STS	1'b 0	Reports whether REGIN UV has been detected. 0: Not detected 1: Detected
1	R	SELF_TEST_STS_ OV	1'b 0	Reports whether ADC self-test OV conditions have been detected 0: Not detected 1: Detected
0	R	SELF_TEST_STS_ UV	1'b 0	Reports whether ADC self-test UV conditions have been detected. 0: Not detected 1: Detected

RD_VA1P8 (4Fh)

Format: Unsigned binary

The RD_VA1P8 command reports the VDD regulator ADC reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	VDD_VALUE	10'b 0000000 000	Reports the latest ADC reading for the VDD regulator. The VDD value can be calculated with the following equation: Value = Reading x 3.2227 (in mV)

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RD_VA3P3 (50h)

Format: Unsigned binary

The RD_VA3P3 command reports the 3V3 regulator's ADC reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	3V3_VALUE	10'b 0000000 000	Reports the latest ADC reading for the 3V3 regulator. The 3V3 value can be calculated with the following equation: Value = Reading x 6.4453 (in mV)

RD_VA5 (51h)

Format: Unsigned binary

The RD_VA5 command reports the REGIN ADC reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	REGIN_VALUE	10'b 0000000 000	Reports the latest ADC reading for REGIN. The REGIN value can be calculated with the following equation: Value = Setting x 6.4453 (in mV)

RD_VASELF (52h)

Format: Unsigned binary

The RD_VASELF command reports the ADC self-test reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	SELF_TEST_VALUE	10'b 0000000 000	Reports the latest 10-bit ADC reading for the internal fixed voltage reference, which functions as an ADC self-test. The self-test value can be calculated with the following equation: Value = Setting x 3.2227 (in mV)

RD_OPENH (53h)

Format: Unsigned binary

The RD_OPENH command reports the open-wire detection results of C0 to C15.

Bits	Access	Bit Name	Default	Description
15	R	CELL_15_OPW_STS	1'b 0	Reports whether C15 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL (00h, bits[3:0]) for this flag to function. 0: Not detected 1: Detected
14	R	CELL_14_OPW_STS	1'b 0	Reports whether C14 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected

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13	R	CELL_13_OPW_STS	1'b 0	Reports whether C13 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
12	R	CELL_12_OPW_STS	1'b 0	Reports whether C12 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
11	R	CELL_11_OPW_STS	1'b 0	Reports whether C11 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
10	R	CELL_10_OPW_STS	1'b 0	Reports whether C10 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
9	R	CELL_9_OPW_STS	1'b 0	Reports whether C9 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
8	R	CELL_8_OPW_STS	1'b 0	Reports whether C8 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
7	R	CELL_7_OPW_STS	1'b 0	Reports whether C7 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
6	R	CELL_6_OPW_STS	1'b 0	Reports whether C6 has as an open wire after a detection is executed. 0: Not detected 1: Detected
5	R	CELL_5_OPW_STS	1'b 0	Reports whether C5 has as an open wire after a detection is executed. 0: Not detected 1: Detected
4	R	CELL_4_OPW_STS	1'b 0	Reports whether C4 has as an open wire after a detection is executed. 0: Not detected 1: Detected
3	R	CELL_3_OPW_STS	1'b 0	Reports whether C3 has as an open wire after a detection is executed. 0: Not detected 1: Detected

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2	R	CELL_2_OPW_STS	1'b 0	Reports whether C2 has as an open wire after a detection is executed. 0: Not detected 1: Detected
1	R	CELL_1_OPW_STS	1'b 0	Reports whether C1 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
0	R	CELL_0_OPW_STS	1'b 0	Reports whether C0 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected

RD_OPENL (54h)

Format: Unsigned binary

The RD_OPENL command reports the C16 open-wire detection result.

Bits	Access	Bit Name	Default	Description
15:1	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
0	R	CELL_16_OPW_STS	1'b 0	Reports whether C16 has as an open wire after a detection is executed. The cell must be enabled from CELL_S_CTRL (00h, bits[3:0]) for this flag to function. 0: Not detected 1: Detected

SFT_GO (55h)

Format: Unsigned binary

The SFT_GO command reports the open-wire detection error and completion. It also controls the start of the open wire and the clearing of NVM CRC.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
10	R	OPEN_WIRE_ERR_STS	1'b 0	Reports whether an error has occurred during open-wire detection (e.g. cell-balancing is already operating). 0: False 1: True
9	R	OPEN_WIRE_DONE_STS	1'b 0	Reports whether open-wire detection is complete. When true, open-wire detection is complete. Write 0 to bit[8] of this command to clear this flag. 0: False 1: True
8	R/W	OPEN_WIRE_GO	1'b 0	Write 1 to this bit to schedule an open-wire check. Write 0 to this bit to clear the results of a completed open-wire detection.
7:1	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
0	R/W	NVM_CRC_DO	1'b 0	Write 0 to this bit to clear the results. Write 1 to this bit to schedule an NVM CRC.

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SELF_CFG (56h)

Format: Unsigned binary

The SELF_CFG command enables NVM CRC as well as 3V3 UV and VDD UV fault protection. It also enables open-wire detection when the device starts up, open-wire fault protection, NVM CRC, ADC self-test check, and 3V3, VDD, and REGIN UV monitoring.

Bits	Access	Bit Name	Default	Description
15	R/W (can lock to read-only)	NVM_FAULT_EN	1'b 0	Enables the NVM CRC error event to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
14	R/W (can lock to read-only)	3V3_VDD_FAULT_EN	1'b 0	Enables the 3V3 UV or VDD UV event (via the analog comparator and ADC monitoring) to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
13:11	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
10	R/W (can lock to read-only)	OPEN_WIRE_PON	1'b 0	Enables open-wire detection when the device starts up (exits shutdown mode). 0: Disabled 1: Enabled This bit allows OTP.
9	R/W (can lock to read-only)	OPEN_WIRE_FAULT_EN	1'b 0	Enables the open wire event to provide fault protection. 0: Disabled 1: Enabled This bit allows OTP.
8:7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R/W (can lock to read-only)	NVM_CRC_EN	1'b 1	Enables the NVM CRC. 0: Disabled 1: Enabled This bit allows OTP.
5:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3	R/W (can lock to read-only)	ADC_SELF_TEST_EN	1'b 1	Enables the ADC self-test check that indicates whether the applied voltage is within the allowed range. 0: Disabled 1: Enabled This bit allows OTP.
2	R/W (can lock to read-only)	VDD_EN	1'b 1	Enables the ADC's VDD monitoring check to ensure that the digital 1.8V supply exceeds the defined UV level. 0: Disables VDD check 1: Enables VDD check This bit allows OTP.

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1	R/W (can lock to read-only)	3V3_EN	1'b 1	Enables the ADC's 3V3 UV monitoring to ensure that the 3.3V supply exceeds the defined UV level. 0: Disabled 1: Enabled This bit allows OTP.
0	R/W (can lock to read-only)	REGIN_EN	1'b 1	Enables the ADC's REGIN monitoring to ensure that the REGIN supply exceeds the defined UV level. 0: Disables REGIN check 1: Enables REGIN check This bit allows OTP.

OPEN_CFG (57h)

Format: Unsigned binary

The OPEN_CFG command configures the open-wire threshold and the length of each pull-up and pull-down phase.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11:8	R/W	OPW_CHECK_TH	4'b 0100	Sets the open-wire threshold used during the detection sequence. LSB: 39.06mV Range: 39.06mV to 624.96mV Value (mV) = Setting x 39.06 These bits allow OTP.
7:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3:0	R/W	OPW_CHECK_LEN	4'b 0111	Sets the length of each pull-up and pull-down phase. LSB: 1ms Offset: 1ms Range: 1ms to 16ms Value (ms) = Setting + 1 These bits allow OTP.

REGIN_UV (58h)

Format: Unsigned binary

The REGIN_UV command configures the threshold for REGIN under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
8:0	R	REGIN_UV_LIMIT	9'b 101101 101	Sets the threshold for REGIN UV conditions, which is applied to the ADC readings reported in REGIN_VALUE (51h, bits[9:0]). LSB: 12.89mV Range: 0mV to 6586.79mV Value (mV) = Setting x 12.89

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V3P3_UV (59h)

Format: Unsigned binary

The V3P3_UV command configures the threshold for 3V3 under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
7:0	R/W	3V3_UV_LIMIT	8'b 11110 000	Sets the threshold for 3V3 UV conditions, which is applied to the ADC reading reported in 3V3_VALUE (50h, bits[9:0]). LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89 These bits allow OTP.

VDD_UV (5Ah)

Format: Unsigned binary

The VDD_UV command configures the threshold for VDD under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
7:0	R	VDD_UV_LIMIT	8'b 10000 100	Sets the threshold for VDD 1.8V UV conditions, which is applied to the ADC reading reported in VDD_VALUE (4Fh, bits[9:0]). LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89

SELF_THR (5Bh)

Format: Unsigned binary

The SELF_THR command configures the thresholds for self-test over-voltage (OV) and under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:8	R	SELF_TEST_OV_ LIMIT	8'b 01100 101	Sets the threshold for self-test OV conditions, which is applied to SELF_TEST_VALUE (52h, bits[9:0]) ADC readings. LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89
7:0	R	SELF_TEST_UV_ LIMIT	8'b 01010 101	Sets the threshold for self-test UV conditions, which is applied to the SELF_TEST_VALUE ADC readings. LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89

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FT_STS1 (5Dh)

Format: Unsigned binary

The FT_STS1 command reports the fault status, including die temperature, charge and discharge short-circuit, charge over-current (OC), discharge OCP threshold 1 (OC1), and discharge OCP threshold 2 (OC2), NTC cell hot, NTC cell cold, NTC PCB hot, V_{TOP} over-voltage (OV) and under-voltage (UV), open-wire, cell mismatch, dead cell, cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	R	DIE_TEMP_FAULT_STS	1'b 0	Reports whether a die temperature condition is triggering a fault. 0: False 1: True
14	R	SC_CHG_FAULT_STS	1'b 0	Reports whether a charge short-circuit condition is triggering a fault. 0: False 1: True
13	R	SC_DCHG_FAULT_STS	1'b 0	Reports whether a discharge short-circuit condition is triggering a fault. 0: False 1: True
12	R	OC_CHG_FAULT_STS	1'b 0	Reports whether a charge OC condition is triggering a fault. 0: False 1: True
11	R	OC2_DCHG_FAULT_STS	1'b 0	Reports whether an OC2 condition is triggering a fault. 0: False 1: True
10	R	OC1_DCHG_FAULT_STS	1'b 0	Reports whether an OC1 condition is triggering a fault. 0: False 1: True
9	R	NTC_CELL_COLD_FAULT_STS	1'b 0	Reports whether an NTC cell monitoring fault is triggered due to the NTC temperature exceeding the NTC cold limit. 0: False 1: True
8	R	NTC_CELL_HOT_FAULT_STS	1'b 0	Reports whether an NTC cell monitoring fault is triggered due to the NTC temperature exceeding the NTC hot limit. 0: False 1: True
7	R	PCB_MNTR_FAULT_STS	1'b 0	Reports whether an NTC PCB monitor condition is triggering a fault. 0: False 1: True
6	R	VTOP_OV_FAULT_STS	1'b 0	Reports whether a V_{TOP} OV condition is triggering a fault. 0: False 1: True
5	R	VTOP_UV_FAULT_STS	1'b 0	Reports whether a V_{TOP} UV condition is triggering a fault. 0: False 1: True

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4	R	OPEN_WIRE_ FAULT_STS	1'b 0	Reports whether an open-wire condition is triggering a fault. 0: False 1: True
3	R	CELL_MSMT_ FAULT_STS	1'b 0	Reports whether a cell mismatch condition is triggering a fault. 0: False 1: True
2	R	CELL_DEAD_ FAULT_STS	1'b 0	Reports whether a dead cell condition is triggering a fault. 0: False 1: True
1	R	CELL_OV_FAULT_ STS	1'b 0	Reports whether a cell OV condition is triggering a fault. 0: False 1: True
0	R	CELL_UV_FAULT_ STS	1'b 0	Reports whether a cell UV condition is triggering a fault. 0: False 1: True

FT_STS2 (5Eh)

Format: Unsigned binary

The FT_STS2 command reports fault statuses, including short-circuit removal detection, over-current (OC) and short-circuit recovery failures, driver turn-on failures, VDD UV, 3V3 UV, and OTP CRC fault events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
13	R	RMVL_BUSY	1'b 0	When true, short-circuit removal detection is busy. 0: False 1: True
12	R	OC_DCHG_ RECOVERY_ FAILED	1'b 0	When true, automatic recovery has failed. Use OC1_DCHG_FAULT_CLR (5Fh, bit[10]) or OC2_DCHG_FAULT_CLR (5Fh, bit[11]) to clear this bit. 0: False 1: True
11	R	OC_CHG_ RECOVERY_ FAILED	1'b 0	When true, automatic recovery has failed. Use OC_CHG_FAULT_CLR (5Fh, bit[12]) to clear this bit. 0: False 1: True
10	R	SC_DCHG_ RECOVERY_ FAILED	1'b 0	When true, automatic recovery has failed. Use SC_DCHG_FAULT_CLR (5Fh, bit[13]) to clear this bit. 0: False 1: True
9	R	SC_CHG_ RECOVERY_ FAILED	1'b 0	When true, automatic recovery has failed. Use SC_CHG_FAULT_CLR (5Fh, bit[14]) to clear this bit. 0: False 1: True
8:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3	R	DRIVER_FAULT_STS	1'b 0	Reports whether a driver turn-on condition is triggering a fault. 0: False 1: True

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2	R	VDD_FAULT_STS	1'b 0	Reports whether a VDD UV condition is triggering a fault. A VDD fault can be triggered by the ADC's VDD UV monitoring or the VDD analog UV comparator. The VDD analog comparator is always enabled, meaning when 3V3_VDD_FAULT_EN (56h, bit[14]) is enabled, it can trigger a fault even when ADC's VDD UV monitoring (VDD_EN) is disabled. 0: False 1: True
1	R	3V3_FAULT_STS	1'b 0	Reports whether a 3V3 UV condition is triggering a fault. A 3V3 fault can be triggered by the ADC's 3V3 UV monitoring or the 3.3V analog UV comparator. The 3.3V analog comparator is always enabled, meaning when 3V3_VDD_FAULT_EN is enabled, it can trigger a fault even when the ADC's 3V3 UV monitoring (3V3_EN) is disabled. 0: False 1: True
0	R	OTP_CRC_FAULT_STS	1'b 0	Reports whether an OTP CRC condition is triggering a fault. This bit can be cleared with OTP_CRC_CLR (60h, bit[14]). 0: False 1: True

FT_CLR (5Fh)

Format: Unsigned binary

The FT_CLR command clears faults, including die temperature, charge and discharge short-circuit, charge over-current (OC), discharge OCP threshold 1 (OC1), and discharge OCP threshold 2 (OC2), cell NTC hot, cell NTC cold, NTC PCB monitor, V_{TOP} over-voltage (OV) and under-voltage (UV), open wire, cell mismatch, dead cell, cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	W	DIE_TEMP_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a die temperature fault. This is a self-clearing register.
14	W	SC_CHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a charge short-circuit fault. This is a self-clearing register.
13	W	SC_DCHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a discharge short-circuit fault. This is a self-clearing register.
12	W	OC_CHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a charge OC fault. This is a self-clearing register.
11	W	OC2_DCHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear an OC2 fault. This is a self-clearing register.
10	W	OC1_DCHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear an OC1 fault. This is a self-clearing register.
9	W	NTC_CELL_COLD_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell NTC cold fault. This is a self-clearing register.
8	W	NTC_CELL_HOT_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell NTC hot fault. This is a self-clearing register.
7	W	PCB_MNTR_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear an NTC PCB monitor fault. This is a self-clearing register.
6	W	VTOP_OV_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a battery pack OV fault. This is a self-clearing register.
5	W	VTOP_UV_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a battery pack UV fault. This is a self-clearing register.

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4	W	OPEN_WIRE_ FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell open-wire fault. This is a self-clearing register.
3	W	CELL_MSMT_ FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a mismatched cell fault. This is a self-clearing register.
2	W	CELL_DEAD_ FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a dead cell fault. This is a self-clearing register.
1	W	CELL_OV_FAULT_ CLR	1'b 0	Write 1 to this bit to manually clear a cell OV fault. This is a self-clearing register.
0	W	CELL_UV_FAULT_ CLR	1'b 0	Write 1 to this bit to manually clear a cell UV fault. This is a self-clearing register.

FT_REC (60h)

Format: Unsigned binary

The FT_REC command controls the manual fault clearing function for 3.3V and 1.8V under-voltage (UV), OTP CRC, and MOSFET driver events. This command also enables automatic recovery from an NTC PCB monitor, NTC cell charge, and NTC cell discharge fault, in addition to defining the NTC cell hot/cold recovery mode.

Bits	Access	Bit Name	Default	Description
15	W	3V3_VDD_FAULT_ CLR	1'b 0	Write 1 to this bit to manually clear 3.3V and 1.8V UV faults. This is a self-clearing register.
14	W	OTP_CRC_CLR	1'b 0	Write 1 to this bit to manually clear an OTP CRC fault. This is a self-clearing register.
13	W	DRIVER_FAULT_ CLR	1'b 0	Write 1 to this bit to manually clear a MOSFET driver fault. This is a self-clearing register.
12	R/W (can lock to read-only)	DIE_TEMP_FAULT_ REC	1'b 0	Enables automatic recovery for die temperature conditions (when the temperature drops). 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP.
11	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
10	R/W (can lock to read-only)	SC_CHG_REC	1'b 0	Enables an automatic recovery attempt for charge short-circuit conditions. 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP
9	R/W (can lock to read-only)	SC_DCHG_REC	1'b 0	Enables an automatic recovery attempt for discharge short-circuit conditions. 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP.
8	R/W (can lock to read-only)	OC_CHG_REC	1'b 0	Enables an automatic recovery attempt for charge OC conditions. 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP.

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7	R/W (can lock to read-only)	OC2_DCHG_REC	1'b 0	Enables an automatic recovery attempt for OC2 conditions. 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP.
6	R/W (can lock to read-only)	OC1_DCHG_REC	1'b 0	Enables an automatic recovery attempt for OC1 conditions. 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP.
5	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
4	R/W (can lock to read-only)	PCB_MNTR_REC	1'b 0	Enables automatic recovery from an NTC PCB monitor type fault. Set this bit to 0 for manual recovery. 0: Disabled 1: Enabled This bit allows OTP.
3	R/W	NTC_CHG_REC_MODE	1'b 0	Defines the recovery logic from an NTC hot/cold condition in charge mode. 0: NTC voltage [>/<] NTC_CELL_xxxx_CHG (where xxxx = HOT OR COLD) ± NTC_CELL_HYST (4Bh, bits[15:11]) 1: (NTC voltage [>/<] NTC_CELL_xxxx_CHG ± NTC_CELL_HYST) or if the charger is removed, (NTC voltage [>/<] NTC_CELL_xxxx_THR_IN_USE ± NTC_CELL_HYST) In this logic, NTC_CELL_xxxx_CHG is either NTC_CELL_HOT_CHG (4Ah, bits[9:0]) or NTC_CELL_COLD_CHG (4Bh, bits[9:0]) by comparing and selecting one of these values. The signs within the brackets are determined by the fault. When the current is within the standby boundaries in fault mode, NTC_CELL_xxxx_THR_IN_USE depends on the CELL_HOT_STBY_MODE (61h, bit[2]) setting (available vs. conservative) or the CELL_COLD_STBY_MODE (61h, bit[3]) setting (available vs conservative). This bit allows OTP.
2	R/W (can lock to read-only)	NTC_CELL_CHG_REC	1'b 0	Enables automatic recovery from an NTC cell type fault (the temperature is back within the nominal range) in charge mode. Set this bit to 0 for manual recovery. 0: Disabled 1: Enabled This bit allows OTP.
1	R/W (can lock to read-only)	NTC_CELL_DCHG_REC	1'b 0	Enables automatic recovery from an NTC cell type fault (the temperature is back within the nominal range) in discharge mode or standby mode. Set this bit to 0 for manual recovery. 0: Disabled 1: Enabled This bit allows OTP.
0	R	RESERVED	N/A	Reserved. Do not change the value of this bit.

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FT0_CFG (61h)

Format: Unsigned binary

The FT0_CFG command enables automatic cell over-voltage (OV) or under-voltage (UV) fault recovery, configures MOSFET behavior when a cell OV/UV fault occurs, and sets the recovery logic from cell OV/UV faults. It also enables the additional recovery logic for the recovery of CHG MOSFETs during cell OV/UV faults. This command configures MOSFET behavior if a cell NTC fault occurs, enables the additional recovery logic, and sets the standby current direction in response to an NTC charge or discharge fault.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11	R/W (can lock to read-only)	CELL_OV_REC	1'b 0	Enables automatic recovery for a cell OV fault. 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP.
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
9	R/W (can lock to read-only)	CELL_OV_LOGIC_SEL	1'b 0	Selects which logic is used for status recovery from cell OV conditions. 0: The status recovers once the cell falls below the difference between the OV threshold and hysteresis 1: The status recovers by following either logic below: • The cell falls below the OV threshold, and V_{PACKP} falls below the difference between V_{TOP} and 1.6V • The cell falls below the difference between the OV threshold and hysteresis This bit allows OTP.
8	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
7	R/W (can lock to read-only)	CELL_UV_REC	1'b 0	Enables automatic recovery for a cell UV fault. 0: Manual recovery 1: Automatic recovery attempt This bit allows OTP.
6	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
5	R/W (can lock to read-only)	CELL_UV_LOGIC_SEL	1'b 0	Selects which logic is used for status recovery from cell UV conditions. 0: The status recovers once the cell exceeds the sum of the UV threshold and hysteresis 1: The status recovers by following either logic below: • The cell exceeds the UV threshold, and V_{PACKP} exceeds the sum of V_{TOP} and 270mV • The cell exceeds the sum of the UV threshold and hysteresis This bit allows OTP.
4	R	RESERVED	N/A	Reserved. Do not change the value of this bit.

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3	R/W	CELL_COLD_STBY_ MODE	1'b 0	Defines the selection criteria for the NTC cold threshold when the battery pack current is within the STBY_CUR_TH (06h, bits[2:1]) range. 0: Available. The colder threshold (and higher voltage) is selected between NTC_CELL_COLD_DISCH (49h, bits[9:0]) and NTC_CELL_COLD_CHG (4Bh, bits[9:0]), and applied when the battery pack current is within the standby region 1: Conservative. The hotter threshold (and lower voltage) is selected between NTC_CELL_COLD_DISCH and NTC_CELL_COLD_CHG, and applied when the battery pack current is within the standby region
2	R/W	CELL_HOT_STBY_ MODE	1'b 0	Defines the selection criteria for the NTC hot threshold when the battery pack current is within the STBY_CUR_TH range. 0: Available. The hotter threshold (and lower voltage) is selected between NTC_CELL_HOT_CHG (4Ah, bits[9:0]) and NTC_CELL_HOT_DISCH (48h, bits[9:0]), and applied when the battery pack current is within the standby region 1: Conservative. The colder threshold (and higher voltage) is selected between NTC_CELL_HOT_CHG and NTC_CELL_HOT_DISCH, and applied when the battery pack current is within the standby region
1:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

FT1_CFG (62h)

Format: Unsigned binary

The FT1_CFG command configures the short-circuit removal detection retries, the delay between short-circuit removal detection and a retry, and battery pack pull-up current and time during short-circuit removal detection.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:13	R/W	SC_PUP_ RETRY_N	2'b 00	Sets the number of short-circuit removal detection retries. 2’b00: Keeps trying 2’b01: 1 try 2’b10: 2 tries 2’b11: 4 tries These bits allow MTP.
12:7	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
6:4	R/W	SCOC_RETRY_ DELAY	2'b 00	Sets the delay between short-circuit removal detection and a retry. 0x0: 1s 0x1: 2s 0x2: 4s 0x3: 6s 0x4: 10s 0x5: 15s 0x6: 20s 0x7: 25s These bits allow MTP.

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3:2	R/W	SCOC_DET_TIME	2'b 00	Sets the time for SCOC_PUP (62h, bits[1:0]). 0x0: 125ms 0x1: 250ms 0x2: 500ms 0x3: 1s These bits allow MTP.
1:0	R/W	SCOC_PUP	2'b 00	Sets the battery pack pull-up current during short-circuit removal detection. 0x0: 250μA 0x1: 500μA 0x2: 750μA 0x3: 250μA These bits allow MTP.

FT2_CFG (63h)

Format: Unsigned binary

The FT2_CFG command configures the charge and discharge over-current (OC) automatic recovery configuration.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11:10	R/W	OC_CHG_RETRY	2'b 00	Sets the number of charge OC reconnection attempts. 2’b00: 1 time 2’b01: 2 times 2’b10: 3 times 2’b11: Keeps trying These bits allow MTP.
9:8	R/W	OC_CHG_COOL	2'b 00	Sets the charge OC cool-down time. 2’b00: 100ms 2’b01: 200ms 2’b10: 500ms 2’b11: 1s These bits allow MTP.
7:6	R/W	OC2_DCHG_RETRY	2'b 00	Sets the number of the OC2 reconnection attempts. 2’b00: 1 time 2’b01: 2 times 2’b10: 3 times 2’b11: Keeps trying These bits allow MTP.
5:4	R/W	OC2_DCHG_COOL	2'b 00	Sets the OC2 cool-down time. 2’b00: 100ms 2’b01: 200ms 2’b10: 500ms 2’b11: 1s These bits allow MTP.

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3:2	R/W	OC1_DCHG_RETRY	2'b 00	Sets the number of OC1 reconnection attempts. 2’b00: 1 time 2’b01: 2 times 2’b10: 3 times 2’b11: Keeps trying These bits allow MTP.
1:0	R/W	OC1_DCHG_COOL	2'b 00	Sets the OC1 cool-down time. 2’b00: 100ms 2’b01: 200ms 2’b10: 500ms 2’b11: 1s These bits allow MTP.

RD_CCIRQL (65h)

Format: Two’s complement (combined with CC_ACC_MSBS, set via 66h, bits[9:0])

The RD_CCIRQL command reports the accumulated Coulomb counter reading for the least significant bit (LSB).

Bits	Access	Bit Name	Default	Description
15:0	R	CC_ACC_LSBS	16'b 00000000 00000000	Reports the accumulated Coulomb counter reading for the LSB. This content is latched from CC_RT_ACC_LSBS (67h, bits[15:0]) when a Coulomb counting accumulation has been completed. The reading is complement-signed and 26 bits long (combined with CC_ACC_MSBS). The value ranges from -33554432 to +33554431.

RD_CCIRQH (66h)

Format: Unsigned binary, two’s complement

The RD_CCIRQH command reports the accumulated Coulomb counter reading for the most significant bit (MSB).

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	CC_ACC_MSBS	10'b 0000000 000	Reports the accumulated Coulomb counter reading for the MSB. This content is latched from CC_RT_ACC_MSBS (68h, bits[9:0]) when a Coulomb counting accumulation has been completed. The reading is complement-signed and 26 bits long (combined with CC_ACC_LSBS, set via 65h, bits[15:0]). The value ranges from -33554432 to +33554431. The MSB accumulated Coulomb counter reading value can be calculated with the following equation: Value (mΩ x A x s) = Reading / 32768 / 5

RD_CCACCQL (67h)

Format: Two’s complement (combined with CC_RT_ACC_MSBS)

The RD_CCACCQL command reports the real-time accumulated Coulomb counter reading for the LSB.

Bits	Access	Bit Name	Default	Description
15:0	R	CC_RT_ACC_LSBS	16'b 00000000 00000000	Returns the real-time accumulated Coulomb counter reading for the LSB. These bits are constantly updated when Coulomb counting is active. The reading is complement-signed and 26 bits long (combined with CC_RT_ACC_MSBS, set via 68h, bits[9:0]). The value ranges from -33554432 to +33554431.

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RD_CCACCQH (68h)

Format: Unsigned binary, two's complement

The RD_CCACCQH command reports the real-time accumulated Coulomb counter reading for the MSB.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R	CC_RT_ACC_MSBS	10'b 0000000 000	Returns the real-time accumulated Coulomb counter reading for the LSB. This register is constantly updated when Coulomb counting is active. The reading is complement-signed and 26 bits long (combined with CC_RT_ACC_LSBS, set via 67h, bits[15:0]). The value ranges from -33554432 to +33554431. The LSB real-time accumulated Coulomb counter reading value can be calculated with the following equation: Value (mΩ x A x s) = Reading / 32768 / 5

RD_VPACKP (69h)

Format: Unsigned binary

The RD_VPACKP command reports the PACKP high-resolution voltage reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	VPACK_V	15'b 00000000 0000000	Returns the PACKP high-resolution voltage reading, which can be calculated with the following equation: Voltage = Reading x 80000 / 32768 (in mV)

RD_VTOP (6Ah)

Format: Unsigned binary

The RD_VTOP command reports the VTOP-to-AGND high-resolution voltage reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	VTOP_V	15'b 00000000 0000000	Returns the VTOP-to-AGND high-resolution voltage reading, which can be calculated with the following equation: Voltage = Reading x 80000 / 32768 (mV)

RD_ITOP (6Bh)

Format: Two's complement

The RD_ITOP command reports the battery pack current reading (synchronous to VTOP_V, set via 6Ah, bits[14:0]).

Bits	Access	Bit Name	Default	Description
15:0	R	VTOP_I	16'b 00000000 00000000	Returns the battery pack current reading (synchronous to VTOP_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). Current = Reading x 100 / 32768 / R_{SENSE} (in A)

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RD_VCELL1 (6Ch)

Format: Unsigned binary

The RD_VCELL1 command reports cell 1's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_1_V	15'b 0000000 0000000	Returns cell 1's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_VCELL2 (6Eh)

Format: Unsigned binary

The RD_VCELL2 command reports cell 2's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_2_V	15'b 00000000 0000000	Returns cell 2's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_VCELL3 (70h)

Format: Unsigned binary

The RD_VCELL3 command reports cell 3's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_3_V	15'b 00000000 0000000	Returns cell 3's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL4 (72h)

Format: Unsigned binary

The RD_VCELL4 command reports cell 4's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_4_V	15'b 00000000 0000000	Returns cell 4's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL5 (74h)

Format: Unsigned binary

The RD_VCELL5 command reports cell 5's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_5_V	15'b 00000000 0000000	Returns cell 5's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

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RD_VCELL6 (76h)

Format: Unsigned binary

The RD_VCELL6 command reports cell 6's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_6_V	15'b 00000000 0000000	Returns cell 6's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL7 (78h)

Format: Unsigned binary

The RD_VCELL7 command reports cell 7's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_7_V	15'b 00000000 0000000	Returns cell 7's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL8 (7Ah)

Format: Unsigned binary

The RD_VCELL8 command reports cell 8's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_8_V	15'b 00000000 0000000	Returns cell 8's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL9 (7Ch)

Format: Unsigned binary

The RD_VCELL9 command reports cell 9's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_9_V	15'b 00000000 0000000	Returns cell 9's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL10 (7Eh)

Format: Unsigned binary

The RD_VCELL10 command reports cell 10's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_10_V	15'b 00000000 0000000	Returns cell 10's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

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RD_VCELL11 (80h)

Format: Unsigned binary

The RD_VCELL11 command reports cell 11's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_11_V	15'b 00000000 0000000	Returns cell 11's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL12 (82h)

Format: Unsigned binary

The RD_VCELL12 command reports cell 12's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_12_V	15'b 00000000 0000000	Returns cell 12's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL13 (84h)

Format: Unsigned binary

The RD_VCELL13 command reports cell 13's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_13_V	15'b 00000000 0000000	Returns cell 13's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL14 (86h)

Format: Unsigned binary

The RD_VCELL14 command reports cell 14's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_14_V	15'b 00000000 0000000	Returns cell 14's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VCELL15 (88h)

Format: Unsigned binary

The RD_VCELL15 command reports cell 15's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_15_V	15'b 00000000 0000000	Returns cell 15's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

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RD_VCELL16 (8Ah)

Format: Unsigned binary

The RD_VCELL16 command reports cell 16's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	CELL_16_V	15'b 00000000 0000000	Returns cell 16's high-resolution reading, which can be calculated with the following equation: Voltage = Reading x 5000 / 32768 (in mV)

RD_VNTC4 (8Ch)

Format: Unsigned binary

The RD_VNTC4 command reports NTC4's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	NTC4_HIRES_V	15'b 00000000 0000000	Returns NTC4's high-resolution voltage ADC reading. This reading is ratiometric to the NTCB pin, which has a 3.3V nominal value. NTC4's high-resolution voltage ADC reading value can be calculated with the following equation: Value = Reading x 100 / 32768 (% of NTCB)

RD_VNTC3 (8Dh)

Format: Unsigned binary

The RD_VNTC3 command reports NTC3's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	NTC3_HIRES_V	15'b 00000000 0000000	Returns NTC3's high-resolution voltage ADC reading. This reading is ratiometric to the NTCB pin, which has a 3.3V nominal value. NTC3's high-resolution voltage ADC reading value can be calculated with the following equation: Value = Reading x 100 / 32768 (% of NTCB)

RD_VNTC2 (8Eh)

Format: Unsigned binary

The RD_VNTC2 command reports NTC2's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	NTC2_HIRES_V	15'b 00000000 0000000	Returns NTC2's high-resolution voltage ADC reading. This reading is ratiometric to the NTCB pin, which has a 3.3V nominal value. NTC2's high-resolution voltage ADC reading value can be calculated with the following equation: Value = Reading x 100 / 32768 (% of NTCB)

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RD_VNTC1 (8Fh)

Format: Unsigned binary

The RD_VNTC1 command reports NTC1's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	NTC1_HIRES_V	15'b 00000000 0000000	Returns NTC1's high-resolution voltage ADC reading. This reading is ratiometric to the NTCB pin, which has a 3.3V nominal value. NTC1's high-resolution voltage ADC reading value can be calculated with the following equation: Value = Reading x 100 / 32768 (% of NTCB)

RD_VGPIO3 (90h)

Format: Unsigned binary

The RD_VGPIO3 command reports GPIO3's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	GPIO3_VOLTAGE	15'b 00000000 0000000	Returns GPIO3's high-resolution voltage reading, which can be calculated with the following equation: Voltage = Reading x 3300 / 32768 (in mV)

RD_VGPIO2 (91h)

Format: Unsigned binary

The RD_VGPIO2 command reports GPIO2's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	GPIO2_VOLTAGE	15'b 00000000 0000000	Returns GPIO2's high-resolution voltage reading, which can be calculated with the following equation: Voltage = Reading x 3300 / 32768 (in mV)

RD_VGPIO1 (92h)

Format: Unsigned binary

The RD_VGPIO1 command reports GPIO1's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	GPIO1_VOLTAGE	15'b 00000000 0000000	Returns GPIO1's high-resolution voltage reading, which can be calculated with the following equation: Voltage = Reading x 3300 / 32768 (in mV)

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RD_TDIE (93h)

Format: Unsigned binary

The RD_TDIE command reports the die temperature's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	DIE_T_VOLTAGE	15'b 000000000 000000	Returns the die temperature high-resolution reading, which is proportional to the internal die temperature. The temperature can be calculated with the following equation: T = Reading x 0.01481 - 269.12 (in °C)

RD_V1P8 (94h)

Format: Unsigned binary

The RD_V1P8 command reports the 1.8V regulator's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	VDD_VOLTAGE	15'b 000000000 000000	Returns the 1.8 regulator (VDD)'s high-resolution reading. The VDD voltage can be calculated with the following equation: Voltage = Reading x 3300 / 32768 (in mV)

RD_V3P3 (95h)

Format: Unsigned binary

The RD_V3P3 command reports the 3.3V regulator's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	3V3_VOLTAGE	15'b 000000000 000000	Returns the 3.3V regulator (3V3)'s high-resolution reading. The 3V3 voltage can be calculated with the following equation: Voltage = Reading x 6600 / 32768 (in mV)

RD_V5 (96h)

Format: Unsigned binary

The RD_V5 command reports REGIN's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:0	R	REGIN_VOLTAGE	15'b 000000000 000000	Returns REGIN's high-resolution reading. The REGIN voltage can be calculated with the following equation: Voltage = Reading x 6600 / 32768 (in mV)

CC_STS (97h)

Format: Unsigned binary

The CC_STS command reports the Coulomb counter status.

Bits	Access	Bit Name	Default	Description
15:1	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
0	R	CC_STATUS	1'b 0	Reports whether the Coulomb counter is running. 0: False 1: True

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ADC_STS (98h)

Format: Unsigned binary

The ADC_STS command reports the status of the internal scheduler and the feature command scheduler.

Bits	Access	Bit Name	Default	Description
15:13	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
12:11	R	VADC_FSM	2'b 00	Reports the status of the internal scheduler. 0x0: Idle 0x1: Refreshes the voltage protection reading 0x2: Ready for the feature command 0x3: Not allowed
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
9:8	R	VADC_SCHEDULER	2'b 00	Reports the status of the feature command scheduler. 0x0: Free 0x1: Executes voltage ADC scan 0x2: Executes cell-balancing 0x3: Executes open-wire detection
7:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

ADC_CTRL (99h)

Format: Unsigned binary

The ADC_CTRL command reports whether an error has occurred when starting the high-resolution voltage scan. It also controls the start of a high-resolution scan for all the selected channels.

Bits	Access	Bit Name	Default	Description
15:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R	SCAN_ERROR_STS	1'b 0	Reports whether an error has occurred when starting the high-resolution voltage scan (e.g. if open-wire detection is already running). 0: False 1: True
1	R	SCAN_DONE_STS	1'b 0	Reports whether the high-resolution voltage scan status is complete (true) or not (false). 0: False 1: True
0	R/W	ADC_SCAN_GO	1'b 0	Write 1 to this bit to start a high-resolution scan for all the selected channels.

CC_CFG (9Ah)

Format: Unsigned binary

The CC_CFG command configures Coulomb counting. It enables Coulomb counting accumulation, back-to-back accumulation mode, and power-save mode. The command also sets the Coulomb counter integration length and reports the Coulomb counting results, such as the state machine error and completion.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.

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14	R/W	CC_B2B_ACC_CTRL	1'b 0	Controls back-to-back accumulation mode. When enabled, a new Coulomb counting conversion automatically restarts as soon as the current count is completed. With back-to-back conversions enabled, CC_RT_ACC_LSBS (67h, bits[15:0]) and CC_RT_ACC_MSBS (68h, bits[9:0]) are automatically cleared and do not report the progress of the new accumulation. 0: Disabled 1: Enabled This bit allows OTP.
13:8	R/W	CC_INT_CNT	6'b 111111	Sets the Coulomb counter integration length. The length is set as the number of time slots (32ms each). 0x00: 1 slot (32ms) 0x01: 2 slots (64ms) 0x3F: 64 slots (2048ms) These bits allow OTP.
7:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
5	R	CC_ERROR_STS	1'b 0	Reports whether a Coulomb counting state machine error has been detected. 0: Not detected 1: Detected
4	R	CC_DONE	1'b 0	Reports whether Coulomb counting accumulation has completed (true) or not (false). 0: False 1: True
3	R/W	CC_PWR_SAVE	1'b 0	Enables the Coulomb counter to enter power-save mode. When disabled, power-save mode is not used. Power-save mode reduces overall current consumption at the expense of accuracy since the current is effectively assumed to be constant during the voltage protection monitoring scan interval. Power-save mode refreshes the ADC current (I_{ADC}) reading only during a refreshing voltage protection reading, and it accumulates the results of the last conversions without running the ADC to obtain a new reading during the feature command ready scheduler. 0: Disabled 1: Enabled This bit allows OTP.
2	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
1	R/W	CC_EN_SAFE	1'b 0	Enables Coulomb counting conversions in safe mode. 0: Disabled 1: Enabled This bit allows OTP.
0	R/W (can lock to read-only)	CC_EN	1'b 0	Enables Coulomb counting accumulation. If Coulomb counting is enabled, the device cannot be in standby mode. 0: Disabled 1: Enabled This bit allows OTP.

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TRIMG_IPCB (9Bh)

Format: Two's complement

The TRIMG_IPCB command configures the current-sense PCB gain correction for the compensation of sense resistors and SMT variation.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
9:0	R/W (can lock to read-only)	I_PCB_GAIN_VALUE	10'b 0000000000	Sets the current-sense PCB gain correction, which can can compensate for sense resistors and SMT variation. The correction is applied to both Coulomb counting and synchronous current ADC readings. It is not applied to short-circuit or over-current detection. The setting is 10-bit complement-signed. The gain can be calculated with the following equation: Gain (%) = Setting x 0.0244 + 100 These bits allow MTP.

HR_SCAN0 (9Ch)

Format: Unsigned binary

The HR_SCAN0 command enables ADC cell measurement compensation for the voltage drop caused by the cell's input resistor. It also enables voltage and current ADC scanning for the synchronous VTOP current, low-dropout (LDO) regulators, die temperature, NTCs, GPIO, PACKP, VTOP voltage (V_{TOP}), and cell voltage.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
11	R/W	CELL_1K_COMP	1'b 0	Enables ADC cell measurement compensation for the voltage drop caused by the cell input resistor, R_{CELL_FILTER}. This configuration should be enabled when the input filter resistance exceeds 500Ω. For R_{CELL_FILTER} below 500Ω, this should be disabled. 0: Disabled 1: Enabled This bit allows OTP.
10	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
9	R/W (can lock to read-only)	VTOP_SYNC_EN	1'b 1	Enables the battery pack current reading that is synchronous with the VTOP_V (6Ah, bits[14:0]) reading to be updated during the high-resolution voltage ADC scan. When disabled, the synchronous VTOP_I (6Bh, bits[15:0]) current reading cannot be updated. 0: Disabled 1: Enabled This bit allows OTP.
8:7	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
6	R/W (can lock to read-only)	SCAN_LDOS_EN	1'b 0	Enables VDD, REGIN, 3V3 readings to be updated during the high-resolution voltage ADC scan. 0: Disabled 1: Enabled This bit allows OTP.

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5	R/W (can lock to read-only)	SCAN_DIE_T	1'b 1	Enables the die temperature to be updated during the high-resolution voltage ADC scan. 0: Disabled 1: Enabled This bit allows OTP.
4	R/W (can lock to read-only)	SCAN_NTCS_EN	1'b 1	Enables the NTCs' scan to be updated during the high-resolution voltage ADC scan, according to the enable setting of each individual NTC channel. 0: Disabled 1: Enabled This bit allows OTP.
3	R/W (can lock to read-only)	SCAN_GPIO_EN	1'b 1	Enables GPIO readings to be updated during the high-resolution voltage ADC scan, according to each individual GPIO enable setting. 0: Disabled 1: Enabled This bit allows OTP.
2	R/W (can lock to read-only)	SCAN_PACKP_EN	1'b 1	Enables the PACKP reading to be updated during the high-resolution voltage ADC scan. 0: Disabled 1: Enabled This bit allows OTP.
1	R/W (can lock to read-only)	SCAN_VTOP_EN	1'b 1	Enables the stack's top voltage (VTOP to AGND) reading to be updated during the high-resolution voltage ADC scan. 0: Disabled 1: Enabled This bit allows OTP.
0	R/W (can lock to read-only)	SCAN_VCELLS_EN	1'b 1	Enables the cell readings to be updated during the high-resolution voltage ADC scan, according to the enable setting of each individual cell. When disabled, the cell readings are excluded from the high-resolution voltage ADC scan. 0: Disabled 1: Enabled This bit allows OTP.

HR_SCAN1 (9Dh)

Format: Unsigned binary

The HR_SCAN1 command enables the high-resolution ADC scan for cell 1 to cell 16.

Bits	Access	Bit Name	Default	Description
15	R/W (can lock to read-only)	CELL_16_VI_READ_EN	1'b 1	Enables cell 16's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN (9Ch, bit[0]) is enabled and CELL_S_CTRL (00h, bits[3:0]) is 16 cells. 0: Disabled 1: Enabled This bit allows OTP.

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14	R/W (can lock to read-only)	CELL_15_VI_READ_EN	1'b 1	Enables cell 15's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0xE. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 15 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
13	R/W (can lock to read-only)	CELL_14_VI_READ_EN	1'b 1	Enables cell 14's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0xD. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 14 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
12	R/W (can lock to read-only)	CELL_13_VI_READ_EN	1'b 1	Enables cell 13's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0xC. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 13 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
11	R/W (can lock to read-only)	CELL_12_VI_READ_EN	1'b 1	Enables cell 12's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0xB. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 12 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
10	R/W (can lock to read-only)	CELL_11_VI_READ_EN	1'b 1	Enables cell 11's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0xA. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 11 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
9	R/W	CELL_10_VI_READ_EN	1'b 1	Enables cell 10's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0x9. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 10 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
8	R/W	CELL_9_VI_READ_EN	1'b 1	Enables cell 9's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0x8. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 9 is also provided. 0: Disabled 1: Enabled This bit allows OTP.

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7	R/W	CELL_8_VI_READ_EN	1'b 1	Enables cell 8's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0x7. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 8 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
6	R/W	CELL_7_VI_READ_EN	1'b 1	Enables cell 7's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 7 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
5	R/W	CELL_6_VI_READ_EN	1'b 1	Enables cell 6's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 6 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
4	R/W	CELL_5_VI_READ_EN	1'b 1	Enables cell 5's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 5 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
3	R/W	CELL_4_VI_READ_EN	1'b 1	Enables cell 4's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 4 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
2	R/W	CELL_3_VI_READ_EN	1'b 1	Enables cell 3's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 3 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
1	R/W	CELL_2_VI_READ_EN	1'b 1	Enables cell 2's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 2 is also provided. 0: Disabled 1: Enabled This bit allows OTP.
0	R/W	CELL_1_VI_READ_EN	1'b 1	Enables cell 1's high-resolution voltage. This bit is effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading synchronous with cell 1 is also provided. 0: Disabled 1: Enabled This bit allows OTP.

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HR_SCAN2 (9Eh)

Format: Unsigned binary

The HR_SCAN2 command enables the ADC voltage scans for NTC1 to NTC4 and the high-resolution voltage scans for GPIO1 to GPIO3.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
8	R/W (can lock to read-only)	NTC4_READ_EN	1'b 0	Enables NTC4's high-resolution voltage scan. This bit is effective when SCAN_NTCS_EN (9Ch, bit[4]) is enabled. 0: Disabled 1: Enabled This bit allows OTP.
7	R/W (can lock to read-only)	NTC3_READ_EN	1'b 0	Enables NTC3's high-resolution voltage scan. This bit is effective when SCAN_NTCS_EN is enabled. 0: Disabled 1: Enabled This bit allows OTP.
6	R/W (can lock to read-only)	NTC2_READ_EN	1'b 0	Enables NTC2's high-resolution voltage scan. This bit is effective when SCAN_NTCS_EN is enabled. 0: Disabled 1: Enabled This bit allows OTP.
5	R/W (can lock to read-only)	NTC1_READ_EN	1'b 0	Enables NTC1's high-resolution voltage scan. This bit is effective when SCAN_NTCS_EN is enabled. 0: Disabled 1: Enabled This bit allows OTP.
4:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R/W (can lock to read-only)	GPIO3_READ_EN	1'b 0	Enables GPIO3's high-resolution voltage. This bit is effective when SCAN_GPIO_EN (9Ch, bit[3]) is enabled. 0: Disabled 1: Enabled This bit allows OTP.
1	R/W (can lock to read-only)	GPIO2_READ_EN	1'b 0	Enables GPIO2's high-resolution voltage. This bit is effective when SCAN_GPIO_EN is enabled. 0: Disabled 1: Enabled This bit allows OTP.
0	R/W (can lock to read-only)	GPIO1_READ_EN	1'b 0	Enables GPIO1's high-resolution voltage. This bit is effective when SCAN_GPIO_EN is enabled. 0: Disabled 1: Enabled This bit allows OTP.

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SILC_INFO1 (A0h)

Format: Unsigned binary

The SILC_INFO1 command defines the size of the readback (in words) before appending a cyclic redundancy check (CRC).

Bits	Access	Bit Name	Default	Description
15:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
5:0	R/W	XFR_NUM_RD_ WORDS	6'b 000001	When CRC is enabled, these bits define the size of the readback in words before appending a CRC. After each read transaction, this bit self-resets back to 2 bytes. 6'b000001: 1 word / 2 bytes 6'b111111: 63 words / 126 bytes

COMM_CFG (A3h)

Format: Unsigned binary

The COMM_CFG command defines the configurable device address and enables using cyclic redundancy check (CRC) across the communication protocol.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
14:8	R/W (can lock to read-only)	DEVICE_ADD	7'b 0000001	Sets the configurable device address. These bits allow MTP.
7:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R/W (can lock to read-only)	USE_COMM_CRC	1'b 0	Enables using CRC across the communication protocol. 0: Disabled 1: Enabled This bit allows OTP.
1:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

BAL_STS (A4h)

Format: Unsigned binary

The BAL_STS command reports whether automatically balancing cycles are skipped due to a hot die temperature, a detected discharge current, a detected standby current, or a detected charge current. It also shows the number of automatically balancing cycles that are actually performed and reports whether cell-balancing is currently ongoing.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
10	R	AUTO_BAL_ SKIPPED_HOT	1'b 0	When true, automatically balancing cycles are skipped due to the die temperature being too hot. 0: False 1: True
9	R	AUTO_BAL_ SKIPPED_ DISCHARGE	1'b 0	When true, automatically balancing cycles are skipped due to a detected discharge current. 0: False 1: True

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8	R	AUTO_BAL_ SKIPPED_STANDBY	1'b 0	When true, automatically balancing cycles are skipped due to a detected standby current. 0: False 1: True
7	R	AUTO_BAL_ SKIPPED_CHARGE	1'b 0	When true, automatically balancing cycles are skipped due to a detected charge current. 0: False 1: True
6:1	R	AUTO_BALANCING_ COUNT_STS	6'b 000000	Shows the number of automatically balancing cycles that are actually performed. To be valid, BAL_DONE_STS (A6h, bit[1]) must be set to true. If any balancing cycle is skipped, the reason can be verified by reading bit[10], bit[9], bit[8], or bit[7] of this command. These bits are not updated when AUTO_BAL_ALWAYS (A7h, bit[2]) is enabled.
0	R	BALANCING_ACTIVE	1'b 0	Reports whether cell-balancing is currently ongoing. 0: False 1: True

BAL_LIST (A5h)

Format: Unsigned binary

The BAL_LIST command reports which cell is balanced during the next balancing session.

Bits	Access	Bit Name	Default	Description
15	R/W	CELL_16_TO_ BALANCE	1'b 0	When true, cell 16 is balanced during the next balancing session. When false, cell 16 is skipped. 0: False 1: True
14	R/W	CELL_15_TO_ BALANCE	1'b 0	When true, cell 15 is balanced during the next balancing session. When false, cell 15 is skipped. 0: False 1: True
13	R/W	CELL_14_TO_ BALANCE	1'b 0	When true, cell 14 is balanced during the next balancing session. When false, cell 14 is skipped. 0: False 1: True
12	R/W	CELL_13_TO_ BALANCE	1'b 0	When true, cell 13 is balanced during the next balancing session. When false, cell 13 is skipped. 0: False 1: True
11	R/W	CELL_12_TO_ BALANCE	1'b 0	When true, cell 12 is balanced during the next balancing session. When false, cell 12 is skipped. 0: False 1: True
10	R/W	CELL_11_TO_ BALANCE	1'b 0	When true, cell 11 is balanced during the next balancing session. When false, cell 11 is skipped. 0: False 1: True
9	R/W	CELL_10_TO_ BALANCE	1'b 0	When true, cell 10 is balanced during the next balancing session. If false, cell 10 is skipped. 0: False 1: True

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8	R/W	CELL_9_TO_ BALANCE	1'b 0	When true, cell 9 is balanced during the next balancing session. When false, cell 9 is skipped. 0: False 1: True
7	R/W	CELL_8_TO_ BALANCE	1'b 0	When true, cell 8 is balanced during the next balancing session. When false, cell 8 is skipped. 0: False 1: True
6	R/W	CELL_7_TO_ BALANCE	1'b 0	When true, cell 7 is balanced during the next balancing session. When false, cell 7 is skipped. 0: False 1: True
5	R/W	CELL_6_TO_ BALANCE	1'b 0	When true, cell 6 is balanced during the next balancing session. When false, cell 6 is skipped. 0: False 1: True
4	R/W	CELL_5_TO_ BALANCE	1'b 0	When true, cell 5 is balanced during the next balancing session. When false, cell 5 is skipped. 0: False 1: True
3	R/W	CELL_4_TO_ BALANCE	1'b 0	When true, cell 4 is balanced during the next balancing session. When false, cell 4 is skipped. 0: False 1: True
2	R/W	CELL_3_TO_ BALANCE	1'b 0	When true, cell 3 is balanced during the next balancing session. When false, cell 3 is skipped. 0: False 1: True
1	R/W	CELL_2_TO_ BALANCE	1'b 0	When true, cell 2 is balanced during the next balancing session. When false, cell 2 is skipped. 0: False 1: True
0	R/W	CELL_1_TO_ BALANCE	1'b 0	When true, cell 1 is balanced during the next balancing session. When false, cell 1 is skipped. 0: False 1: True

BAL_CTRL (A6h)

Format: Unsigned binary

The BAL_CTRL command reports whether an error occurs when balancing starts or cell-balancing is completed. It also controls the start for both manual and automatic cell-balancing.

Bits	Access	Bit Name	Default	Description
15:3	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
2	R	BAL_ERROR_STS	1'b 0	Reports whether an error occurs when balancing starts (e.g. if open-wire detection is already running). 0: False 1: True

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1	R	BAL_DONE_STS	1'b 0	Reports whether cell-balancing is completed. 0: False 1: True
0	R/W	BALANCE_GO	1'b 0	Controls the start for both manual and automatic cell-balancing. When turned on, balancing begins. 0: Off 1: On

BAL_CFG (A7h)

Format: Unsigned binary

The BAL_CFG command configures the number of repetitions to execute the balancing list. It also enables continuous balancing and automatic balancing.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
7:3	R/W	BAL_REPETITION	5'b 11111	Sets the number of repetitions for each execution of the balancing list. When set to 31 repetitions, 32 balancing cycles are executed. LSB: 1 repetition Range: 0 to 31 repetitions Value (repetitions) = Setting These bits allow OTP.
2	R/W (can lock to read-only)	AUTO_BAL_ALWAYS	1'b 0	This bit is used only when automatic cell-balancing is enabled. When disabled, automatic cell-balancing uses bits[7:3] of this command to control how many iterations the device repeats. When enabled, balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, disable this bit. 0: Disabled 1: Enabled This bit allows OTP.
1	R/W (can lock to read-only)	BALANCE_MODE_REG	1'b 0	Controls the cell-balancing mode. 0: Manual cell-balancing 1: Automatic cell-balancing This bit allows OTP.
0	R/W (can lock to read-only)	BALANCE_MODE_CTRL	1'b 0	This bit is used only when automatic cell-balancing is enabled. This feature is only available on I^2C versions of the MP2795. 0: Register control (BALANCE_GO, set via A6h, bit[0]) 1: GPIO3 control (the direction of GPIO3 is set as the input, and the input type is set as digital input). When set to high, balancing begins. This bit allows OTP.

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BAL_THR (A8h)

Format: Unsigned binary

The BAL_THR command configures the cell-balancing threshold and the minimum cell voltage to run automatic cell-balancing. The command also enables suspending automatic balancing if the die temperature is too hot, and it enables automatic balancing at the standby/charging current.

Bits	Access	Bit Name	Default	Description
15:13	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
12:10	R/W	BAL_MSM_TH	3'b 010	Sets the cell-balancing threshold used by the automatic cell-balancing algorithm. LSB: 9.765 mV Offset: 19.5 mV Range: 19.5 mV to 87.855 mV Value (mV) = Setting x 9.765 + 19.5 These bits allow OTP.
9	R/W	STOP_ON_HOT	1'b 0	This bit is used only when automatic cell-balancing is enabled. 0: Does not suspend automatic cell-balancing if the silicon digital die temperature is too hot 1: Suspends automatic cell-balancing if the silicon digital die temperature is too hot
8	R	RESERVED	N/A	Reserved. Do not change the value of this bit.
7	R/W	ABAL_ON_STBY	1'b 0	This bit is used only when automatic cell-balancing is enabled. 0: Automatic balancing does not run when the current is between 0A and the standby threshold 1: Automatic balancing can run when the current is between 0A and the standby threshold
6	R/W	ABAL_ON_CHARGE	1'b 0	This bit is used only when automatic cell-balancing is enabled. 0: Automatic balancing does not run when there is a charge current that exceeds the charge standby threshold 1: Automatic balancing can run when there is a charge current that exceeds the charge standby threshold
5:0	R/W	CELL_BAL_MIN	6'b 100001	Sets the qualifying minimum cell voltage to run automatic cell-balancing. When a cell is below this level, it is excluded from the balancing list, while other qualifying cells could be balanced if they meet applicable criteria. LSB: 39.0625 mV Range: 2500 mV to 4960.9375 mV Value (mV) = Setting x 39.0625 These bits allow OTP.

MEM_STATUS (B4h)

Format: Unsigned binary

The MEM_STATUS command reports the status of the multiple-time programmable (MTP) memory.

Bits	Access	Bit Name	Default	Description
15:6	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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5:3	R	MTP_STATUS	3'b 001	Returns the thermometer-coded confirmation status of the MTP: 3'bxx1: MTP Page 1 has been fully configured, and the MTP-backed registers can be loaded and use NVM CRC if enabled 3'bx1x: MTP Page 2 has been fully configured, and the MTP-backed registers can be loaded and use NVM CRC if enabled 3'b1xx: MTP Page 3 has been fully configured, and the MTP-backed registers can be loaded and use NVM CRC if enabled
2:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

OTP_CRC_STATUS (B6h)

Format: Unsigned binary

The OTP_CRC_STATUS command reports the one-time programmable (OTP) cyclic redundancy check (CRC) error status.

Bits	Access	Bit Name	Default	Description
15	R	OTP_CRC_ERROR	N/A	Reports whether an OTP CRC error has been detected. This bit is set by a CRC error during OTP restoration, and it is reset by the restore command. 0: Not detected 1: Detected
14:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

NVM_CRC_STATUS (B7h)

Format: Unsigned binary

The NVM_CRC_STATUS command reports the non-volatile memory (NVM) cyclic redundancy check (CRC) error status.

Bits	Access	Bit Name	Default	Description
15	R	NVM_CRC_ERROR	N/A	Reports whether an NVM CRC error has been detected. This bit is set by a CRC error during NVM restoration, and it is reset by the restore command. 0: Not detected 1: Detected
14:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

OTP_STORE_CMD (B8h)

Format: Unsigned binary

The OTP_STORE_CMD command reports whether the store function is in progress. It also enables storing all multiple-time programmable (MTP) registers and the MTP cyclic-redundancy check (CRC) code in the non-volatile memory (NVM).

Bits	Access	Bit Name	Default	Description
15	R	STORE_IN_PROGRESS	1'b 0	Reports whether the store function is in progress. 0: Storage of register data to the MTP memory is not in progress 1: Storage of register data to the MTP memory is in progress
14:4	R	RESERVED	N/A	Reserved. Do not change the value of these bits.
3	R/W	STORE_NVM_CMD	1'b 0	Stores all MTP registers and the MTP CRC code in the NVM if STORE_CMD_ACCESS_CODE (B9h, bits[15:0]) has been configured with the correct code. This is a self-clearing register.
2:0	R	RESERVED	N/A	Reserved. Do not change the value of these bits.

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STORE_CMD_ACCESS_CODE (B9h)

Format: Unsigned binary

The STORE_CMD_ACCESS_CODE command controls access to the store command.

Bits	Access	Bit Name	Default	Description
15:0	R/W	STORE_CMD_ ACCESS_CODE	16'b 00000000 00000000	Before enabling the STORE_NVM_CMD (B8h, bit[3]), 0xA5B6 must be written to these bits to allow for the store command. These bits should be cleared once storage is complete.

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LOCK REGISTER MAP

The MP2795 supports the configuration register lock function. This prevents critical safety settings from changing due to unforeseen circumstances All the bits in an address that are not populated by a register should be treated as reserved. The value of these reserved bits may be 0 or 1, and should be set to 0 when there are write operations changing other bits in the same address. Setting these reserved bits to 0 does not change the value of the reserved bits. Once the lock bit is set to 1, it cannot be set to 0 unless the MP2795 is reset.

All of the locking bits support the multiple-time programmable (MTP) memory, and the default value is 0. If the lock bit in the MTP is set to 1, the corresponding setting register cannot be modified anymore. Before setting the MTP command, carefully consider whether to set the locking bit to 1.

Table 17 shows the lock register map.

Table 17: Lock Register Map

Register Location and Bit Position for Locking	Locked Address Name and Location	Locked Field Bit Position and Name
AAh, bit[15]	FET_MODE (13h)	Bit[11]: CHG_SOFTON_OC_LIM Bit[9]: TURNON_TIMEOUT_FAULT Bit[8]: CHG_TURNON_TIMER
	FET_CFG (14h)	Bits[14:12]: FET_DRV_LVL Bits[11:9]: CHG_SOFTON_PUP Bits[2:0]: DSG_SOFTON_DV
AAh, bit[14]	FET_MODE (13h)	Bit[3]: FET_ON_RUN_SC_DET_EN
AAh, bit[13]	WDT_CFG (10h)	Bits[15:9]: WDT_BITE_CFG Bits[8:2]: WDT_BARK_CFG Bit[0]: WDT_COM_CTRL
AAh, bit[12]	PINS_CFG (0Dh)	Bit[8]: GPIO_LV_CFG Bit[6]: WDT_RST_EN Bit[5]: WDT_RPT Bit[0]: ALERT_POL
AAh, bit[11]	GPIO_CFG (0Ch)	Bit[11]: GPIO3_FSEL Bit[10]: GPIO3_PUP Bit[9]: GPIO3_TYPE Bit[8]: GPIO3_IO Bit[6]: GPIO2_PUP Bit[5]: GPIO2_TYPE Bit[4]: GPIO2_IO Bit[2]: GPIO1_PUP Bit[1]: GPIO1_TYPE Bit[0]: GPIO1_IO
AAh, bit[10]	LOAD_CHARGER_CFG (09h)	Bit[5]: CH_CONN_P_SBY
AAh, bit[9]	LOAD_CHARGER_CFG (09h)	Bit[2]: LD_PLUGIN_DET_EN Bit[1]: CH_PLUGIN_DET_EN
AAh, bit[8]	RGL_CFG (08h)	Bit[2]: V3P3_SHDN_EN
AAh, bit[6]	STB_CFG: 0x06	Bits[5:4]: STBY_MONITOR_CFG
AAh, bit[5]	STB_CFG: 0x06	Bit[6]: STBY_PFET_EN

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AAh, bit[3]	ACT_CFG (05h)	Bit[9]: FT_STATE_SEL
AAh, bit[2]	ACT_CFG (05h)	Bit[1]: FET_CFG
AAh, bit[1]	ACT_CFG (05h)	Bit[0]: FET_SRC
ABh, bit[14]	HR_SCAN2 (9Eh)	Bit[8]: NTC4_READ_EN Bit[7]: NTC3_READ_EN Bit[6]: NTC2_READ_EN Bit[5]: NTC1_READ_EN
ABh, bit[13]	HR_SCAN2 (9Eh)	Bit[2]: GPIO3_READ_EN Bit[1]: GPIO2_READ_EN Bit[0]: GPIO1_READ_EN
ABh, bit[12]	HR_SCAN1 (9Dh)	Bit[15]: CELL_16_V_READ_EN Bit[14]: CELL_15_V_READ_EN Bit[13]: CELL_14_V_READ_EN Bit[12]: CELL_13_V_READ_EN
ABh, bit[11]	TRIMG_IPCB (9Bh)	Bits[9:0]: I_PCB_GAIN_VALUE
ABh, bit[7]	DIE_CFG (46h)	Bit[3]: DIE_TEMP_DIG_FAULT_EN
ABh, bit[6]	DIE_CFG (46h)	Bit[1]: DIE_TEMP_DIG_EN
ABh, bit[4]	CELLFT_CTRL (35h)	Bit[5]: CELL_OV_FAULT_EN Bit[2]: CELL_UV_FAULT_EN
ABh, bit[3]	PACKFT_CTRL (34h)	Bit[12]: CELL_MSMT_FAULT_EN Bit[9]: CELL_DEAD_FAULT_EN Bit[5]: VTOP_OV_FAULT_EN_CTRL Bit[1]: VTOP_UV_FAULT_EN_CTRL
ABh, bit[2]	SCFT_CTRL (2Ah)	Bit[5]: SC_CHG_FAULT_EN Bit[4]: SC_DCHG_FAULT_EN Bit[1]: SC_CHG_EN_CTRL Bit[0]: SC_DCHG_EN_CTRL
ABh, bit[1]	OCFT_CTRL (23h)	Bit[8]: OC_CHG_FAULT_EN Bit[7]: OC2_DCHG_FAULT_EN Bit[6]: OC1_DCHG_FAULT_EN Bit[2]: OC_CHG_EN_CTRL Bit[1]: OC2_DCHG_EN_CTRL Bit[0]: OC1_DCHG_EN_CTRL
ABh, bit[0]	INT0_EN (19h)	Bit[15]: INT_ALERT_CTRL
ACh, bit[15]	COMM_CFG (A3h)	Bits[14:8]: DEVICE_ADD
ACh, bit[14]	COMM_CFG (A3h)	Bit[2]: USE_COMM_CRC
ACh, bit[13]	HR_SCAN1 (9Dh)	Bit[11]: CELL_12_V_READ_EN Bit[10]: CELL_11_V_READ_EN
ACh, bit[11]	FET_MODE (13h)	Bit[4]: CHG_SOFTON_EN Bit[0]: DSG_SOFTON_EN
ACh, bit[10]	NTC_CFG (47h)	Bit[15]: PCB_MNTR_FAULT_EN
ACh, bit[9]	NTC_CFG (47h)	Bit[14]: NTC_CELL_COLD_FAULT_EN Bit[13]: NTC_CELL_HOT_FAULT_EN

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ACh, bit[8]	NTC_CFG (47h)	Bit[10]: NTCB_DYNAMIC_ON
ACh, bit[7]	NTC_CFG (47h)	Bit[7]: NTC4_TYPE_SEL
ACh, bit[6]	NTC_CFG (47h)	Bit[6]: NTC4_EN
ACh, bit[5]	NTC_CFG (47h)	Bit[5]: NTC3_TYPE_SEL
ACh, bit[4]	NTC_CFG (47h)	Bit[4]: NTC3_EN
ACh, bit[3]	NTC_CFG (47h)	Bit[3]: NTC2_TYPE_SEL
ACh, bit[2]	NTC_CFG (47h)	Bit[2]: NTC2_EN
ACh, bit[1]	NTC_CFG (47h)	Bit[1]: NTC1_TYPE_SEL
ACh, bit[0]	NTC_CFG (47h)	Bit[0]: NTC1_EN
ADh, bit[15]	CELL_UV (38h)	Bits[11:8]: CELL_UV_DG Bits[7:0]: CELL_UV
ADh, bit[14]	CELL_OV (39h)	Bits[11:8]: CELL_OV_DG Bits[7:0]: CELL_OV
ADh, bit[13]	NTCC_OTHR_DSG (48h)	Bits[9:0]: NTC_CELL_HOT_DISCH
	NTCC_UTHR_DSG (49h)	Bits[9:0]: NTC_CELL_COLD_DISCH
	NTCC_OTHR_CHG (4Ah)	Bits[9:0]: NTC_CELL_HOT_CHG
	NTCC_UTHR_CHG (4Bh)	Bits[15:11]: NTC_CELL_HYST Bits[9:0]: NTC_CELL_COLD_CHG
ADh, bit[10]	CELLS_CTRL (00h)	Bits[3:0]: CELL_S_CTRL
ADh, bit[9]	SELF_CFG (56h)	Bit[15]: OTP_FAULT_EN
ADh, bit[8]	SELF_CFG (56h)	Bit[14]: 3V3_VDD_FAULT_EN
ADh, bit[7]	SELF_CFG (56h)	Bit[10]: OPEN_WIRE_PON
ADh, bit[6]	SELF_CFG (56h)	Bit[9]: OPEN_WIRE_FAULT_EN
ADh, bit[4]	SELF_CFG (56h)	Bit[6]: OTP_CRC_EN
ADh, bit[3]	SELF_CFG (56h)	Bit[3]: ADC_SELF_TEST_EN
ADh, bit[2]	SELF_CFG (56h)	Bit[2]: VDD_EN
ADh, bit[1]	SELF_CFG (56h)	Bit[1]: 3V3_EN
ADh, bit[0]	SELF_CFG (56h)	Bit[0]: REGIN_EN
AEh, bit[15]	DSGSC_CFG (2Bh)	Bits[14:8]: SC_DCHG_DG Bit[5]: SC_DCHG_RNG Bits[4:0]: SC_DCHG_LIM
AEh, bit[14]	CHGSC_CFG (2Ch)	Bits[14:8]: SC_CHG_DG Bit[5]: SC_CHG_RNG Bits[4:0]: SC_CHG_LIM
AEh, bit[13]	DSGOC_LIM (24h)	Bit[13]: OC2_DCHG_RNG Bits[12:8]: OC2_DCHG_LIM
	DSGOC_DEG (25h)	Bit[14]: OC2_DCHG_DGL_RNG Bits[13:8]: OC2_DCHG_DGL

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AEh, bit[12]	DSGOC_LIM (24h)	Bit[5]: OC1_DCHG_RNG Bits[4:0]: OC1_DCHG_LIM
	DSGOC_DEG (25h)	Bit[6]: OC1_DCHG_DGL_RNG Bits[5:0]: OC1_DCHG_DGL
AEh, bit[11]	CHGOC_DEG (26h)	Bit[14]: OC_CHG_DGL_RNG Bits[13:8]: OC_CHG_DG Bit[5]: OC_CHG_RNG Bits[4:0]: OC_CHG_LIM
AEh, bit[9]	FT_REC (60h)	Bit[12]: DIE_TEMP_FAULT_REC
AEh, bit[8]	FT_REC (60h)	Bit[10]: SC_CHG_REC
AEh, bit[7]	FT_REC (60h)	Bit[9]: SC_DCHG_REC
AEh, bit[6]	FT_REC (60h)	Bit[8]: OC_CHG_REC
AEh, bit[5]	FT_REC (60h)	Bit[7]: OC2_DCHG_REC
AEh, bit[4]	FT_REC (60h)	Bit[6]: OC1_DCHG_REC
AEh, bit[2]	FT_REC (60h)	Bit[4]: PCB_MNTR_REC
AEh, bit[1]	FT0_CFG (61h)	Bit[11]: CELL_OV_REC Bit[7]: CELL_UV_REC
AEh, bit[0]	FT_REC (60h)	Bit[2]: NTC_CELL_CHG_REC Bit[1]: NTC_CELL_DCHG_REC
AFh, bit[6]	FT0_CFG (61h)	Bit [9]: CELL_OV_LOGIC_SEL
AFh, bit[3]	FT0_CFG (61h)	Bit[5]: CELL_UV_LOGIC_SEL
B0h, bit[15]	PACKFT_CTRL (34h)	Bit[8]: CELL_DEAD_EN
B0h, bit[13]	CELLFT_CTRL (35h)	Bit[4]: CELL_OV_EN_CTRL Bit[1]: CELL_UV_EN_CTRL
B0h, bit[11]	BAL_CFG (A7h)	Bit[2]: AUTO_BAL_ALWAYS
B0h, bit[10]	BAL_CFG (A7h)	Bit[1]: BALANCE_MODE_REG
B0h, bit[9]	BAL_CFG (A7h)	Bit[0]: BALANCE_MODE_CTRL (I^2C versions only)

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APPLICATION INFORMATION

PCB Layout Guidelines

Proper PCB layout is critical to reduce noise, and to optimize the device's accuracy and reliability. For the best results, refer to Figure 22, Figure 23, and Figure 24, and follow the guidelines below:

1. Route the ground plane to reduce ground noise and prevent stray current (see Figure 22).

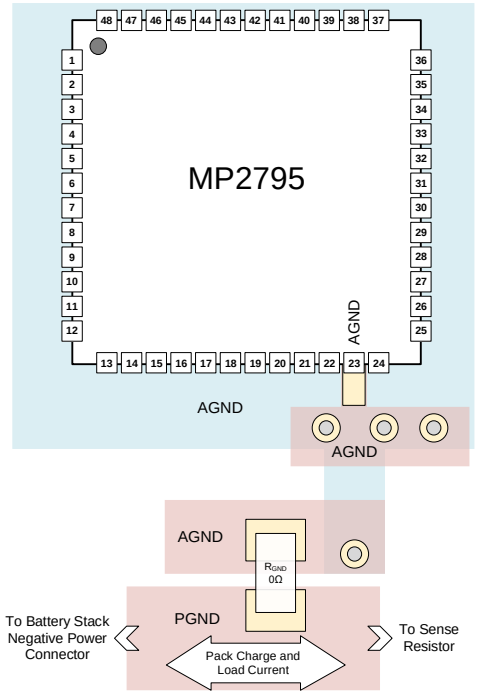


Figure 22: Recommended Layout for AGND

2. Connect the AGND pin to a dedicated ground plane. Then connect the AGND plane to the negative terminal of the battery stack via a 0Ω resistor.
3. Check the schematic and layout to ensure that each component is connected to the correct ground (power vs. signal). For example, the diodes protecting the different power terminals should be connected to the power ground.
4. Consider the expected maximum peak load current, then check the power ground length, width, and thickness to ensure that there is an appropriate low-resistance path that prevents voltage drops.
5. The REGIN, VDD, VREF, 3V3, and NTCB pins require external decoupling capacitors, which should be placed as close as possible to each pin. Minimize the trace inductance from these pins to AGND (see Figure 23).

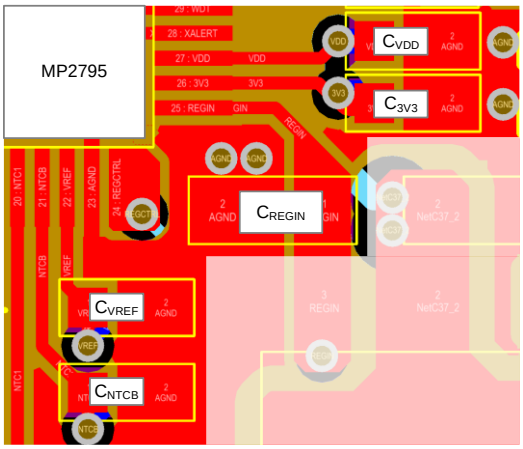


Figure 23: Recommended Layout for Decoupling Capacitors

6. Consider Kelvin connections at the sense resistor. A sense resistor with a dedicated sensing pad is ideal, where a simple two-terminal sense resistor can be used in a 4-wire sensing configuration.
7. Route the sensing signals to SRP and SRN in parallel to avoid coupling interfering signals (see Figure 24).

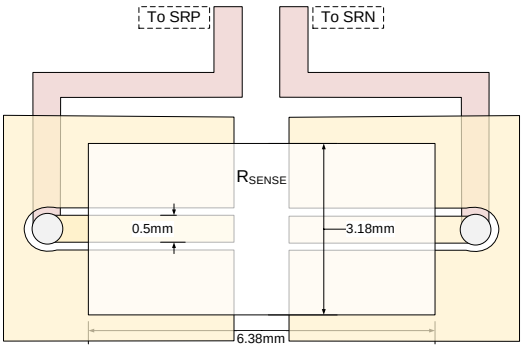


Figure 24: 2512 Sense Resistor Using 4-Wire Footprint

8. Connect the temperature sensors (NTCx) (where x = 1 to 4) to AGND using the star connection technique to avoid contaminating the voltage reading with the resistive voltage drop caused by the load or charging ground current.
9. Route the two wires connecting the NTCx pins together in twisted pairs to avoid coupling interfering signals. This is recommended if NTCx is located off-board.

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TYPICAL APPLICATION CIRCUIT

Figure 25 shows the typical external components and connections required to interface the MP2795 to the battery pack and the system.

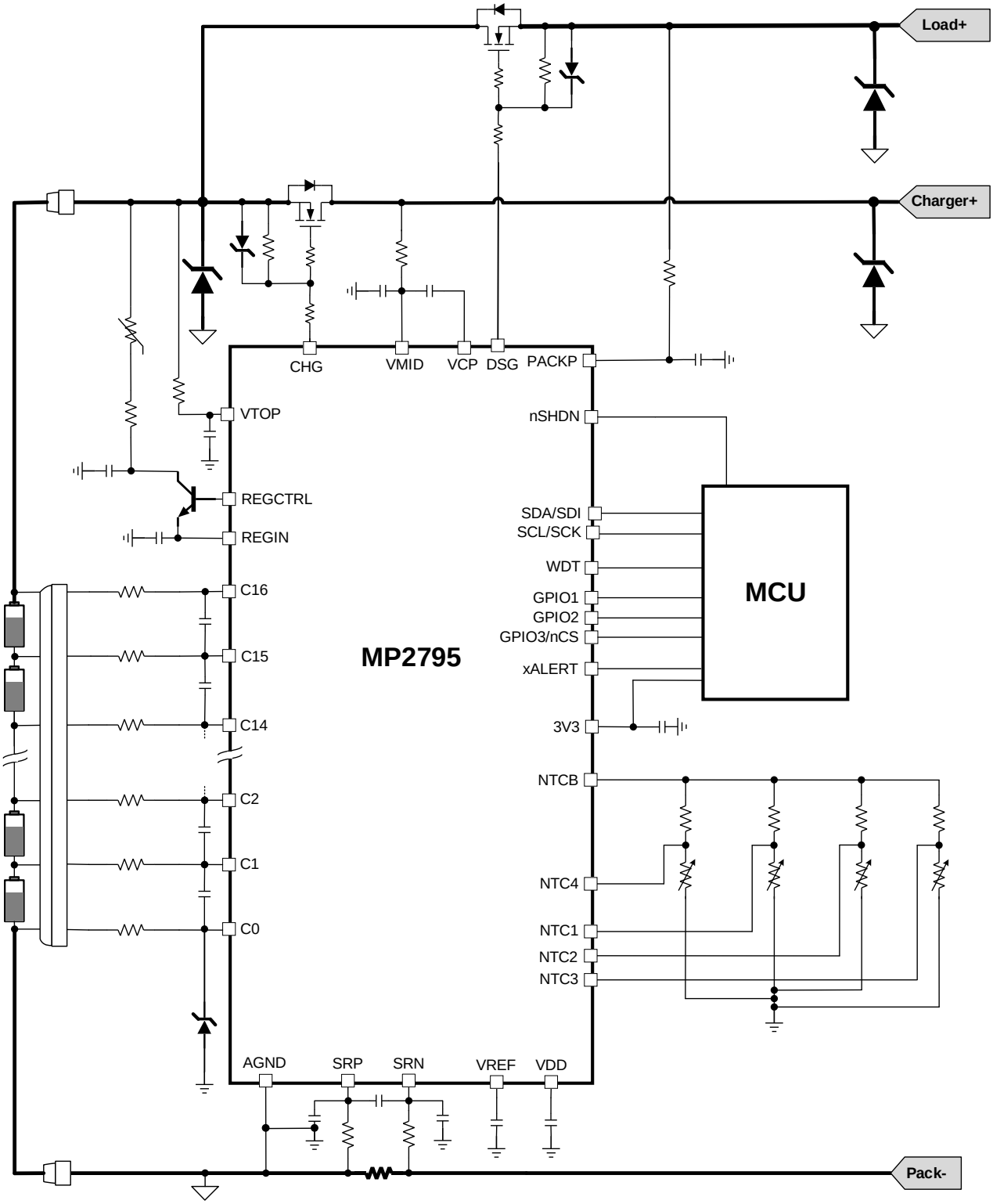


Figure 25: Typical Application Circuit for the MP2795

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Recommended External Components

Figure 26 shows a detailed view of all the typical recommended external components.

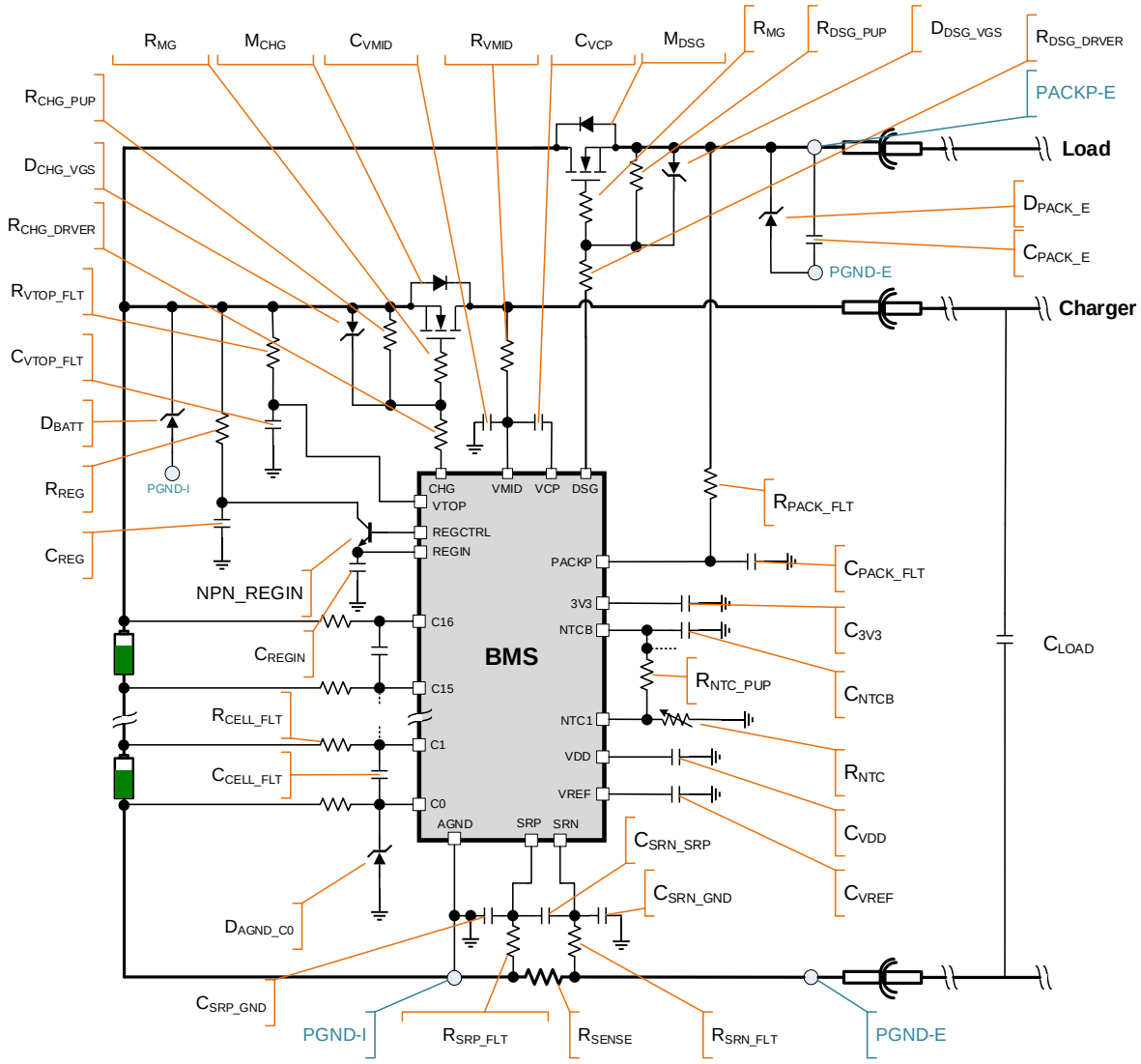


Figure 26: Recommended External Component Diagram

Table 18 on page 144 provides guidance regarding which parameters should be evaluated when selecting each BOM component (see the Configuration for External or Internal Cell-Balancing section on page 148 for more details on cell-balancing). Refer to the MP2795 evaluation board datasheet to see each BOM component.

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Table 18: Recommended Components

Parameter Identifier	Parameter Description	Component Description	Parameter Comments	Min	Typ	Max	Unit
General							
$D_{AGND-C0}$	Recommended Zener diode voltage rating	AGND-C0 Zener diode voltage			3.3		V
C_{PACK_E}	Capacitance	External pack capacitor			47	200	µF
Pin Filtering							
C_{VTOP_FLT}	Required capacitance	VTOP-filtering capacitor			470		nF
R_{VTOP_FLT}	Required resistance	VTOP-filtering resistor			20		Ω
C_{PACK_FLT}	Required capacitance	PACKP-filtering capacitor	If R_{PACK_FLT} increases, C_{PACK_FLT} should be proportionally decreased		10		nF
R_{PACK_FLT}	Required resistance	PACKP-filtering resistor			100		Ω
R_{VMID}	Required resistance	VMID-filtering resistor			100		Ω
Cell Voltage Sensing							
C_{CELL_FLT}	Required capacitance	Cell-filtering capacitor			100		nF
R_{CELL_FLT}	Required resistance	Cell-filtering resistor		20	100		Ω
N-Channel MOSFET Driver							
$D_{CHG-VGS}$	Recommended Zener diode voltage rating	Diode charge (CHG) V_{GS} protection	For a CHG N-channel MOSFET with a ±20V maximum gate-source voltage (V_{GS}). If the CHG N-channel MOSFET has a smaller V_{GS}, decrease the Zener voltage accordingly		16		V
$D_{DSG-VGS}$	Recommended Zener diode voltage rating	Diode discharge (DSG) V_{GS} protection	For a DSG N-channel MOSFET with a ±20V maximum V_{GS}. If the DSG N-channel MOSFET has a smaller V_{GS}, decrease the Zener voltage accordingly		16		V
R_{CHG_PUP}	Recommended resistance	Charge N-channel MOSFET pull-up resistor			10		MΩ
R_{DSG_PUP}	Recommended resistance	Discharge N-channel MOSFET pull-up resistor			10		MΩ
R_{CHG_DRVER}	Required resistance	N-channel MOSFET charge driver protection resistor			100		Ω
R_{DSG_DRVER}	Required resistance	N-channel MOSFET discharge driver protection resistor			100		Ω

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R_{MG}	Required resistance	N-channel MOSFET gate protection resistor			100		Ω
Current Sensing							
R_{SRN_FLT}	Recommended resistance	SRN filtering resistor			100		Ω
C_{SRN_GND}	Recommended capacitance	SRN-to-ground filtering capacitor			100		nF
C_{SRN_SRP}	Recommended capacitance	SRN/SRP differential filtering capacitor			100		nF
R_{SRP_FLT}	Recommended resistance	SRP filtering resistor			100		Ω
C_{SRP_GND}	Recommended capacitance	SRP-to-ground filtering capacitor			100		nF
R_{SENSE}	Recommended resistance	Pack current-sense resistor	The min and max values are recommended and are based on the current-sense range	0.2	2	5	mΩ
Regulators							
C_{3V3}	Required capacitance	3.3V capacitor		0.47	1	10	µF
C_{VCP}	Required capacitance	VCP-VMID capacitor			47		nF
	Required voltage rating		The rating can be proportionally reduced if fewer than 16 stacked cells are used	80			V
C_{VDD}	Required capacitance	VDD bypass capacitor			1		µF
C_{VMID}	Required capacitance	VMID bypass capacitor			100		nF
C_{VREF}	Required capacitance	VREF bypass capacitor			1		µF
C_{REGIN}	Required capacitance	REGIN capacitor			3.3		µF
C_{REG}	Required capacitance	Regulator capacitor			1		µF
R_{REG}	Regulator-limiting resistance	Regulator-limiting resistance			500		Ω
Temperature Sensing							
R_{NTC_PUP}	Typical resistance	NTC pull-up	This is a typical value. Generally, the NTC pull-up value should match the NTC thermistor value at 25°C		10		kΩ
R_{NTC}	Typical resistance	NTC thermistor	If a smaller resistance is used, the NTCB current limit should be evaluated and compared to the total resistance connected to NTCB in the worst-case scenario (hot temperatures)		10		kΩ
C_{NTCB}	NTCB capacitance	NTCB capacitor				10	nF

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Configuration for External or Internal Cell-Balancing

Cell-balancing can be implemented via the internal balancing MOSFETs for up to 58mA. Higher cell-balancing current is possible with external MOSFETs or bipolar junction transistors (BJTs) (see Figure 27).

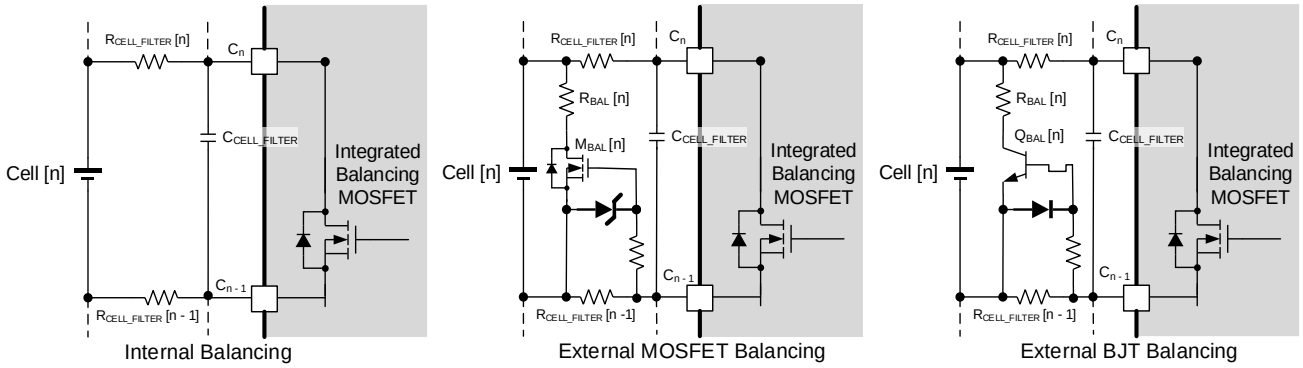


Figure 27: Typical Schematics Internal vs. External Balancing Configurations

The recommended components for each of these three balancing configurations are provided in Table 19 as well as Table 20 and Table 21 on page 149. Table 19 show recommended components for internal MOSFET balancing.

Table 19: Recommended Component Selection for Internal MOSFET Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for internal balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		100		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for internal balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	20	100		Ω

The amount of current provided in an internal balancing configuration is easily derived by following the required resistance for the cell-filtering resistor (R_{CELL_FILTER}) and considering the integrated MOSFET balancing resistance ($R_{DS(ON)_BAL_FET}$). For example, for a lithium cell at 4V where R_{CELL_FILTER} is 20Ω, the resistive path allows for 58mA once the integrated balancing resistor MOSFET is enabled.

For higher balancing current, Table 20 and Table 21 on page 149 provide guidance on selecting the MOSFET or BJT circuit components.

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Table 20 shows recommended components for external MOSFET balancing.

Table 20: Recommended Component Selection for External MOSFET Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		10		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	800	1000		Ω
R_{BAL}	Required resistance	Cell-balancing current-limiting resistor	Adjust this value to set the balancing current and verify the power dissipation compared to the package limit.		43		Ω
V_{TH_MBAL}	MOSFET V_{GS} threshold	External balancing MOSFET (M_{BAL})	A higher voltage threshold may prevent the MOSFET from turning on.		1.5	1.8	V

The external balancing MOSFETs should be selected using Table 19 on page 126. Choose a MOSFET with a sufficiently low gate-source voltage (V_{GS}) threshold. For simplification, assume that the integrated MOSFET-balancing resistance can be ignored. The available V_{GS} that turns on the MOSFET is generated across R_{CELL_FILTER}, meaning its voltage is half of the lithium cell voltage (e.g. 4.2V / 2 = 2.1V). In this scenario, the V_{GS} threshold for the external balancing MOSFET (M_{BAL}) should be below 2.1V with an appropriate safety margin. The safety margin should allow for voltage drops on the integrated MOSFET balancing resistor. This drop can be caused by the following:

- Changes in the operating conditions
- Shifts in the M_{BAL} V_{GS} threshold across operating conditions
- Drops that develop across the sensing wires due to the balancing current

Table 21 shows recommended components for external BJT balancing.

Table 21: Recommended Component Selection for External BJT Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		100		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	20	100	1000	Ω
R_{BAL}	Required resistance	Cell-balancing current-limiting resistor	Adjust this value to set the balancing current and verify the power dissipation compared to package limit.		43		Ω
h_{FE_QBAL}	BJT DC current gain	External balancing BJT (Q_{BAL})	A lower h_{FE_QBAL} may limit the external balancing current.	50			

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Because the required resistance for the cell-balancing current-limiting resistor (R_{BAL}) sets the balancing current and dissipates most of the power, ensure that an appropriate resistor and resistor package are selected, especially for resistors below 100Ω. For example, if R_{BAL} is 43Ω, there is 410mW of power dissipation when the lithium cell voltage is 4.2V. This means that a minimum 2512 package (6432 metric) should be used.

It is also important to consider the thermal design of the overall board and enclosure. The MP2795 can simultaneously balance only odd or even cells, meaning 8 cells in a 16-cell system. When balancing is run continuously on 8 cells, 3.28W is dissipated as heat with a 43Ω R_{BAL}. To keep the MP2795 in the allowed temperature range, consider how this additional heat can be dissipated, as it is added to the amount of heat generated by other components.

The MP2795 includes compensation for the voltage drop across R_{CELL_FILTER} via the one-time programmable (OTP) command set via CELL_1K_COMP (9Ch, bit[11]). When enabled, this bit compensates for a 1kΩ R_{CELL_FILTER}. Generally, CELL_1K_COMP should be enabled if R_{CELL_FILTER} is a minimum of 500Ω.

Selecting the VCP Capacitor

When multiple MOSFETs in parallel are used for discharge or charge, the VCP capacitance (C_{VCP}) should be selected to avoid causing an excessive voltage drop while the MOSFETs turn on. Table 22 on page 151 shows values for C_{VCP} depending on the MOSFET's total input capacitance (C_{ISS}) that the DSG or CHG MOSFET driver must drive. The total C_{ISS} is obtained from the MOSFET datasheets.

Design the number of parallel DSG MOSFETs to match the number of parallel CHG MOSFETs. If four parallel DSG MOSFETs are used, then the individual MOSFET's C_{ISS} should be multiplied by 4, and the resulting C_{ISS} should be used.

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Table 22: VCP Capacitor Selection

C_{VCP}	Total C_{ISS}
47nF	47nF
68nF	68nF
100nF	100nF

Unused Pins

For a particular application, some pins may not be required. Table 23 shows how to connect these pins when they are not used.

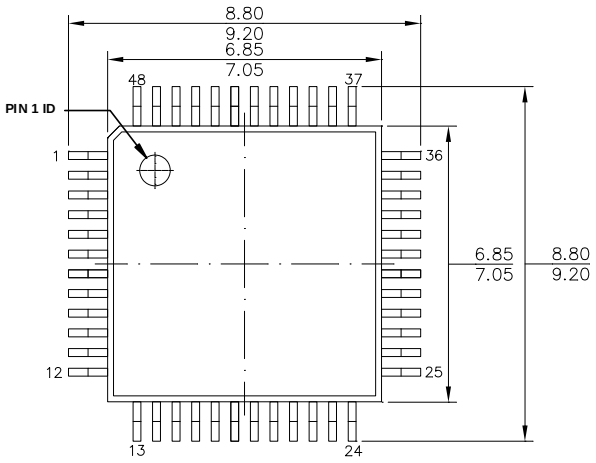
Table 23: Unused Pins Connection

Pin #	Name	Recommendation
1, 2, 3, 4, 5, 6, 46, 47, 48	C8, C9, C10, C11, C12, C13, C14, C15, C16	If fewer than 16 series cells are used, directly connect all unused cell channels to the practical maximum cell channel. For example, if only 10 cells are used, C16 to C10 should be connected together.
15, 16	SRP, SRN	If the current-sense function is not required, connect these pins to AGND.
17, 18, 19, 20	NTC1, NTC2, NTC3, NTC4	Float the unused NTC channels.
21	NTCB	If NTC temperature monitoring is not used, float this pin.
28	XALERT	Float this pin if it is not used.
29	WDT	Float this pin if it is not used.
33	SDO	Float this pin if it is not used.
34	GPIO3/nCS	Float this pin if it is not used. GPIO3 should be set to 20kΩ pull-up mode via the GPIO_CFG (0Ch) command; otherwise, there may be additional power consumption.
35, 36	GPIO1, GPIO2	Float this pin if it is not used. The unused GPIO should be set to 20kΩ pull-up mode via the GPIO_CFG command; otherwise, there may be additional power consumption.
38	PACKP	If the DSG MOSFET driver is not used and the PACKP vs. VTOP comparator is not required, connect this pin to VTOP.
39	DSG	If the high-side MOFSET (HS-FET) drivers are not used and active mode is required, connect this pin to PACKP via a 100Ω resistor and a 1nF capacitor. If active mode is not required, float this pin.
42	VCP	If the HS-FET drivers are not used and active mode is required, connect this pin to VMID via a 47nF VCP capacitor (C_{VCP}). If active mode is not required, float this pin.
43	VMID	If the HS-FET drivers are not used, connect this pin to VTOP.
44	CHG	If the HS-FET drivers are not used and active mode is required, connect this pin to VTOP via a 100Ω resistor and a 1nF capacitor. If active mode is not required, float this pin.

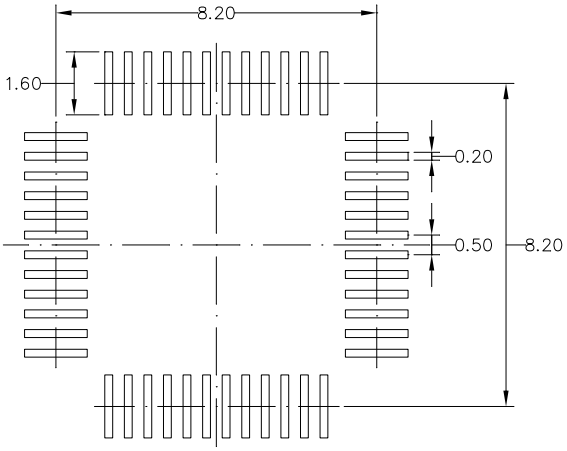
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PACKAGE INFORMATION

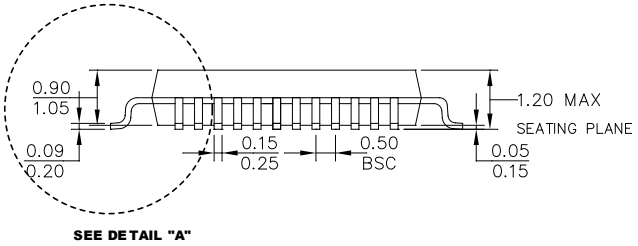
TQFP-48 (7mmx7mm)



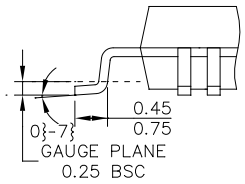
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



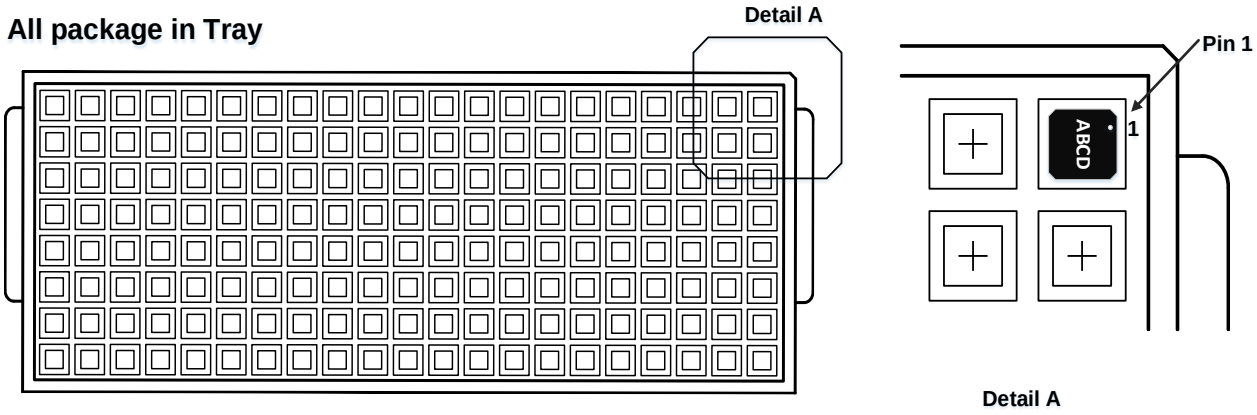
DETAIL "A"

NOTE:

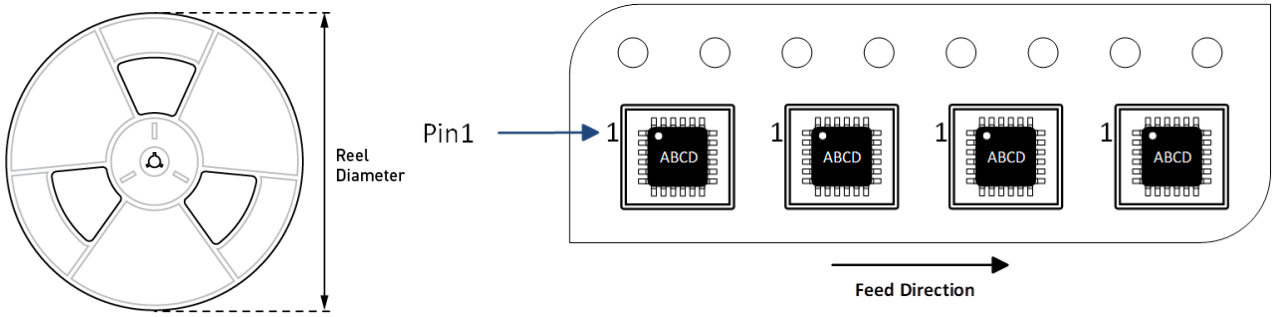
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-143.
6) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2795DFP-xxxx-T	TQFP-48 (7mmx7mm)	N/A	N/A	250pcs	N/A	N/A	N/A



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2795DFP-xxxx-Z	TQFP-48 (7mmx7mm)	2500pcs	N/A	N/A	13in	16mm	12mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/17/2025	Initial Release	-

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