MP9931F

100V Input, Synchronous Step-Down Controller

DESCRIPTION

The MP9931F is a high-voltage, synchronous step-down switching regulator controller that can directly step down voltages from up to 100V. It can drive dual N-channel MOSFET switches.

The MP9931F's adaptive constant-on-time (COT) control architecture provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

Pulse-skip mode (PSM) and ultrasonic mode (USM) enable non-synchronous operation to optimize light-load efficiency.

The MP9931F's switching frequency (f_{SW}) can be configured by an external resistor or synchronized to an external clock for noise-sensitive applications.

Fault protections include precision input over-voltage protection (OVP), output over-current protection (OCP), and thermal shutdown.

The MP9931F is available in a QFN-23 (4.0mmx4.0mm) package.

FEATURES

- Basic Functions:
  - Frequency Spread Spectrum (FSS) for Lower EMI
  - Lossless Low-Side MOSFET (LS-FET) On Resistance ($R_{DS(ON)}$) or Shunt Current Sense
  - Constant-On-Time (COT) Control for Fast Load Transient Response
  - 7V to 100V Input Voltage (V_{IN}) Range
  - Output Voltage (V_{OUT}) Adjustable from 0.8V to 80V
  - 450µA Quiescent Current (I_Q)
  - 4µA Enable (EN) Shutdown Current

FEATURES *(continued)*

  - 60ns Minimum On Time (t_{ON_MIN})
  - Low-Dropout (LDO) Mode: Maximum Duty Cycle Up to 99%
  - Selectable Ultrasonic Mode (USM), Pulse-Skip Mode (PSM), or Forced Continuous Conduction Mode (FCCM) via the MODE Pin
  - Selectable 100kHz to 1000kHz Switching Frequency (f_{SW}) via the FREQ Resistor (R_{FREQ})
  - Power Good (PG) Indicator
  - Selectable Ramp via the RAMP Pin
  - Selectable Current Limit via the ILIM Resistor (R_{ILIM})
  - VDRV Voltage (V_{DRV}) Power from the Output Voltage (V_{OUT}) when V_{OUT} > 8.4V
  - External V_{DRV} with External Voltage Source, which Exceeds Internal V_{DRV}
- Drive Ability:
  - 10V N-Channel MOSFET Gate Driver with 4.2A Source and 5.2A Sink Capability
- Synchronization (SYNCI/SYNCO):
  - SYNCI with External Clock
  - 180° Out-of-Phase SYNCO

APPLICATIONS

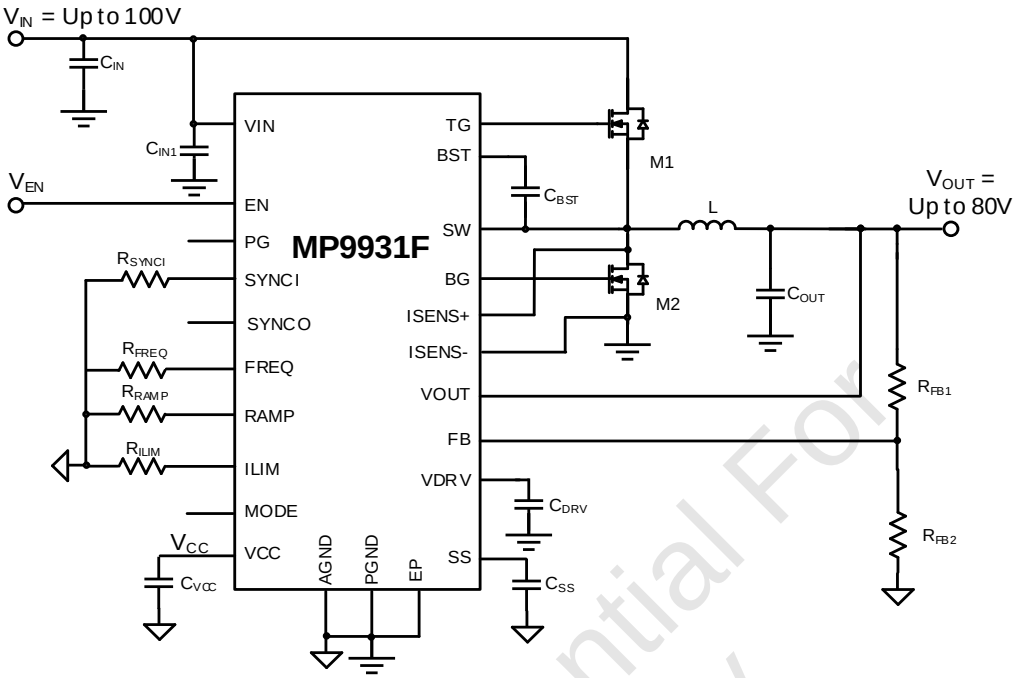
- Energy Storage Systems (ESS)
- USB Power Delivery (PD) Chargers
- Power over Ethernet (PoE) System Power Supplies
- Industrial Power Supplies
- E-Bike Auxiliary Power Supplies
- General-Purpose Power Supplies

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP9931FGR	QFN-23 (4mmx4mm)	*See Below*	1

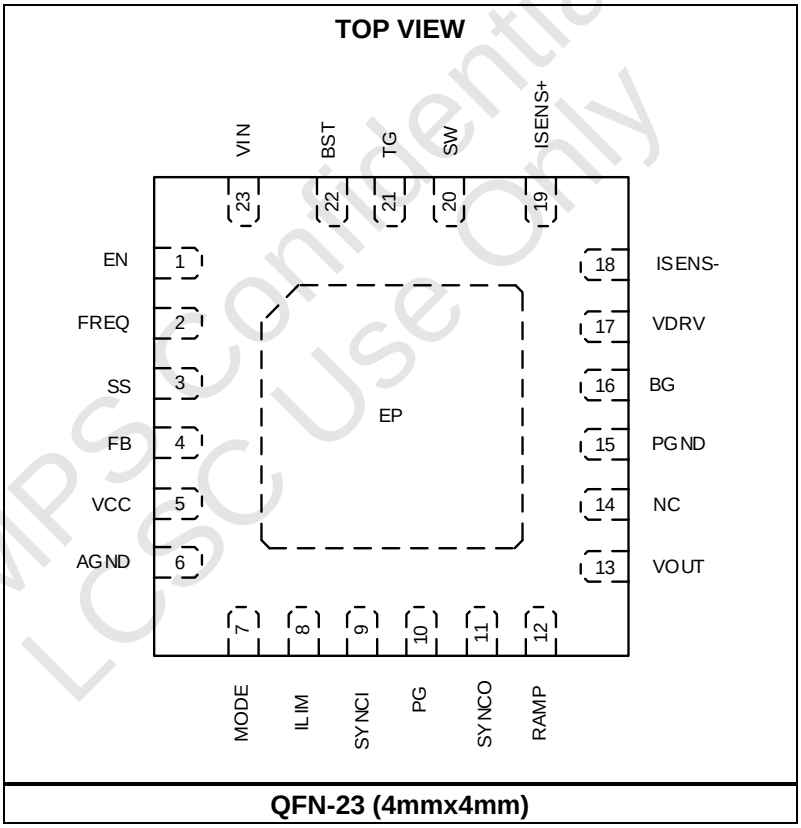
* For Tape & Reel, add suffix -Z (e.g. MP9931FGR-Z).

TOP MARKING

MPSYWW
MP9931
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP9931: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-23 (4mmx4mm)

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PIN FUNCTIONS

<table>
<tr><th>Pin #</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>EN</td><td>Enable control pin. When the EN pin is pulled low, the controller is in shutdown mode and all functions are disabled. When the EN voltage (V_{EN}) is pulled above 1.2V, the soft-start (SS) voltage (V_{SS}) can ramp up, and the pulse-width modulated (PWM) gate-drive signals are delivered to the TG and BG pins.</td></tr>
<tr><td>2</td><td>FREQ</td><td>Switching frequency selection. Connect a resistor between the FREQ and AGND pins to set the switching frequency (f_{SW}). A 1% tolerance resistor is recommended for excellent accuracy. f_{SW} cannot be adjusted online, so it is recommended to turn VIN/EN off then on again after the FREQ pin’s set-up changes.
<table>
<tr><th>FREQ Pin</th><th>f_{SW}</th></tr>
<tr><td>AGND</td><td>100kHz</td></tr>
<tr><td>20kΩ to AGND</td><td>150kHz</td></tr>
<tr><td>45.3kΩ to AGND</td><td>200kHz</td></tr>
<tr><td>80.6kΩ to AGND</td><td>250kHz</td></tr>
<tr><td>124kΩ to AGND</td><td>300kHz</td></tr>
<tr><td>180kΩ to AGND</td><td>400kHz</td></tr>
<tr><td>243kΩ to AGND</td><td>600kHz</td></tr>
<tr><td>VCC</td><td>1MHz</td></tr>
</table></td></tr>
<tr><td>3</td><td>SS</td><td>Soft-start control input. The SS pin configures the soft-start time (t_{SS}) with an external capacitor (C_{SS}) placed between the SS and AGND pins.</td></tr>
<tr><td>4</td><td>FB</td><td>Output feedback. An external resistor divider connected from the output to AGND, tapped to the FB pin, sets the output voltage (V_{OUT}). It is recommended to place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.</td></tr>
<tr><td>5</td><td>VCC</td><td>Internal, 5V low-dropout (LDO) regulator output. Most control circuits are powered from the VCC voltage (V_{CC}). Decouple the VCC pin with a minimum 1µF ceramic capacitor, placed as close to VCC as possible. 2.2µF, ceramic capacitors with X7R or X5R grade dielectrics are recommended due to their stable temperature characteristics.</td></tr>
<tr><td>6</td><td>AGND</td><td>Analog ground. Select the AGND pin as the control circuit’s reference point.</td></tr>
<tr><td>7</td><td>MODE</td><td>Operation mode selection. Pull MODE to V_{CC} to make the part operate in forced continuous conduction mode (FCCM). Float MODE to make the part operate in pulse-skip mode (PSM) with ultrasonic mode (USM) at light loads. Connect MODE to AGND to make the part operate in PSM without USM. The mode can be adjusted online.</td></tr>
<tr><td>8</td><td>ILIM</td><td>Current limit adjustment. Connect a resistor between the ILIM and AGND pins to set the valley current limit. A 1% tolerance resistor is recommended for good accuracy. The current limit can be adjusted online.
<table>
<tr><th>ILIM Pin</th><th>Valley Current Limit</th><th>Negative Current limit</th></tr>
<tr><td>AGND</td><td>25mV</td><td>25mV</td></tr>
<tr><td>51kΩ to AGND</td><td>50mV</td><td>25mV</td></tr>
<tr><td>120kΩ to AGND</td><td>75mV</td><td>50mV</td></tr>
<tr><td>VCC</td><td>100mV</td><td>50mV</td></tr>
</table></td></tr>
<tr><td>9</td><td>SYNCI</td><td>Sync signal input. If an external sync clock is applied to this pin, the internal clock follows the sync frequency (f_{SYNC}).</td></tr>
<tr><td>10</td><td>PG</td><td>Power good (PG) output. The PG pin’s output is an open drain.</td></tr>
<tr><td>11</td><td>SYNCO</td><td>Sync signal output. The SYNCO pin outputs a clock that is 180° out of phase with the internal oscillator clock or external synchronization clock when the device works in continuous conduction mode (CCM), discontinuous conduction mode (DCM), or USM. SYNCO outputs 0V if the device is in sleep mode or over-temperature protection (OTP) is triggered.</td></tr>
</table>

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PIN FUNCTIONS *(continued)*

<table>
<tr><th>Pin #</th><th>Name</th><th>Description</th></tr>
<tr><td>12</td><td>RAMP</td><td>Internal ramp selection. Connect a resistor between RAMP and AGND to set the internal ramp scale. A 1% tolerance resistor is recommended for good accuracy. A large ramp stabilizes chip operation, while a small ramp results in better load transient response performance. RAMP cannot be adjusted online.
<table>
<tr><th>RAMP Pin</th><th>Ramp Scale</th></tr>
<tr><td>AGND</td><td>1</td></tr>
<tr><td>51kΩ to AGND</td><td>0.5</td></tr>
<tr><td>120KΩ to AGND</td><td>0.33</td></tr>
<tr><td>180KΩ to AGND</td><td>2</td></tr>
<tr><td>VCC</td><td>4</td></tr>
</table></td></tr>
<tr><td>13</td><td>VOUT</td><td>V_{OUT} sense and bias supply. The VOUT pin supplies the VDRV voltage (V_{DRV}) and internal VCC regulator. VOUT disables the power from VIN as long as V_{OUT} exceeds 8.4V. The VOUT pin must be connected to the output for the internal on time (t_{ON}) calculation.</td></tr>
<tr><td>14</td><td>NC</td><td>Not connected. Float the NC pin.</td></tr>
<tr><td>15</td><td>PGND</td><td>System ground. The PGND pin is the power ground reference for the internal low-side MOSFET (LS-FET) driver and the VDRV regulator circuit. Connect this pin directly to the negative terminal of the VDRV decoupling capacitor (C_{VDRV}).</td></tr>
<tr><td>16</td><td>BG</td><td>Bottom gate driver. Connect this pin to the gate of the synchronous N-channel MOSFET.</td></tr>
<tr><td>17</td><td>VDRV</td><td>Decoupling input pin for driver power supply. Decouple the VDRV pin with a minimum 4.7µF ceramic capacitor (C_{VDRV}), placed as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended.</td></tr>
<tr><td>18</td><td>ISENS-</td><td>Negative current-sense (CS) input. Lay out ISENS+ and ISENS- with differential pair lines.</td></tr>
<tr><td>19</td><td>ISENS+</td><td>Positive CS input. ISENS+ can be connected to either the LS-FET drain for lossless on resistance ($R_{DS(ON)}$) sensing or a CS resistor (R_{CS}) connected to the LS-FET source for accurate current limit and zero-current detection (ZCD). Lay out ISENS+ and ISENS- with differential pair lines.</td></tr>
<tr><td>20</td><td>SW</td><td>Switch node. The SW pin is the reference for the BST voltage (V_{BST}) supply and high-current returns for the bootstrapped switch.</td></tr>
<tr><td>21</td><td>TG</td><td>Top gate drive. The TG pin drives the top N-channel MOSFET’s gate. The TG driver draws power from the BST capacitor (C_{BST}) and returns power to the SW pin, providing a true floating drive to the top N-channel MOSFET.</td></tr>
<tr><td>22</td><td>BST</td><td>Bootstrap. The BST pin is the positive power supply for the internal, floating high-side MOSFET (HS-FET) driver. Connect a bypass capacitor (C_{BST}) between the BST and SW pins.</td></tr>
<tr><td>23</td><td>VIN</td><td>Input voltage. The VIN pin operates from a 7V to 100V input. A ceramic capacitor is required to prevent large voltage spikes from appearing at the input.</td></tr>
<tr><td>EP</td><td>-</td><td>Exposed pad. Connect the exposed pad to ground.</td></tr>
</table>

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ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN}) ..... -0.3V to +110V
SW .....-0.3V (-5V for <20ns) to +110V
ISENS+.....-0.3V (-5V for <20ns) to +110V
BST - SW..... -0.3V to +14V
V_{DRV} ..... -0.3V to +14V
V_{OUT} .....-0.3V (-5V for <10ns) to +85V
TG - SW.....-0.3V to V_{BST} + 0.3V
BG ..... -0.3V to V_{DRV} + 0.3V
EN .....-0.3V to +6.5V(<100μA when >6V)
All other pins..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) (5)
QFN-23 (4mmx4mm).....4.1W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... 7V to 100V
Output voltage (V_{OUT})..... 0.8V to 80V
External bias voltage (V_{DRV})..... 10.5V to 12V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance

	θ_{JA}	θ_{JB}	
JESDEC (4)	34.7	14.1	°C/W
EV9931F-R-00A (5)	30		°C/W

	θ_{JC_TOP}	θ_{JC_BOT}	
JESDEC (4)	38.1	2.1	°C/W

	ψ_{JT}	
JESDEC (4)	0.7	°C/W
EV9931F-R-00A (5)	5	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The value of θ_{JA} is only valid for comparison with other packages and cannot be used for design purposes. This value is based on a JEDEC51-7 board. They do not represent the performance obtained in an actual application.
5) Measured on the EV9931F-R-00A, a 7.6cmx8cm, 4-layer, 2oz PCB. The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature in the real system, based on equation $T_J = \psi_{JT} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of IC at real application, and T_{CASE_TOP} is case top temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
VDRV Regulator						
VDRV voltage (V_{DRV}) under-voltage lockout (UVLO) rising threshold	$V_{DRV_UV_R}$		6.2	6.5	6.8	V
V_{DRV} UVLO hysteresis	$V_{DRV_UV_HYS}$			600		mV
VDRV voltage	V_{DRV}	I_{DRV} = 0mA	9.7	10	10.3	V
VDRV regulation		I_{DRV} = 20mA		2		%
Output voltage (V_{OUT}) rising threshold, override input voltage (V_{IN}) supplying VDRV	$V_{OUT_VDRV_R}$		8	8.4	8.8	V
V_{OUT} falling threshold, V_{IN} supplying VDRV	$V_{OUT_VDRV_F}$		7	7.4	7.8	V
VCC Regulator						
VCC voltage	V_{CC}	I_{CC} = 0mA	4.8	5	5.2	V
VCC regulation		I_{CC} = 20mA		2		%
Supply Current						
VIN quiescent current	I_Q	V_{IN} = 48V, V_{FB} = 0.84V, V_{OUT} = 0V, PSM		450	500	µA
		V_{IN} = 48V, V_{FB} = 0.84V, V_{OUT} = 12V, PSM		50	60	µA
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		3	4	µA
V_{IN} Over-Voltage Protection (OVP)						
V_{IN} over-voltage (OV) rising threshold	$V_{IN_OV_R}$		102	105	109	V
V_{IN} OV hysteresis	$V_{IN_OV_HYS}$			2		V
Enable (EN) Control						
EN UVLO rising threshold	$V_{EN_UVLO_R}$		1.15	1.2	1.25	V
EN UVLO hysteresis	$V_{EN_UVLO_HYS}$			200		mV
EN input current	I_{EN}	V_{EN} = 2V		0	1	µA
Feedback (FB)						
FB reference voltage	V_{REF}	T_J = 25°C	0.792	0.800	0.808	V
		T_J = -40°C to +125°C	0.788	0.800	0.812	V
Feedback current	I_{FB}	V_{FB} = 1.05V		-50		nA
FB under-voltage (UV) threshold	V_{FB_UV}		27%	30%	33%	V_{REF}
FB UV hysteresis	$V_{FB_UV_HYS}$			20%		V_{REF}
FB OV threshold	V_{FB_OV}		105%	108%	111%	V_{REF}
FB OV recovery hysteresis	$V_{FB_OV_HYS}$			3%		V_{REF}
Soft Start (SS)						
SS capacitor (C_{SS}) charge current	I_{SS}	V_{SS} = 0V	3	4	5	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Switching Frequency (f_{SW})						
Switching frequency	f_{SW}	Connect FREQ to AGND	90	100	115	kHz
		R_{FREQ} = 20kΩ	140	150	170	kHz
		R_{FREQ} = 45.3kΩ	185	200	225	kHz
		R_{FREQ} = 80.6kΩ	235	250	275	kHz
		R_{FREQ} = 124kΩ	275	300	325	kHz
		R_{FREQ} = 180kΩ	370	400	430	kHz
		R_{FREQ} = 243kΩ	550	600	650	kHz
		Connect FREQ to VCC	900	1000	1100	kHz
Min TG on time	$t_{TG_MIN_ON}$			60		ns
Min BG on time	$t_{BG_MIN_ON}$			180		ns
Max TG on time	$t_{TG_MAX_ON}$	V_{IN} - V_{OUT} < 3V		20		µs
		3V < V_{IN} - V_{OUT} < 6V		10		µs
Max duty cycle	D_{MAX}			99.0		%
Minimum f_{SW} in USM	f_{SW_USM}	Ultrasonic mode (USM)	20			kHz
Frequency Spread Spectrum (FSS)						
Maximum spread spectrum frequency	f_{SS_MAX}			110%		fsw
Minimum spread spectrum frequency	f_{SS_MIN}			90%		fsw
FSS modulation (8)	f_{SS_M}			1.5		kHz
Dead Time (DT)						
DT from TG falling to BG rising	$t_{DT_BG_R}$	Trigger point: 5V to 5V		35		ns
DT from BG falling to TG rising	$t_{DT\ BG_F}$	Trigger point: 5V to 5V		35		ns
Synchronization Input and Output (SYNCI/SYNCO)						
SYNCI external clock frequency range	f_{SYNCI}		80%		120%	fsw
SYNCI voltage rising threshold	V_{SYNC_R}		2			V
SYNCI voltage falling threshold	V_{SYNC_F}				0.8	V
Minimum SYNCI pulse width (8)	t_{SYNC_MIN}		50			ns
SYNCO output high logic	V_{SYNCO_H}	I_{SYNCO} = 1mA source	4.7			V
SYNCO output low logic	V_{SYNCO_L}	I_{SYNCO} = 1mA sink			0.3	V
SYNCO pulse duty cycle	D_{SYNCO}			50%		
Phase from PLL clock rising to SYNCO rising (8)	P_{DLY}	50% to 50%		180°		
BST Power						
BST to SW quiescent current, not switching	I_{BST_LKG}	V_{IN} = 48V, V_{FB} = 0.84V, V_{BST-SW} = 10V	16	21	27	µA
Mode Selection						
MODE voltage threshold	V_{PSM}	Pulse-skip mode (PSM) without USM			0.4	V
	V_{USM}	PSM with USM	1		1.6	V
	V_{FCCM}	Forced continuous conduction mode (FCCM)	2.5			V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
RAMP Selection						
RAMP source current	I_{RAMP}	V_{RAMP} = 0V	9	10	11	µA
RAMP voltage (V_{RAMP}) threshold	V_{RAMP1}	Ramp Scale = 1			0.27	V
	$V_{RAMP0.5}$	Ramp Scale = 0.5	0.34		0.65	V
	$V_{RAMP0.33}$	Ramp Scale = 0.33	0.75		1.43	V
	V_{RAMP2}	Ramp Scale = 2	1.56		2.03	V
	V_{RAMP4}	Ramp Scale = 4	2.2			V
f_{SW} Selection						
FREQ source current	I_{FREQ}	V_{FREQ} = 0V	9	10	11	µA
FREQ voltage (V_{FREQ}) threshold	V_{100kHz}	f_{SW} = 100kHz			0.08	V
	V_{150kHz}	f_{SW} = 150kHz	0.13		0.26	V
	V_{200kHz}	f_{SW} = 200kHz	0.35		0.55	V
	V_{250kHz}	f_{SW} = 250kHz	0.64		0.95	V
	V_{300kHz}	f_{SW} = 300kHz	1.05		1.44	V
	V_{400kHz}	f_{SW} = 400kHz	1.56		2.03	V
	V_{600kHz}	f_{SW} = 600kHz	2.16		2.7	V
	$V_{1000kHz}$	f_{SW} = 1000kHz	2.91			V
Current Limit Selection						
ILIM source current	I_{ILIM}	V_{ILIM} = 0V	9	10	11	µA
ILIM voltage (V_{ILIM}) threshold	V_{ILIM_5mV}	Valley current limit voltage = 25mV			0.27	V
	V_{ILIM_50mV}	Valley current limit voltage = 50mV	0.33		0.64	V
	V_{ILIM_75mV}	Valley current limit voltage = 75mV	0.76		1.7	V
	V_{ILIM_100mV}	Valley current limit voltage = 100mV	2.1			V
Power Good (PG)						
PG rising threshold	PG_{TH_R}	FB rising	92%	95%	98%	V_{REF}
		FB falling	102%	105%	108%	V_{REF}
PG falling threshold	PG_{TH_F}	FB falling	87%	90%	93%	V_{REF}
		FB rising	105%	108%	111%	V_{REF}
PG delay	t_{PG_DLY}	PG low to high		300		µs
		PG high to low		150		µs
PG sink current capability	V_{PG}	EN = 2V, sink 4mA			0.4	V
PG leakage current	I_{PG_LKG}	PG high state, V_{PG} = 5V			1.5	µA
Gate Drivers						
TG pull-up resistor	R_{TG_UP}	V_{BST-SW} = 10V, TG high state, I_{TG} = 100mA		1.2		Ω
TG pull-down resistor	R_{TG_DN}	V_{BST-SW} = 10V, TG low state, I_{TG} = -100mA		0.7		Ω
BG pull-up resistor	R_{BG_UP}	V_{DRV} = 10V, BG high state, I_{BG} = 100mA		1.2		Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameters	Symbol	Conditions	Min	Typ	Max	Units
BG pull-down resistor	R_{BG_DN}	V_{DRV} = 10V, BG low state, I_{BG} = -100mA		0.7		Ω
TG, BG source current (7)	I_{OH}	V_{BST-SW} = 10V, V_{DRV} = 10V, TG = SW, BG = PGND		4.2		A
TG, BG sink current (7)	I_{OL}	V_{BST-SW} = 10V, V_{DRV} = 10V, TG = BST, BG = VDRV		5.2		A
Over-Current Protection (OCP)						
Valley current limit voltage	V_{VCL}	ILIM connected to AGND	15	25	35	mV
		R_{ILIM} = 51kΩ	40	50	60	mV
		R_{ILIM} = 120kΩ	65	75	85	mV
		ILIM connected to VCC	90	100	110	mV
Negative Current Limit						
Negative current limit voltage	V_{NCL}	ILIM connected to AGND	17	25	33	mV
		R_{ILIM} = 51kΩ	17	25	33	mV
		R_{ILIM} = 120kΩ	40	50	60	mV
		ILIM connected to VCC	40	50	60	mV
Zero-Current Detection (ZCD)						
ZCD detection voltage	V_{ZCD}		-2	1	+5	mV
Current Temperature Coefficient						
Current temperature coefficient (8)	TC	On resistance ($R_{DS(ON)}$) mode		4500		ppm/°C
		Sense resistor (R_{SENSE}) mode		0		ppm/°C
Thermal Protection						
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{SD_HYS}			20		°C

Notes:

6) Not tested in production; guaranteed by over-temperature (OT) correlation.
7) Not tested in production; derived by design.
8) Not tested in production; derived by sample characterization.

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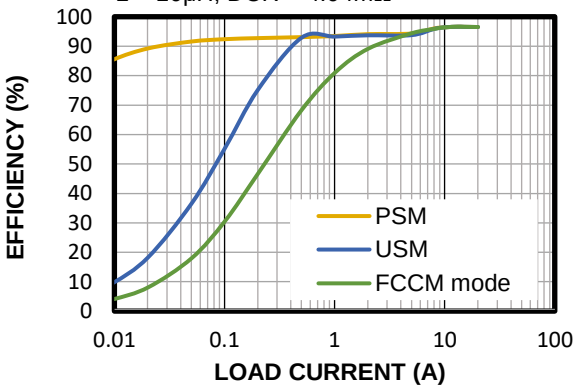
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TYPICAL CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, EN = 2V, PSM, T_A = 25°C, unless otherwise noted.

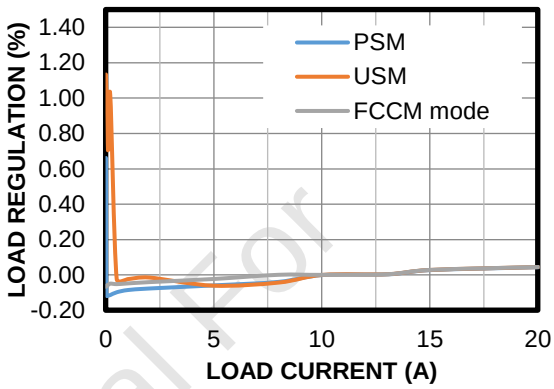
Efficiency vs. Load Current

L = 10µH, DCR = 4.04mΩ



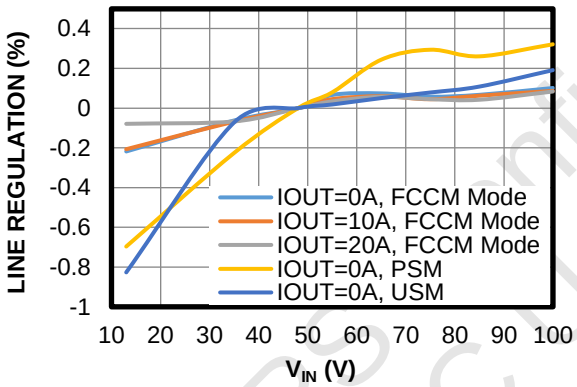
Load Regulation

L = 10µH

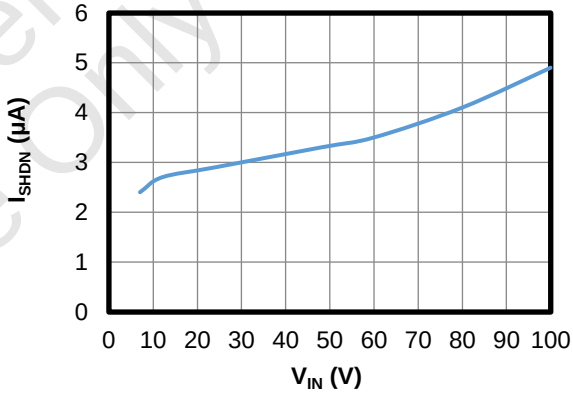


Line Regulation

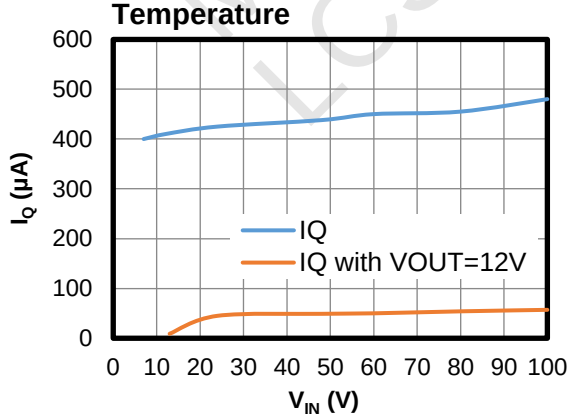
L = 10µH



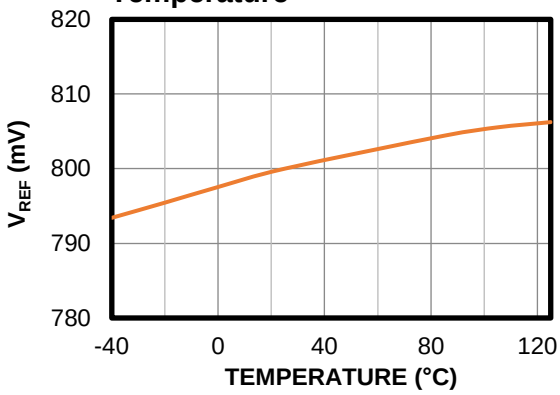
Shutdown Current vs. Temperature



Quiescent Supply Current vs. Temperature



Reference Voltage vs. Temperature



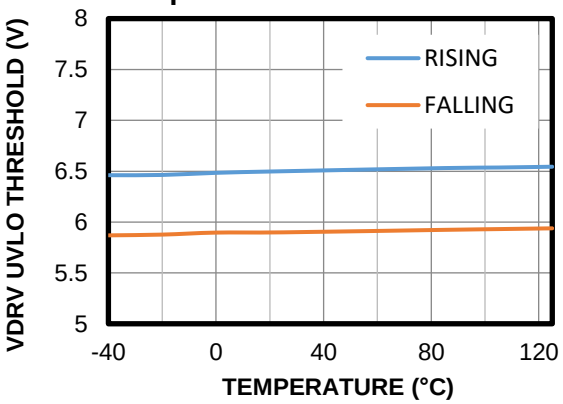
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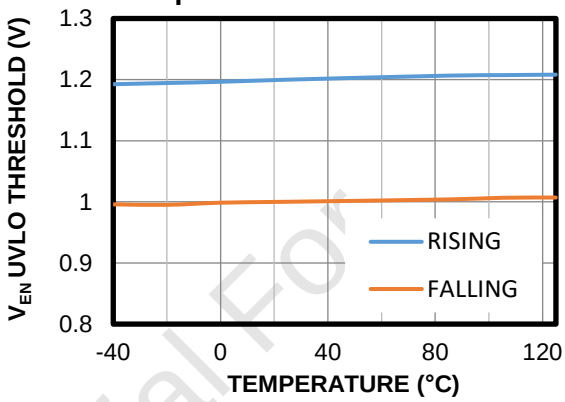
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, EN = 2V, PSM, T_A = 25°C, unless otherwise noted.

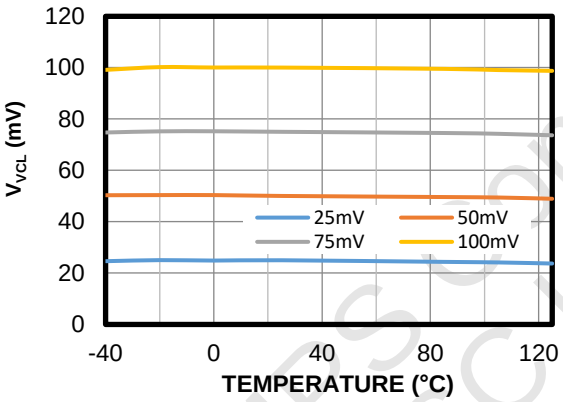
VDRV UVLO Threshold vs. Temperature



EN UVLO Threshold vs. Temperature



Valley Current Limit Voltage vs. Temperature



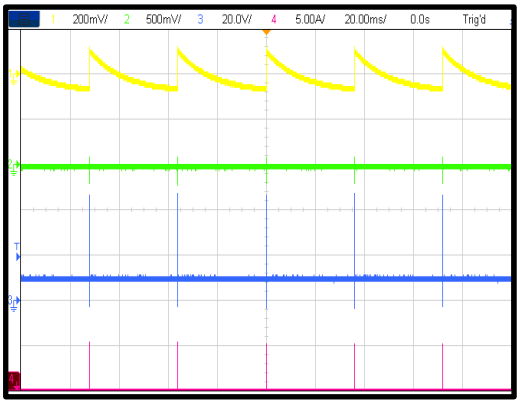
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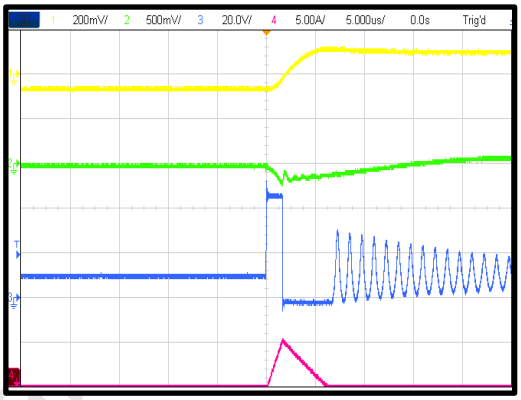
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, PSM, T_A = 25°C, unless otherwise noted.

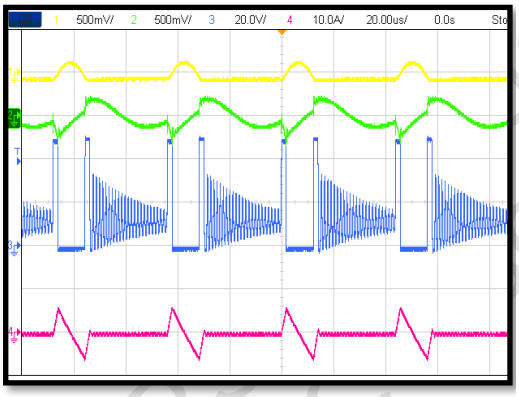
Steady State
I_{OUT} = 0A, PSM



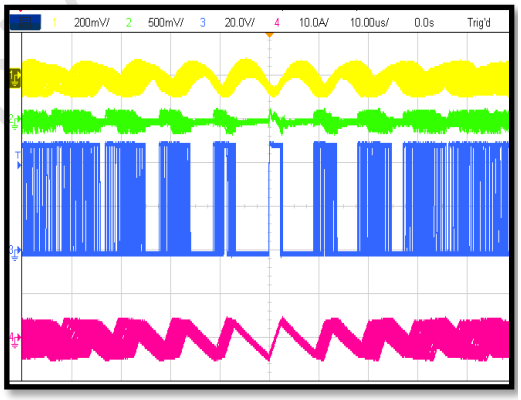
Steady State
I_{OUT} = 0A, PSM



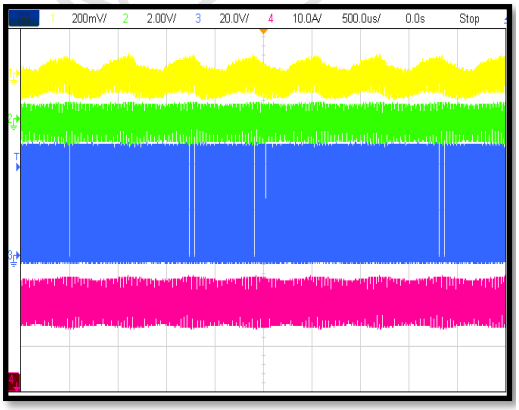
Steady State
I_{OUT} = 0A, USM



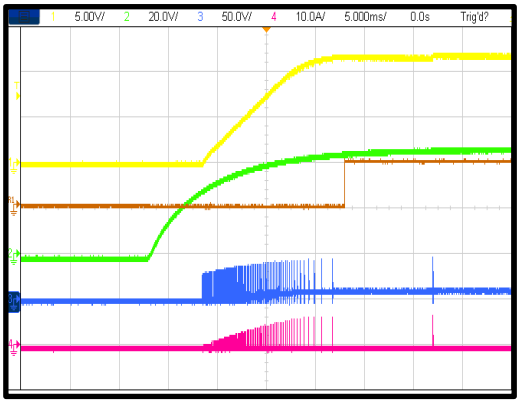
Steady State
I_{OUT} = 0A, FCCM



Steady State
I_{OUT} = 20A



Start-Up through VIN
I_{OUT} = 0A, PSM



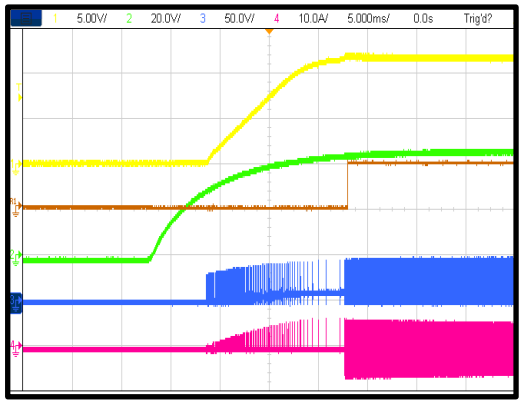
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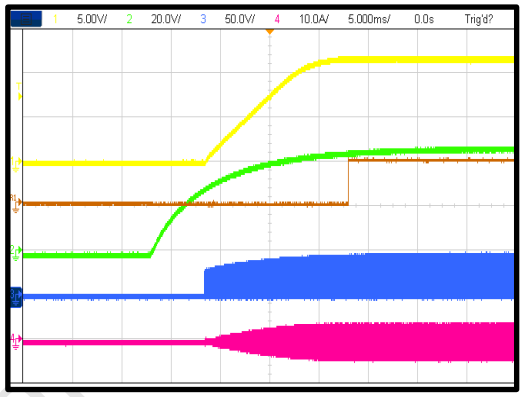
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, PSM, T_A = 25°C, unless otherwise noted.

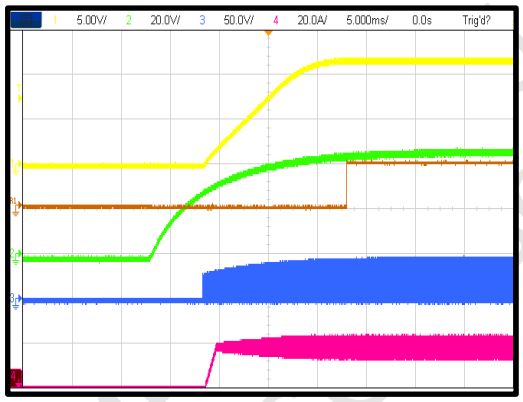
Start-Up through VIN
I_{OUT} = 0A, USM



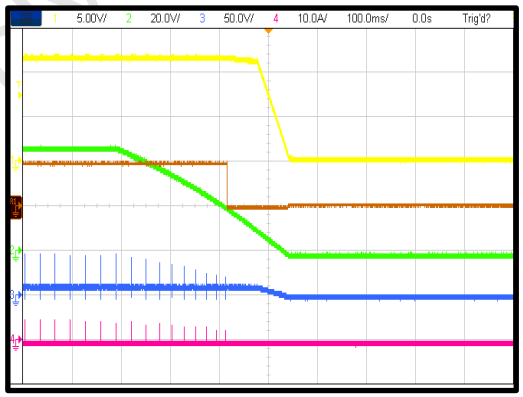
Start-Up through VIN
I_{OUT} = 0A, FCCM



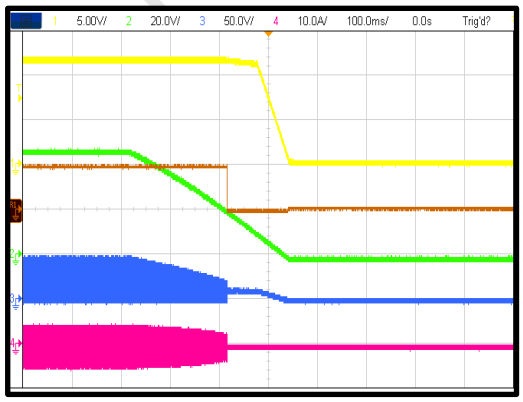
Start-Up through VIN
I_{OUT} = 20A



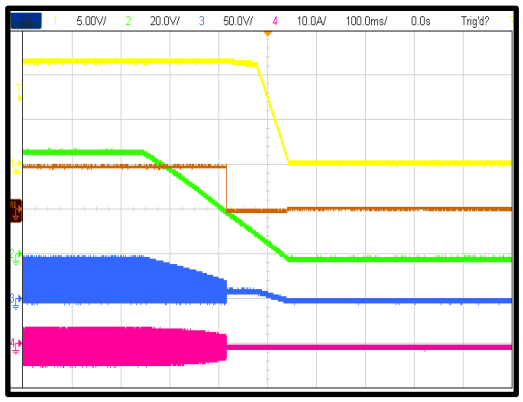
Shutdown through VIN
I_{OUT} = 0A, PSM



Shutdown through VIN
I_{OUT} = 0A, USM



Shutdown through VIN
I_{OUT} = 0A, FCCM



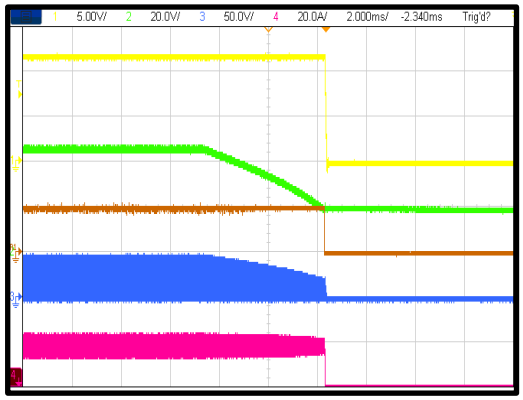
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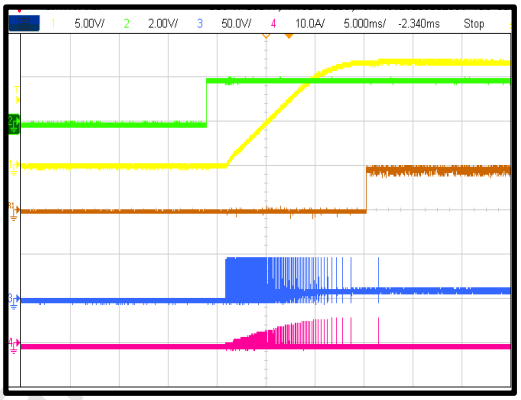
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, PSM, T_A = 25°C, unless otherwise noted.

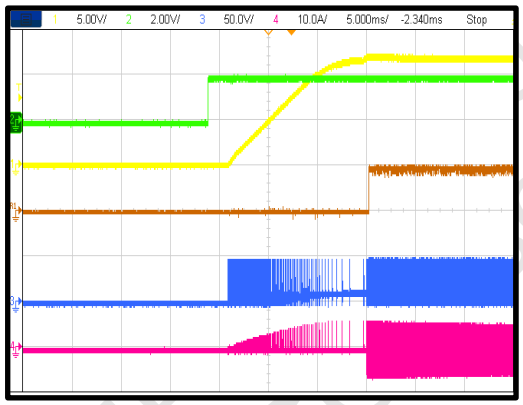
Shutdown through VIN
I_{OUT} = 20A



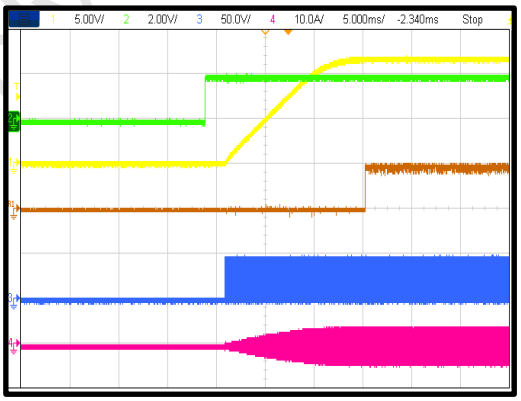
Start-Up through EN
I_{OUT} = 0A, PSM



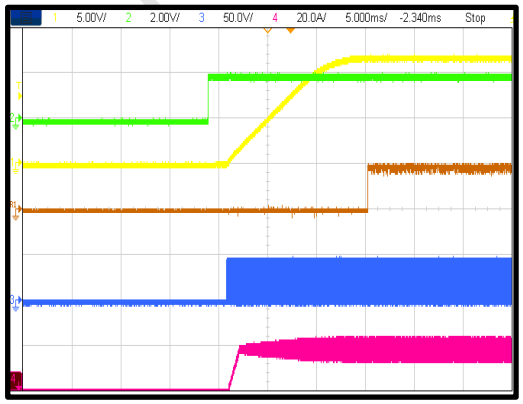
Start-Up through EN
I_{OUT} = 0A, USM



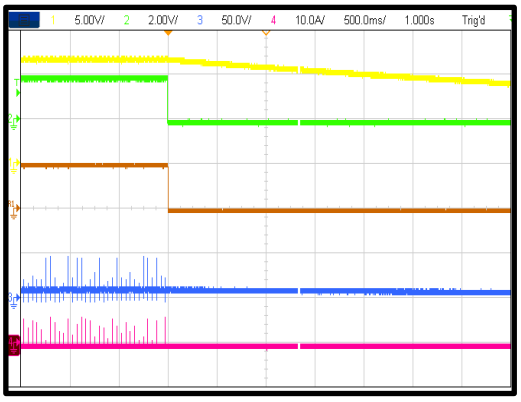
Start-Up through EN
I_{OUT} = 0A, FCCM



Start-Up through EN
I_{OUT} = 20A



Shutdown through EN
I_{OUT} = 0A, PSM



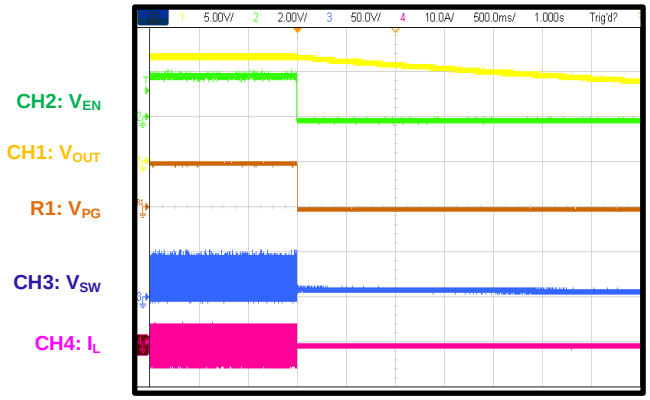
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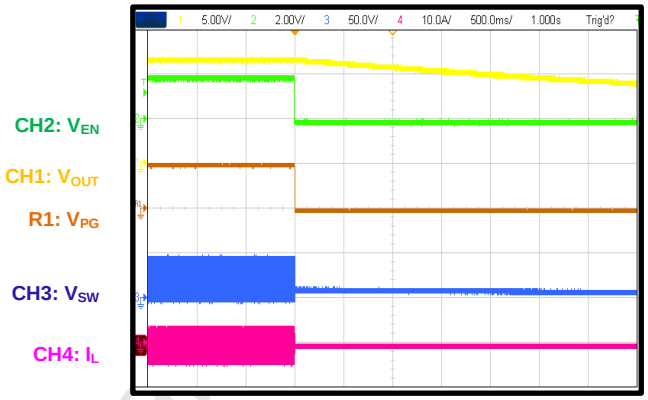
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, PSM, T_A = 25°C, unless otherwise noted.

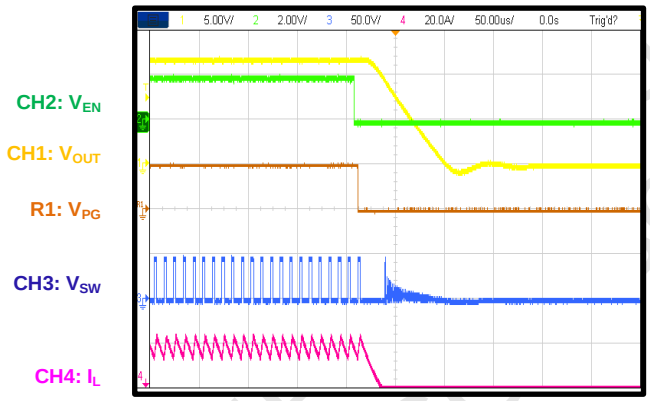
Shutdown through EN
I_{OUT} = 0A, USM



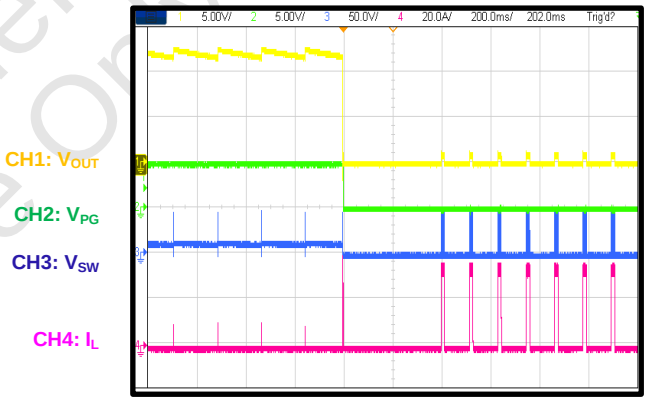
Shutdown through EN
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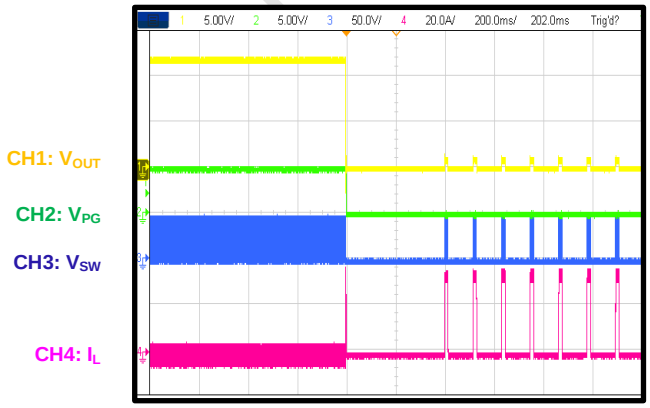
Shutdown through EN
I_{OUT} = 20A



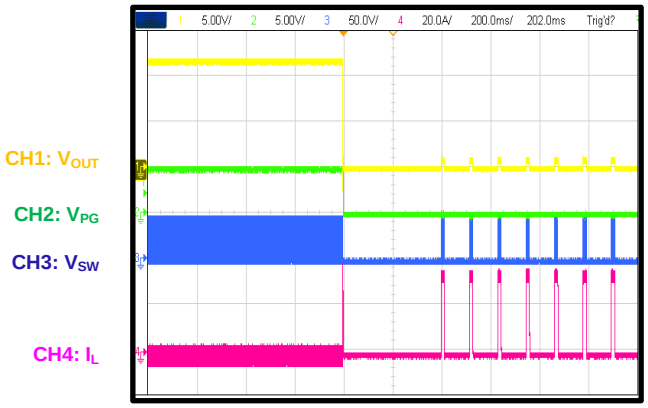
SCP Entry
I_{OUT} = 0A, PSM



SCP Entry
I_{OUT} = 0A, USM



SCP Entry
I_{OUT} = 0A, FCCM



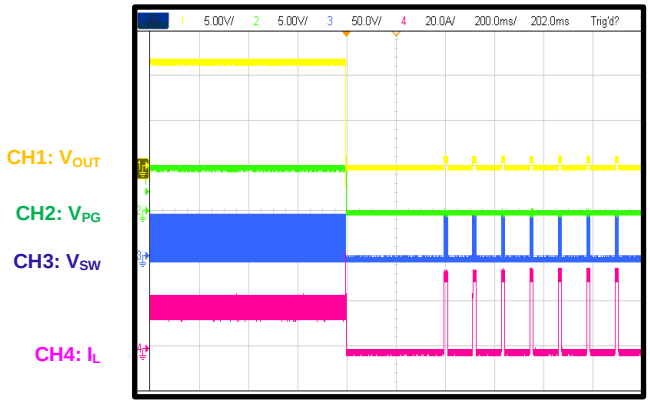
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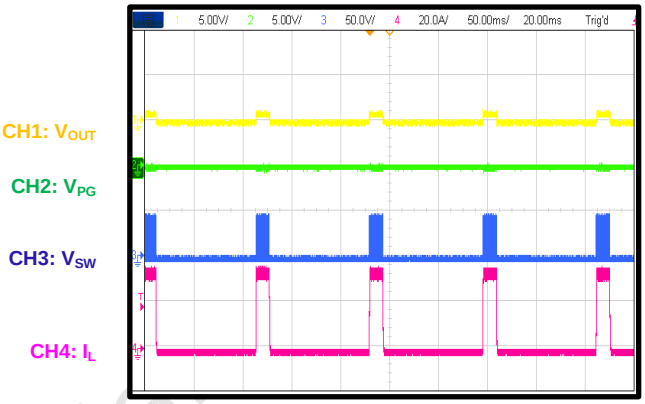
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, PSM, T_A = 25°C, unless otherwise noted.

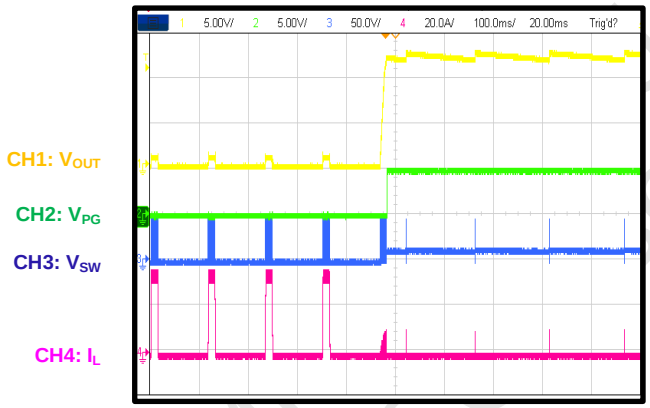
SCP Entry
I_{OUT} = 20A



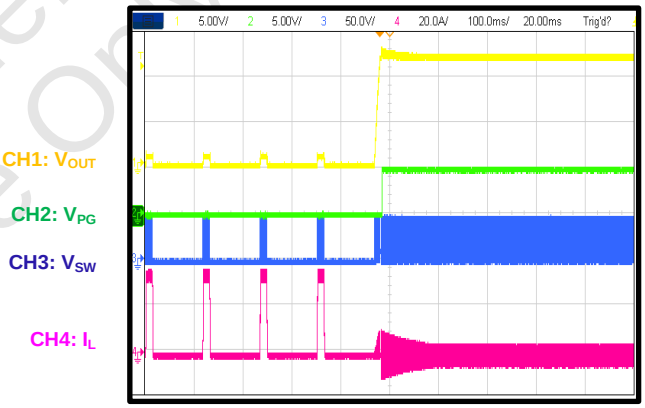
SCP Steady State
V_{OUT} short to PGND



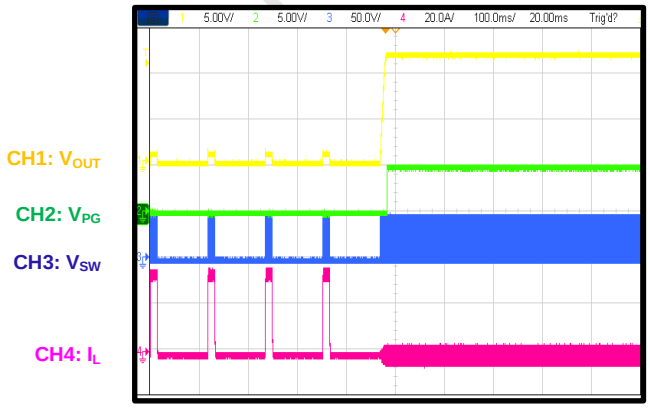
SCP Recovery
I_{OUT} = 0A, PSM



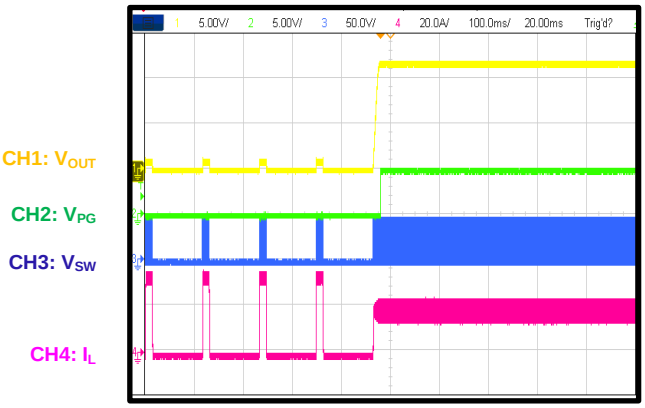
SCP Recovery
I_{OUT} = 0A, USM



SCP Recovery
I_{OUT} = 0A, FCCM



SCP Recovery
I_{OUT} = 20A



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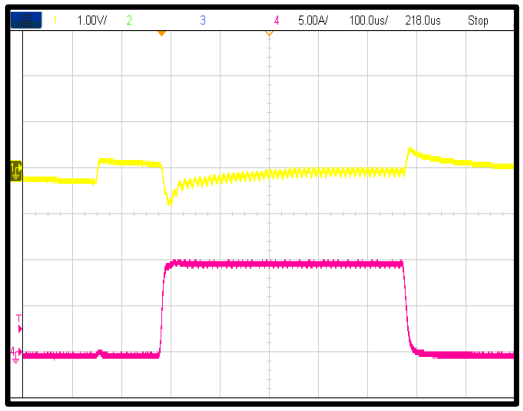
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, L = 10µH, PSM, T_A = 25°C, unless otherwise noted.

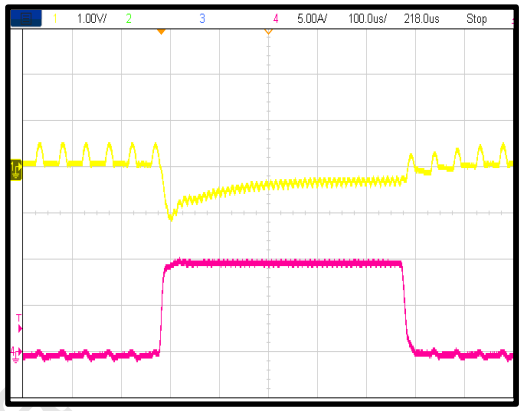
Load Transient Response

I_{OUT} = 0A to 10A, PSM, slew rate = 1A/µs



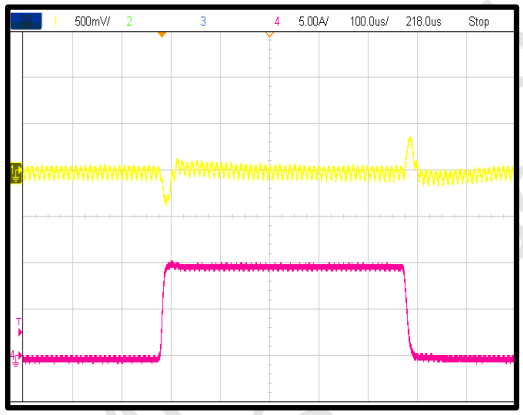
Load Transient Response

I_{OUT} = 0A to 10A, USM, slew rate = 1A/µs



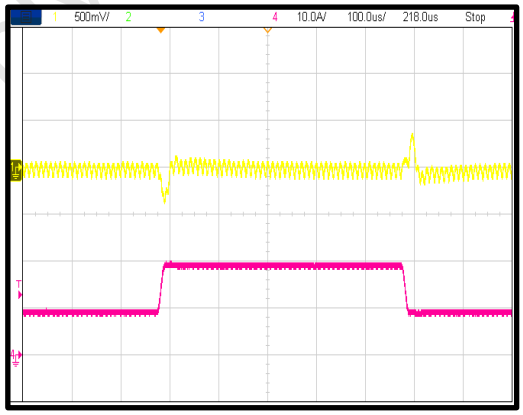
Load Transient Response

I_{OUT} = 0A to 10A, FCCM, slew rate = 1A/µs



Load Transient Response

I_{OUT} = 10A to 20A, slew rate = 1A/µs



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FUNCTIONAL BLOCK DIAGRAM

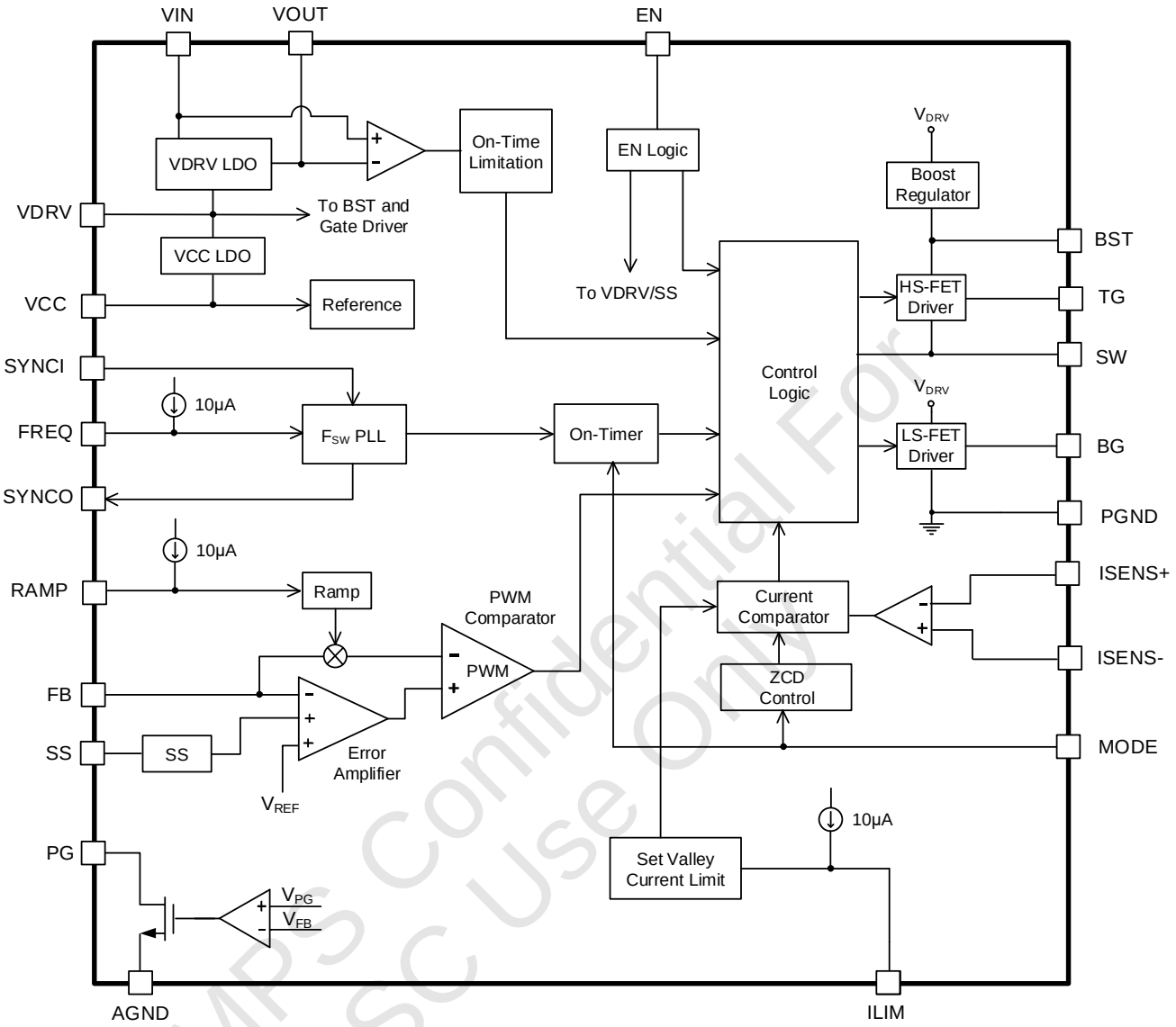


Figure 1: Functional Block Diagram

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OPERATION

Overview

The MP9931F is a high-performance, step-down, synchronous converter controller IC with a wide input voltage (V_{IN}) range. It implements constant-on-time (COT) control mode and a configurable switching frequency (f_{SW}) control architecture to regulate the output voltage (V_{OUT}) with external N-channel MOSFET switches.

Adaptive COT control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides excellent load and line regulation.

Under normal load conditions, the controller operates in full pulse-width modulation (PWM) mode. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates that there is an insufficient V_{OUT}. The on time (t_{ON}) is determined by V_{OUT} and V_{IN} to make f_{SW} fairly constant across the V_{IN} range.

Internal compensation is applied to COT control for stable operation, even when ceramic capacitors are used as the output capacitors. Internal compensation improves the jitter performance without affecting line or load regulation.

Heavy-Load Operation

When the output current (I_{OUT}) is high and the inductor current (I_L) is always above 0A, this is called continuous conduction mode (CCM). Figure 2 shows CCM.

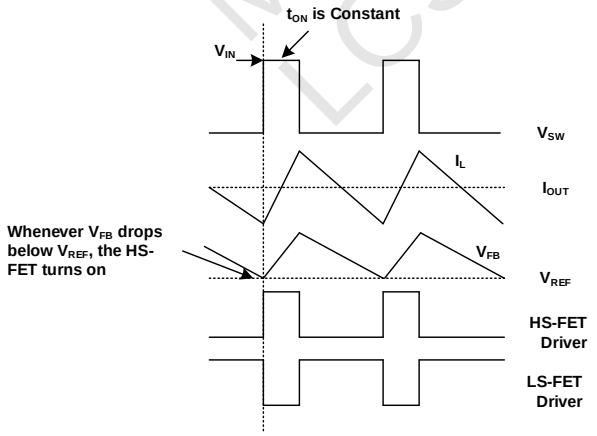


Figure 2: Heavy-Load Operation

When V_{FB} is below V_{REF}, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the low-side MOSFET (LS-FET) turns on until the next period.

There is a dead short between the input and PGND if both the HS-FET and LS-FET are on at the same time. This is called shoot-through. To prevent shoot-through, a dead time (DT) is generated internally between the HS-FET off time and LS-FET on time, and vice versa.

In CCM, f_{SW} is fairly constant; this is also called PWM mode.

In light-load conditions, the MP9931F can be set to different modes, which are described in detail below.

Operation Modes

The MP9931F works with a fixed frequency under heavy-load conditions. When load current decreases, the MP9931F can work in forced CCM (FCCM), pulse skip mode (PSM), or ultrasonic mode (USM) based on the MODE pin setting (see Table 1). The operation mode can also be changed online.

Table 1: MODE Setting

MODE Pin	Light-Load Mode
AGND	PSM without USM
Floating	PSM with USM
VCC	FCCM

Pulse-Skip Mode (PSM)

As the load decreases, I_L also decreases. If I_L reaches 0A, the device transitions from CCM to discontinuous conduction mode (DCM). Figure 3 shows light-load operation.

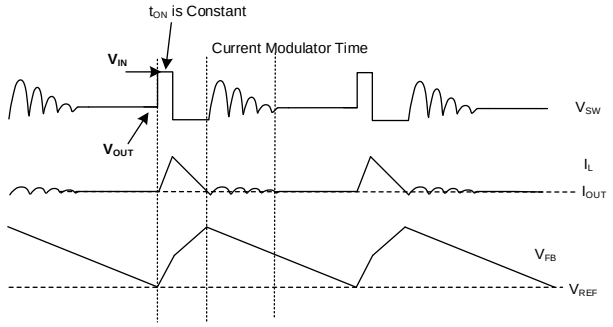


Figure 3: Light Load Operation

When V_{FB} is below V_{REF}, HS-FET turns on for a fixed interval. When the HS-FET turns off, the

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LS-FET turns on until I_L reaches 0A. In DCM, V_{FB} does not reach V_{REF} while I_L approaches 0A. Both the BG and TG pins pull low whenever I_L reaches 0A. Under light-load or no-load conditions, the output drops very slowly and the MP9931F reduces f_{SW} naturally. This greatly improves efficiency under light-load conditions. At light loads, the HS-FET does not turn on as frequently as it does under heavy-load conditions. This is also called PSM.As I_{OUT} increases from a light-load condition, the time period within which the current modulator regulates becomes shorter. In this scenario, the HS-FET turns on more frequently, which increases f_{SW} correspondingly. I_{OUT} reaches the critical level ($I_{OUT_CRITICAL}$) when the current modulator time is zero. $I_{OUT_CRITICAL}$ can be calculated with Equation (1):

$$I_{OUT_CRITICAL} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

Ince I_{OUT} exceeds the critical level, the device runs in CCM. After that, f_{SW} is fairly constant across the I_{OUT} range.

Forced Continuous Conduction Mode (FCCM)

If the load is light while the MP9931F operates in FCCM, the LS-FET does not turn off when I_L reaches the zero-current detection (ZCD) threshold. I_L goes negative flowing from VOUT to PGND when LS-FET is on. This forces I_L to work in CCM with a fixed frequency, producing a lower V_{OUT} ripple than in PSM.

Figure 4 shows FCCM. The HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the next period.

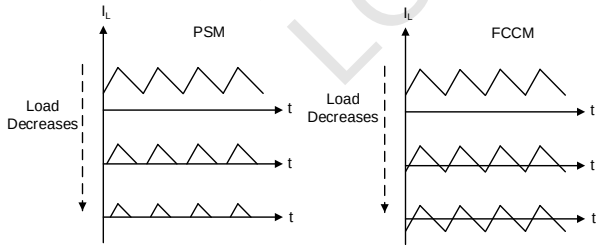


Figure 4: PSM and FCCM

Ultrasonic Mode (USM)

USM keeps f_{SW} above audible frequency areas under light-load conditions. Once the device goes into a light load, t_{ON} shrinks and the ZCD threshold drops to prevent f_{SW} from falling below 20kHz.

Low-Dropout (LDO) Mode

Low-dropout (LDO) mode is designed to improve dropout when V_{IN} is close to V_{OUT} by further increasing the HS-FET's t_{ON} after the minimum off time (t_{OFF}) is reached. In LDO mode, the MP9931F is designed to operate in t_{ON} extended mode, as long as the voltage across the BST and SW pins (V_{BST-SW}) exceeds the BST under-voltage lockout (UVLO) threshold (V_{BST_UVLO}).

If V_{BST-SW} drops below V_{BST_UVLO}, the BST UVLO circuit turns off the HS-FET. After the BST capacitor (C_{BST}) voltage is recharged to exceed V_{BST_UVLO}, the HS-FET turns on again to regulate V_{OUT}. Since the BST regulation voltage exceeds V_{BST_UVLO}, the HS-FET can remain on for a long time without needing to refresh C_{BST}, which increases the effective duty cycle of the switching regulator.

LDO mode makes the MP9931F suitable for applications where V_{IN} is close to V_{OUT}. The maximum extended t_{ON} is limited by V_{IN} - V_{OUT}. When 3V < V_{IN} - V_{OUT} < 6V, the maximum extended t_{ON} is 10µs. When V_{IN} - V_{OUT} < 3V, the maximum extended t_{ON} is 20µs. When the SS pin is pulled up to VCC, LDO mode is disabled.

Frequency Spread Spectrum (FSS)

To improve EMI performance, the MP9931F integrates a frequency spread spectrum (FSS) circuit. ±10% of f_{SW} variation is added to the fundamental f_{SW} set by the FREQ pin. It is modulated at a 1.5kHz frequency.

Constant Current (CC) Mode

The MP9931F provides constant current (CC) mode for battery charging. Pull the SS pin up to VCC via a 10kΩ resistor to enable CC mode. In this scenario, output under-voltage (UV) protection and LDO mode are disabled. In addition, connect FB to AGND via a resistor or divide FB from VCC to set V_{FB} below 0.8V. V_{OUT} finally charges up to (V_{IN} x max duty cycle) under this condition. Figure 5 on page 22 shows the typical connections for SS and FB in CC mode.

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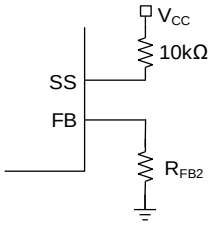


Figure 5: CC Mode

In some CC applications, the maximum V_{OUT} and I_{OUT} must be limited, so set the maximum V_{OUT} with FB resistor dividers.

Figure 6 shows the typical connection for SS and FB for CC + constant voltage (CV) mode applications.

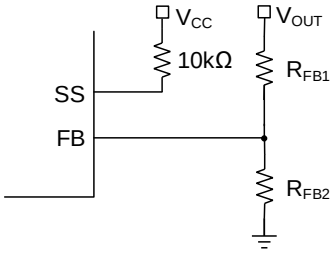


Figure 6: CC + CV Mode

The average CC current (I_{CC}) is set by the valley current limit and inductor current ripple. I_{CC} can be estimated with Equation (2):

$$I_{CC} = \frac{V_{VCL}}{R_S} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

It is recommended to use shunt resistor current-sensing for CC mode to achieve better accuracy across the full temperature range.

Synchronization

The MP9931F's frequency (internal oscillator set via the FREQ pin) can be synchronized to an external clock with a range that is ±20% of the configured f_{SW} through the SYNCI pin. When adding one clock signal to the SYNCI pin, the internal clock's rising edge is synchronized to the external clock's rising edge.

Floating Driver and Bootstrap Charging

The floating top gate driver is powered by an external bootstrap (BST) capacitor (C_{BST}), which is typically refreshed when the HS-FET turns off. This floating driver has its own UVLO protection.

VDRV Power Supply and VCC Regulator

Both the HS-FET and LS-FET drivers are powered from the DRV voltage (V_{DRV}). Typically, a 4.7µF ceramic capacitor is required at the VDRV pin to prevent large voltage spikes.

An internal LDO linear regulator supplies VCC power from V_{DRV}. Most of the internal logic circuits are powered from the VCC regulator. It is recommended to place a 2.2µF ceramic capacitor from VCC to AGND. V_{IN}, V_{DRV}, and the VCC voltage (V_{CC}) have their own UVLO circuits to protect the chip from operating at an insufficient supply voltage.

When V_{IN} power is supplied and EN is high, the MP9931F regulates V_{DRV} from V_{IN} first. If V_{OUT} > 8.4V, the device slowly scales down V_{DRV} and makes it approximately equal to V_{OUT}. Then disable the first LDO (LDO1, V_{IN} to V_{DRV}) and enable the second LDO (LDO2, V_{OUT} to V_{DRV}) (see Figure 7). When V_{OUT} falls below 7.4V, the source to V_{DRV} changes back to V_{IN}, and V_{DRV} scales accordingly.

If 8.4V < V_{OUT} < 10V, the V_{DRV} LDO2 is in LDO mode, and V_{DRV} is almost equal to V_{OUT}. When V_{OUT} exceeds 10V, V_{DRV} is regulated to 10V so that that MP9931F can obtain a higher efficiency for internal driver loss.

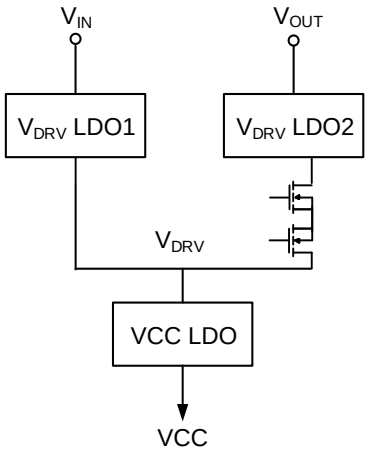


Figure 7: Internal LDO Structure

V_{DRV} can also be powered from the external voltage source. If the external bias voltage exceeds the internal V_{DRV}, this can reduce power loss. The recommended power-on sequence for external V_{DRV} bias is V_{IN} on, V_{DRV} on, then EN on.

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Enable (EN) and Configurable UVLO

The EN pin enables and disables the MP9931F. When applying a voltage below 0.4V, the device is in shutdown mode. After the voltage rises to the EN high threshold (typically 1.2V), the device is enabled and starts switching operation. Switching operation is disabled when the EN voltage falls below its falling threshold.

Tie EN to VIN through a resistor divider (R_{EN_UP} and R_{EN_DOWN}) to configure the V_{IN} start-up threshold (see Figure 8).

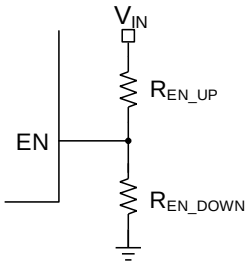


Figure 8: EN Resistor Dividers

The EN pin can be directly connected to VIN via a pull-up resistor, which limits the EN input current below 100μA and prevents damage to the internal EN circuit.

For example, when connecting 100V to VIN, the pull-up resistor should exceed 935kΩ. R_{PULL_UP} can be calculated with Equation (3):

$$R_{PULL_UP} \geq (100V - 6.5V) / 100\mu A = 935k\Omega \quad (3)$$

Switching Frequency (f_{SW})

f_{SW} selection is a tradeoff between efficiency and component size. Low-frequency operation increases efficiency by reducing MOSFET switching loss, but this requires larger inductance and capacitance to maintain a low output voltage ripple. f_{SW} can be set by the resistor (R_{FREQ}) connected to FREQ and AGND (see Table 2).

Table 2: Switching Frequency Selection

FREQ Pin	f_{SW}
0Ω	100kHz
20kΩ to AGND	150kHz
45.3kΩ to AGND	200kHz
80.6kΩ to AGND	250kHz
124kΩ to AGND	300kHz
180kΩ to AGND	400kHz
243kΩ to AGND	600kHz
VCC	1MHz

When EN is high and V_{CC} exceeds its UVLO threshold, the MP9931F starts to work by sourcing a current pulse to the FREQ pin to detect the FREQ setting. This detection sets f_{SW} and latches the setting after the device starts up.

Current Sense (CS)

The MP9931F implements a lossless current-sense (CS) scheme designed to limit the I_L during an overload or short-circuit (SC) condition. Figure 9 shows the CS method using the LS-FET's on-state resistance.

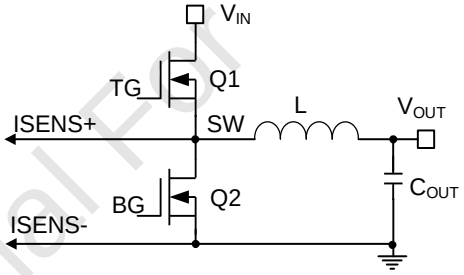


Figure 9: MOSFET $R_{DS(ON)}$ Current-Sensing

Figure 10 shows an alternative implementation with a current-shunt resistor (R_S). The MP9931F senses I_L during the PWM off time.

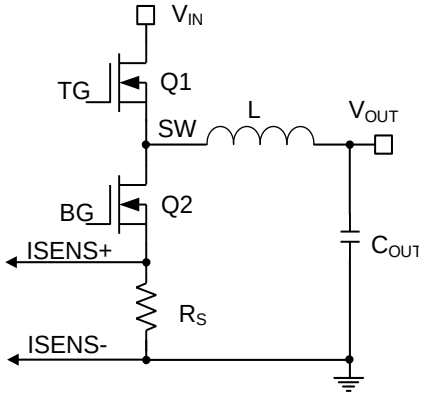


Figure 10: Shunt Resistor Current-Sensing

The MP9931F has four fixed options for the current limit setting (see Table 3 on page 24).

When using lossless current-sensing, the MP9931F monitors I_L by the LS-FET's on-state resistance. The current limit can be estimated with Equation (4):

$$I_{LIM} = \frac{V_{VCL}}{R_{DS(ON)}} \quad (4)$$

When using shunt resistor current-sensing, R_S monitors I_L. Its value is chosen based on the current-limit threshold. The relationship between

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the inductor valley current (I_{ILIM}) and R_S can be calculated with Equation (5):

$$I_{LIM} = \frac{V_{VCL}}{R_S} \quad (5)$$

The typical value for R_S is between 2mΩ and 10mΩ.

The MP9931F detects the appropriate mode at start-up and sets the temperature coefficient (T_C) accordingly. The device provide a T_C of +4500ppm/°C to generally track the LS-FET's $R_{DS(ON)}$ temperature variation. Conversely, the MP9931F has no T_C in R_{SENSE} mode. This controls the I_L valley during a steady state overload at the output.

Valley Current Limit and Negative Current Limit Setting

The ILIM pin sources a reference current that flows to the external resistor (R_{ILIM}) to configure the current limit sense voltage. Connect the ILIM pin to AGND through R_{ILIM} to configure the current limit sense voltage between the ISENS+ and ISENS- pins (see Table 3).

Table 3: Valley Current Limit Threshold

ILIM Pin	Valley Current Limit Voltage	Negative Current Limit Voltage
AGND	25mV	25mV
51kΩ to AGND	50mV	25mV
120kΩ to AGND	75mV	50mV
VCC	100mV	50mV

If the voltage difference between ISENS+ and ISENS- exceeds the valley current limit threshold, TG cannot be pulled high.

If the ILIM pin detects a negative current below its limit threshold, the device turns off the LS-FET to limit the negative current.

Over-Current Protection (OCP)

The MP9931F features hiccup mode, cycle-by-cycle, over-current (OC) limit control. The device limits the voltage between the ISENS+ and ISENS- pins for the valley current. PWM is not allowed to initiate a new cycle before I_L falls to the valley threshold.

If a cycle-by-cycle OC condition occurs, V_{OUT} drops until V_{FB} falls below the under-voltage (UV) threshold (typically 30% of V_{REF}). Once a UV condition is triggered, the MP9931F enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground.

The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. Once the OC condition is removed, the MP9931F exits hiccup mode.

RAMP Setting

The RAMP pin can be used to select the ramp scale. Connect a resistor (R_{RAMP}) to AGND to set the ramp scale. Table 4 shows the relationship between the ramp scale and the internal R value for the ramp calculation.

Table 4: RAMP Scale vs. Internal R

RAMP Pin	Ramp Scale	R (kΩ)
AGND	1	2077
51kΩ to AGND	0.5	4077
120kΩ to AGND	0.33	6077
180kΩ to AGND	2	1077
VCC	4	577

The ramp can be estimated with Equation (6):

$$RAMP(mV) = K_{DIV} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times R(k\Omega)} \quad (6)$$

K_{DIV} is fixed to 0.44×10^4.

Where K_{DIV} is fixed to 0.44×10^4. For example, to select ramp scale = 1 for a 48V input and 12V output, Ramp should be about 21mV.

A larger ramp improves stability but results in worse transient performance.

Power Good (PG) Function

The MP9931F includes an open-drain power good (PG) output that indicates whether the regulator's V_{OUT} is within its nominal range. When V_{OUT} is out of this range, the PG output is pulled low. PG should be pulled up to a voltage source through a resistor (R_{PG}, e.g. 100kΩ).

The PG pin has self-driving capability. If the MP9931F is off and the PG pin is pulled up to another DC power source through a resistor, the PG pin can also be pulled low via a self-driving circuit.

Figure 11 on page 25 shows the relationship between the PG-clamped voltage and the pull-up current

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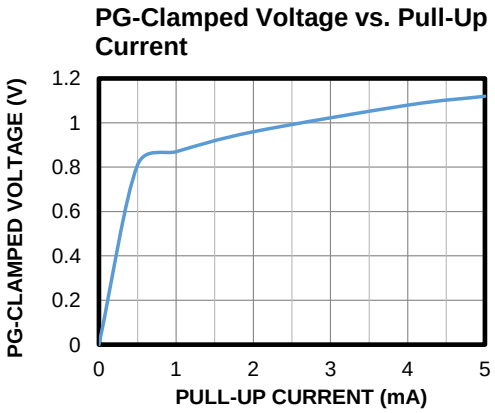


Figure 11: PG-Clamped Voltage vs. Pull-Up Current

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up. When the chip starts, the internal circuitry generates an SS voltage (V_{SS}) that ramps up from 0V to V_{CC}. When V_{SS} is below the internal V_{REF}, V_{SS} overrides V_{REF}, so the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} is used as the reference.

An external capacitor (C_{SS}) connected from SS to AGND is charged by an internal current source, producing a ramped voltage. The soft-start time (t_{SS}) is set by C_{SS}, and can be calculated with Equation (7):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \times 1.3 \quad (7)$$

Where C_{SS} is the value of external SS capacitor, V_{REF} is the internal reference voltage, and I_{SS} is the SS charge current.

Typically, I_{SS} is 4μA. SS is reset if a protection occurs, except for output and input OVP.

If C_{SS} = 47nF, t_{SS} is about 12.2ms.

Pre-Biased Start-Up

The MP9931F is designed for monotonic start-up into pre-biased loads. If V_{OUT} is pre-biased to a certain voltage during start-up, the MP9931F does not switch until V_{SS} ramps up to the value referenced to the V_{OUT} bias voltage. The BST voltage (V_{BST}) refreshes under this condition.

Input Over-Voltage Protection (V_{IN} OVP)

The MP9931F monitors the VIN pin to detect an input over-voltage (OV) event.

If the device is configured for CCM, V_{IN} OVP is triggered, the device changes to pulse-frequency modulation (PFM) mode. Once V_{IN} drops below the V_{IN} OVP falling threshold, the part recovers and resumes CCM switching again.

Output Over-Voltage Protection (OVP)

V_{OUT} is monitored by V_{FB}. If V_{FB} reaches 108% of the reference, this triggers OVP. Once OVP is triggered, the MP9931F stops switching. Once V_{OUT} drops to 105% of the regulation voltage, the device recovers to normal loop control.

Over-Temperature Protection (OTP)

The MP9931F provides over-temperature protection (OTP) by monitoring the IC temperature internally. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature (T_J) exceeds the OTP rising threshold, the whole chip shuts down. This is a non-latch protection. Once T_J drops below the OTP falling threshold, the device resumes normal operation by initiating SS.

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APPLICATION INFORMATION

Setting the Output Voltage

Figure 12 shows how to set V_{OUT} with the external resistor divider.

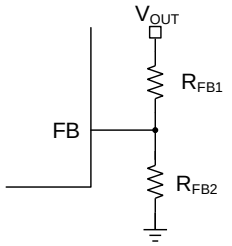


Figure 12: V_{OUT} Setting Resistor

If R_{FB1} is determined, then R_{FB2} can be estimated with Equation (8):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (8)$$

Table 5 shows the resistor options for common output voltages.

Table 5: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
12	160 (1%)	11.5 (1%)
33	324 (1%)	8.06 (1%)

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. Use ceramic capacitors for the best performance. Place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R dielectrics are recommended due to their stable temperature characteristics and low ESR.

The input capacitors should have a ripple current rating that exceeds the converter's maximum input ripple current (I_{CIN_MAX}). The input ripple current (I_{CIN}) can be calculated with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating that exceeds half the maximum load current (I_{LOAD_MAX}).

C_{IN} determines the converter's V_{IN} ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, select C_{IN} to meet the system's specifications.

ΔV_{IN} can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (13)$$

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW}. The capacitance also dominates ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

When using POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (15)$$

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching V_{IN}. A larger-value inductor results in less ripple current and a lower ΔV_{OUT}; however, a larger-value inductor also has a larger physical size, a higher series resistance, and a lower saturation

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It is recommended to choose an inductor so that the peak-to-peak inductor ripple current (ΔI_L) is 20% to 50% of the maximum output current (I_{OUT_MAX}). The peak inductor current (I_{L_PEAK}) should be below the saturation current. The inductance (L) can be estimated with Equation (16):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

Choose an inductor that will not saturate under the maximum I_{L_PEAK}. I_{L_PEAK} can be calculated with Equation (17):

$$I_{L_PEAK} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (17)$$

Design Example

Table 6 shows a design example with specifications following the application guidelines :

Table 6: Design Example

V_{IN}	48V
V_{OUT}	12V
I_{OUT}	0A to 20A

Figure 14 on page 29 shows the detailed application schematic for V_{OUT} = 12V. This application is the basis for the typical performance waveforms. For more detailed device applications, refer to the related evaluation board datasheet(s).

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PCB Layout Guidelines

For a controller, layout is an important design step. Poor layout can result in reduced performance, EMI problems, resistive loss, and even system instability. For the best results, refer to Figure 13 and follow the steps below:

1. Keep the input power loop between the input capacitor (C_{IN}), HS-FET, and LS-FET as small as possible.
2. Make the SW trace as short and wide as possible.
3. Place one small decoupling capacitor (C_{VDRV}) close to the IC's VDRV pin and PGND pin.
4. Route the feedback (FB) loop far away from noisy sources, such as the SW trace.
5. Place the feedback resistor divider as close as possible to the FB pin.
6. Place the VCC capacitors as close as possible to the VCC pin.
7. Use a short, wide resistor for current-sensing when shunt resistor current-sensing is used.
8. Lay out the gate drive traces as directly as possible. Lay out the forward and return traces close together (either running side by side or on top of one other on adjacent layers) to minimize the gate drive path inductance.
9. Route the sensing traces (ISENS+ and ISENS-) with differential pair lines and the smallest closed area. Avoid crossing noisy areas, such as the SW or high-side gate drive traces.
10. Place the filter capacitor for the current-sense signal as close to the IC pins as possible.
11. Separate the VOUT for the FB sense and the VDRV power supply layout to avoid the FB sense being interrupted.
12. Tie the input and output capacitors' ground returns close together with a large PGND copper area.
13. For heavy loads, lay out with large copper, additional layers, and more vias for heatsinks.

Figure 13 shows the recommended component placement for the MP9931F. Figure 14 on page 29 shows the corresponding schematic for this layout.

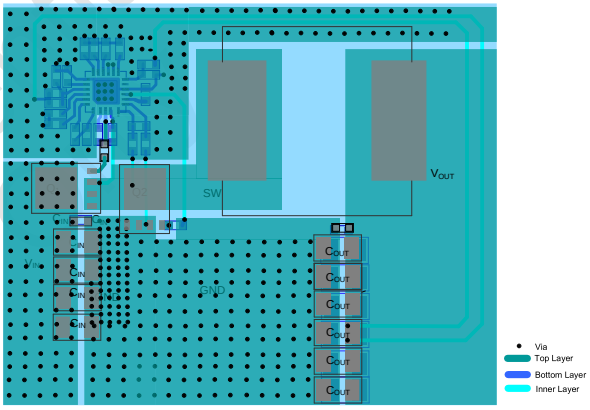


Figure 13: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

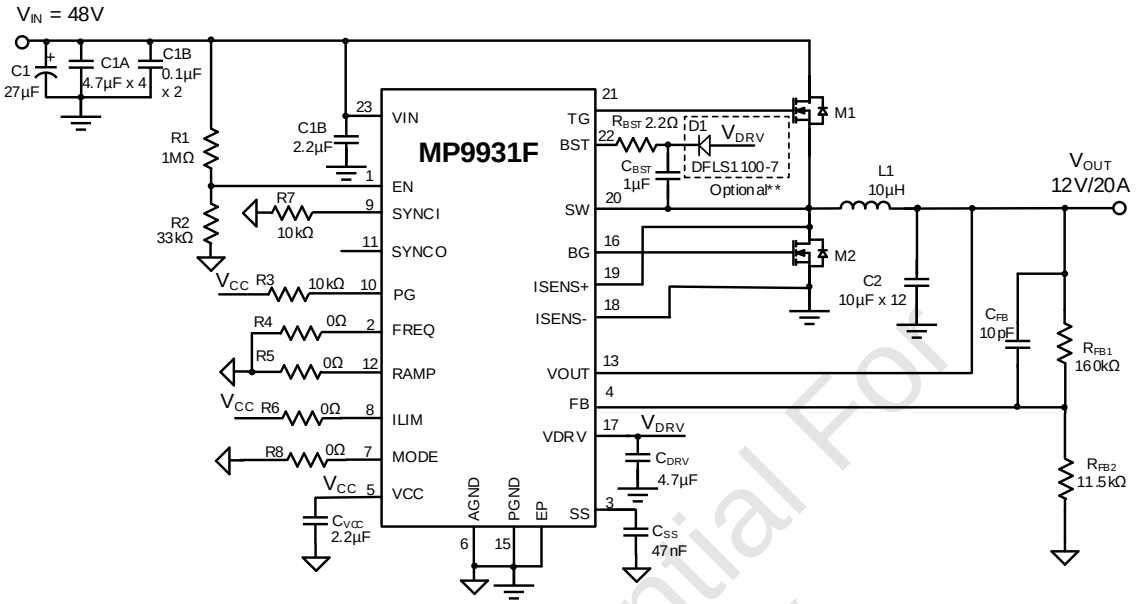


Figure 14: Typical Application Circuit for 12V Output (9)

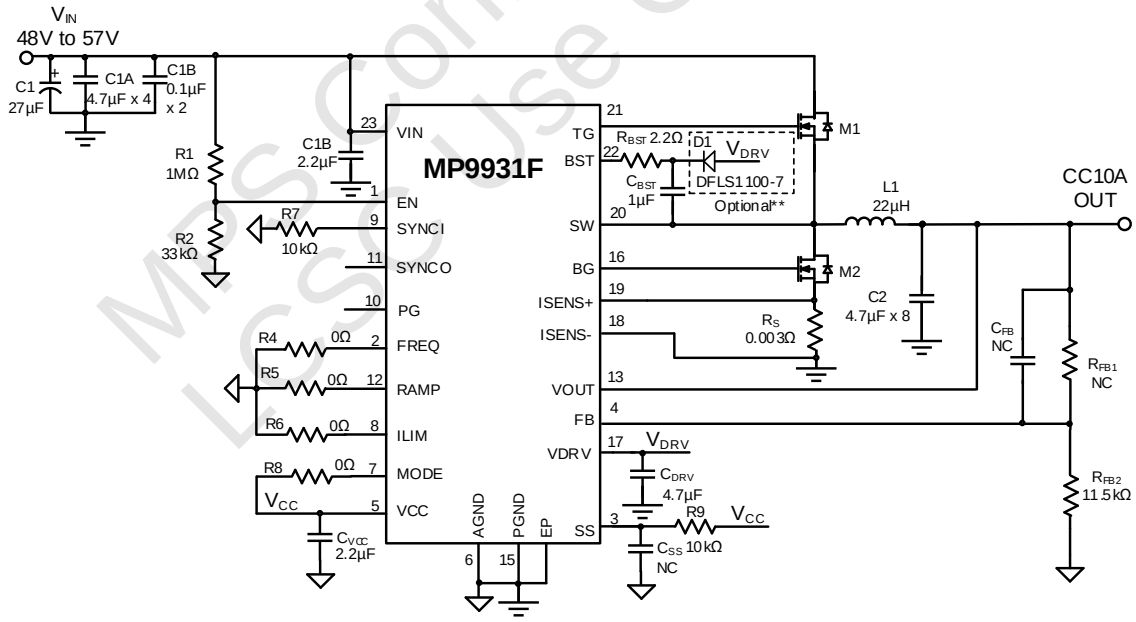


Figure 15: Typical Application Circuit for Constant Current 10A Output (9)

Note:

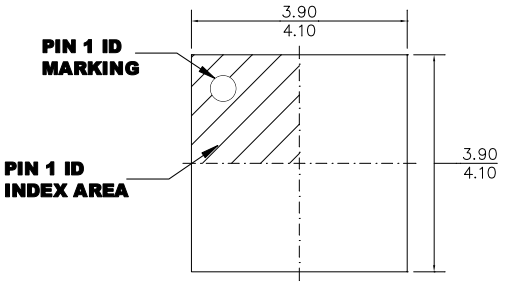
9) If the PCB layout for the input power loop between the input capacitor (C_{IN}), HS-FET, and LS-FET is not small, add an optional diode (D1).

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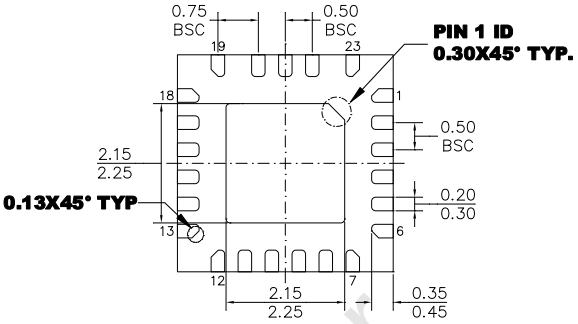
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PACKAGE INFORMATION

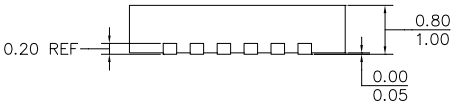
QFN-23 (4mmx4mm)



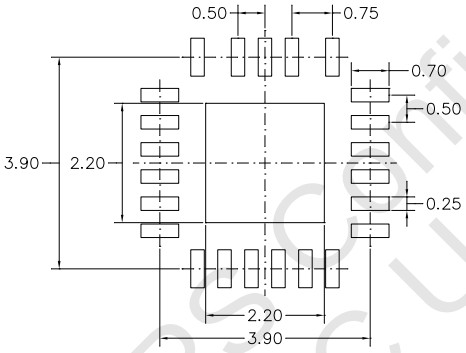
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

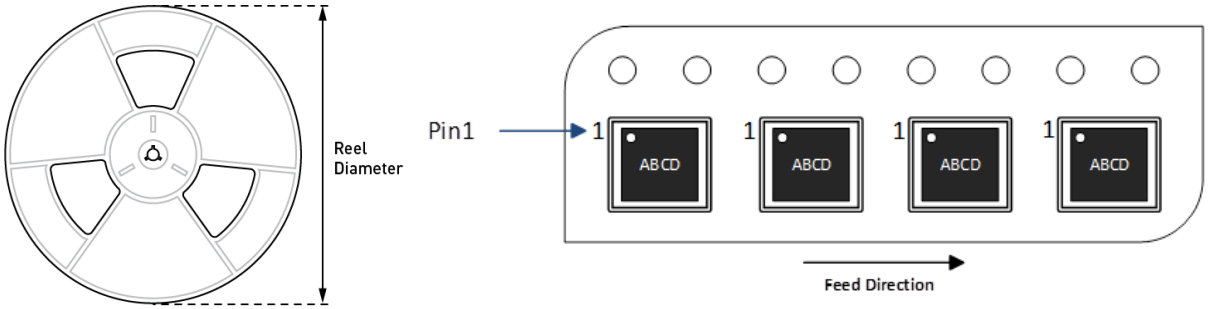
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP9931FGR-Z	QFN-23 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/2/2026	Initial Release	-

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