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Nyfea product specification

PRODUCT SPECIFICATION

Customer: _____

Product Name: I/O Expander with Interrupt Output

Part NO: FCA9535

Issue Date: _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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Table Of Contents

1 Features 4

2 Applications 4

3 Description 4

4 Device Information 4

5 Pin Configuration 5

6 Specifications 6

6.1 Absolute Maximum Ratings 6

6.2 ESD Ratings 6

6.3 Electrical Characteristic 6

7 Detailed Description 7

7.1 Port Structure 7

7.2 Register Map 8

7.2.1 Input Port X Registers 8

7.2.2 Output Port X Registers 8

7.2.3 Polarity Inversion Port X Registers 8

7.2.4 Configuration Port X Registers 9

7.3 Serial Interface 10

7.3.1 Bus Overview 10

7.3.2 Serial Bus Address 11

7.3.3 Writing and Reading Operation 12

7.3.4 Port Control 14

7.3.5 High.Speed (Hs) Mode 16

7.4 Interrupt Output 16

8 Application and Implementation 17

8.1 Quick Feature Guide 17

8.2 Typical Application 17

8.3 High Current.Drive Load Application 18

8.4 Layout Example 19

9 Packaging Information 20

9.1 Package Outline (TSSOP.24) 20

9.2 Package Outline (WQFN.24) 21

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9.3 Tape and Reel Information 22
10 Ordering Information 22

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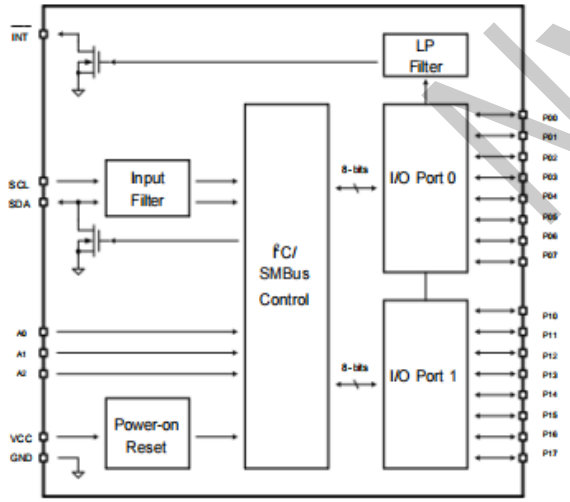
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1 Features

- Alternative to xCA9535
- Supply Range:1.6V~5.5V
- Temperature Range:-55℃~+125℃
- Standby Current:0.5μA
- High-Current Drive Capability
- Open-Drain Active-Low Interrupt Output

2 Applications

- Servers
- Routers
- Communication Cabinet
- Industrial Automation
- Products with GPIO-Limited Processors



3 Description

This device offers general-purpose parallel input/output (GPIO) expansion through the standard I²C serial interface. Port data is transferred via the two-wire I²C protocol, supporting communication clock rates of up to 1 MHz (extendable to 2 MHz when high-speed mode is enabled).

The device integrates 16 totem-pole I/O ports (P07–P00 and P17–P10), which are capable of directly driving LEDs. Each individual bit of the GPIO ports can be independently configured as either an input or an output. Upon power-on, all I/O ports are defaulted to the input state.

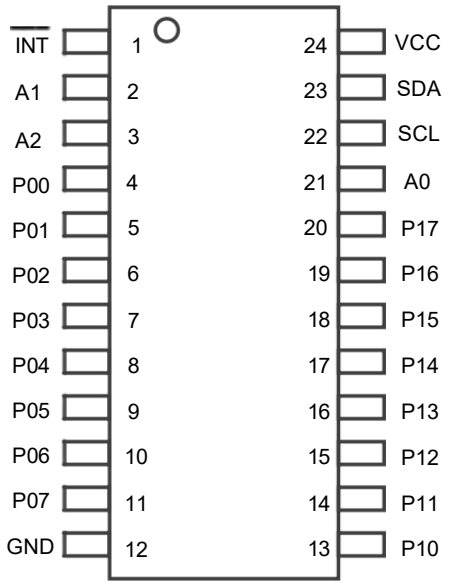
4 Device Information

DEVICENAME	PACKAGE	BODYSIZE(NOM)
FCA9535T	TSSOP(24)	7.80mm×4.40mm
FCA9535Q	WQFN(24)	4.00mm×4.00mm

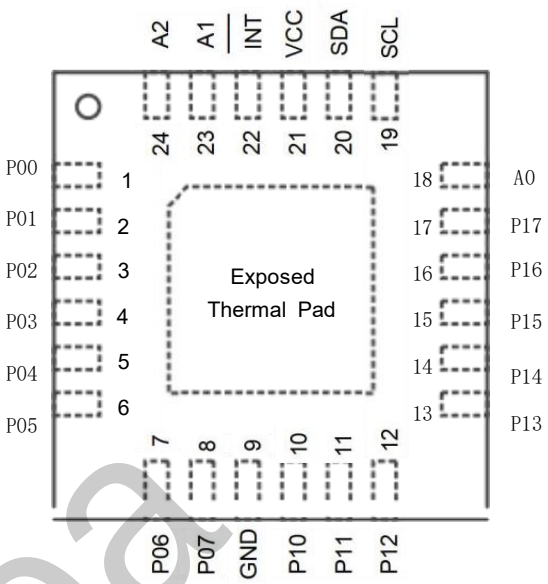
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5 Pin Configuration

FCA9535T
Top View



FCA9535Q
Top View



PIN			DESCRIPTION
NAME	TSSOP	HWQFN	
A0	21	18	Address input 0. Connect directly to VCC or GND.
A1	2	23	Address input 1. Connect directly to VCC or GND.
A2	3	24	Address input 2. Connect directly to VCC or GND.
GND	12	9	Ground.
INT	1	22	Interrupt open-drain output. Connect to VCC through a pull-up resistor.
P00 ~ P07	4 ~ 11	1 ~ 8	P-port I/O. At power on, all I/Os are configured as inputs.
P10 ~ P17	13 ~ 20	10 ~ 17	P-port I/O. At power on, all I/Os are configured as inputs.
SCL	22	19	Serial clock bus. Connect to VCC through a pull-up resistor.
SDA	23	20	Serial data bus. Connect to VCC through a pull-up resistor.
VCC	24	21	Supply voltage.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Voltage	- 0.5	6	V
Storage Temperature	- 65	150	° C
Input-output Clamp Current		± 20	mA
Continuous Output Current		± 50	mA
Continuous Current through GND		- 250	mA
Continuous Current through VCC		+ 160	mA

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

6.2 ESD Ratings

		VALUE	UNIT
Electrostatic Discharge	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	± 8000	V
Latch-up	Latch-Up, per JESD 78, Class IA	± 200	mA

6.3 Electrical Characteristic

Over temperature range of -55~+125℃ and supply range of 1.6~5.5V, unless otherwise noted. Typical values at +25° C and 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage, V_{CC}		1.6	3.3	5.5	V
Operating Temperature, T_A		- 55		125	° C
Quiescent Current, I_{CC}			0.5	5	μA
P-port High-level Output Voltage, V_{OH}	I_{OH} = -8mA, V_{CC} = 3V		2		V
	I_{OH} = -8mA, V_{CC} = 4.75V		4.2		V
	I_{OH} = -10mA, V_{CC} = 3V		1.8		V
	I_{OH} = -10mA, V_{CC} = 4.75V		4.2		V
P-port Low-Level Output Current, I_{OL}	V_{OL} = 0.5V, V_{CC} = 1.6V~5.5V	8			mA
	V_{OL} = 0.7V, V_{CC} = 1.6V~5.5V	10			mA
SDA Low-level Output Current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 1.6V~5.5V	3			mA
INT Low-level Output Current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 1.6V~5.5V	3			mA
Input Current, I_I	V_I = V_{CC} or GND			± 1	μA

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7 Detailed Description

7.1 Port Structure

A simplified cicuirt diagram of P-port I/Os is shown in Figure 1.

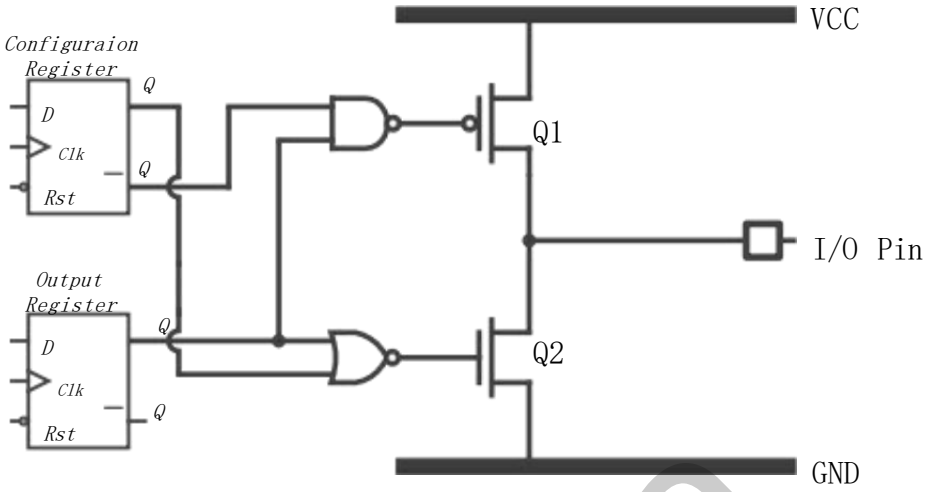


Figure 1. Simplified Circuit Diagram of P-port I/Os

When an I/O pin is configured as an input, both FETs Q1 and Q2 are turned off, presenting a high-impedance (Hi-Z) state to the external circuitry. In this mode, the voltage applied to the input pin may be driven above the supply voltage (VCC), up to an absolute maximum of 5.5 V.

When an I/O pin is configured as an output, either Q1 or Q2 is enabled, depending on the logic state stored in the Output Port register. A logic high enables Q1, creating a low-impedance path from the I/O pin to VCC; a logic low enables Q2, creating a low-impedance path from the I/O pin to GND. In this configuration, the external voltage applied to the I/O pin must not exceed the recommended operating levels to ensure proper device functionality and reliability.

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7.2 Register Map

The device's register file is organized as two symmetrical sets of registers, each dedicated to one of the two 8-bit I/O ports (Port 0 and Port 1). Each set comprises four 8-bit registers, with every bit position corresponding to a specific I/O pin—for example, bit 0 of Port 0 corresponds to pin P00, bit 1 to P01, and so on. The pointer addresses for these registers are listed in Table 1.

Table 1. Pointer Address and Register Map

POINTER	REGISTER NAME	ATTRIBUTION	DEFAULT VALUE
0x00	Input Port 0	R only	0xFF
0x01	Input Port 1	R only	0xFF
0x02	Output Port 0	R/W	0xFF
0x03	Output Port 1	R/W	0xFF
0x04	Polarity Inversion Port 0	R/W	0x00
0x05	Polarity Inversion Port 1	R/W	0x00
0x06	Configuration Port 0	R/W	0xFF
0x07	Configuration Port 1	R/W	0xFF

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7.2.1 Input Port X Registers

The Input Port X registers reflect the incoming logic levels present on the I/O pins, regardless of whether each pin is configured as an input or an output by the Configuration Port X register. These registers are read-only; write operations to them have no effect. At power- on, these registers default to all logic 1s.

7.2.2 Output Port X Registers

The Output Port X registers reflect the outgoing logic levels that are being driven on pins configured as outputs by the Configuration Port X register. Bit values in these registers have no effect on pins that are defined as inputs. Reads from these registers return the value stored in the output flip- flop that controls the pin drive state, rather than the actual logic level present on the pin itself.

7.2.3 Polarity Inversion Port X Registers

The Polarity Inversion Port X registers allow the user to invert the polarity of the data read from the Input Port X registers. When a bit in this register is set to 1, the corresponding bit in the Input

Port X register data is inverted (a low input is read as high, and vice versa). When a bit is cleared to 0, the input data polarity is retained without inversion.

7.2.4 Configuration Port X Registers

The Configuration Port X registers configure the direction of each I/O pin. When a bit in this register is set to 1, the corresponding pin is configured as an input with the output driver placed in a high- impedance (Hi- Z) state. When a bit is cleared to 0, the corresponding pin is configured as an output with the driver actively enabled.

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7.3 Serial Interface

7.3.1 Bus Overview

The I²C/SMBus interface employs a two-wire serial architecture that supports both multi-master and multi-slave configurations. The device which initiates a data transfer is designated as the master, while the target device responding to the master is referred to as the slave. The master assumes responsibility for generating the serial clock (SCL) signal and arbitrating access to the bus.

Each data transfer consists of eight serial clock pulses followed by an acknowledge (ACK) bit. During data transmission, the SDA line must remain stable while SCL is at a logic high level, as any transition on SDA during this interval is recognized as either a START or STOP condition. The timing parameters annotated in Figure 2 are specified in Table 2.

Table 2. Timing Diagram Requirements

SYMBOL	PARAMETER	FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	1	400	1	2000	kHz
$t_{SU:STA}$	Repeated START condition setup time	0.6	-	0.26	-	us
$t_{HD:STA}$	Repeated START condition hold time	0.6	-	0.26	-	us
$t_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	us
t_{BUF}	Bus free time between STOP and START	1.3	-	0.5	-	us
$t_{SU:DAT}$	Data setup time	0.1	-	0.05	-	us
$t_{HD:DAT}$	Data hold time	0	-	0	-	us
t_{HIG}	SCL clock high period	0.6	-	0.26	-	us
t_{LOW}	SCL clock low period	1.3	-	0.5	-	us
t_R	Clock and data rise time	-	300	-	120	ns
t_F	Clock and data fall time	-	300	-	120	ns

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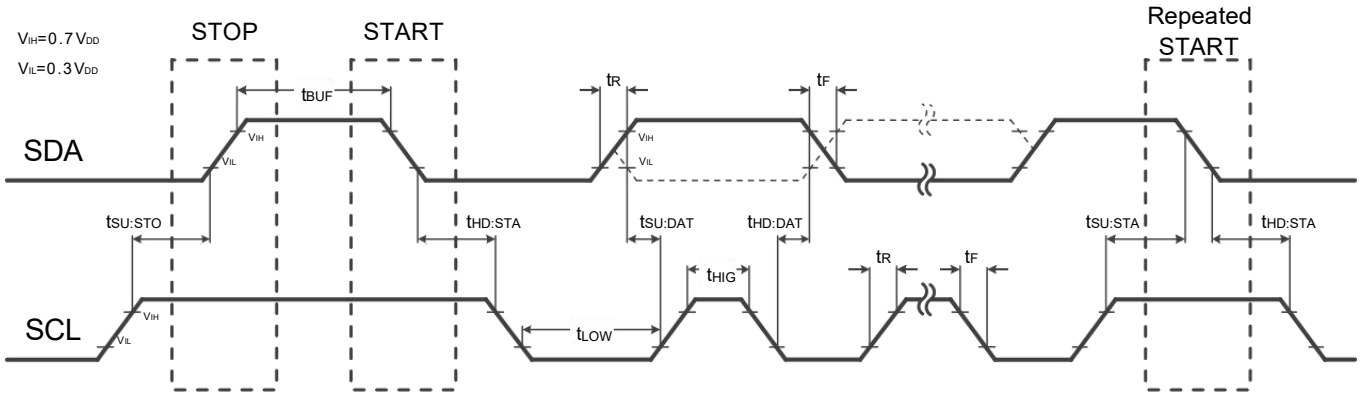


Figure 2. Two-Wire Timing Diagram

7.3.2 Serial Bus Address

The device provides three hardware address pins, allowing up to eight devices to be addressed on the same I²C bus. Table 2 lists the pin logic levels and their corresponding address assignments.

To ensure reliable communication, the logic states of these address pins must remain constant throughout each bus transaction; changing them during an active session may result in communication errors. Each address pin must be tied to either VCC or GND—floating connections are not permitted.

The slave address byte is composed of a 7- bit address field followed by a single direction bit that indicates whether the master intends to perform a read or a write operation. All data bytes transmitted on the bus are sent with the most significant bit (MSB) first.

Table 3. Address Pin Connection and Slave Address

A2	A1	A0	DEVICE TWO-WIRE ADDRESS
GND	GND	GND	0x40 (write), 0x41 (read)
GND	GND	VCC	0x42 (write), 0x43 (read)
GND	VCC	GND	0x44 (write), 0x45 (read)
GND	VCC	VCC	0x46 (write), 0x47 (read)
VCC	GND	GND	0x48 (write), 0x49 (read)
VCC	GND	VCC	0x4A (write), 0x4B (read)
VCC	VCC	GND	0x4C (write), 0x4D (read)
VCC	VCC	VCC	0x4E (write), 0x4F (read)

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7.3.3 Writing and Reading Operation

Register Write Operation and Pointer Byte

When the R/W bit is set to 0 (write), the first byte transmitted by the host after the slave address byte is interpreted as the pointer byte. The device uses this pointer to select the target register for the current read or write operation. The data byte follows the pointer byte and contains the value to be written to the specified register. The complete bus transaction, as illustrated in Figure 3, consists of a START condition, the address byte, the pointer byte, the data byte, and a STOP condition. During this sequence, the device pulls the SDA line low at the ninth clock pulse (ACK bit) of each received byte to indicate successful reception and readiness to accept the next byte.

Pointer Auto- Increment Function

The device incorporates a pointer auto- increment (or auto- shift) feature. Upon completion of each register access, the pointer automatically advances to the corresponding register of the same type in the other port. For example, after writing a byte to the Output Port 0 register, the next data byte is directed to the Output Port 1 register; the subsequent byte then wraps back to Output Port 0, and so on. The bus timing for this sequential write operation is shown in Figure 4.

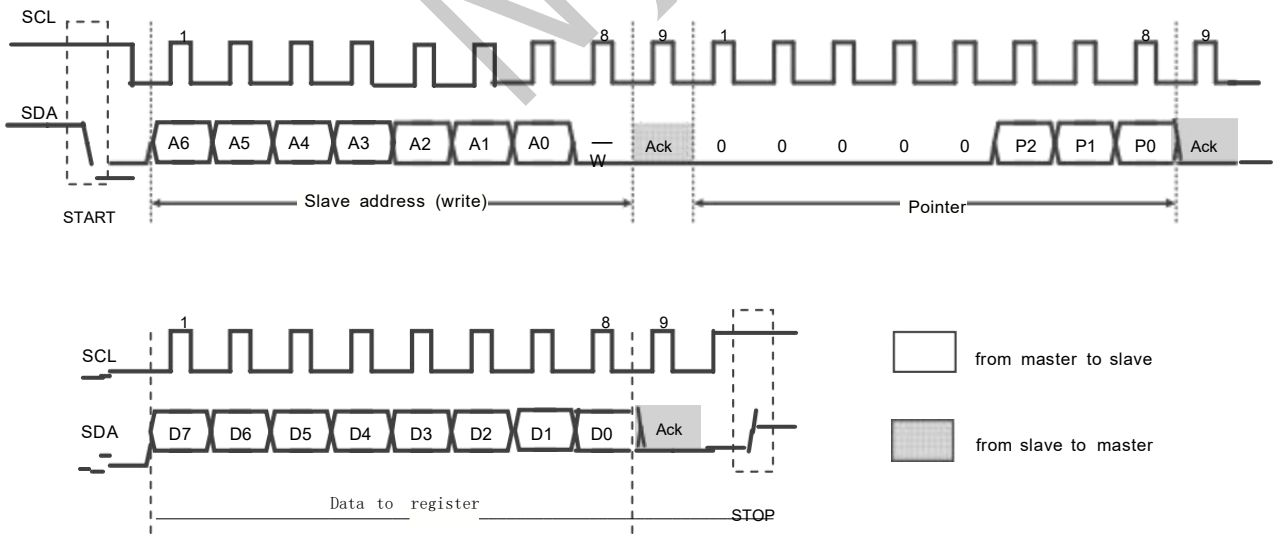


Figure 3. Two-Wire Timing Diagram for Write One Byte

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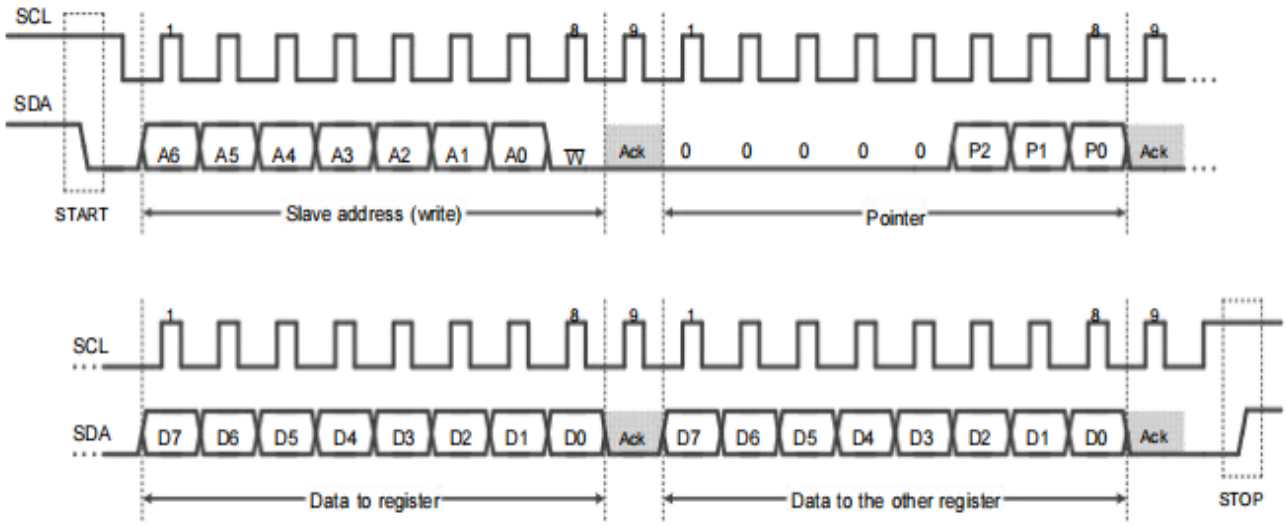


Figure 4. Two-Wire Timing Diagram for Write Two Bytes

When the R/W bit is set to 1 (read), the host may begin reading data bytes immediately following the slave address byte. The content of the data returned by the device is determined by the current pointer value. Therefore, in a read operation, the host must first set the pointer to the desired register address, and then issue a repeated START condition to initiate a new bus transaction before reading the target data. The specific bus timing for this sequence is illustrated in Figure 5.

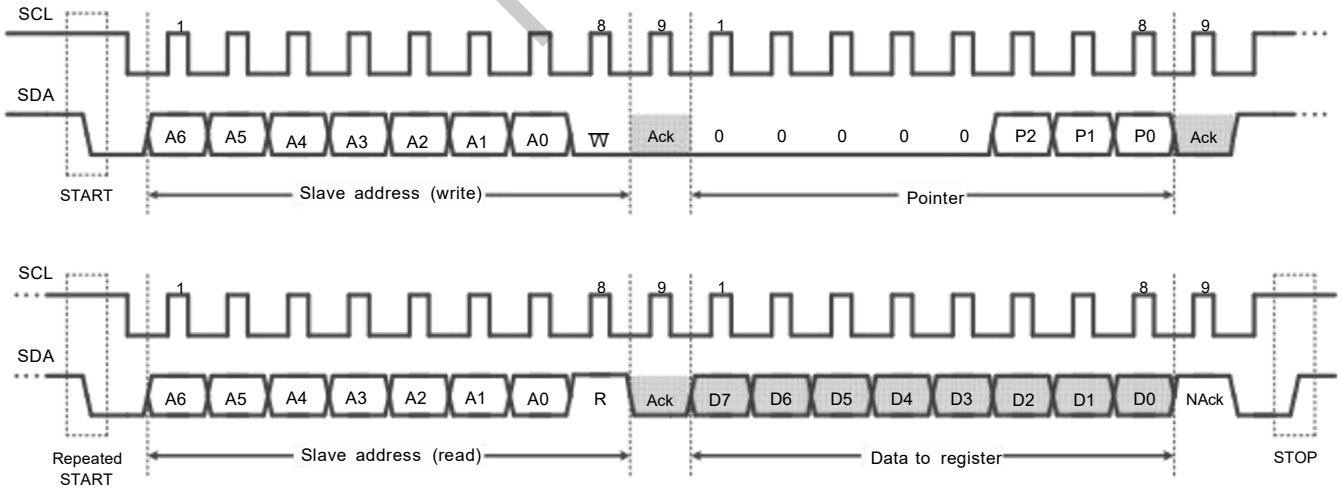


Figure 5. Two-Wire Timing Diagram for Read One Byte

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Read operations support multi-byte access. The specific bus timing is shown in Figure 6.

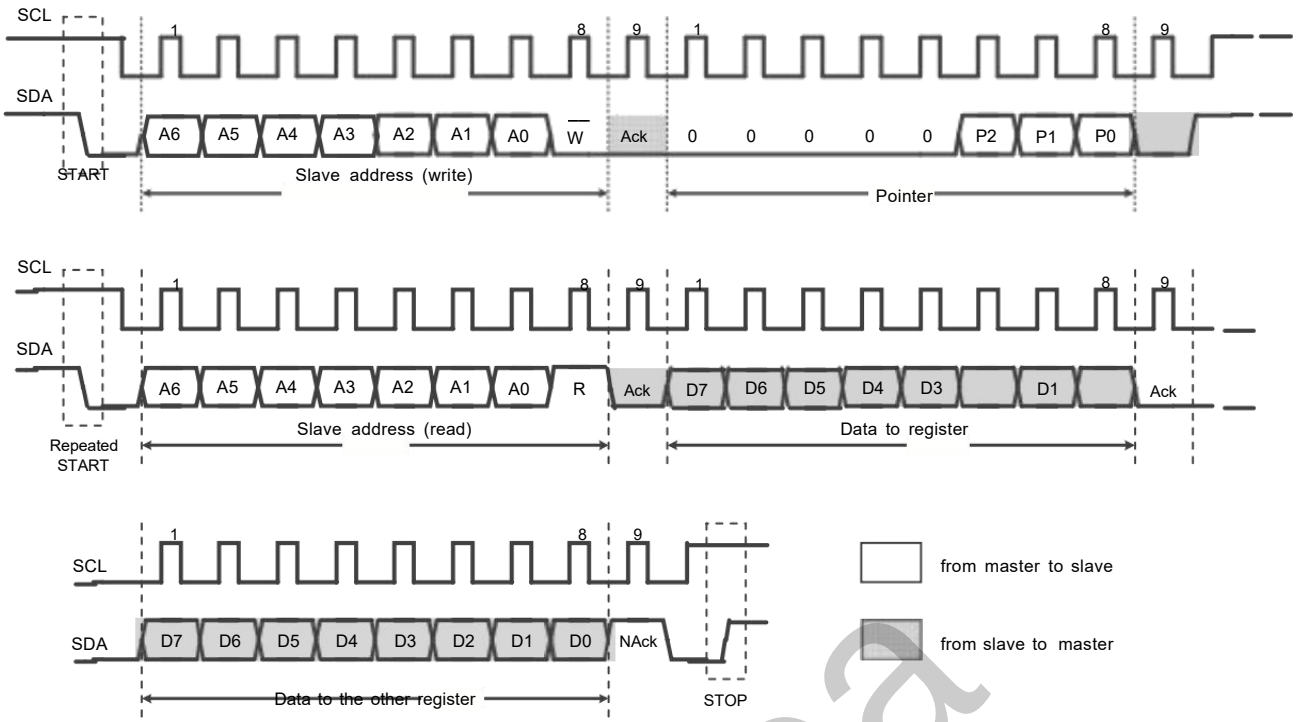


Figure 6. Two-Wire Timing Diagram for Read Two Bytes

7.3.4 Port Control

The FCA9535 drives the output state of each I/O pin under the condition that the pin has been configured as an output via the Configuration Port X register. The relationship between the Output Port X register values and the resulting control of the I/O ports is illustrated in Figure 7.

During a write operation, the device latches the received data to the I/O pins at the rising edge of SCL corresponding to the ACK bit of each data byte. This ensures that the output pins are updated synchronously with the completion of each byte transfer.

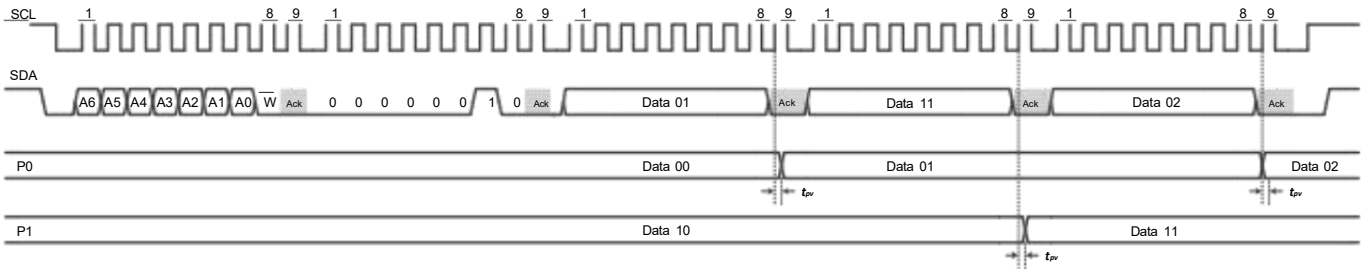


Figure 7. Write to Output Port X Registers

The FCA9535 is capable of acquiring the logic level of each I/O pin regardless of whether the pin is configured as an input or an output. The effect of reading the input register on the interrupt signal is illustrated in Figures 8 and 9.

During the ACK bit of each data byte in a read operation, the device samples the logic level of the I/O pin and loads it into the input register at the rising edge of SCL. This sampling event subsequently clears any pending interrupt condition.

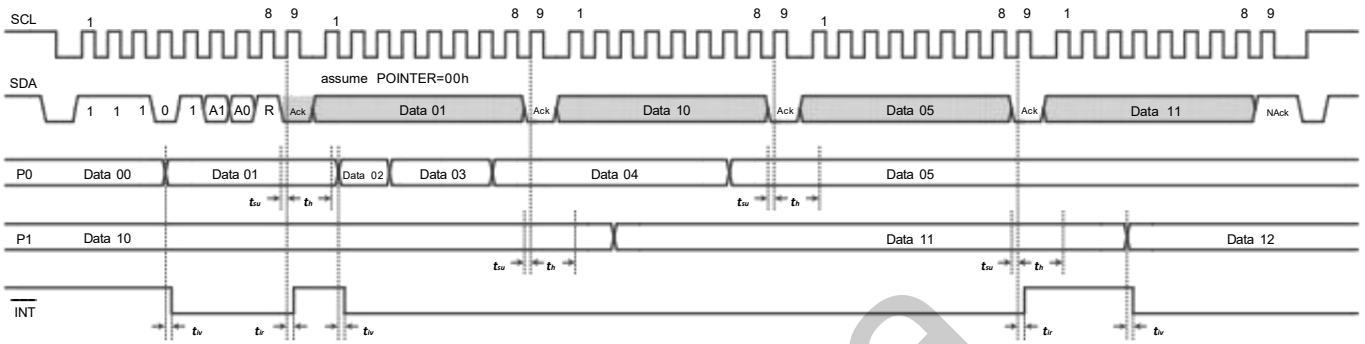


Figure 8. Read Input Port Registers, Scenario 1

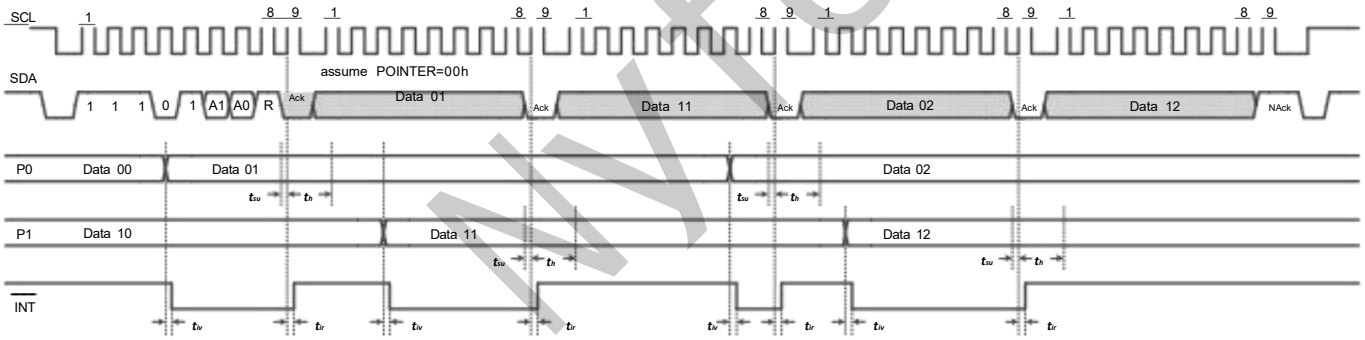


Figure 9. Read Input Port Registers, Scenario 2

Table 4. Switching Characteristics

SYMBOL	PARAMETER	FROM	TO	MIN	TYP	MAX	UNIT
t_{pv}	Outpu Data Valid Time	SCL	GPIO			1	us
t_{su}	Input Data Setupt Time	GPIO	SCL		1		us
t_h	Input Data Hold Time	GPIO	SCL		1		us
t_{iv}	Interrupt Valid Time	GPIO	INT			4	us
t_{ir}	Interrupt Reset Delay	SCL	INT			4	us

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7.3.5 High.Speed (Hs) Mode

To operate the I²C bus at frequencies above 1 MHz, the master must first issue an Hs- mode master code (0000 1xxx) as the first byte following a START condition. This code switches the bus into high- speed operation. The FCA9535 does not acknowledge this byte; however, it responds by reconfiguring its input filters on the SDA and SCL pins, as well as the output filter on the SDA pin, to operate in Hs- mode, thereby enabling data transfers at speeds up to 2 MHz.

After the Hs- mode master code has been sent, the master transmits a standard slave address to initiate the actual data- transfer transaction. The bus remains in Hs- mode until a STOP condition is issued. Upon detecting a STOP condition, the device automatically reverts its input and output filters to fast- mode operation.

7.4 Interrupt Output

The device provides an open- drain interrupt output pin that can be directly connected to the interrupt input of a host microprocessor. By asserting this interrupt signal, the chip actively notifies the host whenever a change in logic level is detected on any remote I/O pin.

Two key points should be noted regarding the assertion and de- assertion of the interrupt signal:

- The interrupt is triggered only by a logic- level change on an I/O pin that is configured as an input.
- The interrupt signal is not latched. If the I/O pin logic level returns to the state it held at the last sampling instant, the interrupt is cleared immediately.

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8 Application and Implementation

NOTE

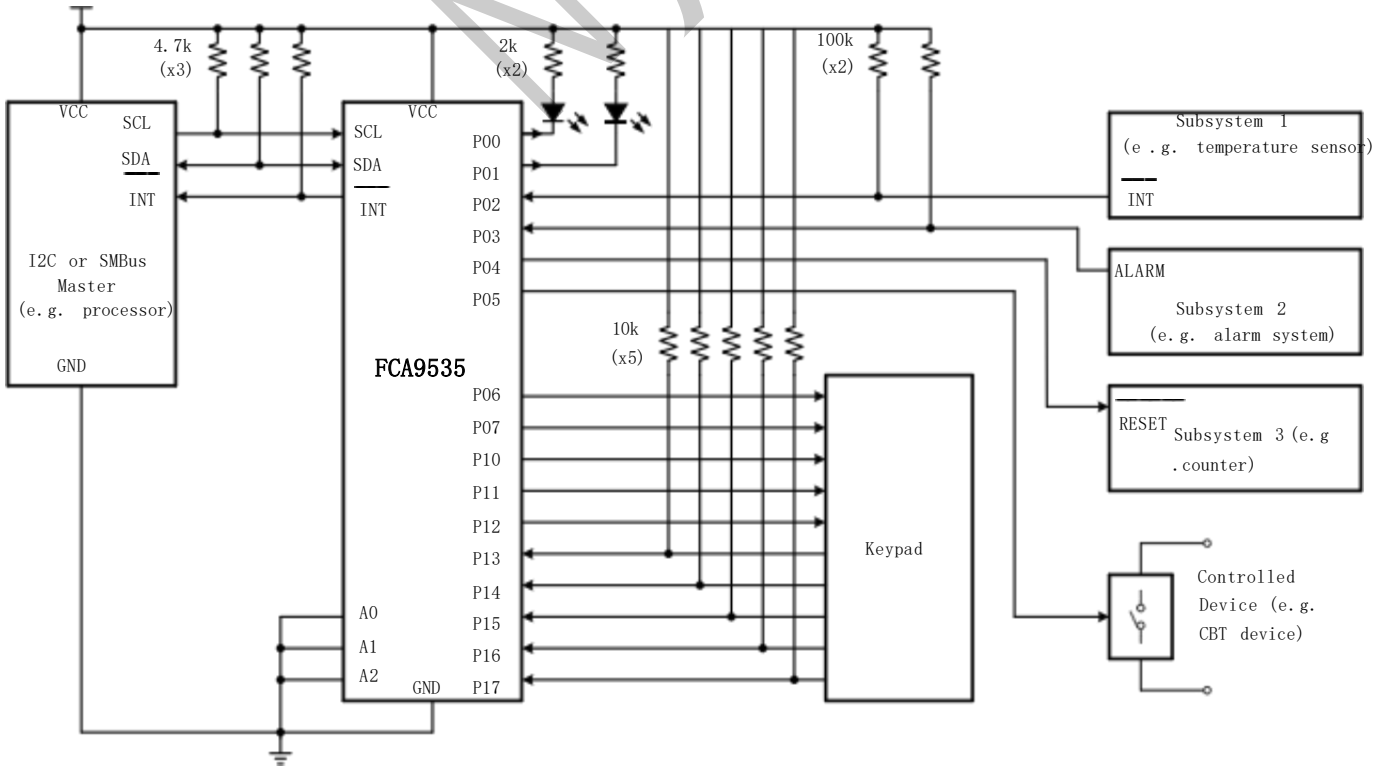
The following contents are notes and suggestions for the use of FCA9535 family, and NYFEA does not warrant its accuracy or completeness . Customers are responsible for determing suitability of components for their purpose, as well as validating and testing their design implementation to confirm system functionality.

8.1 Quick Feature Guide

Table 5. Selection Table

DEVICE	TYPE	I/O	ADDRESS	BUILT-IN PULLUP	RESET INPUT
FCA8574	Quasi bi-dir.	8	0100 xxxb		
FCA9534	Totem-pole	8	0100 xxxb		
FCA9538	Totem-pole	8	1110 0xxb		√
FCA9554	Totem-pole	8	0100 xxxb	√	
FCA9535	Totem-pole	16	0100 xxxb		
FCA9539	Totem-pole	16	1110 1xxb		√
FCA9555	Totem-pole	16	0100 xxxb	√	

8.2 Typical Application



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8.3 High Current.Drive Load Application

The I/O pins of the device are capable of sinking a minimum of 10 mA each. To achieve higher current-driving capability, multiple I/O pins can be connected together in parallel through short- wire connections. As illustrated in Figure 10, when paralleling multiple pins, each pin must have its own individual current-limiting resistor, and proper synchronization of the output switching is required to prevent any potential damage to the device.

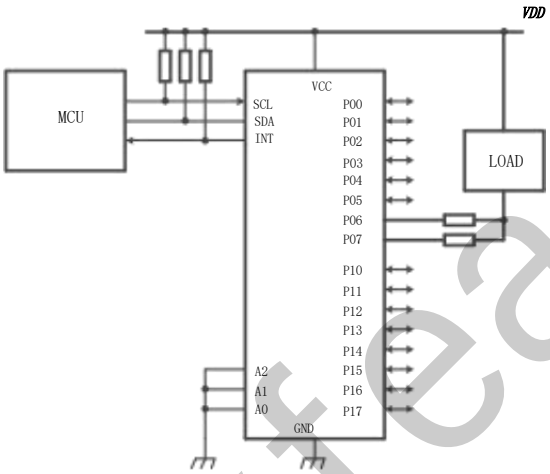
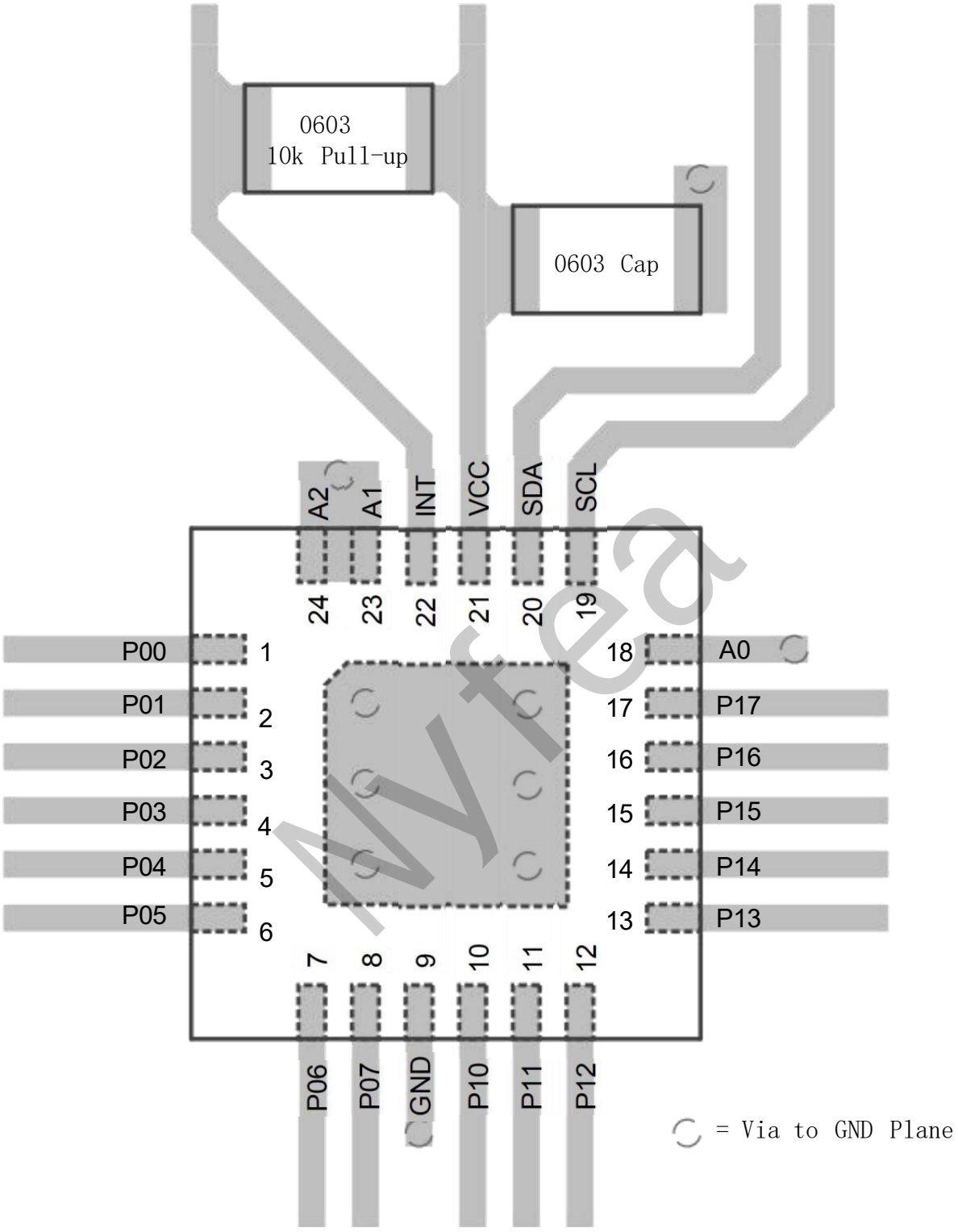


Figure 10. High Current-Drive Load Application

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8.4 Layout Example

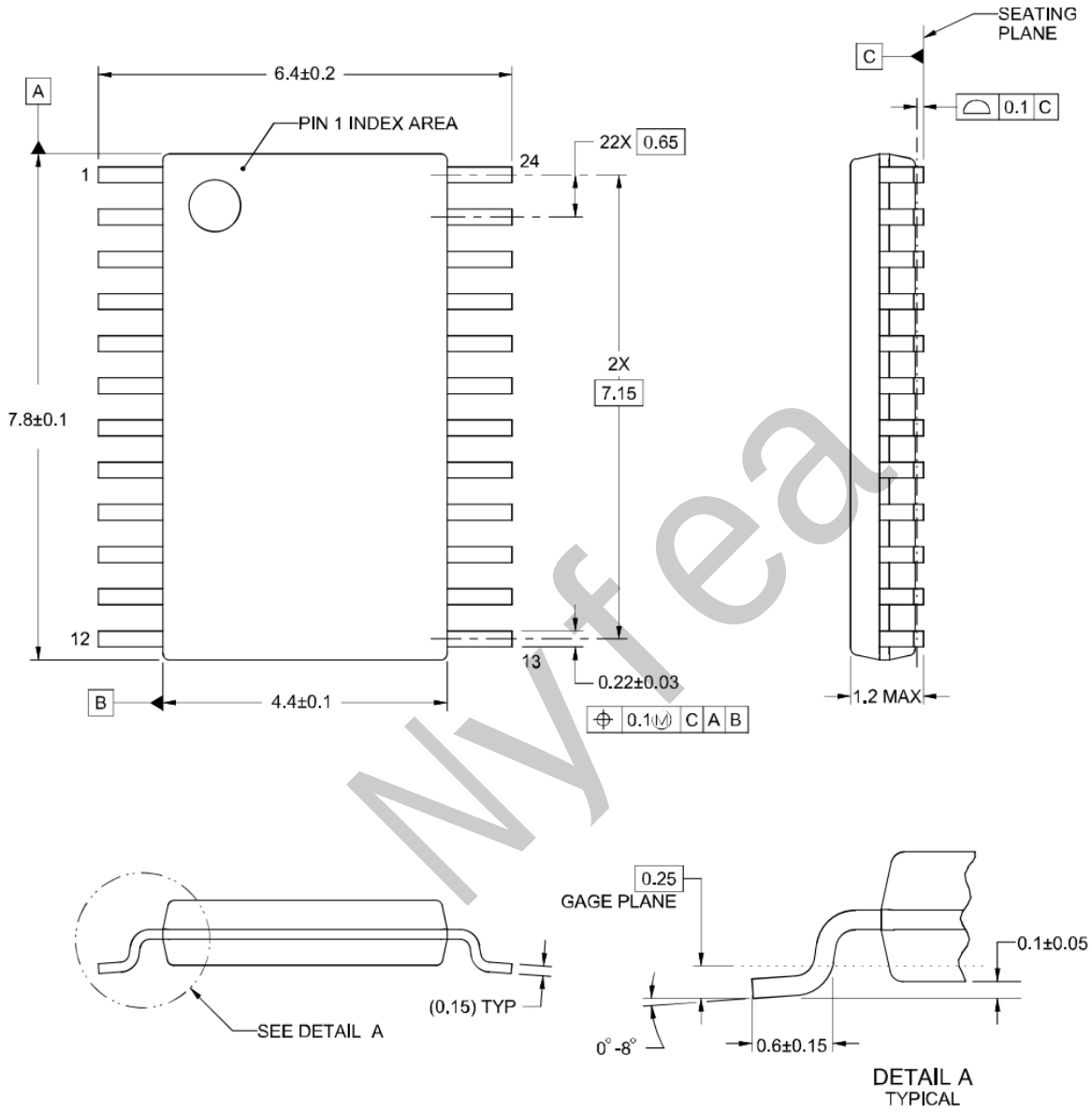


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9 Packaging Information

All dimensions mentioned below are in millimeters.

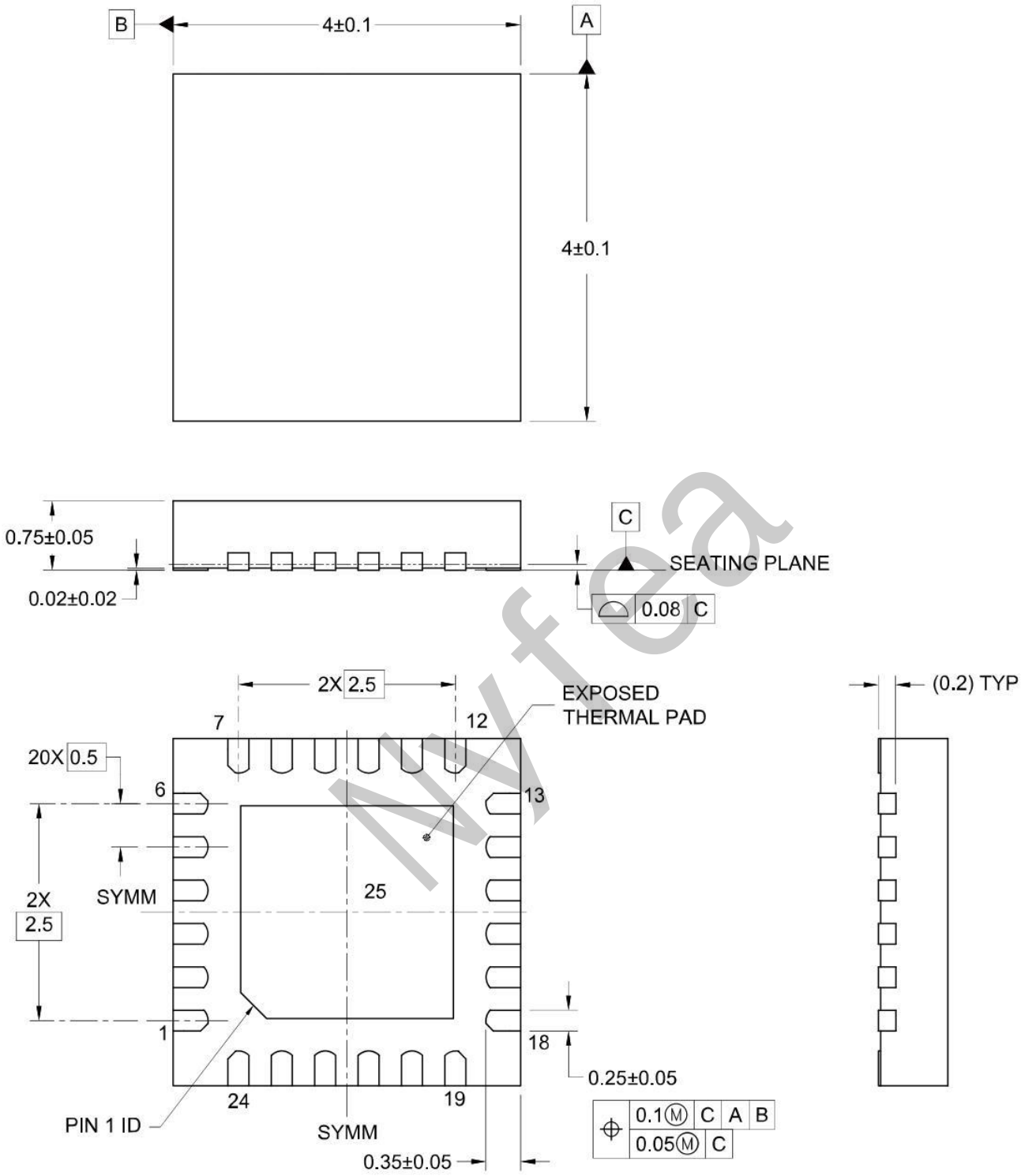
9.1 Package Outline (TSSOP.24)



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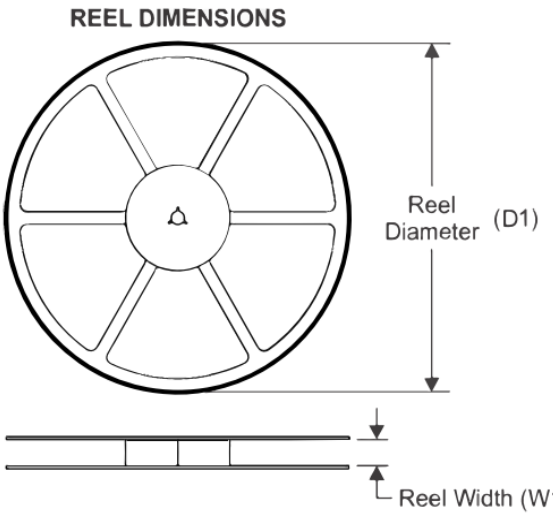
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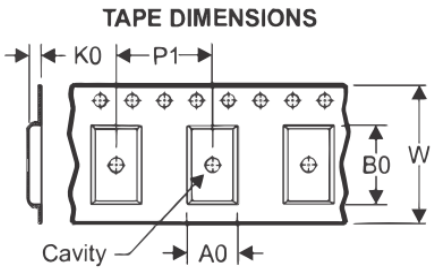
9.2 Package Outline (WQFN.24)



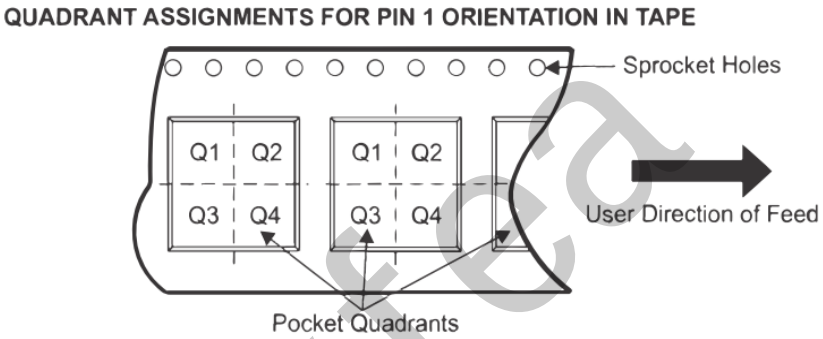
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9.3 Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PACKAGE	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1
TSSOP-24	330	16.4	6.80	8.30	1.60	8.00	16.00	Q1
WQFN-24	329	12.4	4.30	4.30	1.10	8.00	12.00	Q1

Note: All dimensions mentioned above are in millimeters.

10 Ordering Information

ORDER CODE	DEVICE	PACKAGE	QUANTITY	NOTES
FCA9535T-T&R	FCA9535T	TSSOP (24)	4000	Tape&Reel
FCA9535Q-T&R	FCA9535Q	WQFN (24)	4000	Tape&Reel

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