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Nyfea product specification

PRODUCT SPECIFICATION

Customer: _____

Product Name: I/O Expander with Interrupt Output

Part NO: FCA9555

Issue Date: _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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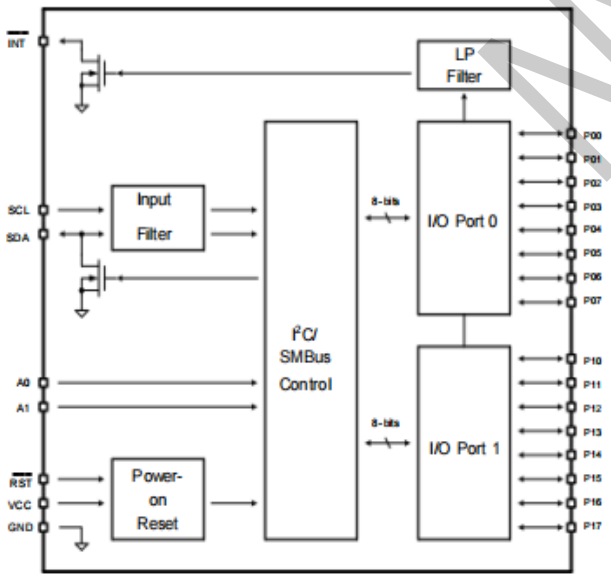
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1 Features

- Alternative to xCA9555
- Supply Range:1.6V~5.5V
- Temperature Range:-55℃~+125℃
- Standby Current:0.5μA
- High-Current Drive Capability
- Open-Drain Active-Low Interrupt Output

2 Applications

- Servers
- Routers
- Communication Cabinet
- Industrial Automation
- Products with GPIO-Limited Processors



3 Description

This device offers general-purpose parallel input/output (GPIO) expansion through the standard I²C serial interface. Port data is transferred via the two-wire I²C protocol, supporting communication clock rates of up to 1 MHz (extendable to 2 MHz when high-speed mode is enabled).

The device integrates 16 totem-pole I/O ports (P07 - P00 and P17 - P10), which are capable of directly driving LEDs. Each individual bit of the GPIO ports can be independently configured as either an input or an output. Upon power-on, all I/O ports are defaulted to the input state.

4 Device Information

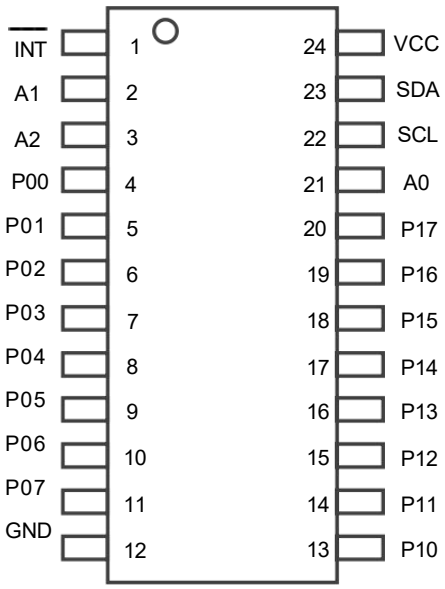
DEVICENAME	PACKAGE	BODYSIZE (NOM)
FCA9555T	TSSOP (24)	7.80mm×4.40mm
FCA9555Q	WQFN (24)	4.00mm×4.00mm

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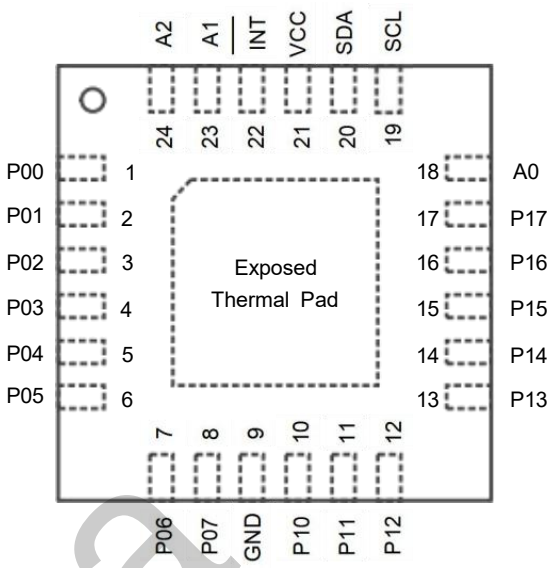
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5 Pin Configuration

FCA9555T
Top View



FCA9555Q
Top View



PIN			DESCRIPTION
NAME	TSSOP	WQFN	
A0	21	18	Address input 0. Connect directly to VCC or GND.
A1	2	23	Address input 1. Connect directly to VCC or GND.
A2	3	24	Address input 2. Connect directly to VCC or GND.
GND	12	9	Ground.
INT	1	22	Interrupt open-drain output. Connect to VCC through a pull-up resistor.
P00 ~ P07	4 ~ 11	1 ~ 8	P-port I/O. At power on, all I/Os are configured as inputs.
P10 ~ P17	13 ~ 20	10 ~ 17	P-port I/O. At power on, all I/Os are configured as inputs.
SCL	22	19	Serial clock bus. Connect to VCC through a pull-up resistor.
SDA	23	20	Serial data bus. Connect to VCC through a pull-up resistor.
VCC	24	21	Supply voltage.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Voltage	- 0.5	6	V
Storage Temperature	- 65	150	° C
Input-output Clamp Current		± 20	mA
Continuous Output Current		± 50	mA
Continuous Current through GND		- 250	mA
Continuous Current through VCC		+ 160	mA

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

6.2 ESD Ratings

		VALUE	UNIT
Electrostatic Discharge	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	± 8000	V
Latch-up	Latch-Up, per JESD 78, Class IA	± 200	mA

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6.3 Electrical Characteristic

Over temperature range of -55~+125° C and supply range of 1.6~5.5V, unless otherwise noted. Typical values at +25° C and 3.3V.

PARAMETER	TEST CONDITIONS	MIN MAX	TYP	UNIT
Supply Voltage, V_{CC}		1.6 5.5	3.3	V
Operating Temperature, T_A		- 55 125		° C
Quiescent Current, I_{CC}			0.5 5	μA
P-port High-level Output Voltage, V_{OH}	I_{OH} = -8mA, V_{CC} = 3V		2	V
	I_{OH} = -8mA, V_{CC} = 4.75V		4.2	V
	I_{OH} = -10mA, V_{CC} = 3V		1.8	V
	I_{OH} = -10mA, V_{CC} = 4.75V		4.2	V
P-port Low-Level Output Current, I_{OL}	V_{OL} = 0.5V, V_{CC} = 1.6V~5.5V	8		mA
	V_{OL} = 0.7V, V_{CC} = 1.6V~5.5V	10		mA
SDA Low-level Output Current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 1.6V~5.5V	3		mA
INT Low-level Output Current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 1.6V~5.5V	3		mA
Input Current, I_I	V_I = V_{CC} or GND		± 1	μA

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7 Detailed Description

7.1 Port Structure

A simplified cicuirt diagram of P-port I/Os is shown in Figure 1.

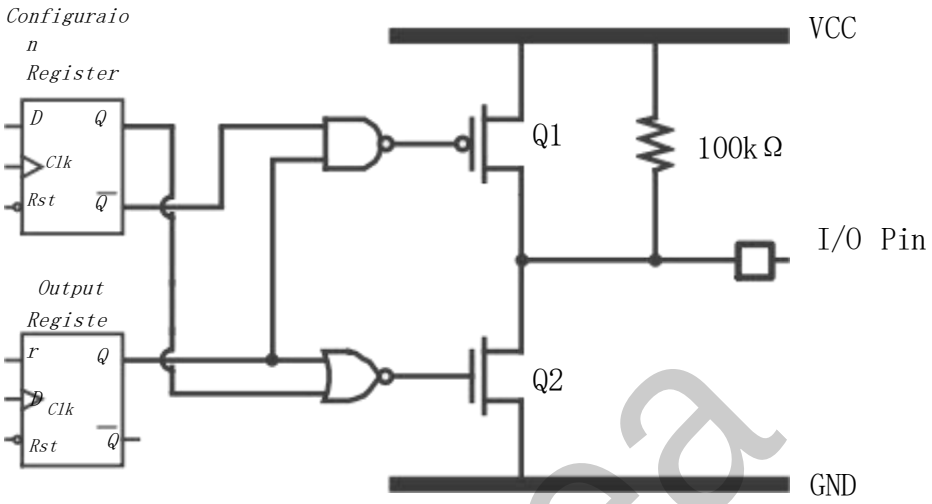


Figure 1. Simplified Circuit Diagram of P-port I/Os

When an I/O pin is configured as an input, both FETs Q1 and Q2 are turned off, resulting in a high-impedance state. Under this condition, the voltage applied to the pin may be raised above VCC, up to a maximum of 5.5V.

When an I/O pin is configured as an output, either Q1 or Q2 is enabled based on the corresponding bit value in the Output Port register. This establishes a low-impedance path between the I/O pin and either VCC or GND. To ensure proper operation, any external voltage applied to the pin must remain within the recommended operating levels.

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7.2 Register Map

The FCA9555 register file is organized as two symmetric sets of registers, each responsible for controlling one of the two I/O ports (Port 0 and Port 1) on a byte-by-byte basis. Each set contains four 8-bit registers, with every bit corresponding to a specific I/O pin — for example, bit 0 of Port 0 corresponds to pin P00, and so forth. The pointer addresses for the register map are listed in Table 1.

Table 1. Pointer Address and Register Map

POINTER	REGISTER NAME	ATTRIBUTION	DEFAULT VALUE
0x00	Input Port 0	R only	0xFF
0x01	Input Port 1	R only	0xFF
0x02	Output Port 0	R/W	0xFF
0x03	Output Port 1	R/W	0xFF
0x04	Polarity Inversion Port 0	R/W	0x00
0x05	Polarity Inversion Port 1	R/W	0x00
0x06	Configuration Port 0	R/W	0xFF
0x07	Configuration Port 1	R/W	0xFF

Input Port X Registers: These registers reflect the incoming logic levels present on the I/O pins, irrespective of whether each pin is configured as an input or an output by the Configuration Port X register. Reads from these registers return the current pin states; write operations have no effect. The power-on default value for these registers is all 1s.

Output Port X Registers: These registers reflect the outgoing logic levels for pins that are configured as outputs by the Configuration Port X register. Bit values in these registers have no effect on pins defined as inputs. Reads from these registers return the value stored in the output flip-flop, rather than the actual voltage level present on the pin.

Polarity Inversion Port X Registers: These registers allow the user to invert the polarity of the data read from the Input Port X registers. Setting a bit to 1 inverts the corresponding Input Port X register data; clearing a bit to 0 leaves the data polarity unchanged.

Configuration Port X Registers: These registers determine the direction of each I/O pin. Setting a bit to 1 configures the corresponding pin as an input with a high-impedance output driver. Clearing a bit to 0 configures the corresponding pin as an output.

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7.3 Serial Interface

7.3.1 Bus Overview

I2C/SMBus is a two-wire serial communication protocol that supports multi-master and multi-slave architectures. The device that initiates a transaction is referred to as the master, while the device responding to the master is called the slave. The master is responsible for generating the serial clock (SCL) and managing bus access.

Data is transmitted in 8-bit bytes, with each byte followed by an acknowledge bit. During data transfer, the SDA line must remain stable while SCL is high, as any transition on SDA during this period is interpreted as either a START or a STOP condition. The timing parameters for Figure 2 are defined in Table 2..

Table 2. Timing Diagram Requirements

SYMBOL	PARAMETER	FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	1	400	1	2000	kHz
$t_{SU:STA}$	Repeated START condition setup time	0.6	-	0.26	-	us
$t_{HD:STA}$	Repeated START condition hold time	0.6	-	0.26	-	us
$t_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	us
t_{BUF}	Bus free time between STOP and START	1.3	-	0.5	-	us
$t_{SU:DAT}$	Data setup time	0.1	-	0.05	-	us
$t_{HD:DAT}$	Data hold time	0	-	0	-	us
t_{HIG}	SCL clock high period	0.6	-	0.26	-	us
t_{LOW}	SCL clock low period	1.3	-	0.5	-	us
t_R	Clock and data rise time	-	300	-	120	ns
t_F	Clock and data fall time	-	300	-	120	ns

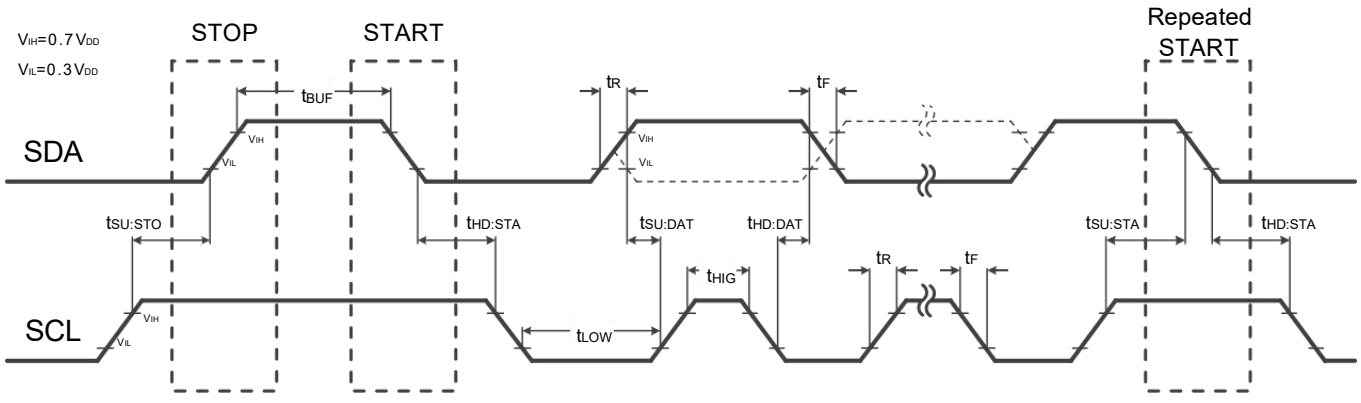


Figure 2. Two-Wire Timing Diagram

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7.3.2 Serial Bus Address

The FCA9555 provides three address pins, enabling up to eight devices to be addressed on a single I2C bus. Table 2 defines the pin logic levels and their corresponding address assignments. To ensure reliable operation, the logic level on each address pin must remain fixed throughout all communications; any change may lead to system failures. Address pins should be tied directly to either VCC or GND and must never be left floating.

The slave address byte is composed of seven address bits, followed by a direction bit that specifies whether the subsequent transaction is a read or a write operation. All data bytes are transmitted with the most significant bit (MSB) first.

Table 3. Address Pin Connection and Slave Address

A2	A1	A0	DEVICE TWO-WIRE ADDRESS
GND	GND	GND	0x40 (write), 0x41 (read)
GND	GND	VCC	0x42 (write), 0x43 (read)
GND	VCC	GND	0x44 (write), 0x45 (read)
GND	VCC	VCC	0x46 (write), 0x47 (read)
VCC	GND	GND	0x48 (write), 0x49 (read)
VCC	GND	VCC	0x4A (write), 0x4B (read)
VCC	VCC	GND	0x4C (write), 0x4D (read)
VCC	VCC	VCC	0x4E (write), 0x4F (read)

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7.3.3 Writing and Reading Operation

When the R/W bit is 0 (write operation), the first byte transmitted by the host following the slave address byte is interpreted as a pointer. The FCA9555 uses this pointer to select the target register for the subsequent read or write access. The data byte that follows the pointer byte contains the value to be written to the specified register. The complete bus transaction sequence—illustrated in Figure 3—consists of a START condition, slave address byte, pointer byte, data byte, and STOP condition. The FCA9555 asserts an ACK by pulling SDA low during the ninth clock pulse to confirm successful reception of each byte and readiness for the next.

The FCA9555 also incorporates a pointer auto-increment (or auto-rollover) feature. After each register access, the pointer automatically advances to the other register of the same type within the register set. For example, after writing a byte to the Output Port 0 register, the next byte will be written to the Output Port 1 register; the subsequent byte will return to Output Port 0, and this alternating pattern continues accordingly. The timing for this operation is depicted in Figure 4.

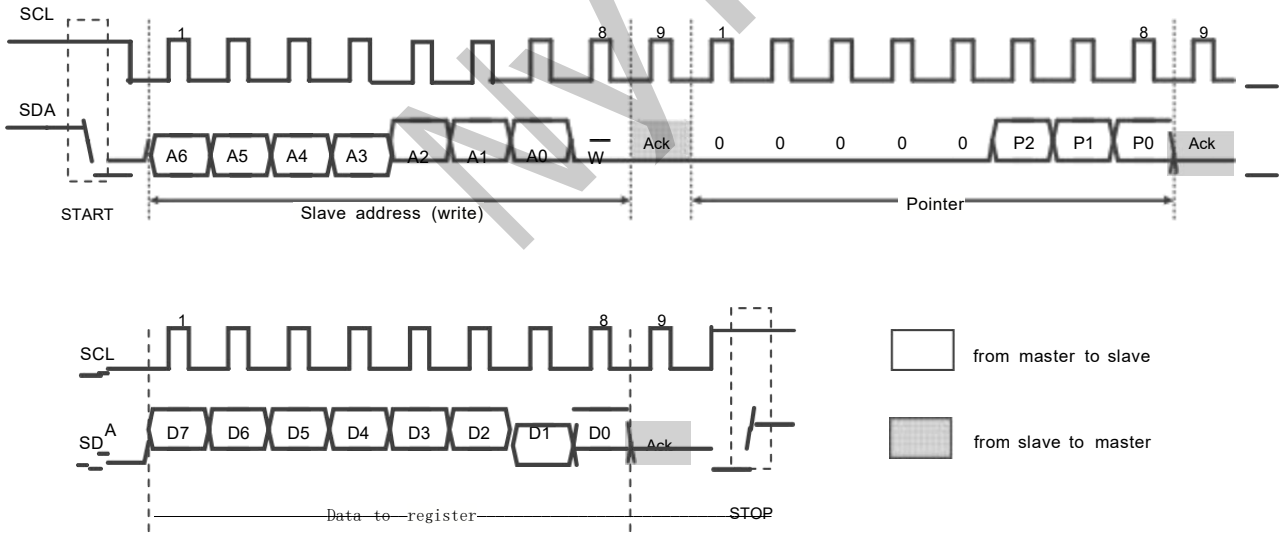


Figure 3. Two-Wire Timing Diagram for Write One Byte

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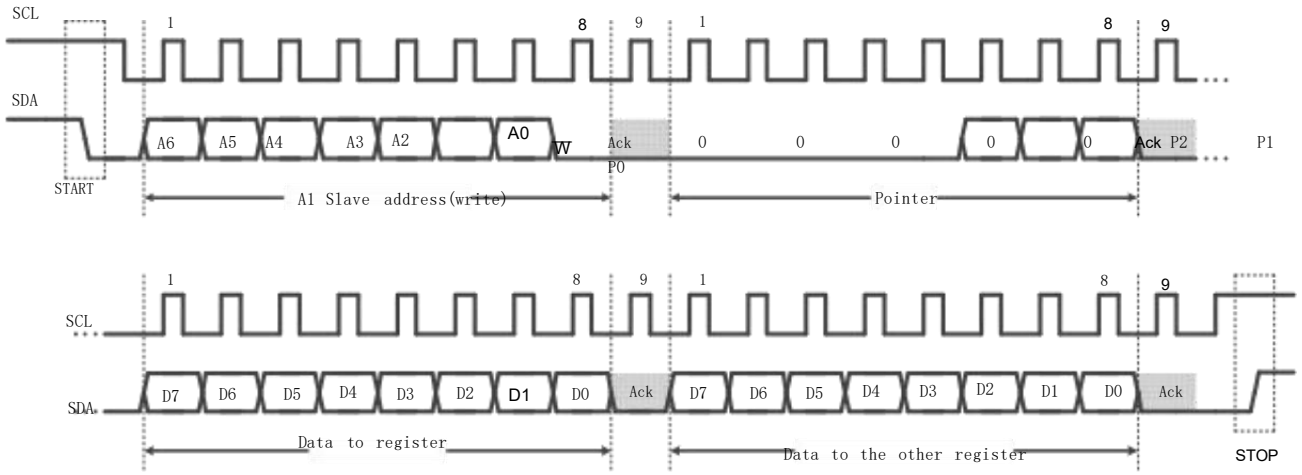


Figure 4. Two-Wire Timing Diagram for Write Two Bytes

When the R/W bit is set to 1 (read operation), the host may begin reading data bytes immediately after transmitting the slave address byte. The data returned by the device is determined by the current pointer setting. Consequently, for a read operation, the host must first configure the pointer to the desired register, then restart communication to retrieve the target data. The bus timing for this sequence is illustrated in Figure 5.

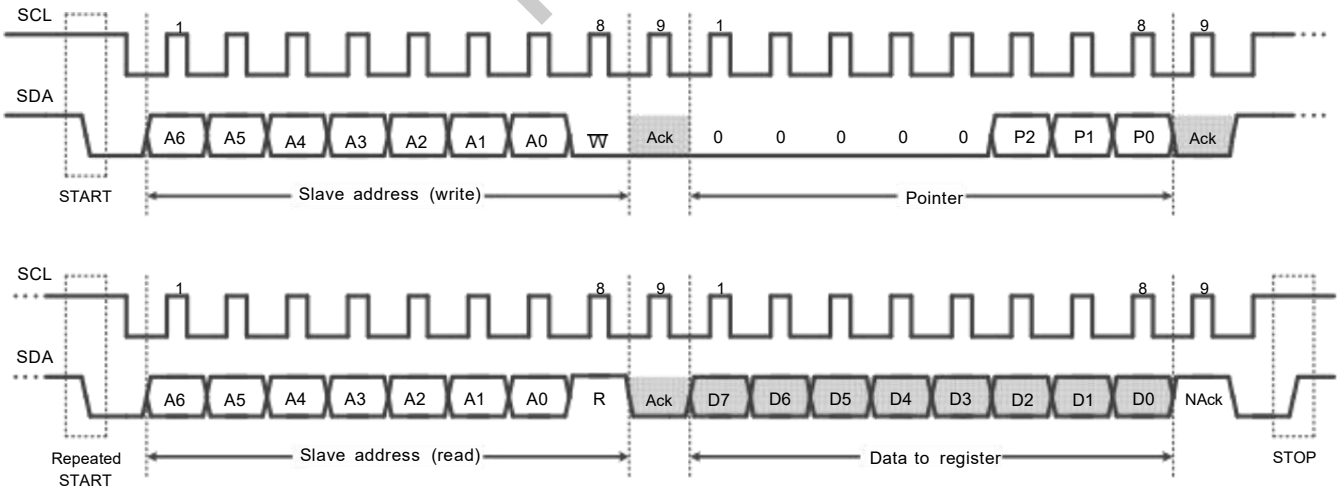


Figure 5. Two-Wire Timing Diagram for Read One Byte

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Read operations support multi-byte access. The specific bus timing is shown in Figure 6.

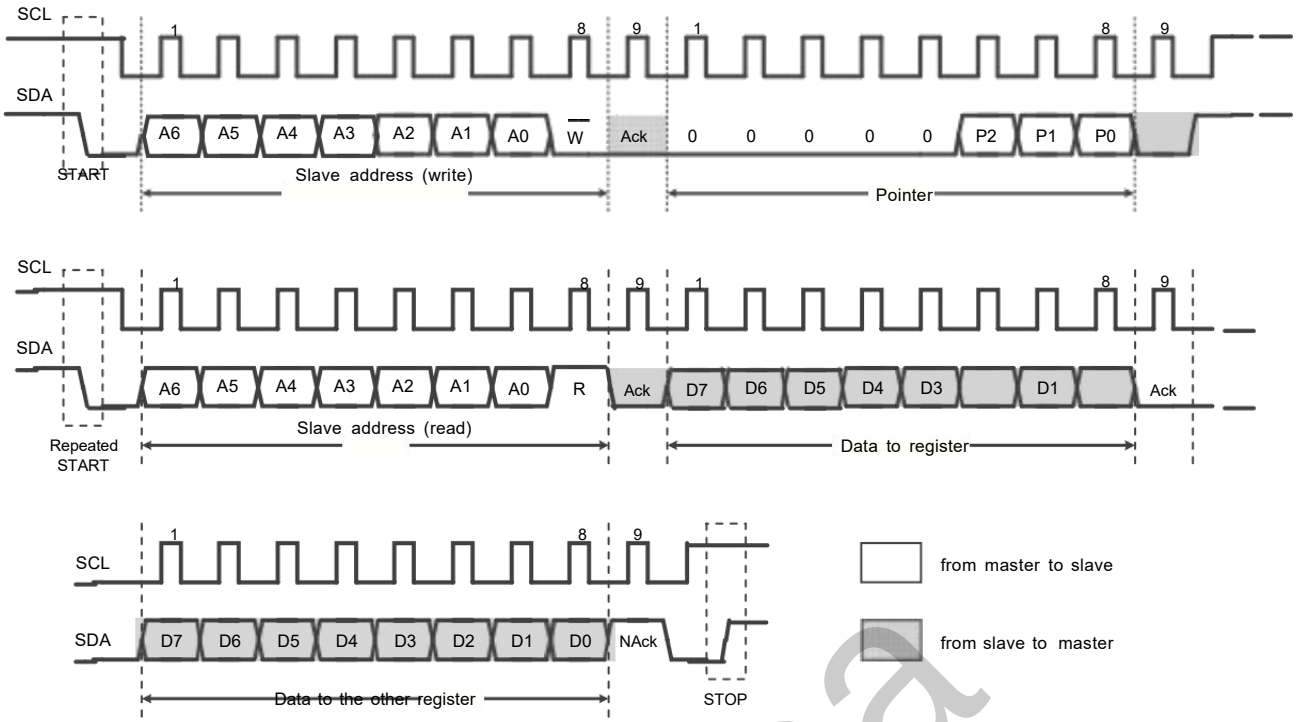


Figure 6. Two-Wire Timing Diagram for Read Two Bytes

7.3.4 Port Control

The FCA9555 drives the output state of an I/O pin only when that pin has been configured as an output via the corresponding Configuration register. The relationship between the Output Port X register and the resulting I/O pin states is illustrated in Figure 7.

Data written to the device is latched to the I/O pins on the rising edge of SCL during the acknowledge cycle of each transmitted data byte..

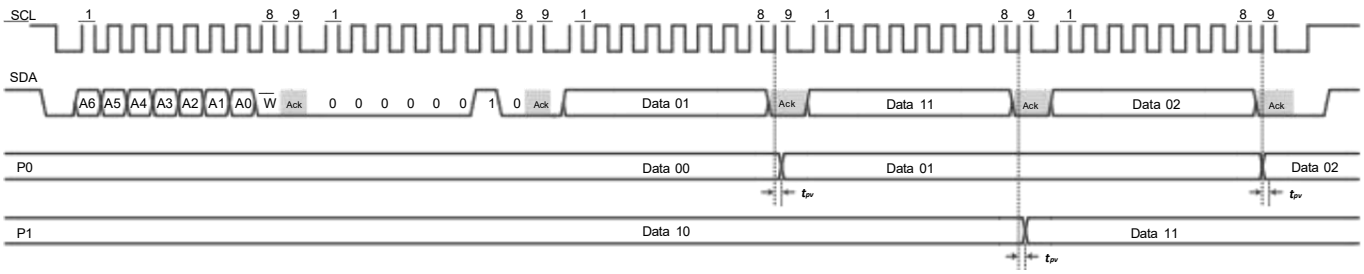


Figure 7. Write to Output Port X Registers

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The FCA9555 can capture the logic level of an I/O pin regardless of whether the pin is configured as an input or an output. The relationship between reading the Input register and its effect on the interrupt signal is illustrated in Figures 8 and 9. During the acknowledge cycle of each data byte, the device samples the pin's logic state into the Input register on the rising edge of SCL, which subsequently clears the interrupt.

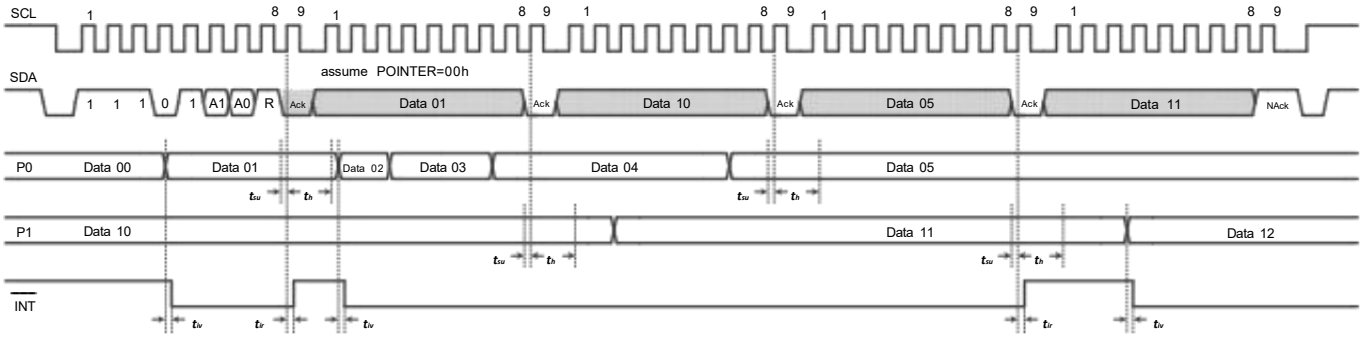


Figure 8. Read Input Port Registers, Scenario 1

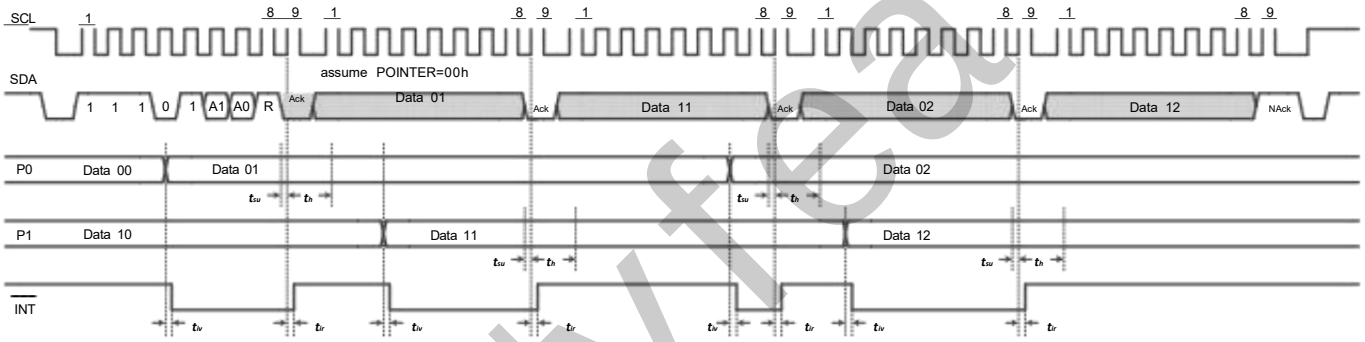


Figure 9. Read Input Port Registers, Scenario 2

Table 4. Switching Characteristics

SYMBOL	PARAMETER	FROM	TO	MIN	TYP	MAX	UNIT
t_{pv}	Outpu Data Valid Time	SCL	GPIO			1	us
t_{su}	Input Data Setupt Time	GPIO	SCL		1		us
t_h	Input Data Hold Time	GPIO	SCL		1		us
t_{iv}	Interrupt Valid Time	GPIO	INT			4	us
t_{ir}	Interrupt Reset Delay	SCL	INT			4	us

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7.3.5 High.Speed (Hs) Mode

To operate the I2C bus at frequencies above 1 MHz, the master must issue an Hs-mode master code (0000 1xxx) as the first byte following a START condition. This code instructs the bus to transition into high-speed operation. The FCA9555 does not acknowledge this byte; however, it responds by reconfiguring its input filters on the SDA and SCL pins, as well as the output filter on the SDA pin, to suit Hs-mode operation, thereby enabling data transfers at speeds up to 2 MHz.

After the Hs-mode master code has been sent, the master transmits an I2C slave address to begin the actual data transfer. The bus remains in Hs-mode until a STOP condition is issued. Upon detecting the STOP condition, the FCA9555 returns its input and output filters to the fast-mode configuration

7.4 Interrupt Output

The FCA9555 provides an open-drain interrupt output pin that can be connected directly to a microprocessor's interrupt input. Through this interrupt signal, the device can proactively alert the host processor to any logic-level changes occurring on the remote I/O pins.

Two important points must be understood regarding the assertion and de-assertion of the interrupt signal:

1) The interrupt is triggered solely by a logic-level transition on an I/O pin that has been configured as an input.

2) The interrupt signal is not latched. If the I/O pin returns to its previously sampled logic state, the interrupt will be cleared immediately.

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8 Application and Implementation

NOTE

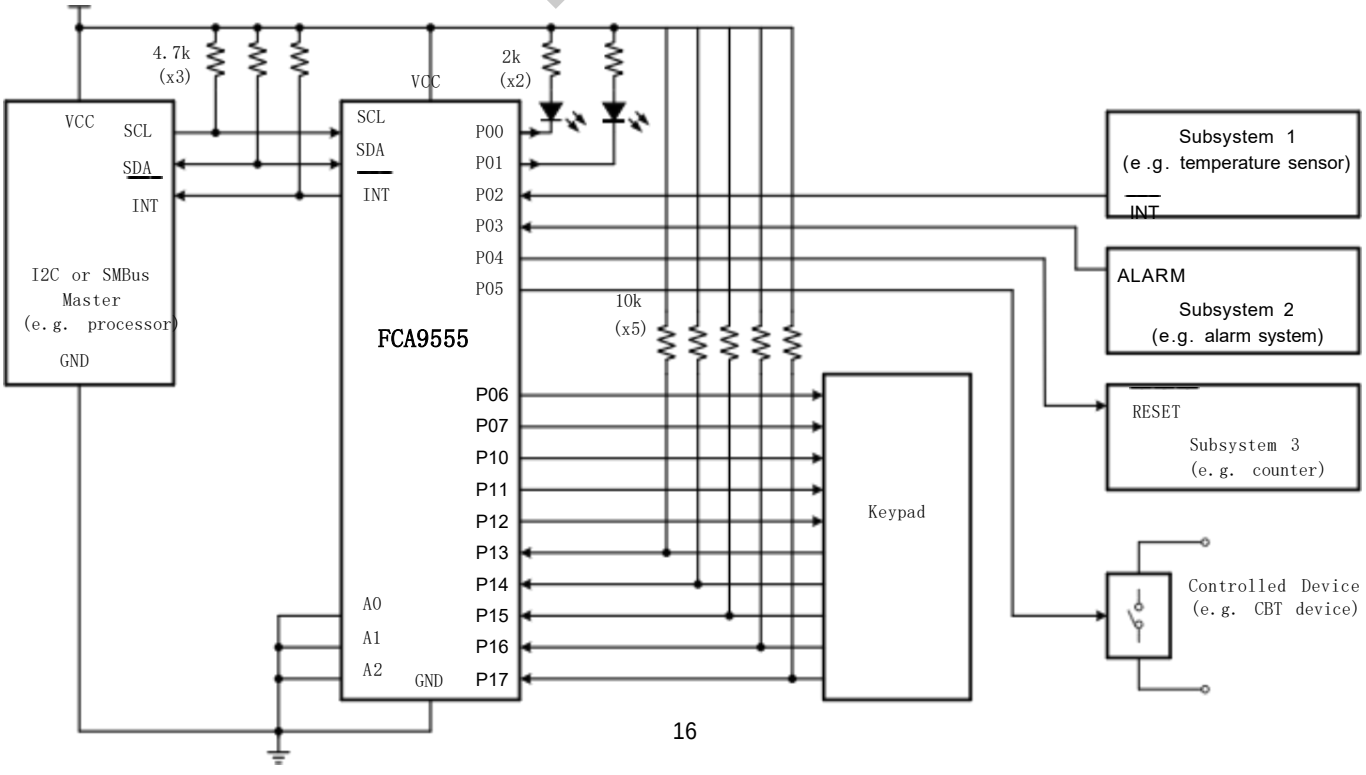
The following content provides usage notes and recommendations for the FCA9555 family. NYFEA does not warrant the accuracy or completeness of this information. Customers are solely responsible for determining the suitability of the components for their intended applications, and for validating and testing their design implementations to confirm proper system functionality.

8.1 Quick Feature Guide

Table 5. Selection Table

DEVICE	TYPE	I/O	ADDRESS	BUILT-IN PULLUP	RESET INPUT
FCA8574	Quasi bi-dir.	8	0100 xxxb		
FCA9534	Totem-pole	8	0100 xxxb		
FCA9538	Totem-pole	8	1110 0xxb		√
FCA9554	Totem-pole	8	0100 xxxb	√	
FCA9535	Totem-pole	16	0100 xxxb		
FCA9539	Totem-pole	16	1110 1xxb		√
FCA9555	Totem-pole	16	0100 xxxb	√	

8.2 Typical Application



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8.3 High Current.Drive Load Application

The I/O pins of the FCA9555 can deliver a minimum sink/source current of 10mA per pin. Furthermore, multiple I/O pins may be shorted together in parallel to increase the overall current-driving capability. As illustrated in Figure 10, each I/O pin must be equipped with its own current-limiting resistor, and the switching of all parallel-connected pins must be properly synchronized to avoid potential damage to the device.

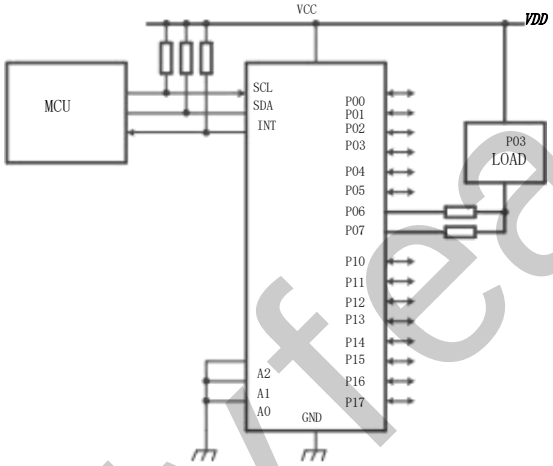
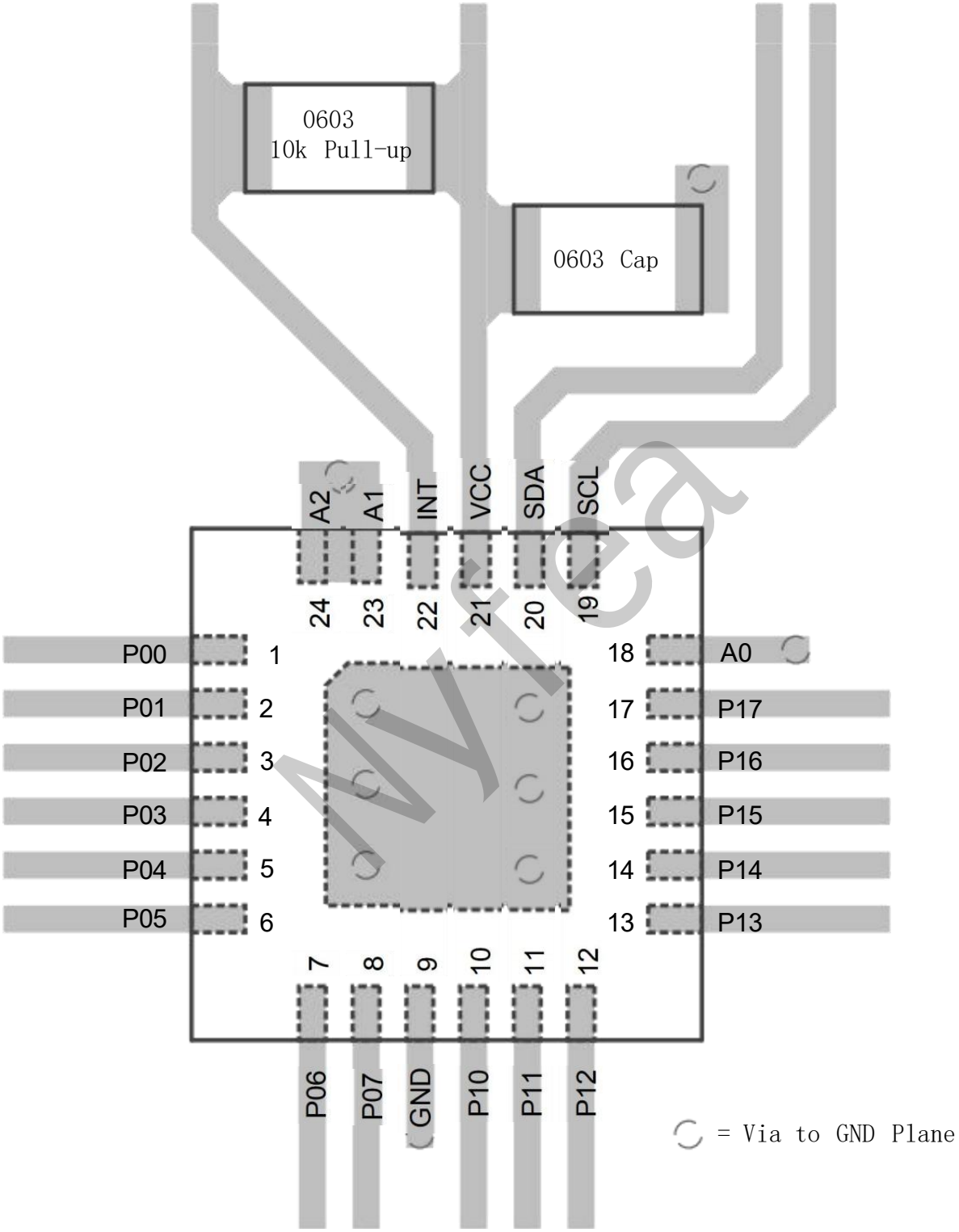


Figure 10. High Current-Drive Load Application

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8.4 Layout Example

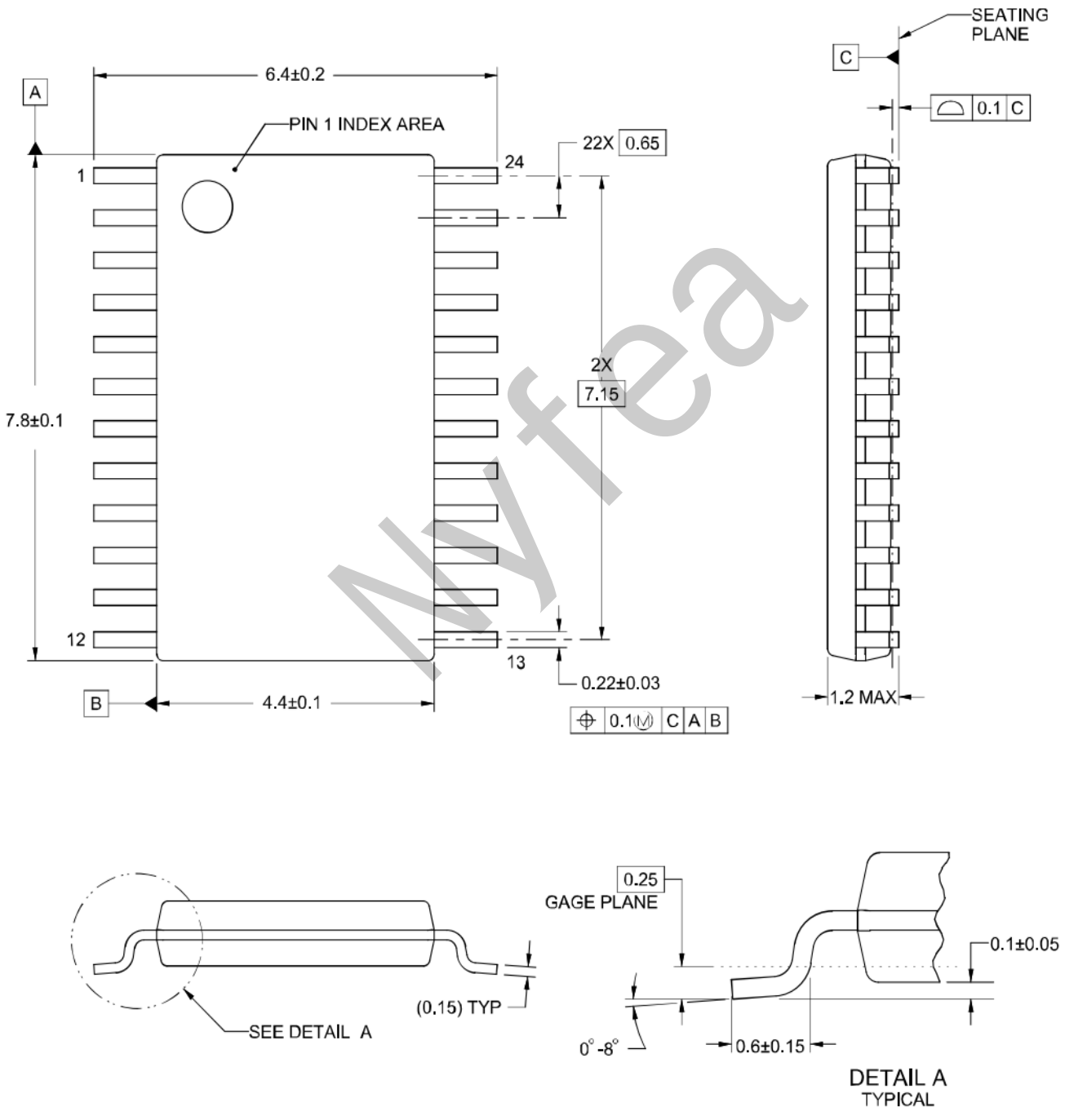


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9 Packaging Information

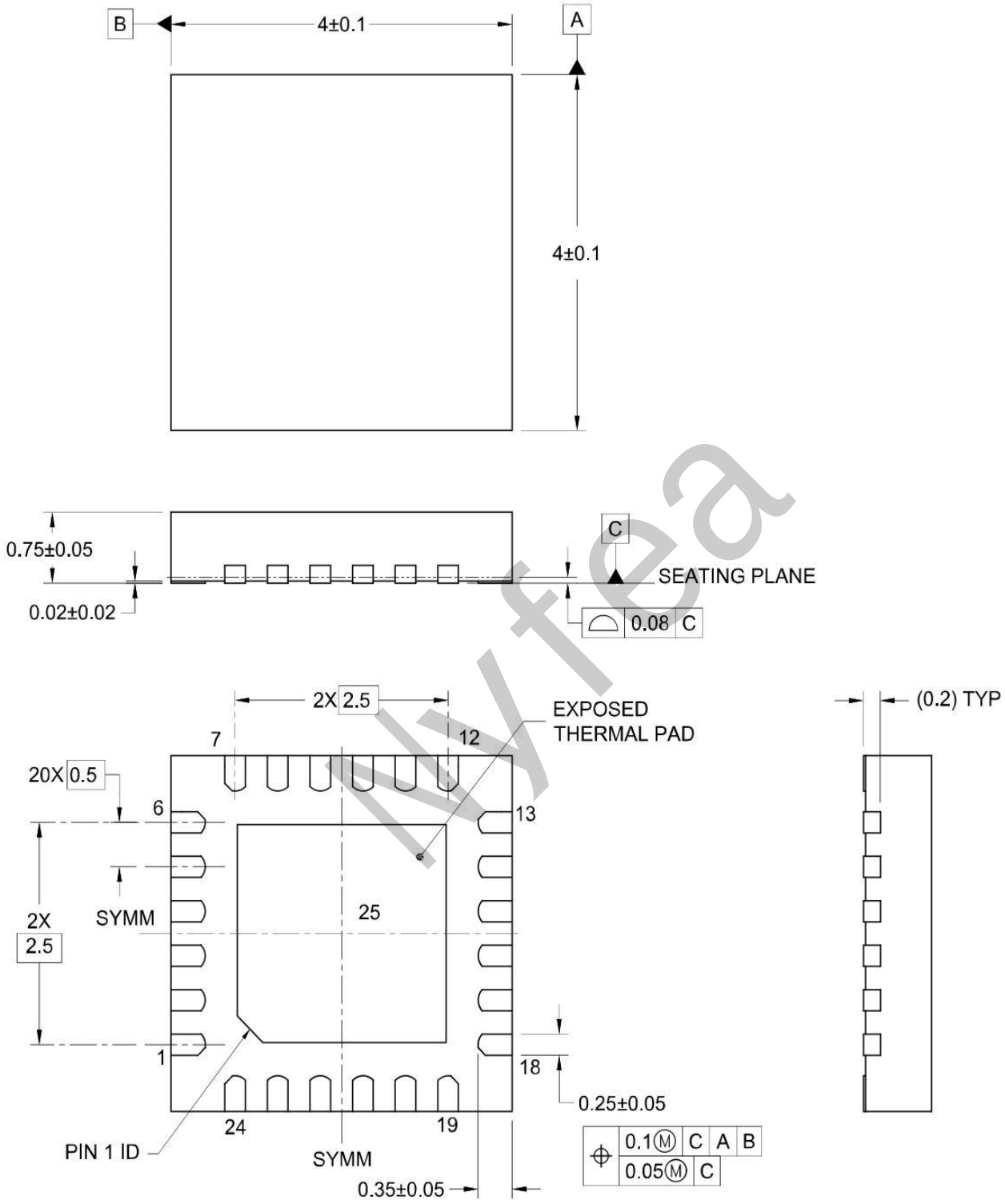
All dimensions mentioned below are in millimeters.

9.1 Package Outline (TSSOP.24)



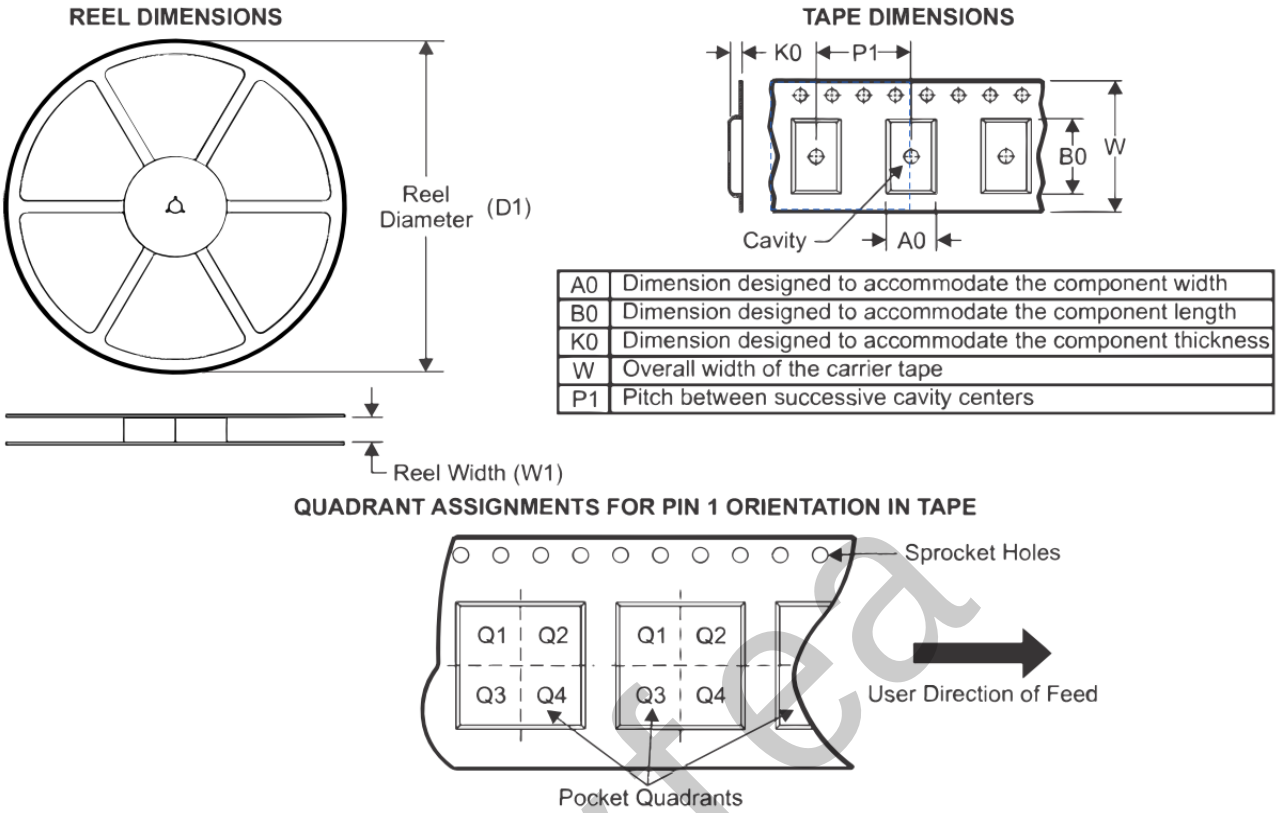
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9.2 Package Outline (WQFN.24)



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9.3 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

PACKAGE	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1
TSSOP-24	330	16.4	6.80	8.30	1.60	8.00	16.00	Q1
WQFN-24	329	12.4	4.30	4.30	1.10	8.00	12.00	Q1

Note: All dimensions mentioned above are in millimeters.

10 Ordering Information

ORDER CODE	DEVICE	PACKAGE	QUANTITY	NOTES
FCA9555T-T&R	FCA9555T	TSSOP (24)	4000	Tape&Reel
FCA9555Q-T&R	FCA9555Q	WQFN (24)	4000	Tape&Reel

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