MCP Specification

221FBGA, 11.5x13x1.0mmt
32GB eMMC + 24Gb (8Gb*3) TDP LPDDR3 SDRAM

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datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- Final datasheet	16th Apr. 2019	Final	S.H.Kim

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1. FEATURES

<Common>
• Operating Temperature : -25°C ~ 85°C
• Package : 221Ball FBGA Type - 11.5mm x 13mm x 1.0mmt
0.5mm ball pitch

<eMMC>
• embedded MultiMediaCard Ver. 5.1 compatible.
• SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard.
- Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types.
- Non-supported Features : Large Sector Size (4KB).
• Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems).
• Data bus width : 1bit (Default), 4bit and 8bit.
• MMC I/F Clock Frequency : 0 ~ 200MHz
MMC I/F Boot Frequency : 0 ~ 52MHz
• Power : Interface power → V_{CCQ} (1.70V ~ 1.95V or 2.7V ~ 3.6V), Memory power → V_{CC} (2.7V ~ 3.6V)

<LPDDR3 SDRAM>
• Double-data rate architecture; two data transfers per clock cycle
• Bidirectional data strobes (DQS_t, DQS_c), These are transmitted/received with data to be used in capturing data at the receiver
• Differential clock inputs (CK_t and CK_c)
• Differential data strobes (DQS_t and DQS_c)
• Commands & addresses entered on both positive and negative CK edges; data and data mask referenced to both edges of DQS
• 8 internal banks for concurrent operation
• Data mask (DM) for write data
• Burst Length: 8
• Burst Type: Sequential
• Read & Write latency : Refer to Table 45 LPDDR3 AC Timing Table
• Auto Precharge option for each burst access
• Configurable Drive Strength
• All Bank Refresh, Per Bank Refresh and Self Refresh
• Partial Array Self Refresh and Temperature Compensated Self Refresh
• Write Leveling
• CA Calibration
• HSUL_12 compatible inputs
• VDD1/VDD2/VDDQ/VDDCA
: 1.8V/1.2V/1.2V / 1.2V
• No DLL : CK to DQS is not synchronized
• Edge aligned data output, center aligned data input
• On Die Termination using ODT pin
• 2/CS, 2CKE

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[Table 1] LPDDR3 SDRAM Addressing

Items		8Gb
Number of Banks		8
Bank Addresses		BA0-BA2
t_{REFI}(us) 2)		3.9
×16	Row Addresses 3)	R0-R14
	Column Addresses 1), 3)	C0-C10
×32	Row Addresses 3)	R0-R14
	Column Addresses 1), 3)	C0-C9

NOTE :
1) The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
2) t_{REFI} values for all bank refresh is Tc = -25~85°C, Tc means Operating Case Temperature
3) Row and Column Address values on the CA bus that are not used are “don’t care.”

2. GENERAL DESCRIPTION

The KMGX6001BA is a Multi Chip Package Memory which combines 32GB eMMC and 24Gb(8Gb*3) TDP LPDDR3 SDRAM.

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard.
eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance.
There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.
The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

LPDDR3 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

The KMGX6001BA suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 221-ball FBGA Type.

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3. PIN CONFIGURATION

221Ball FBGA														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DNU	VSF	VSS_m	VCCQ_m	DAT6_m	CMD_m	RCLK_m	VSS_m	DAT0_m	DAT5_m	VDDI_m	VSS_m	VSF	DNU
B	VSF	VSS_m	VCC_m	DAT7_m	DAT3_m	VCCQ_m	VSS_m	CLK_m	VCCQ_m	DAT1_m	VSS_m	VCC_m	VCC_m	VSF
C		RST_m	VSS_m	VCC_m	VSS_m	DAT2_m	VCCQ_m	VSS_m	DAT4_m	VSS_m	VCCQ_m	VSS_m	VSS_m	
D		VSF	VSF	VSF	VSF	VSF	VSS_m	VCC_m						
E														
F		VSS_v	VDD1_v	VDD1_v	VDD2_v			VDD2_v	VDD1_v	DQ29_v	DQ30_v	DQ31_v	VSSQ_v	
G		ZQ0_v	ZQ1_v	VSS_v	VDD1_v			VSS_v	VDDQ_v	DQ26_v	VSSQ_v	DQ27_v	DQ28_v	
H		CA9_v	VSS_v	VSSCA_v	VSS_v			VDDQ_v	DQS3_t_v	VSSQ_v	DQ24_v	VDDQ_v	DQ25_v	
J		CA8_v	CA7_v	VSSCA_v	VDD2_v			VSSQ_v	DQS3_c_v	DM3_v	VDDQ_v	DQ15_v	VSSQ_v	
K		VDDCA_v	CA6_v	VSSCA_v	VDD2_v			VSSQ_v	VSSQ_v	VDDQ_v	DQ13_v	VDDQ_v	DQ14_v	
L		VDD2_v	CA5_v	VSS_v	VDD2_v			VDDQ_v	VDDQ_v	VSSQ_v	DQ12_v	VSSQ_v	DQ11_v	
M		VREF(CA)_v	VSS_v	VSS_v	VDD2_v			VSSQ_v	DQS1_t_v	VDDQ_v	DQ10_v	VDDQ_v	DQ9_v	
N		VDDCA_v	CK_c_v	VSS_v	VDD2_v			VSS_v	DQS1_c_v	DM1_v	VDDQ_v	DQ8_v	VSSQ_v	
P		VSSCA_v	CK_t_v	VSS_v	VDD2_v			VDD2_v	VSSQ_v	ODT1)	VDD2_v	VSS_v	VREF(DQ)_v	
R		CKE1_v	VSS_v	VSS_v	VDD2_v			VSS_v	DQS0_c_v	DM0_v	VDDQ_v	DQ7_v	VSSQ_v	
T		CKE0_v	CS1_c_v	VSS_v	VDD2_v			VSSQ_v	DQS0_t_v	VDDQ_v	DQ5_v	VDDQ_v	DQ6_v	
U		VDDCA_v	CS0_c_v	VSSCA_v	VDD2_v			VDDQ_v	VDDQ_v	VSSQ_v	DQ3_v	VSSQ_v	DQ4_v	
V		VDDCA_v	CA4_v	VSSCA_v	VDD2_v			VSSQ_v	VSSQ_v	VDDQ_v	DQ1_v	VDDQ_v	DQ2_v	
W		CA2_v	CA3_v	VSSCA_v	VDD2_v			VSSQ_v	DQS2_c_v	DM2_v	VDDQ_v	DQ0_v	VSSQ_v	
Y		CA0_v	CA1_v	VSS_v	VSS_v			VDDQ_v	DQS2_t_v	VSSQ_v	DQ23_v	VDDQ_v	DQ22_v	
AA	DNU	VSS_v	VDD1_v	VSS_v	VDD1_v			VSS_v	VDDQ_v	DQ21_v	VSSQ_v	DQ20_v	DQ19_v	DNU
AB	DNU	DNU	VDD1_v	VDD1_v	VDD2_v			VDD2_v	VDD1_v	DQ18_v	DQ17_v	DQ16_v	DNU	DNU

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221 FBGA: Top View (Ball Down)

	LPDDR3		Ground
	eMMC		ODT
	Power		DNU / VSF

NOTE :
1) In case ODT function is not used, ODT pin should be considered as NC.
ODT will be connected to rank 0. The ODT Input to rank 1 (if 2nd rank is present) will be connected to Ground in the package.

4. PIN DESCRIPTION

Pin Name	Pin Function (eMMC)
DAT0_m~DAT7_m	Data Input / Output
CLK_m	Clock
RCLK_m	Data Strobe
CMD_m	Command
RST_m	Reset
VCC_m	Power Supply for Flash
VCCQ_m	Power Supply for Controller
VDDI_m	External Capacitance for Internal power stability
VSS_m	Ground for Controller/Flash

Pin Name	Pin Function (LPDDR3)
CK_t_v, CK_c_v	System Differential Clock
CKE0_v, CKE1_v	Clock Enable
CS0_c_v, CS1_c_v	Chip Selection
CA0_v ~ CA9_v	Command / Address Inputs
DM0_v ~ DM3_v	Data Input / Output Mask
DQS0_t_v ~ DQS3_t_v	Data Strobe Bi-directional
DQS0_c_v ~ DQS3_c_v	Data Strobe Complementary
DQ0_v ~ DQ31_v	Data Input / Output
VDD1_v	Core Power Supply 1
VDD2_v	Core Power Supply 2
VDDCA_v	Input Receiver Power Supply
VDDQ_v	I/O Power Supply
VREF(CA)_v	Reference Voltage for CA Input Receiver
VREF(DQ)_v	Reference Voltage for DQ Input Receiver
VSS_v	Ground
VSSCA_v	Ground for CA Input Receivers
VSSQ_v	I/O Ground
ZQ0_v, ZQ1_v	Reference Pin for Output Drive Strength Calibration
ODT	On die termination

Pin Name	Pin Function
DNU	Do Not Use
VSF	Vendor Specific Function

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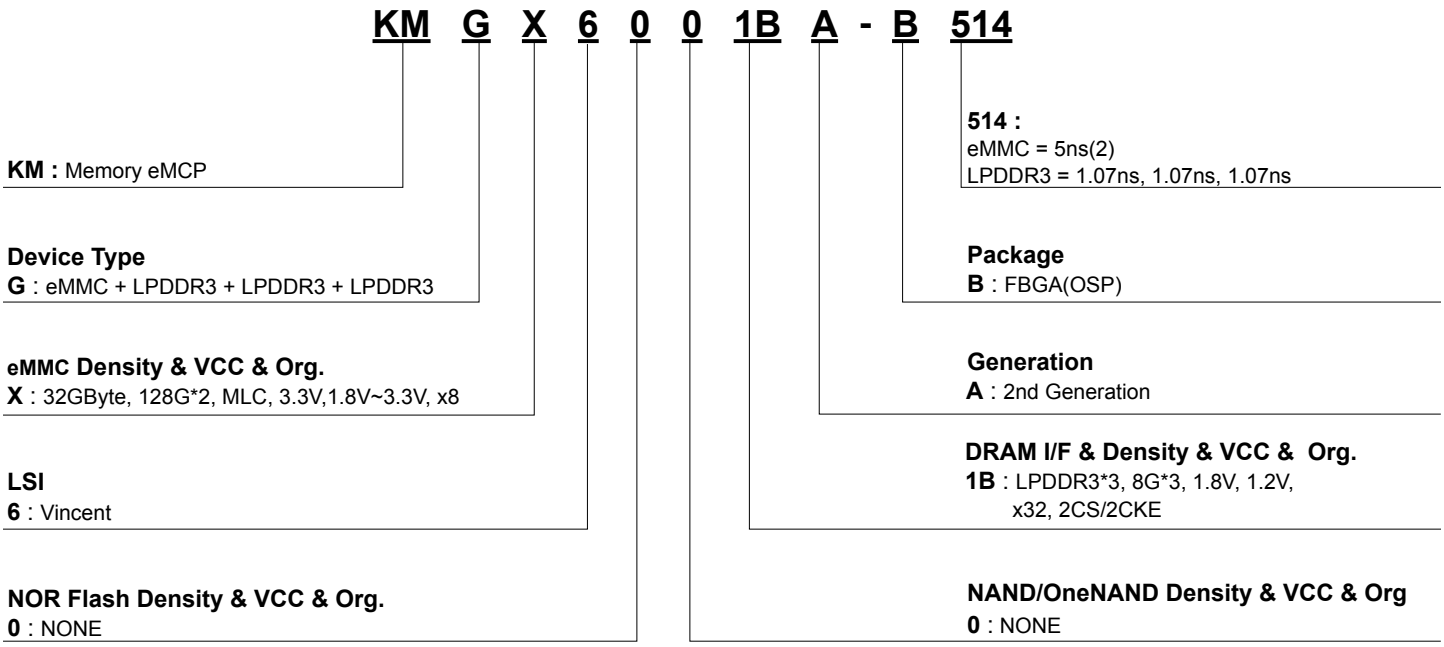
5. ORDERING INFORMATION



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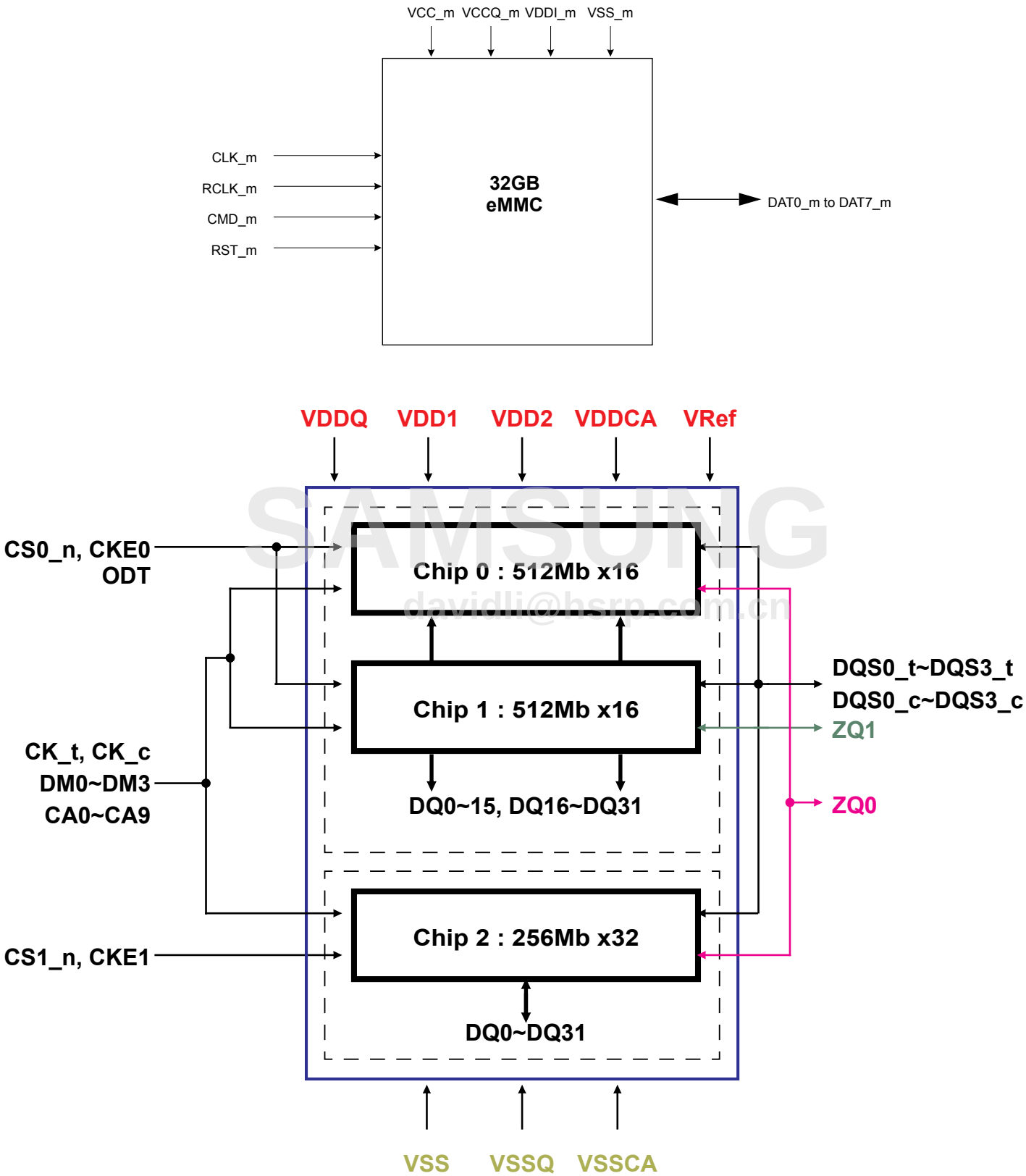
6. FUNCTIONAL BLOCK DIAGRAM



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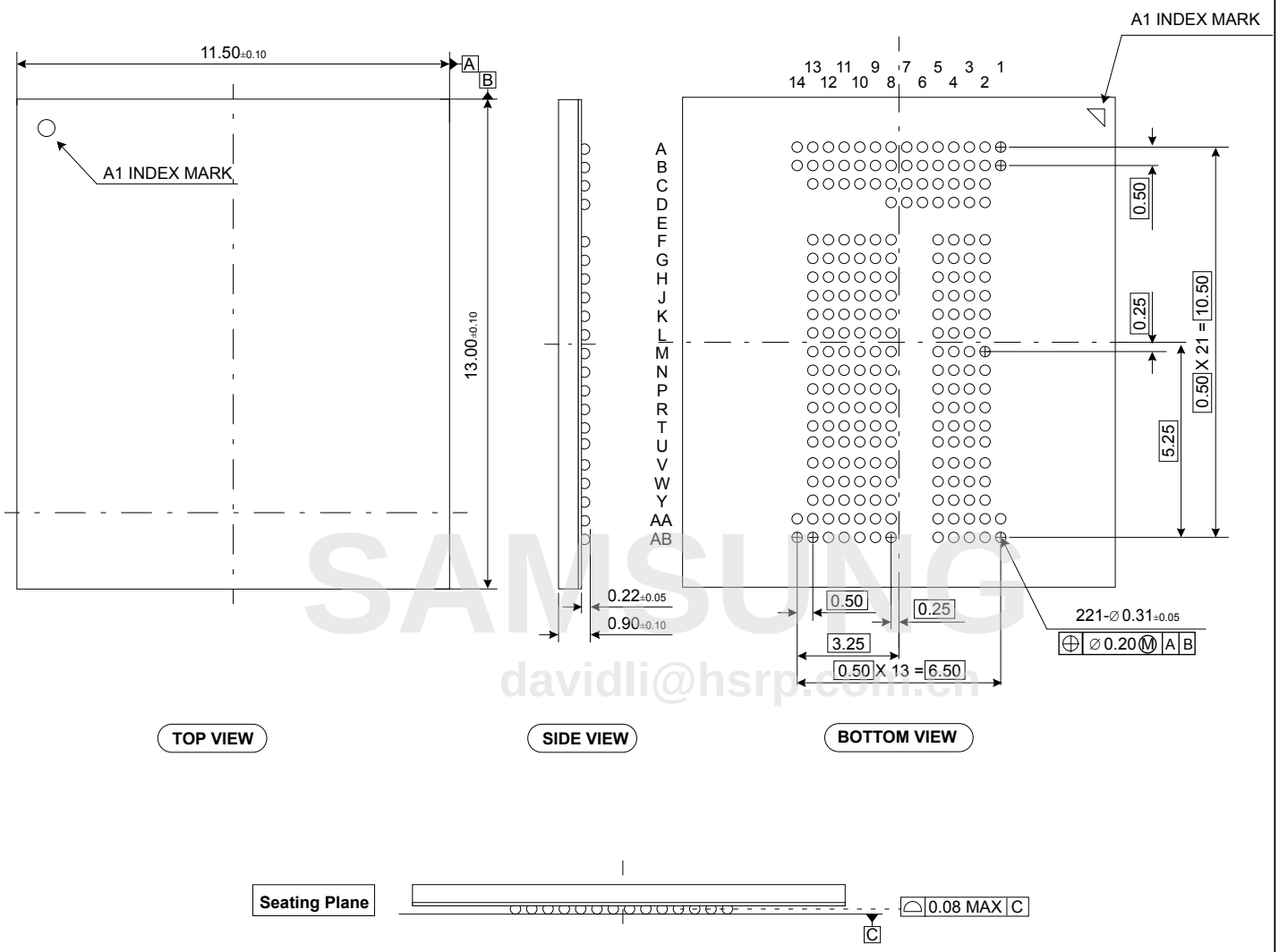
7. PACKAGE DIMENSION

221-Ball Fine pitch Ball Grid Array Package (measured in millimeters)

Units:millimeters



NOTE

1. 221 x ∅0.31 Dimensions apply to solder balls post reflow. Pre-reflow diameter is 0.30mm.

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32GB eMMC

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1.0 Product Architecture

- eMMC consists of NAND Flash and Controller. V_{CCQ} is for Controller power and V_{CC} is for flash power.

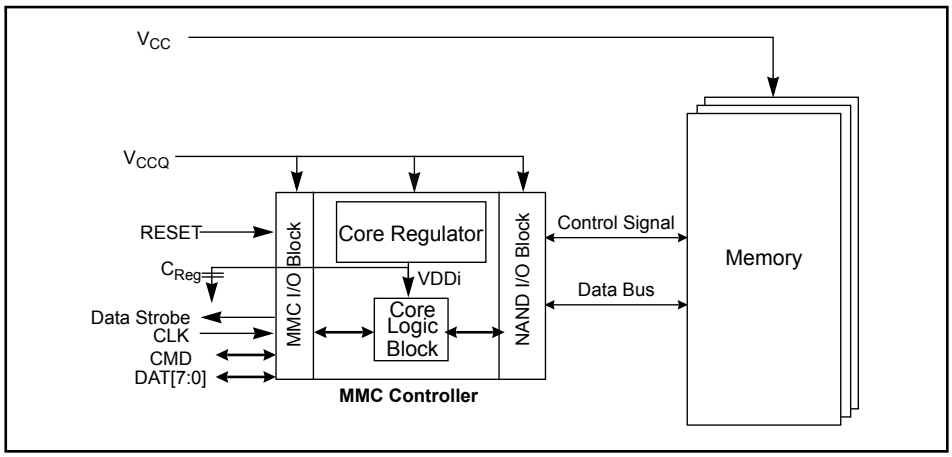

Figure 1. eMMC Block Diagram

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2.0 HS400 MODE

eMMC 5.1 product supports high speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply.
HS400 mode supports the following features:

- DDR Data sampling method
- CLK frequency up to 200MHz DDR (up to 400Mbps)
- Only 8-bits bus width available
- Signaling levels of 1.8V
- Six selectable Drive Strength (refer to the table below)

[Table 1] I/O Driver Strength Types

Driver Type	HS200 & HS400 Support	Nominal Impedance	Approximated Driving Capability Compared to Type-0	Remark
0	Default	50Ω	x1	Default Driver Type. Supports up to 200MHz operation.
1	Optional	33Ω	x1.5	Supports up to 200MHz Operation.
2	Optional	66Ω	x0.75	The weakest driver that supports up to 200MHz operation.
3	Optional	100Ω	x0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design.
4	Optional	40Ω	x1.2	Supports up to 200MHz DDR operation

NOTE :
1) Support of Driver Type-0 is default for HS200 & HS400 Device, while supporting Driver types 1~4 are optional for HS200 & HS400 Device.

[Table 2] Device Type Values (EXT_CSD Register : DEVICE_TYPE [196])

Bit	Device Type	Supportability
7	HS400 Dual Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate eMMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate eMMC @ 52MHz - 1.8V or 3V I/O	Support
1	High-Speed eMMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed eMMC @ 26MHz - at rated device voltage(s)	Support

[Table 3] Extended CSD Revisions (EXT_CSD Register : EXT_CSD_REV [192])

Value	Timing Interface	EXT_CSD Register Value
255-8	Reserved	-
8	Revision 1.8 (for MMC V5.1)	0x08
7	Revision 1.7 (for MMC V5.0)	-
6	Revision 1.6 (for MMC V4.5, V4.51)	-
5	Revision 1.5 (for MMC V4.41)	-
4	Revision 1.4 (Obsolete)	-
3	Revision 1.3 (for MMC V4.3)	-
2	Revision 1.2 (for MMC V4.2)	-
1	Revision 1.1 (for MMC V4.1)	-
0	Revision 1.0 (for MMC V4.0)	-

[Table 4] High Speed Timing Values (EXT_CSD Register : HS_TIMING [185])

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

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3.0 NEW eMMC 5.1 FEATURES

3.1 Overview

[Table 5] Overview

New Feature	JEDEC	Support
Cache Flushing Report	Mandatory	Yes
Background operation control	Mandatory	Yes
Command Queuing	Optional	Yes
Enhanced Strobe	Optional	Yes
RPMB Throughput improve	Optional	Yes
Secure Write Protection	Optional	Yes

3.2 Command Queuing

To facilitate command queuing in eMMC, the device manages an internal task queue that the host can queue during data transfer tasks.

Every task is issued by the host and initially queued as pending. The device works to prepare pending tasks for execution. When a task is ready for execution, its state changes to “ready for execution”.

The host tracks the state of all queued tasks and may order the execution of any task, marked as “ready for execution”, by sending a command indicating its task ID. The device executes the data transfer transaction after receiving the execute command (CMD46/CMD47).

3.2.1 CMD Set Description

[Table 6] CMD Set Description and Details

CMD	Type	Argument	Abbreviation	Purpose
CMD44	ac/R1	[31] Reliable Write Request [30] DAT_DIR - "0" write / "1" read [29] tag request [28:25] context ID [24] forced programming [23] Priority: “0” simple / “1” high [20:16] TASK ID [15:0] number of blocks	QUEUED_TASK _PARAMS	Define direction of operation (Read or Write) and Set high priority CMD Queue with task ID
CMD45	ac/R1	[31:0] Start block address	QUEUED_TASK_ADDRESS	Indicate data address for Queued CMD
CMD46	adtc/R1	[20:16] TASK ID	EXECUTE_READ_TASK	(Read) Transmit the requested number of data blocks
CMD47	adtc/R1	[20:16] TASK ID	EXECUTE_WRITE_TASK	(Write) Transmit the requested number of data blocks
CMD48	ac/R1b	[20:16] Task ID [3:0] TM op-code	CMDQ_TASK _MGMT	Reset a specific task or entire queue. [20:16] when TM op-code = 2h these bits represent TaskID. When TM op-code = 1h these bits are reserved."

3.2.2 New Response : QSR (Queue Status Register)

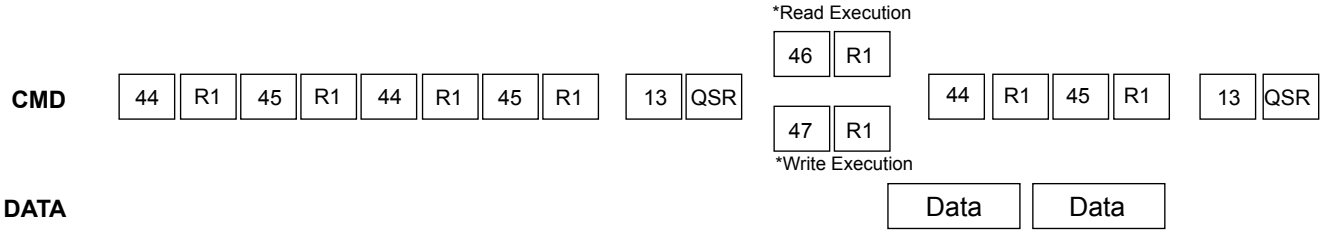
The 32-bit Queue Status Register (QSR) carries the state of tasks in the queue at a specific point in time. The host has read access to this register through device response to SEND_STATUS command (CMD13 with bit[15]=”1”), R1’s argument will be the 32- bit Queue Status Register (QSR). Every bit in the QSR represents the task who’s ID corresponds to the bit index. If bit QSR[i] = “0”, then the queued task with a Task ID i is not ready for execution. The task may be queued and pending, or the Task ID is unused. If bit QSR[i] = “1”, then the queued task with Task ID i is ready for execution.

3.2.3 Send Status : CMD13

CMD13 for reading the Queue Status Register (QSR) by the host. If bit[15] in CMD13’s argument is set to 1, then the device shall send an R1 Response with the QSR instead of the Device Status. * There is still legacy CMD13 with R` response.

3.2.4 Mechanism of CMD Queue Operation

Host issues CMD44 with Task ID number, Sector, Count, Direction, Priority to the device followed by CMD45 and host checks the Queue Status check with CMD13 [15]bits to 1. After that host issues CMD46 for Read or CMD47 for write During CMD queue operation, CMD44/CMD45 is able to be issued at anytime when the CMD line is not in use.



3.2.5 CMD Queue Register Description

Configuration and capability structures shall be added to the EXT_CSD register, as described below.

[Table 7] CMD Queuing Support (EXT_CSD Register : CMDQ_SUPPORT [308])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field indicates whether the device supports command queuing or not.

0x0: CMD Queue function is not supported.
0x1: CMD Queue function is supported.

[Table 8] Command Queue Mode Enable (EXT_CSD Register : CMDQ_MODE_EN [15])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							0x00

This field is used by the host enable command queuing.

0x0: Queue function is not enabled.
0x1: Queue function is enabled.

[Table 9] CMD Queuing Depth (EXT_CSD Register : CMDQ_DEPTH [307])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved			0x0F				

This field is used to calculate the depth of the queue supported by the device.

Bit encoding:
[7:5]: Reserved.
[4:0]: N,a parameter used to calculate the Queue Depth of task queue in the device.
Queue Depth = N+1.

3.3 Enhanced Strobe Mode

This product supports Enhanced Strobe in HS400 mode and refer to the details as described in eMMC5.1 JEDEC standard.

3.4 RPMB Throughput Improve

[Table 10] Related Parameter Register in EXT_CSD : WR_REL_PARAM [166]

Name	Field	Bit	Type
Enhanced RPMB Reliable Write	EN_RPMB_REL_WR	4	R

Bit[4]: EN_RPMB_REL_WR(R)
0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).
0 x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame) or 8KB (Thirthy two 512B frames).

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3.5 Secure Write Protection

Configuration and capability structures shall be added to the EXT_CSD register and Authenticated Device Configuration Area as described below.

[Table 11] Parameter Register in EXT_CSD : SECURE_WP_INFO [211]

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved						SECURE_WP_EN_STATUS	SECURE_WP_SUPPORT

Bit[7:2]: Reserved.
Bit[1]: SECURE_WP_EN_STATUS(R)
0x0: Legacy Write Protection mode.
0x1: Secure Write Protection mode.
Bit[0]: SECURE_WP_SUPPORT(R)
0x0: Secure Write Protection is NOT supported by this device.
0x1: Secure Write Protection is supported by this device.

[Table 12] Authenticated Device Configuration Area[1] : SECURE_WP_MODE_ENABLE

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved							0x00

Bit[7:1] : Reserved.
Bit[0] : SECURE_WP_EN (R/W/E)
The default value of this field is 0x0.

• 0x0 : Legacy Write Protection mode, i.e., TMP_WRITE_PROTECT[12],
PERM_WRITE_PROTECT[13] is updated by CMD27. USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are updated by CMD6.

• 0x1 : Secure Write Protection mode. The access to the write protection related EXT_CSD and
CSD fields depends on the value of SECURE_WP_MASK bit in SECURE_WP_MODE_CONFIG field.

[Table 13] Authenticated Device Configuration Area[2] : SECURE_WP_MODE_CONFIG

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved							0x00

Bit[7:1] : Reserved.
Bit[0] : SECURE_WP_MASK (R/W/E_P)
The default value of this field is 0x0.

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• 0x0: Disabling updating WP related EXT_CSD and CSD fields. CMD27 (Program CSD) will generate generic error for setting TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13]. CMD6 for updating USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] generates SWITCH_ERROR. If a force erase command is issued, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. If CMD28 or CMD29 is issued, then generic error will be occurred. Power-on Write Protected boot partitions will keep protected mode after power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

• 0x1: Enabling updating WP related EXT_CSD and CSD fields. I.e TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13] , USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are accessed using CMD6, CMD8 and CMD27.
If a force erase command is issued and accepted, then ALL THE DEVICE CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked Device will get unlocked. If a force erase command is issued and power-on protected or a permanently-write-protected write protect groups exist on the device, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. An attempt to force erase on an unlocked Device will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register. Write Protection is applied to the WPG indicated by CMD28 with the WP type indicated by the bit[2] and bit[0] of USER_WP[171]. All temporary WP Groups and power-on Write Protected boot partitions become writable/erasable temporarily which means write protect type is not changed. All power-on and permanent WP Groups in user area will not become writable/erasable temporarily. Those temporarily writable/erasable area will become write protected when this bit is cleared to 0x0 by the host or when there is power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

4.0 TECHNICAL NOTES

4.1 S/W Algorithm

4.1.1 Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

4.1.1.1 Enhanced Partition (Area)

SAMSUNG eMMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 2MB user data area is needed to generate 1MB enhanced area).

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512K Bytes).

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4.1.2 Boot Operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

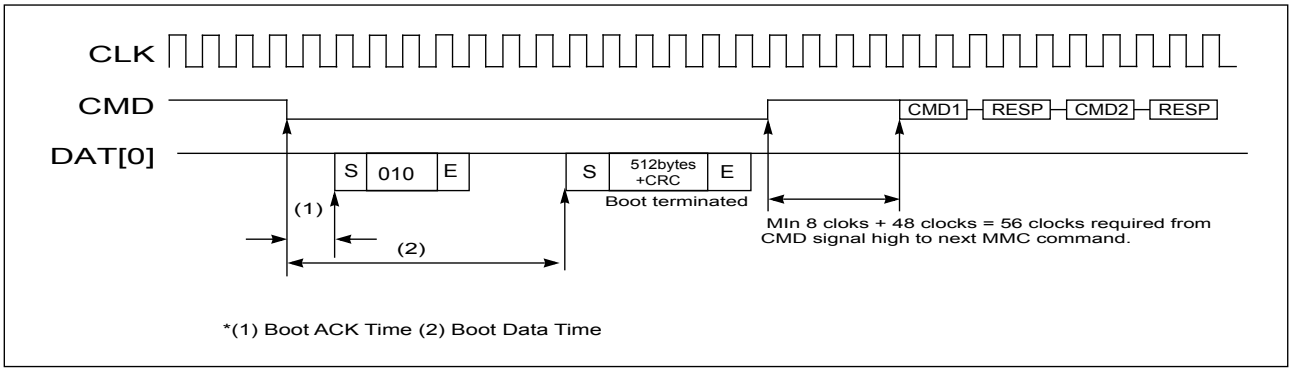

Figure 2. embedded MultiMediaCard State Diagram (Boot Mode)

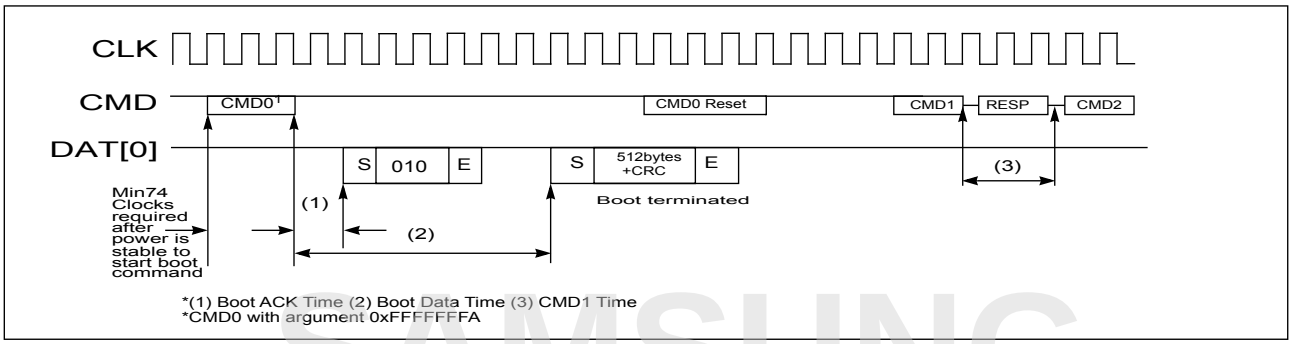

Figure 3. embedded MultiMediaCard State Diagram (Alternative Boot Mode)

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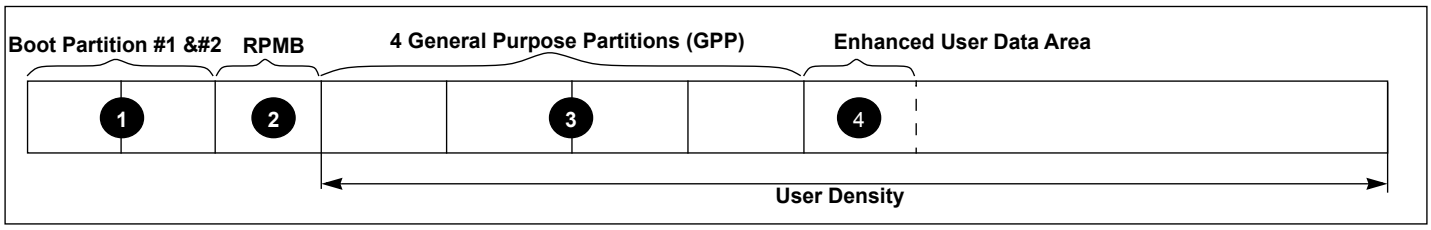
[Table 14] Boot ACK, Boot Data and Initialization Time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 100 ms
(3) Initialization Time[1)]	< 3 secs

NOTE :
1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 6.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 1sec.

4.1.3 User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 64MB in MLC.
This results in decreasing of user density.



[Table 15] Capacity According to Partition

		Boot Partition 1	Boot Partition 2	RPMB
32GB	Default	4,096KB	4,096KB	4,096KB
	Max	4,096KB	4,096KB	4,096KB

[Table 16] Maximum Enhanced Partition Size

Device	Max Enhanced Partition Size
32 GB	15,627,976,704 Byte

[Table 17] User Density Size

Device	User Density Size
32 GB	31,268,536,320 Byte

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4.1.4 Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion.

[Table 18] Auto Power Saving Mode and Exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

[Table 19] Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
Goto Sleep Time	< 1ms	< 1ms

4.1.5 Performance

[Table 20] Performance

Density	Sequential Read	Sequential Write	Unit
32 GB	330	100	MB/s

NOTE :
Test Condition : Bus width x8, HS400, 512KB data transfer, w/o file system overhead, measured on Samsung's internal board.

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5.0 REGISTER VALUE

5.1 OCR Register

The 32-bit operation conditions register stores the V_{CCQ} voltage profile of the eMMC. In addition, this register includes a status information bit. This status bit is set if the eMMC power up procedure has been finished. The OCR register shall be implemented by all eMMCs.

[Table 21] OCR Register

OCR bit	VCCQ Voltage Window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode) -[*Higher than 2GB only]
[31]	eMMC power up status bit (busy)[1]	

NOTE :
1) This bit is set to LOW if the eMMC has not finished the power up routine.
2) The voltage for internal flash memory(V_{CC}) should be 2.7-3.6v regardless of OCR Register value.

5.2 CID Register

[Table 22] CID Register

Name	Field	Width	CID Slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	___[1]
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	___[2]
Product serial number	PSN	32	[47:16]	___[3]
Manufacturing date	MDT	8	[15:8]	___[4]
CRC7 checksum	CRC	7	[7:1]	___[5]
not used, always '1'	-	1	[0:0]	---

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NOTE :
1),4),5) description are same as eMMC JEDEC standard.
2) PRV is composed of the revision count of controller and the revision count of F/W patch.
3) A 32 bits unsigned binary integer. (Random Number)

5.2.1 Product Name Table (In CID Register)

[Table 23] Product Name Table

Part Number	Density	Product Name in CID Register (PNM)
KMGX6001BA-B514	32 GB	0 x 475836424142

5.3 CSD Register

The Card-Specific Data register provides information on how to access the eMMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:
R: Read only.
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 24] CSD Register

Name	Field	Width	Cell Type	CSD Slice	CSD Value
					32 GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Device command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00
Reserved	-	2	R	[75:74]	-
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x06
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x06
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x06
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x06
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x03
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	-	4	R	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	0x06
Not used, always'1'	-	1	—	[0:0]	1

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5.4 Extended CSD Register

The Extended CSD register defines the eMMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the eMMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the eMMC is working in. These modes can be changed by the host by means of the SWITCH command.

R: Read only.
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable

[Table 25] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD Slice	CSD Value
					32GB
Properties Segment					
Reserved[1)]		6	-	[511:506]	-
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x02
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported modes	SUPPORTED_MODES	1	R	[493]	0x03
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operation codes timeout	OPERATION_CODE_TIME-OUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	0xC7810000
Barrier support	BARRIER_SUPPORT	1	R	[486]	0x00
Reserved[1)]		177	-	[485:309]	-
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x01
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x0F
Reserved[1)]		1	-	[306]	-
Number of FW sectors correctly programmed	NUMBER_OF_FW_SEC-TORS_CORRECTLY_PRO-GRAMMED	4	R	[305:302]	0x00
Vendor proprietary health report	VENDOR_PROPRI-ETARY_HEALTH_REPORT	32	R	[301:270]	0x00
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x01
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x00
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x10
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01

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Device version	DEVICE_VERSION	2	R	[263:262]	0x00
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	0x01
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x10000
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SEC-TORS_NUM	4	R	[245:242]	0x00
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Cache flush policy	CACHE_FLUSH_POLICY	1	R	[240]	0x00
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200MHz at V_{CCQ}=1.95V, V_{CC}=3.6V	PWR_CL_200_360	1	R	[237]	0x00
Power class for 200MHz, at V_{CCQ}=1.3V, V_{CC}=3.6V	PWR_CL_200_195	1	R	[236]	0x00
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved[1)]		1	-	[233]	-
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved[1)]		1	-	[227]	-
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	0x07
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x07
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x07
Production state awareness timeout	PRODUC-TION_STATE_AWARENESS_-TIMEOUT	1	R	[218]	0x00
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x07
Sector Count	SEC_COUNT	4	R	[215:212]	0x3A3E000
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00

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Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved[1)]		1	-	[204]	-
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x02
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x0A
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Device type	DEVICE_TYPE	1	R	[196]	0x57
Reserved[1)]		1	-	[195]	-
CSD structure	CSD_STRUCTURE	1	R	[194]	0x02
Reserved[1)]		1	-	[193]	-
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x08
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved[1)]		1	-	[190]	-
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved[1)]		1	-	[188]	-
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved[1)]		1	-	[186]	-
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x01
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x01
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved[1)]		1	-	[182]	-
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved[1)]		1	-	[180]	-
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved[1)]		1	-	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00
Reserved[1)]		1	-	[172]	-
User area write protection register	USER_WP	1	R/W, R/W/C_P &R/W/ E_P	[171]	0x00
Reserved[1)]		1	-	[170]	-
FW configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00

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Enable background operations handshake	BKOPS_EN	1	R/W&R/W/E	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x07
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x747
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved[1)]		1	-	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUC-TION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_-SUPPORT	1	R	[130]	0x01
Reserved[1)]		2	-	[129:128]	-
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	-
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STA-TUS	2	R	[55:54]	0x00
Extended Partitions Attribute	EXT_PARTITIONS_ATTRI-BUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STA-TUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved[1)]		2	-	[28:27]	-
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	0x00

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Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x00
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x39
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00
Reserved[1)]		15	-	[14:0]	-

NOTE :
1) Reserved bits should be read as “0”.

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6.0 AC PARAMETER

6.1 Timing Parameter

[Table 26] Timing Parameter

Timing Parameter		Max Value	Unit
Initialization Time (tINIT)	Normal[1)]	1	s
	After partition setting[2)]	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		20	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout		600	ms
Partition Switching Timeout (after Init)		1	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

NOTE :
1) Normal Initialization Time without partition setting.
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in Chapter 5.4 EXT_CSD register.
3) Be advised Timeout Values specified in Table above are for testing purposes under Samsung test pattern only and actual timeout situations may vary.
4) EXCEPTION_EVENT may occur and the actual timeout values may vary due to user environment.

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6.2 Previous Bus Timing Parameters for DDR52 and HS200 mode are defined by JEDEC Standard

6.3 Bus Timing Specification in HS400 Mode

6.3.1 HS400 Device Input Timing

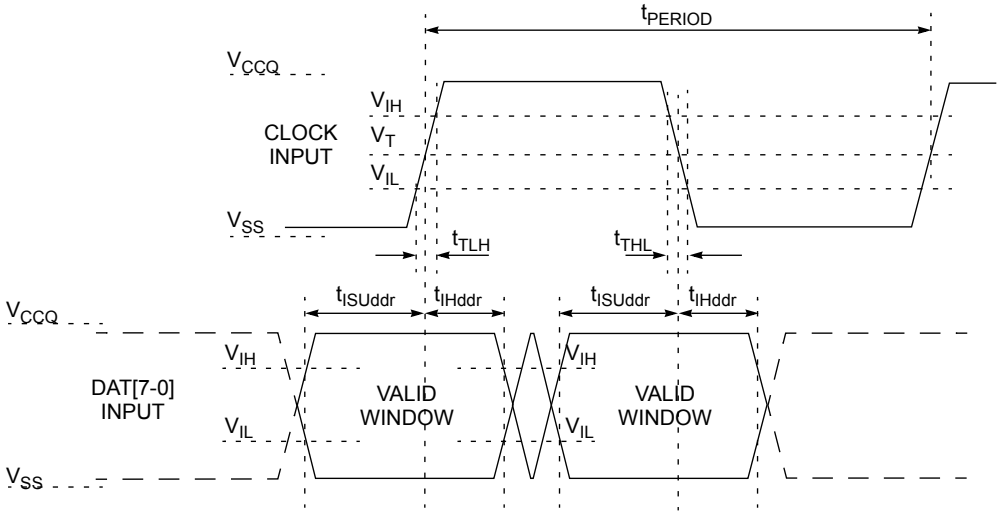

Figure 4. HS400 Device Input Timing

NOTE :
1) t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
2) V_{IH} denotes V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

[Table 27] HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit
Input CLK				
Cycle time data transfer mode	t_{PERIOD}	5		ns
Slew rate	SR	1.125		V/ns
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns
Minimum pulse width	t_{CKMPW}	2.2		ns
Input DAT (Referenced to CLK)				
Input set-up time	t_{ISUddr}	0.4		ns
Input hold time	t_{IHddr}	0.4		ns
Slew rate	SR	1.125		V/ns

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6.3.2 HS400 Device Output Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode.
The device output value of Data Strobe is “High-Z” when the device is not in outputting data (data read, CRC status response).
Data Strobe is toggled only during data read period.

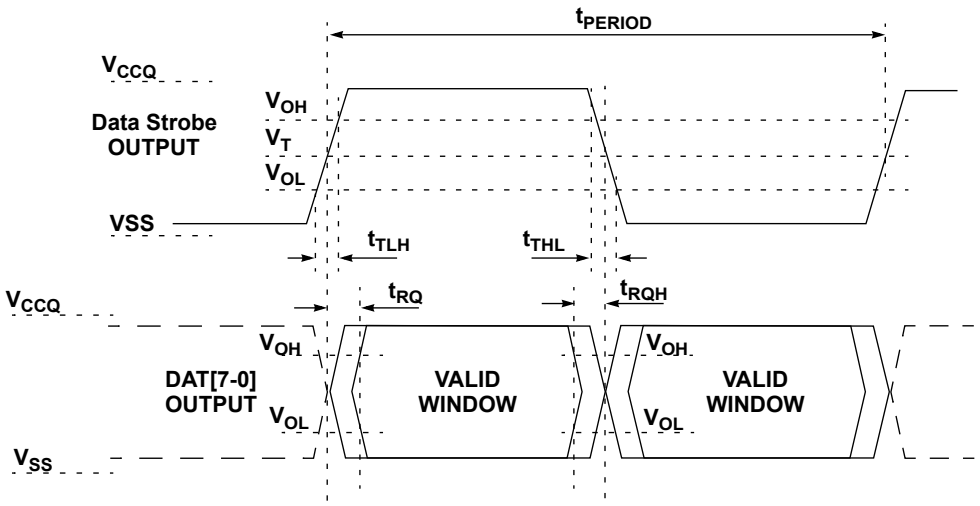

Figure 5. HS400 Device Output Timing

NOTE :
V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

[Table 28] HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit
Data Strobe				
Cycle time data transfer mode	t_{PERIOD}	5		ns
Slew rate	SR	1.125		V/ns
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns
Minimum pulse width	t_{DSMPW}	2.0		ns
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}
Output DAT (Referenced to Data Strobe)				
Output skew	t_{RQ}	-	0.4	ns
Output hold skew	t_{RQH}	-	0.4	ns
Slew rate	SR	1.125		V/ns

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6.4 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

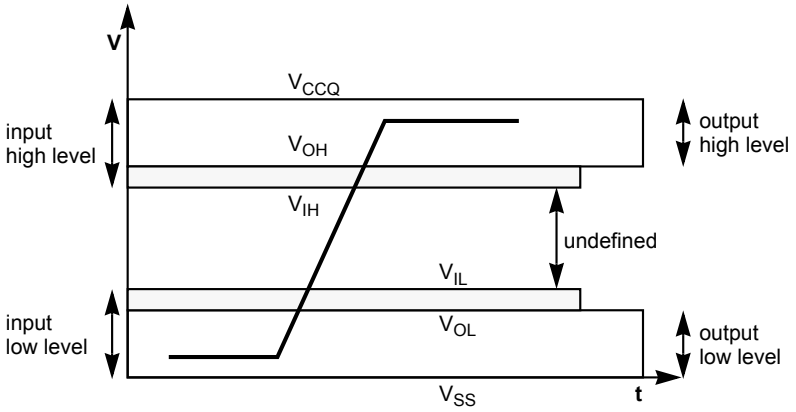

Figure 6. Bus Signal Levels

6.4.1 Open-Drain Mode Bus Signal Level

[Table 29] Open-Drain Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2	-	V	1)
Output LOW voltage	V_{OL}	-	0.3	V	I_{OL} = 2 mA

NOTE :
1) Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.

6.4.2 Push-Pull Mode Bus Signal Level eMMC

The device input and output voltages shall be within the following specified ranges for any V_{CCQ} of the allowed voltage range.

[Table 30] Push-Pull Signal Level—High-Voltage eMMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75*V_{CCQ}	-	V	I_{OH} = -100 uA@V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125*V_{CCQ}	V	I_{OL} = 100 uA@V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625*V_{CCQ}	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25*V_{CCQ}	V	-

[Table 31] Push-Pull Signal Level—1.70 - 1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45V	-	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	-	0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*V_{CCQ} 1)	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{CCQ} 2)	V	-

NOTE :
1) 0.7*V_{CCQ} for MMC4.3 and older revisions.
2) 0.3*V_{CCQ} for MMC4.3 and older revisions.

7.0 DC PARAMETER

7.1 Active Power Consumption During Operation

[Table 32] Active Power Consumption During Operation

Density	V_{CCQ}	V_{CC}	Unit
32 GB	180	100	mA

NOTE :
Power Measurement conditions: Bus configuration =x8 @HS400.
The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

7.2 Standby Power Consumption in Auto Power Saving Mode and Standby State

[Table 33] Standby Power Consumption in Auto Power Saving Mode and Standby State

Density	V_{CCQ}		V_{CC}		Unit
	25°C(Typ)	85°C	25°C(Typ)	85°C	
32 GB	120	400	50	135	uA

NOTE :
Power Measurement conditions: Bus configuration =x8, No CLK.
Typical value is measured at V_{CC}=3.3V, TA=25°C. Not 100% tested.

7.3 Sleep Power Consumption in Sleep State

[Table 34] Sleep Power Consumption in Sleep State

Density	V_{CCQ}		V_{CC}	Unit
	25°C(Typ)	85°C		
32 GB	120	400	0[1)]	uA

NOTE :
Power Measurement conditions: Bus configuration =x8, No CLK.
1) In auto power saving mode, V_{CC} power can not be turned off. However in sleep mode V_{CC} power can be turned off.

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7.4 Supply Voltage

[Table 35] Supply Voltage

Item	Min	Max	Unit
V_{CCQ}	1.70(2.7)	1.95(3.6)	V
V_{CC}	2.7	3.6	
V_{SS}	-0.5	0.5	

7.5 Bus Signal Line Load

The total capacitance C_L of each line of the eMMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 36] Bus Signal Line Load

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			12	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

[Table 37] Capacitance and Resistance for HS400 Mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	

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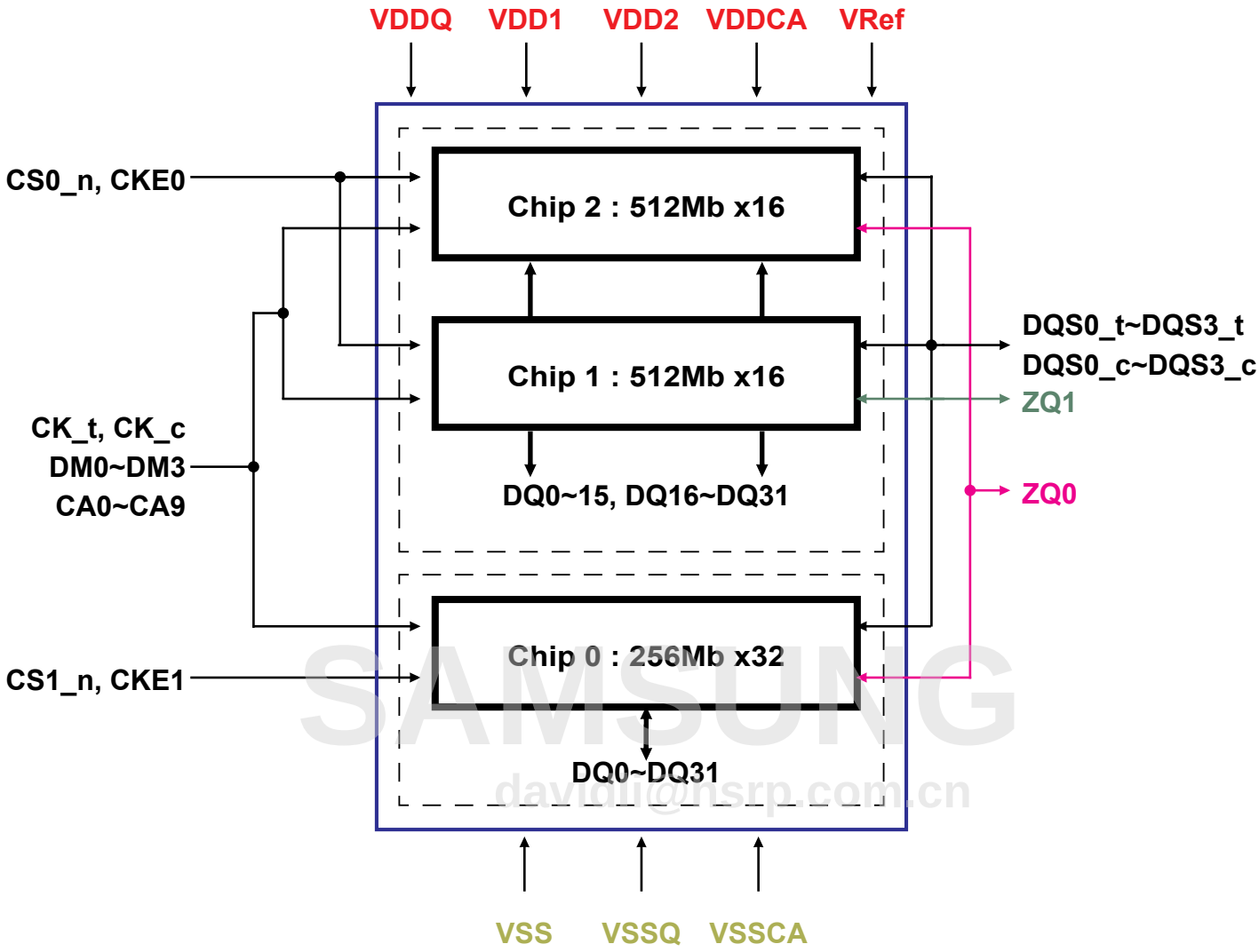
1.0 PACKAGE DIMENSION & PIN DESCRIPTION

1.1 Functional Block Diagram



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1.2 LPDDR3 Pad Definition and Description

[Table 1] Pad Definition and Description

	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth table for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. See Command Truth table for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth table for command code descriptions.
DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	**Data Inputs/Outputs:** Bi-directional data bus
DQS0_t-DQS1_t DQS0_c-DQS1_c (x16) DQS0_t-DQS3_t DQS0_c-DQS3_c (x32)	I/O	**Data Strobes (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0 - DM1 (x16) DM0 - DM3 (x32)	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7, DM1 is the input data mask signal for the data on DQ8-15. For x32 device, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
ODT	Input	**On Die Termination:** This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply.
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
$V_{REF\ (CA)}$	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF\ (DQ)}$	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for Input Receivers**
V_{SSQ}	Supply	**I/O Ground:** Ground for data input/output buffers
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

NOTE :
1) Data includes DQ and DM.

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2.0 Simplified LPDDR3 State Diagram

LPDDR3-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see datasheet of [Command Definition & Timing Diagram].

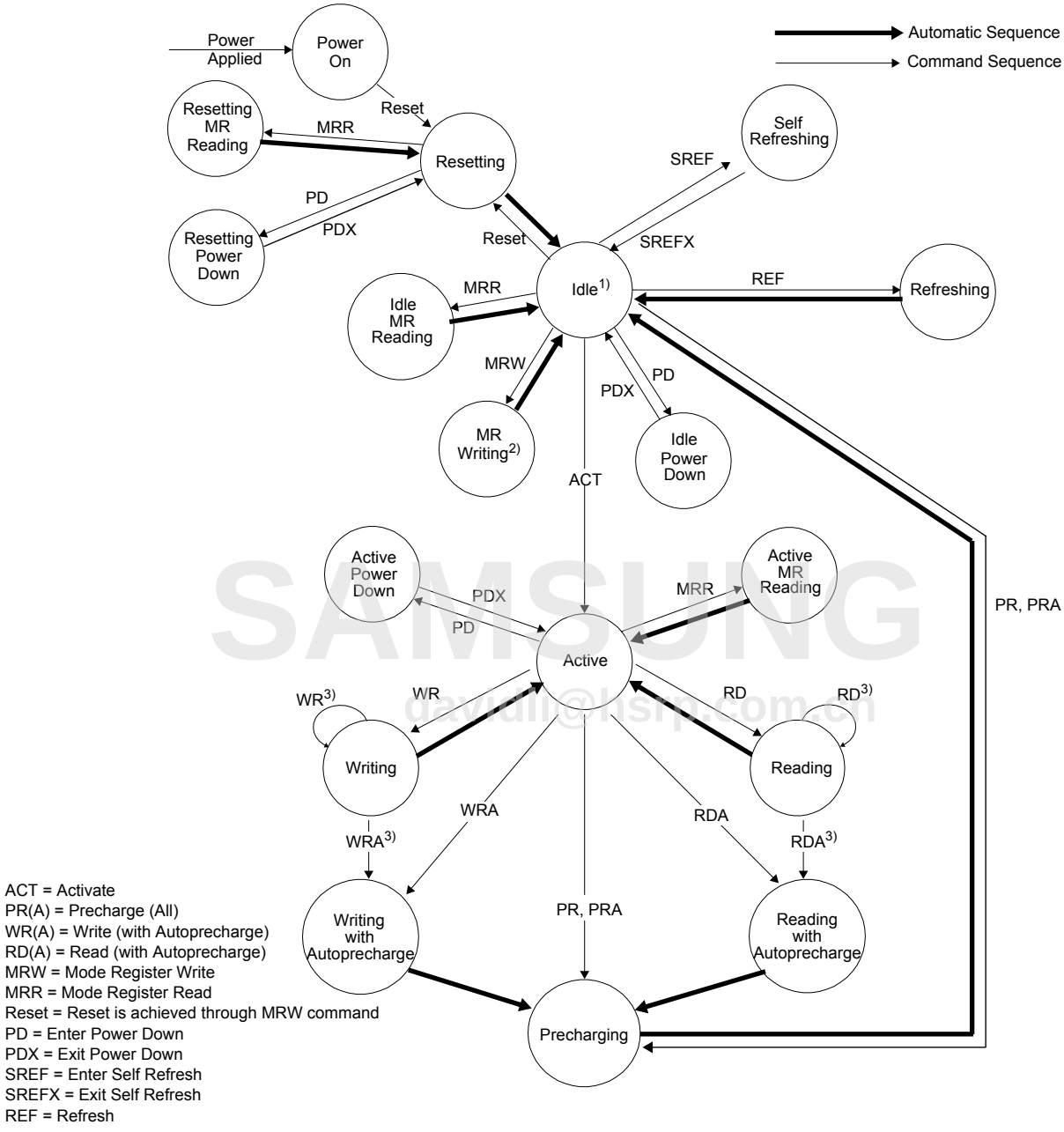

Figure 1. LPDDR3: Simplified Bus Interface State Diagram

NOTE :
1) In the Idle state, all banks are precharged.
2) In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the Idle state. See sections “CA Training” or “Write Leveling”.
3) Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.
4) Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

2.1 Mode Register Definition

2.1.1 Mode Register Assignment and Definition in LPDDR3 SDRAM

Table 2 shows the mode registers for LPDDR3 SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

[Table 2] Mode Register Assignment in LPDDR3 SDRAM

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	(RFU)	WL (Set B)	(RFU)	RZQI (optional)		(RFU)		DAI
1	01_H	Device Feature 1	W	nWR (for AP)			(RFU)		BL		
2	02_H	Device Feature 2	W	WR Lev	WL Select	(RFU)	nWRE	RL & WL			
3	03_H	I/O Config-1	W	(RFU)				DS			
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	LPDDR3 Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11	$0B_H$	ODT Feature		(RFU)					PD CTL	DQ ODT	
12:15	$0C_H$~$0F_H$	(reserved)		(RFU)							
16	10_H	PASR_Bank	W	PASR Bank Mask							
17	11_H	PASR_Seg	W	PASR Segment Mask							
18-31	12_H-$1F_H$	(Reserved)		(RFU)							
32	20_H	DQ Calibration Pattern A	R	See "DQ Calibration" on Operations & Timing Diagram.							
33:39	21_H~27_H	(Do Not Use)									
40	28_H	DQ Calibration Pattern B	R	See "DQ Calibration" on Operations & Timing Diagram.							
41	29_H	CA Training 1	W	See "Mode Register Write-CA Training Mode".							
42	$2A_H$	CA Training 2	W	See "Mode Register Write-CA Training Mode".							
43:47	$2B_H$~$2F_H$	(Do Not Use)									
48	30_H	CA Training 3	W	See "Mode Register Write-CA Training Mode".							
49:62	31_H~$3E_H$	(Reserved)		(RFU)							
63	$3F_H$	Reset	W	X							
64:255	40_H~FF_H	(Reserved)		(RFU)							

NOTE :
1) RFU bits shall be set to ‘0’ during Mode Register writes.
2) RFU bits shall be read as ‘0’ during Mode Register reads.
3) All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4) All Mode Registers that are specified as RFU shall not be written.
5) See vendor device datasheets for details on vendor-specific mode registers.
6) Writes to read-only registers shall have no impact on the functionality of the device.

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MR0_Device Information (MA<7:0> = 00_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)	WL (Set B) Support	(RFU)	RZQI (Optional)		(RFU)		DAI

DAI (Device Auto-Initialization Status)	Read-only	OP<0>	**0_B**: DAI complete **1_B**: DAI still in progress	
RZQI (Built in Self Test for RZQ Information)	Read-only	OP<4:3>	**00_B:** RZQ self test not supported **01_B:** ZQ-pin may connect to VDDCA or float **10_B:** ZQ-pin may short to GND **11_B:** ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)	1-4
WL (Set B) Support	Read-only	OP<6>	**0_B**: DRAM does not support WL (Set B) **1_B**: DRAM supports WL (Set B)	WL (Set B) Option Support

NOTE :
1) RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
2) If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3] = 01 or OP[4:3] =10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3) In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4) In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e 240-Ω +/- 1%).

MR1_Device Feature 1 (MA<7:0> = 01_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)		BL		

BL	Write-only	OP<2:0>	**011_B:** BL8 (default) **All others:** Reserved
nWR [1]	Write-only	OP<7:5>	**If nWRE (MR2 OP<4>) = 0:** **100_B**: nWR=6 **110_B:** nWR=8 **111_B:** nWR=9 **If nWRE (MR2 OP<4>) = 1:** **000_B:** nWR=10 (default) **001_B:** nWR=11 **010_B:** nWR=12 **100_B**: nWR=14 **110_B**: nWR=16 **All others:** Reserved

NOTE :
1) Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

[Table 3] Burst Sequence

C2	C1	C0	BL	Burst Cycle Number and Burst Address Sequence							
				1	2	3	4	5	6	7	8
0_B	0_B	0_B	8	0	1	2	3	4	5	6	7
0_B	1_B	0_B		2	3	4	5	6	7	0	1
1_B	0_B	0_B		4	5	6	7	0	1	2	3
1_B	1_B	0_B		6	7	0	1	2	3	4	5

NOTE :
1) C0 input is not present on CA bus. It is implied zero.
2) The burst address represents C2 - C0.

MR2_Device Feature 2 (MA<7:0> = 02_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Select	(RFU)	nWRE	RL & WL			

RL & WL	Write-only	OP<3:0>	**If OP<6> =0 (WL Set A, default)** **0100_B:** RL = 6 / WL = 3 (≤ 400 MHz) **0110_B:** RL = 8 / WL = 4 (≤ 533 MHz) **0111_B:** RL = 9 / WL = 5 (≤ 600 MHz) **1000_B:** RL = 10 / WL = 6 (≤ 667 MHz, default) **1001_B:** RL = 11 / WL = 6 (≤ 733 MHz) **1010_B:** RL = 12 / WL = 6 (≤ 800 MHz) **1100_B**: RL = 14 / WL = 8 (≤ 933 MHz) **1110_B**: RL = 16 / WL = 8 (≤ 1066MHz) **All others:** Reserved **If OP<6> =1 (WL Set B, optional[2])** **0100_B**: RL = 6 / WL = 3 (≤ 400 MHz) **0110_B**: RL = 8 / WL = 4 (≤ 533 MHz) **0111_B**: RL = 9 / WL = 5 (≤ 600 MHz) **1000_B**: RL = 10 / WL = 8 (≤ 667 MHz, default) **1001_B**: RL = 11 / WL = 9 (≤ 733 MHz) **1010_B**: RL = 12 / WL = 9 (≤ 800 MHz) **1100_B**: RL = 14 / WL = 11 (≤ 933 MHz) **1110_B**: RL = 16 / WL = 13 (≤ 1066MHz) **All others**: reserved
nWRE	Write-only	OP<4>	**0_B**: Enable nWR programming ≤ 9 **1_B**: Enable nWR programming > 9 (default)
WL Select	Write-only	OP<6>	**0_B**: Select WL Set A (default) **1_B**: Select WL Set B (optional[2])
WR Leveling	Write-only	OP<7>	**0_B**: Disable (default) **1_B**: Enable

NOTE :
1) See MR0, OP<7>
2) See MR0, OP<6>

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0001_B**: 34.3-Ω typical pull-down/pull-up **0010_B**: 40-Ω typical pull-down/pull-up (default) **0011_B**: 48-Ω typical pull-down/pull-up **0100_B**: Reserved for 60Ω typical pull-down/pull-up **0110_B**: Reserved for 80Ω typical pull-down/pull-up **1001_B**: 34.3Ω typical pull-down, 40Ω typical pull-up **1010_B**: 40Ω typical pull-down, 48Ω typical pull-up **1011_B**: 34.3Ω typical pull-down, 48Ω typical pull-up **All others:** Reserved

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MR4_Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** 4× t_{REFI}, 4× t_{REFIpb}, 4× t_{REFW} **010_B:** 2× t_{REFI}, 2× t_{REFIpb}, 2× t_{REFW} **011_B:** 1× t_{REFI}, 1× t_{REFIpb}, 1× t_{REFW} (<=85°C) **100_B:** 0.5× t_{REFI}, 0.5× t_{REFIpb}, 0.5× t_{REFW}, do not de-rate SDRAM AC timing **101_B:** 0.25× t_{REFI}, 0.25× t_{REFIpb}, 0.25× t_{REFW}, do not de-rate SDRAM AC timing **110_B:** 0.25× t_{REFI}, 0.25× t_{REFIpb}, 0.25× t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

NOTE :
1) A Mode Register Read from MR4 will reset OP7 to '0'.
2) OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.
3) If OP2 equals '1', the device temperature is greater than 85°C.
4) OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5) LPDDR3 SDRAM might not operate properly when OP[2:0] = 000_B or 111_B.
6) For specified operating temperature range and maximum operating temperature refer to Table 12 Operating Temperature Range.
7) LPDDR3 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 45 LPDDR3 AC Timing Table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8) See "Temperature Sensor" on [Command Definition & Timing Diagram] for information on the recommended frequency of reading MR4.

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR3 Manufacturer ID							

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LPDDR3 Manufacturer ID	Read-only	OP<7:0>	**0000 0000_B:** Reserved **0000 0001_B:** Samsung **0000 0010_B:** Do Not Use **0000 0011_B:** Do Not Use **0000 0100_B:** Do Not Use **0000 0101_B:** Do Not Use **0000 0110_B:** Do Not Use **0000 0111_B:** Do Not Use **0000 1000_B:** Do Not Use **0000 1001_B:** Do Not Use **0000 1010_B:** Reserved **0000 1011_B:** Do Not Use **0000 1100_B:** Do Not Use **0000 1101_B:** Do Not Use **0000 1110_B:** Do Not Use **0000 1111_B:** Do Not Use **1111 1110_B:** Do Not Use **All others:** Reserved

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**0001 0110$_B$:** W-version

NOTE :
1) MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**0000 0000$_B$:** A-version

NOTE :
1) MR7 is vendor specific.

MR8_Basic Configuration 4 (MA<7:0> = 08_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**11$_B$:** S8 SDRAM **All others**: Reserved
Density	Read-only	OP<5:2>	**0110$_B$:** 4Gb **1110$_B$**: 6Gb **0111$_B$:** 8Gb **1101$_B$**: 12Gb **1000$_B$:** 16Gb **1001$_B$:** 32Gb **All others:** Reserved
I/O width	Read-only	OP<7:6>	**00$_B$:** x32 **01$_B$:** x16 **All Others**: Reserved

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MR9_Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

NOTE :
1) Host processor shall not write MR10 with "Reserved" values.
2) LPDDR3 devices shall ignore calibration command when a “Reserved” value is written into MR10.
3) See AC timing table for the calibration latency.
4) If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see Mode Register Write ZQ Calibration Command") or default calibration (through the ZQ_{RESET} command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5) LPDDR3 devices that do not support calibration shall ignore the ZQ Calibration command.
6) Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11_ODT Control (MA<7:0> = $0B_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					PD CTL	DQ ODT	

DQ ODT	Write-only	OP<1:0>	**00_B:** Disable (Default) **01_B:** RZQ/4 **10_B:** RZQ/2 **11_B:** RZQ/1
PD Control	Write-only	OP<2>	**0_B:** ODT disabled by DRAM during power down (default) **1_B:** ODT enabled by DRAM during power down

MR12:15_(Reserved) (MA<7:0> = $0C_H$-$0F_H$):

MR16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

Bank <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the bank (=unmasked, default) **1_B:** refresh blocked (=masked)

OP	Bank Mask	8-Bank SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

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MR17_PASR_Segment Mask (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0>Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the segment (=unmasked, default) **1_B:** refresh blocked (=masked)

Segment	OP	Segment Mask	8Gb
			R14:12
0	0	XXXXXXX1	000_B
1	1	XXXXXX1X	001_B
2	2	XXXXX1XX	010_B
3	3	XXXX1XXX	011_B
4	4	XXX1XXXX	100_B
5	5	XX1XXXXX	101_B
6	6	X1XXXXXX	110_B
7	7	1XXXXXXX	111_B

NOTE :
1) This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

MR18-31_(Reserved) (MA<7:0> = 012_H - $01F_H$):

MR32_DQ Calibration Pattern A (MA<7:0>=20_H):

Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on Operations & Timing Diagram.

MR33:39_(Do Not Use) (MA<7:0> = 21_H-27_H):

MR40_DQ Calibration Pattern B (MA<7:0>=28_H):

Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on Operations & Timing Diagram.

MR41_CA Training 1 (MA<7:0> = 29_H):

Writes to MR41 enables CA Training. See Mode Register Write - CA Training Mode

MR42_ CA Training 2 (MA<7:0> = $2A_H$):

Writes to MR42 exits CA Training. See Mode Register Write - CA Training Mode

MR43:47_ (Do Not Use)(MA<7:0> = $2B_H$-$2F_H$):

MR48_CA Training_3 (MA<7:0>=30_H)

Writes to MR48 enables CA Training. See Mode Register Write - CA Training Mode

MR49:62_(Reserved) (MA<7:0> = 31_H - $3E_H$):

MR63_Reset (MA<7:0> = $3F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X or 0xFC[1)]							

NOTE :
1) For additional information on MRW RESET see "Mode Register Write Command" on [Command Definition & Timing Diagram].

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MR64:255 (Reserved) (MA<7:0> = 40_H-FF_H):

3.0 TRUTH TABLES

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

3.1 Command truth table

[Table 4] Command truth table

	SDR Command Pins			DDR CA pins (10)										
SDRAM Command	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	R1
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	R2
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	R1
			X	MA6	MA7	X								R2
Refresh (per bank)	H	H	L	L	L	H	L	X						R1
			X	X										R2
Refresh (all bank)	H	H	L	L	L	H	H	X						R1
			X	X										R2
Enter Self Refresh	H	L	L	L	L	H	X							R1
	X		X	X										R2
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	R1
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	R2
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	R1
			X	AP[3)]	C3	C4	C5	C6	C7	C8	C9	C10	C11	R2
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	R1
			X	AP[3)]	C3	C4	C5	C6	C7	C8	C9	C10	C11	R2
Precharge[11)] (pre bank, all bank)	H	H	L	H	H	L	H	AB	X		BA0	BA1	BA2	R1
			X	X										R2
NOP	H	H	L	H	H	H	X							R1
			X	X										R2
Maintain PD, SREF (NOP)[4)]	L	L	L	H	H	H	X							R1
			X	X										R2
NOP	H	H	H	X										R1
			X	X										R2
Maintain PD, SREF[4)]	L	L	X	X										R1
			X	X										R2
Enter Power Down	H	L	H	X										R1
	X		X	X										R2
Exit PD, SREF	L	H	H	X										R1
	X		X	X										R2

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NOTE:
1) All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2) Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3) AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4) “X” means “H or L (but a defined logic level)”, except when the LPDDR3 SDRAM is in PD, SREF in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exit procedure, See also Self-Refresh Operation and Basic Power-Down Entry and Exit Timing in LPDDR3 operations & Timing specification.
5) Self refresh exit is asynchronous.
6) V_{REF} must be between 0 and VDDQ during Self Refresh.
7) CAxr refers to command/address bit “x” on the rising edge of clock.
8) CAxf refers to command/address bit “x” on the falling edge of clock.
9) CS_n and CKE are sampled at the rising edge of clock.
10) The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
11) AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.
12) When CS_n is HIGH, LPDDR3 CA bus can be floated.

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3.2 CKE Truth Table

[Table 5] LPDDR3 : CKE Table 1),2)

Device Current State3)	CKE_{n-1} 4)	CKE_n 4)	CS_n5)	Command n6)	Operation6)	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	7
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	7
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	7, 9
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	8
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	10
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE :
1) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2) 'X' means 'Don't care'.
3) "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.
4) "CKE_n" is the logic state of CKE at clock rising edge n; "CKE_{n-1}" was the state of CKE at the previous clock edge.
5) "CS_n" is the logic state of CS_n at the clock rising edge n;
6) "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
7) Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XP} period.
8) Self-Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XSR} time.
9) Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.
10) In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.

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3.3 State Truth Table

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

[Table 6] Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Write value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	8
	Precharge	Deactivate row in bank or banks	Precharging	9, 14
Row Active	Read	Select column, and start read burst	Reading	11
	Write	Select column, and start write burst	Writing	11
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 13
Power On	Reset	Begin Device Auto-Initialization	Resetting	8
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE :

1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.
2) All states and sequences not shown are illegal or reserved.
3) Current State Definitions:
   - Idle: The bank or banks have been precharged, and tRP has been met.
   - Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
   - Reading: A Read burst has been initiated, with Auto Precharge disabled.
   - Writing: A Write burst has been initiated, with Auto Precharge disabled.
4) The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table 1.2, and according to Table 6.
   - Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   - Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
   - Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   - Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5) The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
   - Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
   - Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
   - Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   - Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
   - Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
   - MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
   - Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
6) Bank-specific; requires that the bank is idle and no bursts are in progress.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Not bank-specific reset command is achieved through Mode Register Write command.
9) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10) A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
11) The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12) A Write command may be applied after the completion of the Read burst; burst terminates are not permitted.
13) A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.
14) If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

[Table 7] Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9,10,12
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7,15
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,14
	Write	Select column, and start write burst to Bank m	Writing	7,13,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,14,15
	Write	Select column, and start write burst to Bank m	Writing	7,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Power On	Reset	Begin Device Auto-Initialization	Resetting	11,16
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

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NOTE :

1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2) All states and sequences not shown are illegal or reserved.
3) Current State Definitions:
   - Idle: The bank has been precharged, and tRP has been met.
   - Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Reading: A Read burst has been initiated, with Auto Precharge disabled.
   - Writing: A Write burst has been initiated, with Auto Precharge disabled
4) Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5) The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
   - Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
   - Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.
   - Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
   - MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
6) t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m. Additionally, in the case of multiple banks activated, t_{FAW} must be satisfied.
7) Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
8) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9) MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)
10) MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.)
11) Not bank-specific; requires that all banks are idle and no bursts are in progress.
12) The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.
13) A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
14) Read with auto precharge enabled or a Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the Precharge & Auto Precharge clarification table are followed.
15) A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.
16) Reset command is achieved through Mode Register Write command.

3.4 Data mask truth table

Table 8 provides the data mask truth table.

[Table 8] DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE :
1) Used to mask write data, provided coincident with the corresponding data.

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4.0 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 9] Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	1
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	1,2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	1,3
Voltage on any ball relative to VSS	V_{IN}, V_{OUT}	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	4

NOTE :
1) See Power Ramp for relationships between power supplies.
2) $V_{REFCA} \leq 0.6 \times VDDCA$; however, V_{REFCA} may be $\geq$ VDDCA provided that $V_{REFCA} \leq 300mV$.
3) $V_{REFDQ} \leq 0.7 \times VDDQ$; however, V_{REFDQ} may be $\geq$ VDDQ provided that $V_{REFDQ} \leq 300mV$.
4) Storage Temperature is the case surface temperature on the center/top side of LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

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5.0 AC & DC OPERATING CONDITIONS

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

5.1 Recommended DC Operating Conditions

[Table 10] Recommended DC Operating Conditions

	DRAM	LPDDR3			Unit
		Min	Typ	Max	
VDD1	Core Power1	1.70	1.80	1.95	V
VDD2	Core Power2	1.14	1.20	1.3	V
VDDCA	Input Buffer Power	1.14	1.20	1.3	V
VDDQ	I/O Buffer Power	1.14	1.20	1.3	V

NOTE :
1) VDD1 uses significantly less current than VDD2.
2) The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM package ball.

5.2 Input Leakage Current

[Table 11] Input Leakage Current

	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-6	6	uA	1,2
V_{Ref} supply leakage current	I_{VREF}	-3	3	uA	3,4

NOTE :
1) For CA, CKE, CS_n, CK_t, CK_c. Any input 0V≤VIN≤VDDCA (All other pins not under test = 0V)
2) Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.
3) The minimum limit requirement is for testing purposes. The leakage current on V_{RefCA} and V_{RefDQ} pins should be minimal.
4) $V_{REFDQ} = V_{DDQ}/2$ or $V_{REFCA} = V_{DDCA}/2$. (All other pins not under test = 0V)

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5.3 Operating Temperature Range

[Table 12] Operating Temperature Range

	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	°C

NOTE :
1) Operating Temperature is the case surface temperature on the center top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.
2) Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Extended Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

6.0 AC AND DC INPUT MEASUREMENT LEVELS

6.1 AC and DC Logic Input Levels for Single-Ended Signals

6.1.1 AC and DC Input Levels for Single-Ended CA and CS_n Signals

[Table 13] Single-Ended AC and DC Input Levels for CA and CS_n inputs

Symbol	Parameter	1866			Notes
		Min	Max		
V_{IHCA}(AC)	AC input logic high	V_{REF} + 0.135	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	V_{REF} - 0.135	V	1, 2
V_{IHCA}(DC)	DC input logic high	V_{REF} + 0.100	VDDCA	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	V_{REF} - 0.100	V	1
V_{RefCA}(DC)	Reference Voltage for CA and CS_n inputs	0.49 × VDDCA	0.51 × VDDCA	V	3, 4

NOTE :
1) For CA and CS_n input only pins. V_{Ref} = V_{RefCA}(DC).
2) See Overshoot and Undershoot Specifications.
3) The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from V_{RefCA}(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
4) For reference: approx. VDDCA/2 +/- 12 mV.

6.2 AC and DC Input Levels for CKE

[Table 14] Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter		Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.65 × VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.35 × VDDCA	V	1

NOTE :
1) See Overshoot and Undershoot Specifications.

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6.2.1 AC and DC Input Levels for Single-Ended Data Signals

[Table 15] Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	1866			Notes
		Min	Max		
$V_{IHDQ(AC)}$	AC input logic high	V_{REF} + 0.135	Note 2	V	1, 2, 5
$V_{ILDQ(AC)}$	AC input logic low	Note 2	V_{REF} - 0.135	V	1, 2, 5
$V_{IHDQ(DC)}$	DC input logic high	V_{REF} + 0.100	VDDQ	V	1
$V_{ILDQ(DC)}$	DC input logic low	VSSQ	V_{REF} - 0.100	V	1
$V_{RefDQ(DC)}$ (DQ ODT disabled)	Reference Voltage for DQ, DM inputs	0.49 × VDDQ	0.51 × VDDQ	V	3, 4
$V_{RefDQ(DC)}$ (DQ ODT enabled)	Reference Voltage for DQ, DM inputs	V_{ODTR}/2 - 0.01 × VDDQ	V_{ODTR}/2 + 0.01 × VDDQ	V	3,5,6

NOTE :
1) For DQ input only pins. Vref = $V_{RefDQ(DC)}$.
2) See Overshoot and Undershoot Specifications.
3) The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from V_{RefDQ}(DC) by more than +/-1% VDDQ (for reference: approx. +/ - 12 mV).
4) For reference : approx. V_{DDQ}/2 +/- 12mV.
5) For reference : approx. V_{ODTR}/2 +/- 12mV.
6) The nominal mode register programmed value for RODT and the nominal controller output impedance RON are used for the calculation of V_{ODTR}. For testing purposes a controller RON value of 50Ω is used.

$$V_{ODTR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

6.3 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 2. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). VDD stands for VDDCA for V_{RefCA} and VDDQ for V_{RefDQ}. $V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g 1 sec). This average has to meet the min/max requirements in Table 13. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref}(DC)$ by no more than +/- 1% VDD. Vref(t) cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.

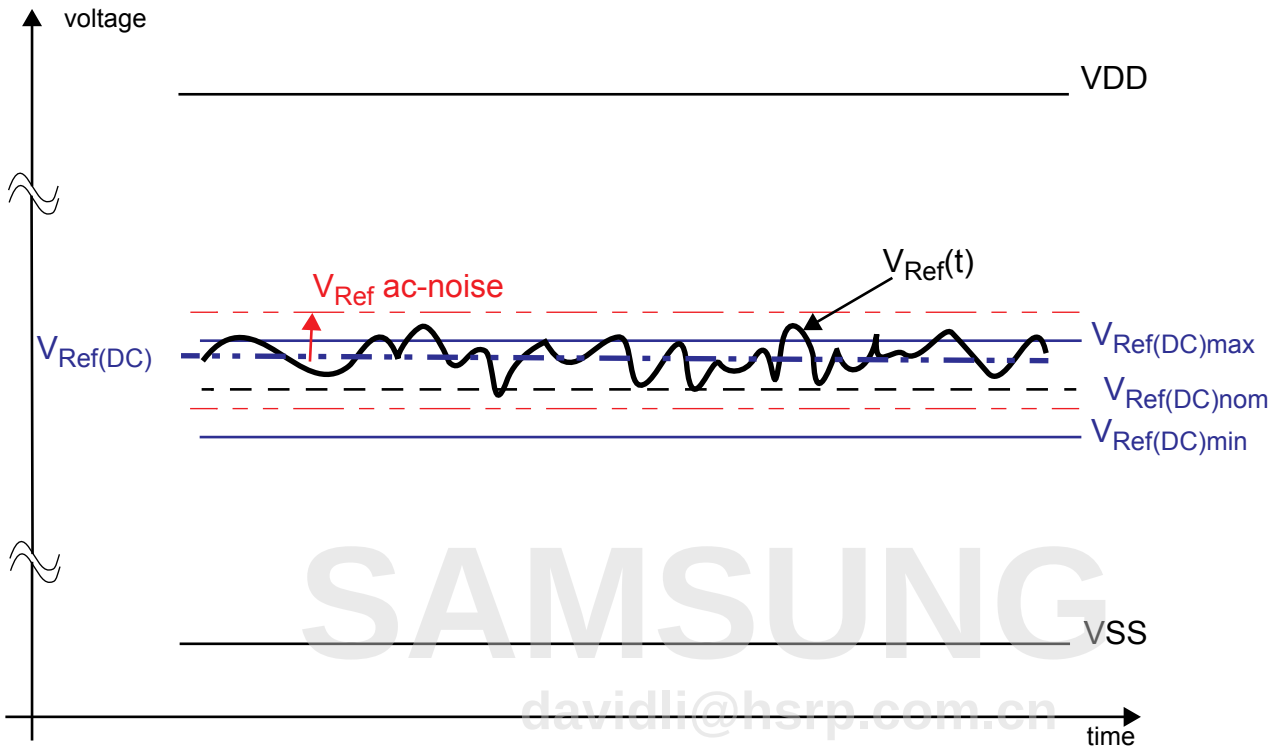

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Figure 2. Illustration of V_{Ref}(DC) tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{Ref}.

"V_{Ref} " shall be understood as $V_{Ref(DC)}$, as defined in Figure 2.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the LPDDR3 setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/-1% of VDD) are included in LPDDR3 timings and their associated deratings.

6.4 Input Signal

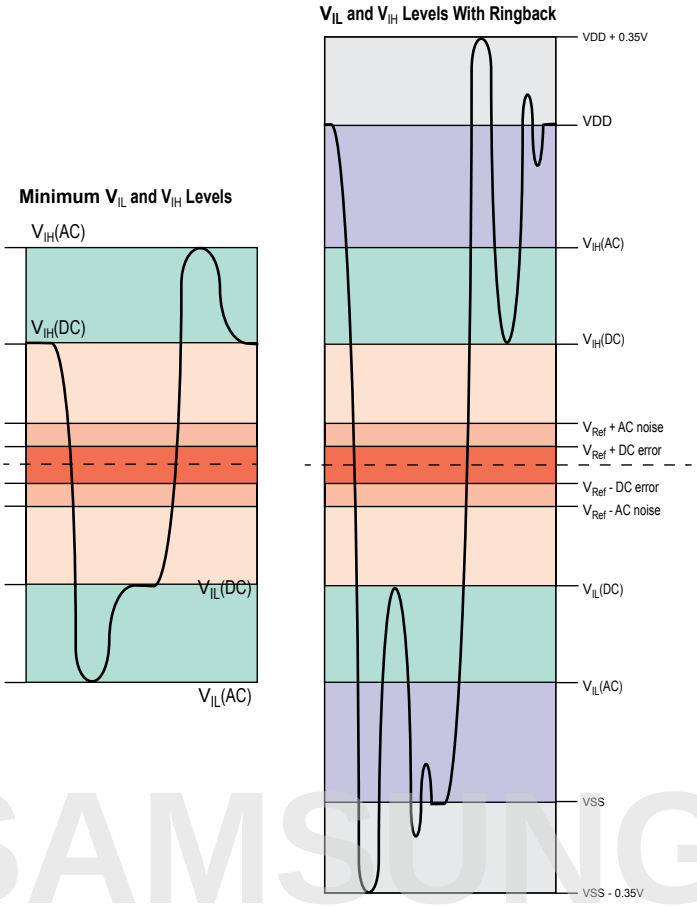

Figure 3. LPDDR3 Input Signal

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NOTE :
1) Numbers reflect nominal values.
2) For CA0-9, CK_t, CK_c, and CS_n, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.
3) For CA0-9, CK_t, CK_c, and CS_n, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ

6.5 AC and DC Logic Input Levels for Differential Signals

6.5.1 Differential signal definition

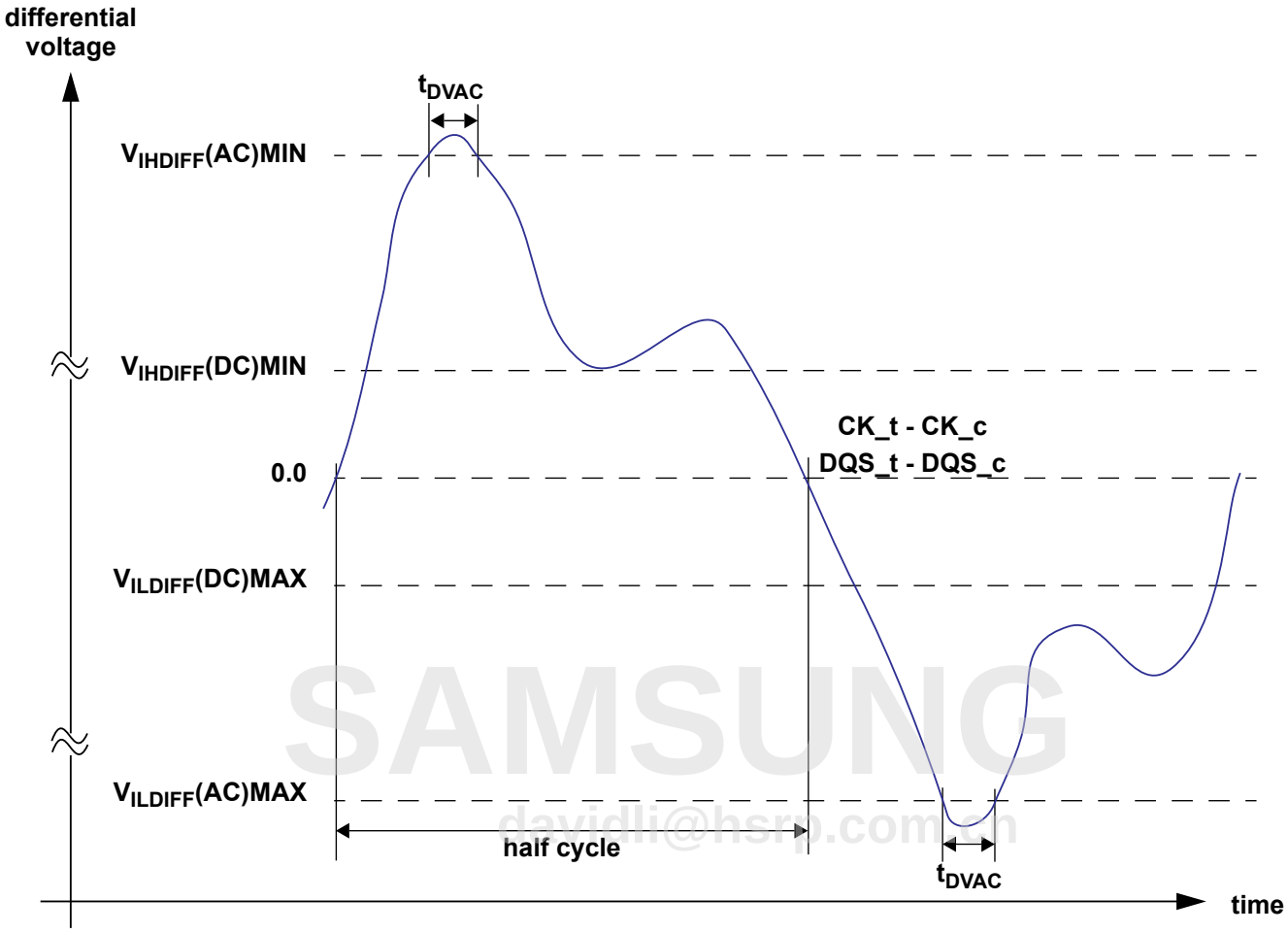

Figure 4. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

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6.5.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)

[Table 16] Differential AC and DC Input Levels

Symbol	Parameter	Value			Notes
		Min	Max		
$V_{IHdiff\ (DC)}$	Differential input high	2 × ($V_{IH(dc)}$ - Vref)	Note 3	V	1
$V_{ILdiff\ (DC)}$	Differential input low	Note 3	2 × ($V_{IL(dc)}$ - Vref)	V	1
$V_{IHdiff\ (AC)}$	Differential input high ac	2 × ($V_{IH(ac)}$ - Vref)	Note 3	V	2
$V_{ILdiff\ (AC)}$	Differential input low ac	Note 3	2 × ($V_{IL(ac)}$ - Vref)	V	2

NOTE :
1) Used to define a differential signal slew-rate. For CK_t - CK_c use $V_{IH/VIL(dc)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(DC)}$ of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2) For CK_t - CK_c use $V_{IH}/V_{IL(AC)}$ of CA and V_{RefCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(AC)}$ of DQs and V_{RefDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3) These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits ($V_{IH(DC)}$ max, $V_{IL(DC)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Figure 10 Overshoot and Undershoot Definition.
4) For CK_t and CK_c, Vref = $V_{RefCA(DC)}$. For DQS_t and DQS_c, Vref = $V_{RefDQ(DC)}$.

[Table 17] Allowed time before ringback tDVAC for DQS_t/DQS_c

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH/Ldiff(AC)}\|$ = 270mV 1866Mbps	
	min	max
> 8.0	40	-
8.0	40	-
7.0	39	-
6.0	36	-
5.0	33	-
4.0	29	-
3.0	21	-
< 3.0	21	-

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[Table 18] Allowed time before ringback tDVAC for CK_t/CK_c

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH/Ldiff(AC)}\|$ = 270mV 1866Mbps	
	min	max
> 8.0	40	-
8.0	40	-
7.0	39	-
6.0	36	-
5.0	33	-
4.0	29	-
3.0	21	-
< 3.0	21	-

6.5.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.
CK_t and CK_c shall meet V_{SEH}(AC)min / V_{SEL}(AC)max in every half-cycle.
DQS_t, DQS_c shall meet V_{SEH}(AC)min / V_{SEL}(AC)max in every half-cycle preceeding and following a valid transition.
Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

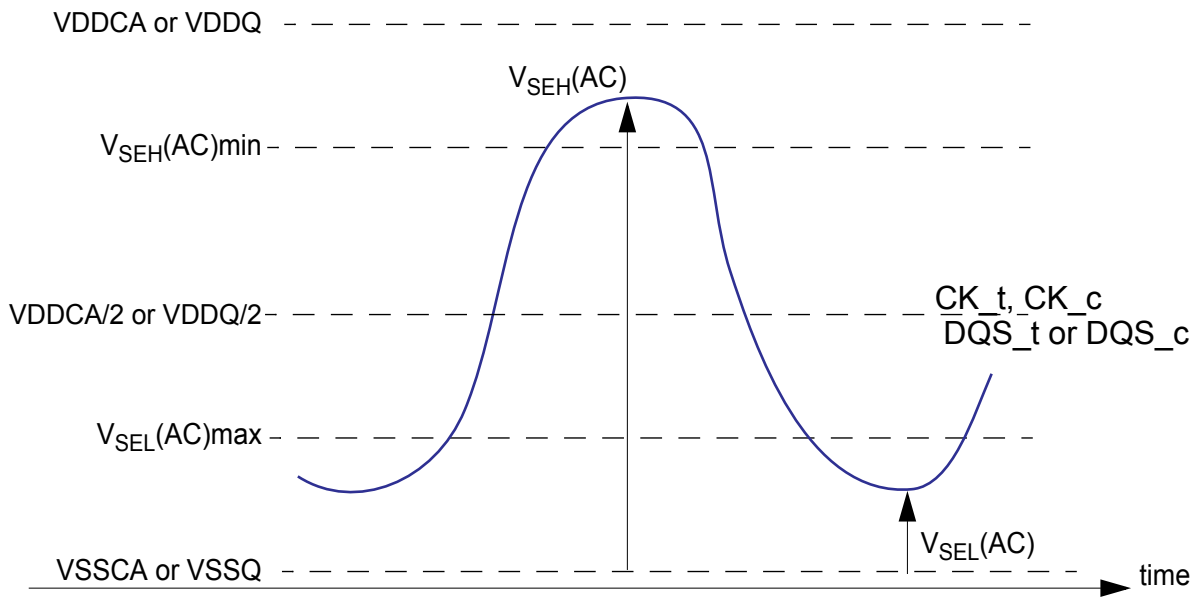

Figure 5. Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS_t, DQS_c and VDDCA/2 for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}(AC)max, V_{SEH}(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.
The single ended requirements for CK_t, CK_c, DQS_t and DQS_c are found in Table 13 and Table 15 respectively.

[Table 19] Single-ended levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
V_{SEH} (AC150)	Single-ended high-level for strobes	(VDDQ/2)+0.150	Note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	(VDDCA/2)+0.150	Note 3	V	1, 2
V_{SEL} (AC150)	Single-ended low-level for strobes	Note 3	(VDDQ/2)-0.150	V	1, 2
	Single-ended low-level for CK_t, CK_c	Note 3	(VDDCA/2)-0.150	V	1, 2
V_{SEH} (AC135)	Single-ended high-level for strobes	(VDDQ / 2) + 0.135	Note 3	V	1,2
	Single-ended high-level for CK_t, CK_c	(VDDCA / 2) + 0.135	Note 3	V	1,2
V_{SEL} (AC135)	Single-ended low-level for strobes	Note 3	(VDDQ / 2) - 0.135	V	1,2
	Single-ended low-level for CK_t, CK_c	Note 3	(VDDCA / 2) - 0.135	V	1,2

NOTE :
1) For CK_t, CK_c use V_{SEH}/$V_{SEL(AC)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use V_{IH}/$V_{IL(AC)}$ of DQs.
2) $V_{IH(AC)}$/$V_{IL(AC)}$ for DQs is based on V_{RefDQ}; $V_{SEH(AC)}$/$V_{SEL(AC)}$ for CA is based on V_{RefCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3) These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(DC)}$ max, $V_{IL(DC)}$min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to 7.5 Overshoot and Undershoot Specifications.

6.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in Table 19. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid-level between of VDD and VSS.

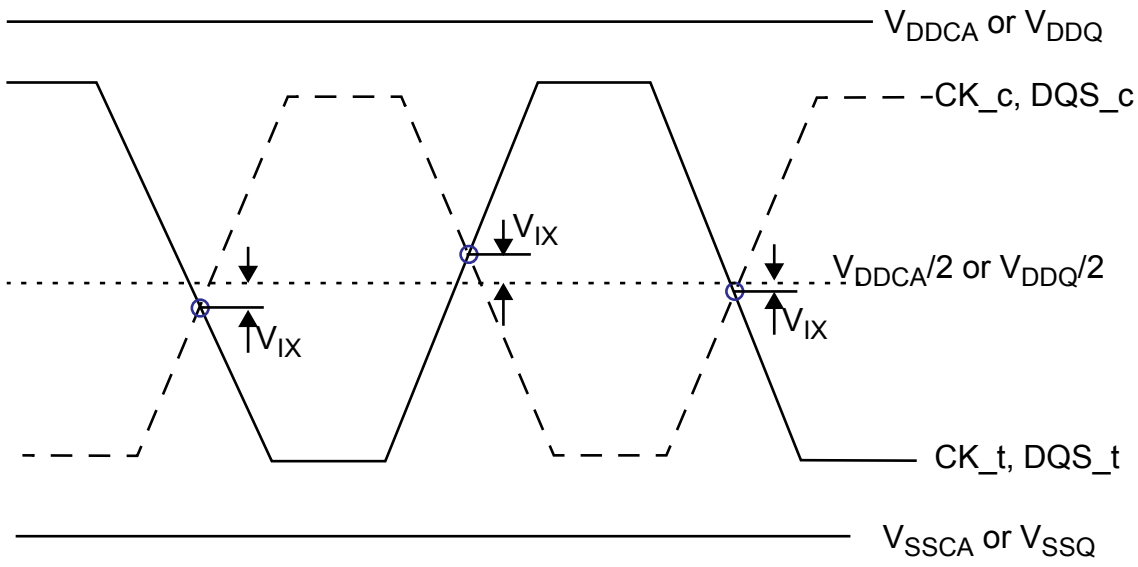

Figure 6. Vix Definition

[Table 20] Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to V_{DDCA}/2 for CK_t, CK_c	-120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to V_{DDQ}/2 for DQS_t, DQS_c	-120	120	mV	1,2

NOTE :
1)The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × VDD of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in VDD. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2) For CK_t and CK_c, Vref = $V_{RefCA(DC)}$. For DQS_t and DQS_c, Vref = $V_{RefDQ(DC)}$.

6.7 Slew Rate Definitions for Single-Ended Input Signals

See CA and CS_n Setup, Hold and Derating for single-ended slew rate definitions for address and command signals.
See Data Setup, Hold and Slew Rate Derating for single-ended slew rate definitions for data signals.

6.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table 21 and Figure 7.

[Table 21] Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff

NOTE :
1) The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.

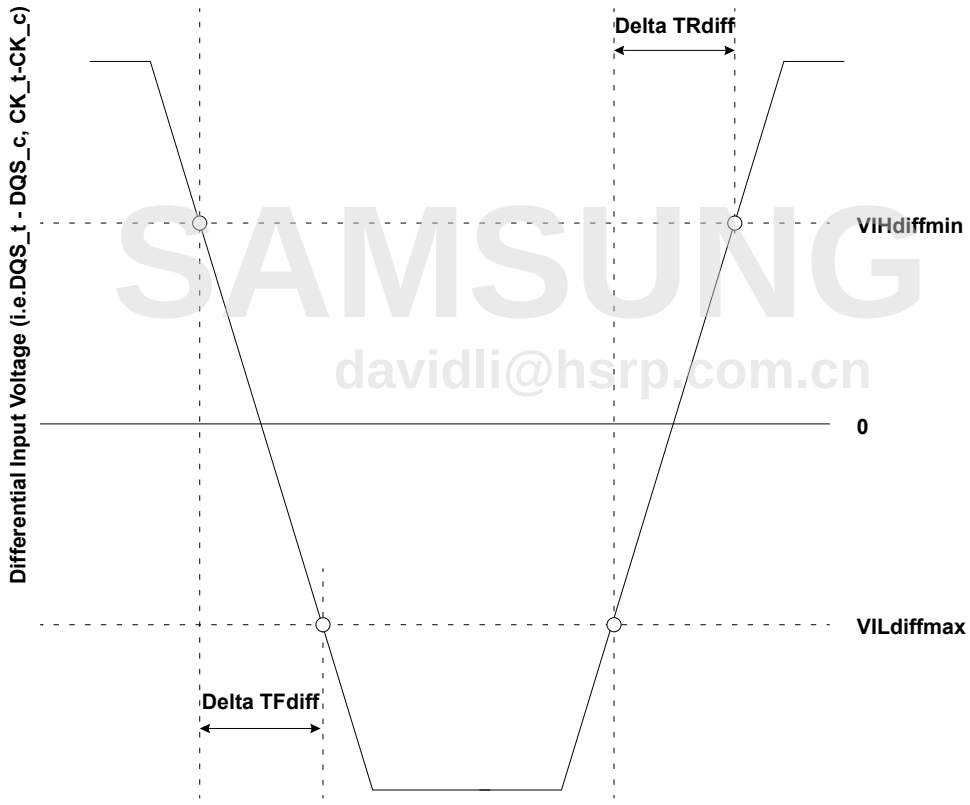

Figure 7. Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c

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7.0 AC AND DC OUTPUT MEASUREMENT LEVELS

7.1 Single Ended AC and DC Output Levels

Table 22 shows the output levels used for measurements of single ended signals.

[Table 22] Single-ended AC and DC Output Levels

Symbol	Parameter		Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)		0.9 × V_{DDQ}	V	1
$V_{OL(DC)}$ ODT disabled	DC output low measurement level (for IV curve linearity)		0.1 × V_{DDQ}	V	2
$V_{OL(DC)}$ ODT enabled	DC output low measurement level (for IV curve linearity)		V_{DDQ} × [0.1 + 0.9 × (R_{ON} / R_{TT} + R_{ON}))]	V	3
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)		V_{RefDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)		V_{RefDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	Min	-15	uA	
		Max	15	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

NOTE :
1) I_{OH} = -0.1mA.
2) I_{OL} = 0.1mA.
3) The min value is derived when using RTT, min and RON,max (+/- 30% uncalibrated, +/-15% calibrated).

7.2 Differential AC and DC Output Levels

Table 23 shows the output levels used for measurements of differential signals (DQS_t, DQS_c).

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[Table 23] Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OHdiff\ (AC)}$	AC differential output high measurement level (for output SR)	+ 0.20 × V_{DDQ}	V	1
$V_{OLdiff\ (AC)}$	AC differential output low measurement level (for output SR)	- 0.20 × V_{DDQ}	V	2

NOTE :
1) I_{OH} = -0.1mA.
2) I_{OL} = 0.1mA.

7.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 24 and Figure 8.

[Table 24] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

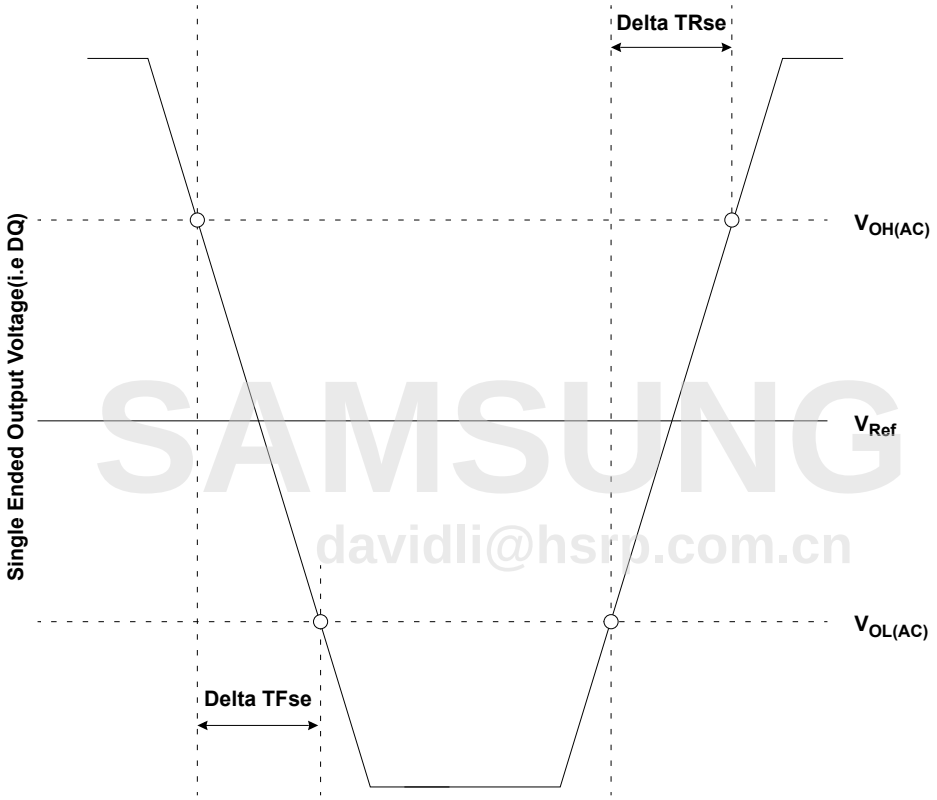

Figure 8. Single Ended Output Slew Rate Definition

[Table 25] Output Slew Rate (single-ended)

Parameter	Symbol	Value		Units
		Min[1)]	Max[2)]	
Single-ended Output Slew Rate (R_{ON} = 40Ω +/- 30%)	SRQse	1.5	4.0	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Signals				

NOTE :
1) Measured with output reference load.
2) The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3) The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

7.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 26 and Figure 9.

[Table 26] Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff\ (AC)}$	$V_{OHdiff\ (AC)}$	[$V_{OHdiff\ (AC)}$ - $V_{OLdiff\ (AC)}$] / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff\ (AC)}$	$V_{OLdiff\ (AC)}$	[$V_{OHdiff\ (AC)}$ - $V_{OLdiff\ (AC)}$] / DeltaTFdiff

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

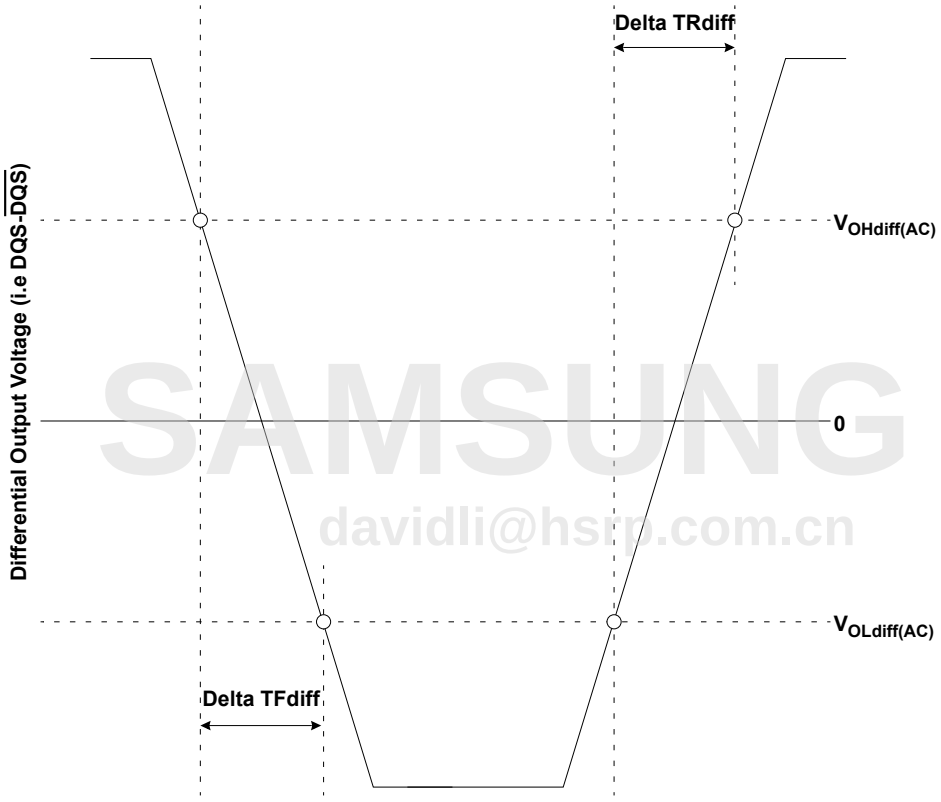

Figure 9. Differential Output Slew Rate Definition

[Table 27] Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (R_{ON} = 40Ω +/- 30%)	SRQdiff	3.0	8.0	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals				

NOTE :
1) Measured with output reference load.
2) The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
3) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

7.5 Overshoot and Undershoot Specifications

[Table 28] AC Overshoot/Undershoot Specification

Parameter		1866	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 10)	Max	0.35	V
Maximum peak amplitude allowed for undershoot area. (See Figure 10)	Max	0.35	V
Maximum area above VDD. (See Figure 10)	Max	0.10	V·ns
Maximum area below VSS. (See Figure 10)	Max	0.10	V·ns

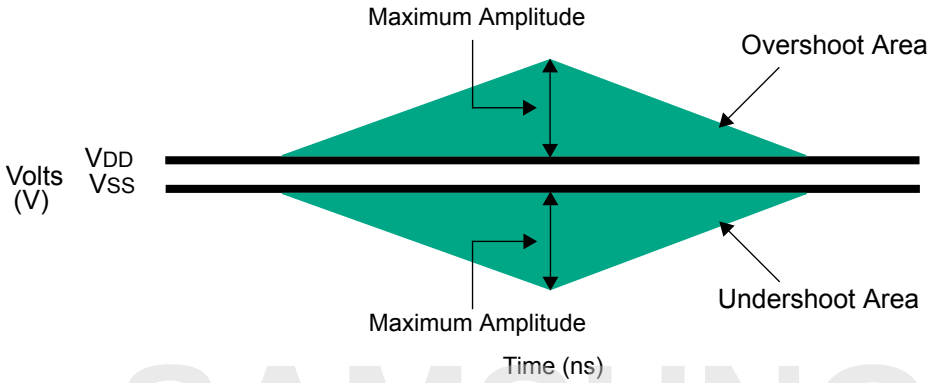

Figure 10. Overshoot and Undershoot Definition

NOTE :
1) VDD stands for VDDCA for CA[9:0], CK_t, CK_c, CS_n, and CKE. VDD stands for VDDQ for DQ, DM, ODT, DQS_t, and DQS_c.
2) VSS stands for VSSCA for CA[9:0], CK_t, CK_c, CS_n, and CKE. VSS stands for VSSQ for DQ, DM, ODT, DQS_t, and DQS_c.
3) Absolute maximum requirements apply.
4) Maximum peak amplitude values are referenced from actual VDD and VSS values.
5) Maximum area values are referenced from maximum operating VDD and VSS values.

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8.0 OUTPUT BUFFER CHARACTERISTICS

8.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

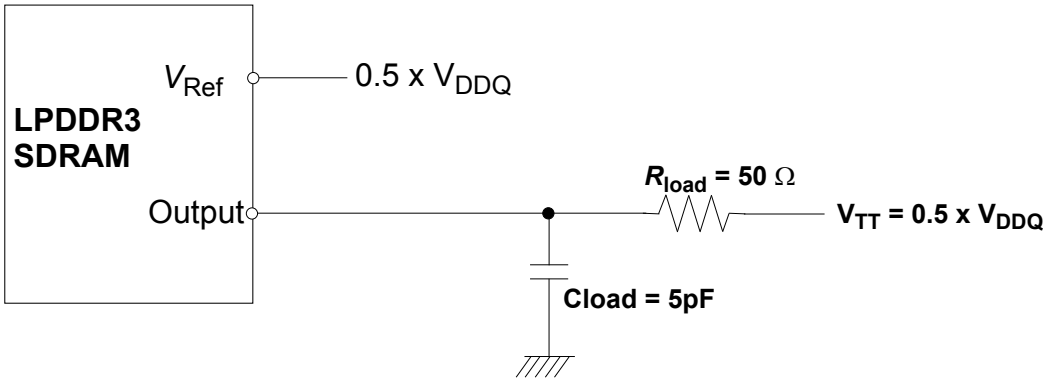

Figure 11. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

NOTE :

1) All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

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9.0 RONPU AND RONPD RESISTOR DEFINITION

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

NOTE :
1)This is under the condition that R_{ONPD} is turned off.

$$RONPD = \frac{Vout}{ABS(Iout)}$$

NOTE :
1) This is under the condition that R_{ONPU} is turned off.

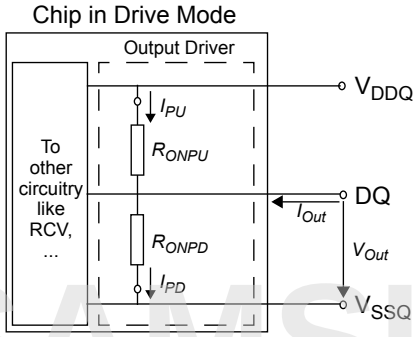

Figure 12. Output Driver: Definition of Voltages and Currents

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9.1 RONPU and RONPD Characteristics with ZQ Calibration

Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ}. Nominal R_{ZQ} is 240Ω

[Table 29] Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	1,2,3,4,6
	R_{ON34PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	1,2,3,4,6
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	1,2,3,4,6
	R_{ON40PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	1,2,3,4,6
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	1,2,3,4,6
	R_{ON48PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	1,2,3,4,6
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5,6

NOTE :
1) Across entire operating temperature range, after calibration.
2) RZQ = 240Ω.
3) The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4) Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x V_{DDQ}.
5) Measurement definition for mismatch between pull-up and pull-down, MMPUPD: Measure RONPU and RONPD, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0
6) Output driver strength measured without ODT.

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9.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

[Table 30] Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
R_{ONPD}	0.5 × VDDQ	85 - (*dRONdT* × |ΔT|) - (*dRONdV* × |ΔV|)	115 + (*dRONdT* × |ΔT|) + (*dRONdV* × |ΔV|)	%	1,2
R_{ONPU}					
R_{TT}		85 - (*dRTTdT* × |ΔT|) - (*dRTTdV* × |ΔV|)	115 + (*dRTTdT* × |ΔT|) + (*dRTTdV* × |ΔV|)		

NOTE :
1) ΔT = T-T (@ calibration), ΔV = V - V (@ calibration)
2) dRONdT, dRONdV, dRTTdV, and dRTTdT are not subject to production test but are verified by design and characterization.

[Table 31] Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	% / C
$dR_{ON}dV$	R_{ON} Voltage Sensitivity	0.00	0.20	% / mV
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.75	% / C
$dR_{TT}dV$	R_{TT} Voltage Sensitivity	0.00	0.20	% / mV

9.3 RONPU and RONPD Characteristics without ZQ Calibration

Output driver impedance R_{ON} is defined by design and characterization as default setting.

[Table 32] Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	R_{ON34PD}	0.5 × VDDQ	24	34.3	44.6	Ω	1
	R_{ON34PU}	0.5 × VDDQ	24	34.3	44.6	Ω	1
40.0Ω	R_{ON40PD}	0.5 × VDDQ	28	40	52	Ω	1
	R_{ON40PU}	0.5 × VDDQ	28	40	52	Ω	1
48.0Ω	R_{ON48PD}	0.5 × VDDQ	33.6	48	62.4	Ω	1
	R_{ON48PU}	0.5 × VDDQ	33.6	48	62.4	Ω	1
60.0Ω	R_{ON60PD}	0.5 × VDDQ	42	60	78	Ω	1
	R_{ON60PU}	0.5 × VDDQ	42	60	78	Ω	1
80.0Ω	R_{ON80PD}	0.5 × VDDQ	56	80	104	Ω	1
	R_{ON80PU}	0.5 × VDDQ	56	80	104	Ω	1

NOTE:
1) Across entire operating temperature range, without calibration.

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9.4 RZQ I-V Curve

[Table 33] RZQ I-V Curve

Voltage[V]	RON = 240Ω (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current [mA] / R_{ON} [Ohms]				Current [mA] / R_{ON} [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	n/a	n/a	0.00	0.00	n/a	n/a
0.05	0.17	0.35	n/a	n/a	-0.17	-0.35	n/a	n/a
0.10	0.34	0.70	n/a	n/a	-0.34	-0.70	n/a	n/a
0.15	0.50	1.03	n/a	n/a	-0.50	-1.03	n/a	n/a
0.20	0.67	1.39	n/a	n/a	-0.67	-1.39	n/a	n/a
0.25	0.83	1.73	n/a	n/a	-0.83	-1.73	n/a	n/a
0.30	0.97	2.05	n/a	n/a	-0.97	-2.05	n/a	n/a
0.35	1.13	2.39	n/a	n/a	-1.13	-2.39	n/a	n/a
0.40	1.26	2.71	n/a	n/a	-1.26	-2.71	n/a	n/a
0.45	1.39	3.01	n/a	n/a	-1.39	-3.01	n/a	n/a
0.50	1.51	3.32	n/a	n/a	-1.51	-3.32	n/a	n/a
0.55	1.63	3.63	n/a	n/a	-1.63	-3.63	n/a	n/a
0.60	1.73	3.93	2.17	2.94	-1.73	-3.93	-2.17	-2.94
0.65	1.82	4.21	n/a	n/a	-1.82	-4.21	n/a	n/a
0.70	1.90	4.49	n/a	n/a	-1.90	-4.49	n/a	n/a
0.75	1.97	4.74	n/a	n/a	-1.97	-4.74	n/a	n/a
0.80	2.03	4.99	n/a	n/a	-2.03	-4.99	n/a	n/a
0.85	2.07	5.21	n/a	n/a	-2.07	-5.21	n/a	n/a
0.90	2.11	5.41	n/a	n/a	-2.11	-5.41	n/a	n/a
0.95	2.13	5.59	n/a	n/a	-2.13	-5.59	n/a	n/a
1.00	2.17	5.72	n/a	n/a	-2.17	-5.72	n/a	n/a
1.05	2.19	5.84	n/a	n/a	-2.19	-5.84	n/a	n/a
1.10	2.21	5.95	n/a	n/a	-2.21	-5.95	n/a	n/a
1.15	2.23	6.03	n/a	n/a	-2.23	-6.03	n/a	n/a
1.20	2.25	6.11	n/a	n/a	-2.25	-6.11	n/a	n/a

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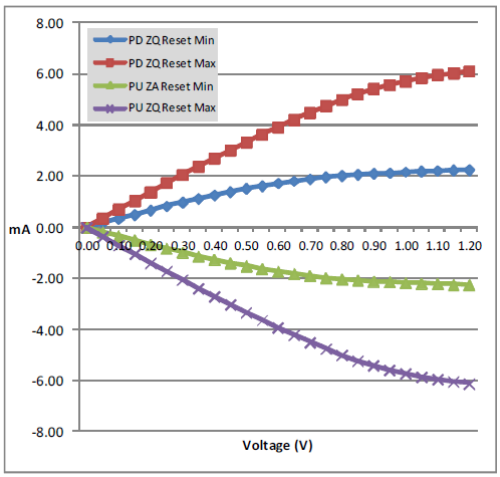

Figure 13. I-V Curve after ZQ Reset

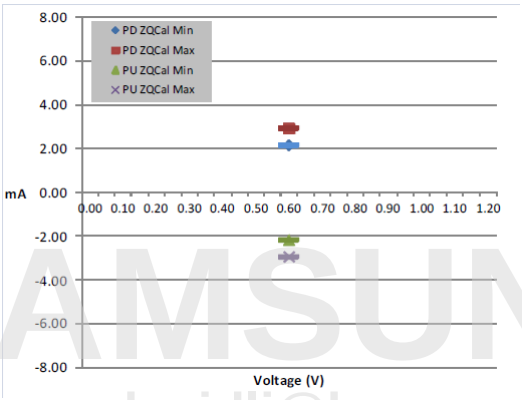

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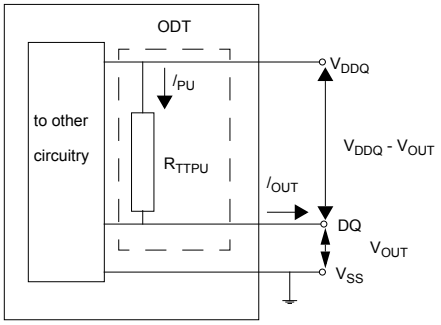
Figure 14. I-V Curve after Calibration

9.5 ODT Levels and I-V Characteristics

On-Die Termination effective resistance, RTT, is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_c pins. A functional representation of the on-die termination is shown in the figure below. RTT is defined by the following formula:
RTTPU = (VDDQ - VOut) / | IOut |



[Table 34] ODT DC Electrical Characteristics, assuming RZQ = 240 ohm after proper ZQ calibration

R_{TT} (ohm)	V_{OUT} (V)	I_{OUT}	
		Min (mA)	Max (mA)
RZQ/1	0.6	-2.17	-2.94
RZQ/2	0.6	-4.34	-5.88
RZQ/4	0.6	-8.68	-11.76

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10.0 INPUT/OUTPUT CAPACITANCE

[Table 35] Input/output capacitance

Parameter	Symbol		Value	Units	Notes
Input capacitance, CK_t and CK_c	CCK	Min	2.88	pF	1,2
		Max	4.02	pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	Min	-0.25	pF	1,2,3
		Max	0.25	pF	1,2,3
Cin, all other input-only pins except CS_n and CKE	CI1	Min	2.74	pF	1,2,4
		Max	4.42	pF	1,2,4
Cin, CS0_n / CS1_n and CKE0 / CKE1	CI2	Min	1.70	pF	1,2,4
		Max	4.56	pF	1,2,4
Cdelta, all other input-only pins except CS_n and CKE	CDI1	Min	-0.72	pF	1,2,5
		Max	0.72	pF	1,2,5
Cdelta, CS0_n / CS1_n and CKE0 / CKE1	CDI2	Min	-0.76	pF	1,2,5,10
		Max	0.76	pF	1,2,5,10
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	Min	2.07	pF	1,2,6,7
		Max	4.15	pF	1,2,6,7
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	Min	-0.2	pF	1,2,7,8
		Max	0.2	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.5	pF	1,2,7,9
		Max	0.5	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	2.44	pF	1,2
		Max	4.37	pF	1,2

(T_{OPER}; V_{DDQ} = 1.14~1.3V; V_{DDCA} = 1.14~1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V)

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NOTE :

1) This parameter applies to both die and package.
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
3) Absolute value of C_{CK_t} - C_{CK_c}.
4) CI applies to CS_n, CKE, CA0-CA9.
5) $C_{DI} = C_I - 0.5 \times (C_{CK\_t} - C_{CK\_c})$
6) DM loading matches DQ and DQS.
7) MR3 I/O configuration DS OP3-OP0 = 0001_B (34.3 Ω typical)
8) Absolute value of C_{DQS_t} and C_{DQS_c}.
9) $C_{DIO} = C_{IO} - 0.5 \times (C_{DQS\_t} + C_{DQS\_c})$ in byte-lane.
10) $C_{DI2} = C_{I2} - 0.25 \times (C_{CK\_t} + C_{CK\_c})$

11.0 IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

11.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: $V_{IN} \leq V_{IL}$(DC) MAX

HIGH: $V_{IN} \geq V_{IH}$(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 36 and Table 37.

[Table 36] Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE :
1) CS_n must always be driven HIGH.
2) 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3) The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

[Table 37] Definition of Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	HLH	HLHLLHL	L
Rising	H	L	N + 4	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N + 4	Read_Falling	LHH	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 7	NOP	HLH	LHLHLHL	L

NOTE :
1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

[Table 38] Definition of Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	HLL	HLHLLHL	L
Rising	H	L	N + 4	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N + 4	Write_Falling	LHH	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 7	NOP	HLL	LHLHLHL	L

NOTE :
1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2) Data masking (DM) must always be driven LOW.
3) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

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11.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

[Table 39] LPDDR3 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: $t_{CK} = t_{CKmin}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}, V_{DDCA}	
	$I_{DD0,in}$	V_{DDQ}	3
Idle power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}, V_{DDCA}	
	$I_{DD2P,in}$	V_{DDQ}	3
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}, V_{DDCA}	
	$I_{DD2PS,in}$	V_{DDQ}	3
Idle non power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}, V_{DDCA}	
	$I_{DD2N,in}$	V_{DDQ}	3
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}, V_{DDCA}	
	$I_{DD2NS,in}$	V_{DDQ}	3
Active power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}, V_{DDCA}	
	$I_{DD3P,in}$	V_{DDQ}	3
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}, V_{DDCA}	
	$I_{DD3PS,in}$	V_{DDQ}	4

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[Table 39] LPDDR3 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Active non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}, V_{DDCA}	
	$I_{DD3N,in}$	V_{DDQ}	4
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}, V_{DDCA}	
	$I_{DD3NS,in}$	V_{DDQ}	4
Operating burst READ current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}, V_{DDCA}	
	I_{DD4RQ}	V_{DDQ}	5
Operating burst WRITE current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}, V_{DDCA}	
	$I_{DD4W,in}$	V_{DDQ}	4
All-bank REFRESH Burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}, V_{DDCA}	
	$I_{DD5,in}$	V_{DDQ}	4
All-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}, V_{DDCA}	
	$I_{DD5AB,in}$	V_{DDQ}	4
Per-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	I_{DD5PB1}	V_{DD1}	
	I_{DD5PB2}	V_{DD2}, V_{DDCA}	
	$I_{DD5PB,in}$	V_{DDQ}	4
Self refresh current (-25°C to +85°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT disabled	I_{DD61}	V_{DD1}	6,7,8,10
	I_{DD62}	V_{DD2}, V_{DDCA}	6,7,8,10
	$I_{DD6,in}$	V_{DDQ}	4,6,7,8,10

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NOTE :

1) Published IDD values are the maximum of the distribution of the arithmetic mean.
2) ODT disabled: MR11[2:0] = 000_B.
3) IDD current specifications are tested after the device is properly initialized.
4) Measured currents are the summation of V_{DD2} and V_{DDCA}.
5) Guaranteed by design with output load = 5pF and RON = 40 ohm.
6) The 1× Self Refresh Rate is the rate at which the LPDDR3 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7) This is the general definition that applies to full-array Self Refresh.
8) Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
9) For all IDD measurements, V_{IHCKE} = 0.8 × V_{DDCA}, V_{ILCKE} = 0.2 × V_{DDCA}.
10) IDD6 85°C is guaranteed, IDD6 25°C is typical of the distribution of the arithmetic mean.

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11.3 IDD Spec Table

[Table 40] IDD Specification for 24Gb TDP LPDDR3

Symbol		Power Supply	16Gb DDP 512M x32	8Gb Mono 256M x32	Units
			1866Mbps		
IDD0	$IDD0_1$	VDD1	14	7	mA
	$IDD0_2$	VDD2,VDDCA	85.6	42.8	mA
	$IDD0_{IN}$	VDDQ	0.4	0.2	mA
IDD2P	$IDD2P_1$	VDD1	2	1	mA
	$IDD2P_2$	VDD2,VDDCA	5	2.5	mA
	$IDD2P_{IN}$	VDDQ	0.4	0.2	mA
IDD2PS	$IDD2PS_1$	VDD1	2	1	mA
	$IDD2PS_2$	VDD2,VDDCA	5	2.5	mA
	$IDD2PS_{IN}$	VDDQ	0.4	0.2	mA
IDD2N	$IDD2N_1$	VDD1	2.4	1.2	mA
	$IDD2N_2$	VDD2,VDDCA	27.6	13.8	mA
	$IDD2N_{IN}$	VDDQ	0.4	0.2	mA
IDD2NS	$IDD2NS_1$	VDD1	2.4	1.2	mA
	$IDD2NS_2$	VDD2,VDDCA	25.6	12.8	mA
	$IDD2NS_{IN}$	VDDQ	0.4	0.2	mA
IDD3P	$IDD3P_1$	VDD1	4	2	mA
	$IDD3P_2$	VDD2,VDDCA	14	7	mA
	$IDD3P_{IN}$	VDDQ	0.4	0.2	mA
IDD3PS	$IDD3PS_1$	VDD1	4	2	mA
	$IDD3PS_2$	VDD2,VDDCA	14	7	mA
	$IDD3PS_{IN}$	VDDQ	0.4	0.2	mA
IDD3N	$IDD3N_1$	VDD1	4	2	mA
	$IDD3N_2$	VDD2,VDDCA	35.6	17.8	mA
	$IDD3N_{IN}$	VDDQ	0.4	0.2	mA
IDD3NS	$IDD3NS_1$	VDD1	4	2	mA
	$IDD3NS_2$	VDD2,VDDCA	33.6	16.8	mA
	$IDD3NS_{IN}$	VDDQ	0.4	0.2	mA
IDD4R	$IDD4R_1$	VDD1	8.8	6.3	mA
	$IDD4R_2$	VDD2,VDDCA	291	202.5	mA
	$IDD4R_Q$	VDDQ	255	255	mA
IDD4W	$IDD4W_1$	VDD1	4.4	2.2	mA
	$IDD4W_2$	VDD2,VDDCA	167	122	mA
	$IDD4W_{IN}$	VDDQ	47.6	43	mA
IDD5	$IDD5_1$	VDD1	80.8	40.4	mA
	$IDD5_2$	VDD2,VDDCA	319.6	159.8	mA
	$IDD5_{IN}$	VDDQ	0.4	0.2	mA
IDD5AB	$IDD5AB_1$	VDD1	6.2	3.1	mA
	$IDD5AB_2$	VDD2,VDDCA	43.6	21.8	mA
	$IDD5AB_{IN}$	VDDQ	0.4	0.2	mA

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[Table 40] IDD Specification for 24Gb TDP LPDDR3

Symbol			Power Supply	16Gb DDP 512M x32	8Gb Mono 256M x32	Units
				1866Mbps		
IDD5PB	$IDD5PB_1$		VDD1	6.2	3.1	mA
	$IDD5PB_2$		VDD2,VDDCA	43.6	21.8	mA
	$IDD5PB_{IN}$		VDDQ	0.4	0.2	mA
IDD6	$IDD6_1$	25°C	VDD1	0.6	0.3	mA
		85°C		9	4.5	
	$IDD6_2$	25°C	VDD2,VDDCA	1.52	0.76	mA
		85°C		29.2	14.6	
	$IDD6_{IN}$	25°C	VDDQ	0.04	0.02	mA
		85°C		0.4	0.2	

NOTE :
1) See Table 39 for notes.

[Table 41] IDD6 Partial Array Self-Refresh Current

Parameter			24Gb TDP		Unit
			25°C	85°C	
IDD6 Partial Array Self-Refresh Current	Full Array	VDD1	0.9	13.5	mA
		VDD2, VDDCA	2.28	43.8	
		VDDQ	0.06	0.6	
	1/2 Array	VDD1	0.75	8.7	mA
		VDD2, VDDCA	1.56	28.2	
		VDDQ	0.06	0.6	
	1/4 Array	VDD1	0.66	6.3	mA
		VDD2, VDDCA	1.29	20.4	
		VDDQ	0.06	0.6	
	1/8 Array	VDD1	0.6	5.1	mA
		VDD2, VDDCA	1.05	16.5	
		VDDQ	0.06	0.6	

NOTE :
1) PASR(Partial Array Self-Refresh) function will be supported upon request. Please contact Samsung for more information.

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12.0 ELECTRICAL CHARACTERISTICS AND AC TIMING

12.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR3 device.

12.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

12.1.2 Definition for tCK(abs)

t_{CK}(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
t_{CK}(abs) is not subject to production test.

12.1.3 Definition for tCH(avg) and tCL(avg)

t_{CH}(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

t_{CL}(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

12.1.4 Definition for tJIT(per)

t_{JIT}(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
t_{JIT}(per) = Min/max of {tCK_i - tCK(avg) where i = 1 to 200}.
$t_{JIT}(per)_{,act}$ is the actual clock jitter for a given system.
$t_{JIT}(per)_{,allowed}$ is the specified allowed clock period jitter.
t_{JIT}(per) is not subject to production test.

12.1.5 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
t_{JIT}(cc) = Max of |{tCK(i +1) - tCK(i)}|.
t_{JIT}(cc) defines the cycle to cycle jitter.
t_{JIT}(cc) is not subject to production test.

12.1.6 Definition for tERR(nper)

t_{ERR}(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
t_{ERR}(nper),$_{act}$ is the actual clock jitter over n cycles for a given system.
t_{ERR}(nper),$_{allowed}$ is the specified allowed clock period jitter over n cycles.
t_{ERR}(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

t_{ERR}(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

t_{ERR}(nper),max can be calculated by the formula shown below

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, t_{ERR}(nper) tables can be generated for each t_{JIT}(per),act value.

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12.1.7 Definition for duty cycle jitter tJIT(duty)

t_{JIT}(duty) is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$

$$tJIT(duty), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

12.1.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

[Table 42] Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	$t_{CK(abs)}$	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	$t_{CH(abs)}$	tCH(avg),min + tJIT(duty),min / tCK(avg)min	$t_{CK(avg)}$
Absolute Clock LOW Pulse Width	$t_{CL(abs)}$	tCL(avg),min + tJIT(duty),min / tCK(avg)min	$t_{CK(avg)}$

NOTE :
1) tCK(avg),min is expressed is ps for this table.
2) tJIT(duty),min is a negative value.

12.2 Period Clock Jitter

LPDDR3 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 45 and how to determine cycle time de-rating and clock cycle de-rating.

12.2.1 Clock period jitter effects on core timing parameters

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR3 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

12.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

12.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

12.2.2 Clock jitter effects on Command/Address timing parameters

(t_{ISCA}, t_{IHCA}, t_{ISCS}, t_{IHCS}, t_{ISCKE}, t_{IHCKE}, t_{ISb}, t_{IHb}, t_{ISCKEb}, t_{IHCKEb})

These parameters are measured from a command/address signal (CKE, CS_n, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

12.2.3 Clock jitter effects on Read timing parameters

12.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per),act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,

if the measured jitter into a LPDDR3-1600 device has tCK(avg) = 1250 ps, tJIT(per),act,min = -92 ps and tJIT(per),act,max= + 134 ps, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (134 - 100)/1250 = .8728 tCK(avg)

12.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

12.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.

These parameters determine absolute Data-Valid window(DVW) at the LPDDR3 device pin.

Absolute min DVW @LPDDR3 device pin =

min { (tQSH(abs)min – tDQSQmax), (tQSL(abs)min – tDQSQmax) }

This minimum DVW shall be met at the target frequency regardless of clock jitter.

12.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

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12.2.4 Clock jitter effects on Write timing parameters

12.2.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

12.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

12.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per),act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per),act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR3-1600 device has tCK(avg)= 1250 ps, tJIT(per),act,min = -93 ps and tJIT(per),act,max= + 134 ps, then

tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-93 + 100)/1250 = 0.7444 tCK(avg)

and

tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (134 - 100)/1250 = 1.2228 tCK(avg)

12.3 LPDDR3 Refresh Requirements by Device Density

[Table 43] LPDDR3 Refresh Requirement Parameters (per density)

Parameter		Symbol	8Gb	Unit
Number of Banks			8	
Refresh Window Tcase ≤ 85°C		t_{REFW}	32	ms
Refresh Window 1/2-Rate Refresh		t_{REFW}	16	ms
Refresh Window 1/4-Rate Refresh		t_{REFW}	8	ms
Required number of REFRESH commands (min)		R	8,192	-
average time between REFRESH commands	REFab	t_{REFI}	3.9	us
	REFpb	t_{REFIpb}	0.4875	us
Refresh Cycle time		t_{RFCab}	210	ns
Per Bank Refresh Cycle time		t_{RFCpb}	90	ns

NOTE :
1) Please refer to LPDDR3 SDRAM Addressing.

[Table 44] LPDDR3 Read and Write Latencies

Parameter	Value	Unit
	1866	
Max. Clock frequency	933	MHz
Max. Data Rate	1866	MT/s
Average Clock Period	1.07	ns
Read Latency	14	tCK(avg)
Write Latency (Set A)	8	tCK(avg)
Write Latency (Set B)[1)]	11	tCK(avg)

NOTE:
1) Write Latency (Set B) support is an optional feature. Refer to MR0 OP<6>.

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12.4 AC Timing

Notes 1), 2), 3) and 4) apply to all parameters.

[Table 45] LPDDR3 AC Timing Table

Parameter	Symbol	Min/Max	Data Rate 1866	Unit
Maximum clock frequency	f_{CK}	-	933	MHz
Clock Timing				
Average Clock Period	$t_{CK(avg)}$	MIN	1.07	ns
		MAX	100	
Average HIGH pulse width	$t_{CH(avg)}$	MIN	0.45	$t_{CK(avg)}$
		MAX	0.55	
Average LOW pulse width	$t_{CL(avg)}$	MIN	0.45	$t_{CK(avg)}$
		MAX	0.55	
Absolute clock period	$t_{CK(abs)}$	MIN	t_{CK}(avg) MIN + t_{JIT}(per) MIN	ns
Absolute clock HIGH pulse width	$t_{CH(abs)}$	MIN	0.43	$t_{CK(avg)}$
		MAX	0.57	
Absolute clock LOW pulse width	$t_{CL(abs)}$	MIN	0.43	$t_{CK(avg)}$
		MAX	0.57	
Clock period jitter (with supported jitter)	$t_{JIT(per)}$, allowed	MIN	-60	ps
		MAX	60	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	$t_{JIT(cc)}$, allowed	MAX	120	ps
Duty cycle jitter (with supported jitter)	$t_{JIT(duty)}$, allowed	MIN	min((t_{CH}(abs),min - t_{CH}(avg),min), (t_{CL}(abs),min - t_{CL}(avg),min)) × t_{CK}(avg)	ps
		MAX	max((t_{CH}(abs),max - t_{CH}(avg),max), (t_{CL}(abs),max - t_{CL}(avg),max)) × t_{CK}(avg)	
Cumulative error across 2 cycles	$t_{ERR(2per)}$, allowed	MIN	-88	ps
		MAX	88	
Cumulative error across 3 cycles	$t_{ERR(3per)}$, allowed	MIN	-105	ps
		MAX	105	
Cumulative error across 4 cycles	$t_{ERR(4per)}$, allowed	MIN	-117	ps
		MAX	117	
Cumulative error across 5 cycles	$t_{ERR(5per)}$, allowed	MIN	-126	ps
		MAX	126	
Cumulative error across 6 cycles	$t_{ERR(6per)}$, allowed	MIN	-133	ps
		MAX	133	
Cumulative error across 7 cycles	$t_{ERR(7per)}$, allowed	MIN	-139	ps
		MAX	139	
Cumulative error across 8 cycles	$t_{ERR(8per)}$, allowed	MIN	-145	ps
		MAX	145	
Cumulative error across 9 cycles	$t_{ERR(9per)}$, allowed	MIN	-150	ps
		MAX	150	
Cumulative error across 10 cycles	$t_{ERR(10per)}$, allowed	MIN	-154	ps
		MAX	154	
Cumulative error across 11 cycles	$t_{ERR(11per)}$, allowed	MIN	-158	ps
		MAX	158	
Cumulative error across 12 cycles	$t_{ERR(12per)}$, allowed	MIN	-161	ps
		MAX	161	

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[Table 45] LPDDR3 AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
			1866	
Cumulative error across n = 13, 14 . . . 19, 20 cycles	$t_{ERR(nper),allowed}$	MIN	$t_{ERR(nper),allowed\ MIN}$ = (1 + 0.68ln(n)) × $t_{JIT(per),\ allowed\ MIN}$	ps
		MAX	$t_{ERR(nper),allowed}$ MAX = (1 + 0.68ln(n)) × $t_{JIT(per),\ allowed\ MAX}$	
ZQ Calibration Parameters				
Initialization calibration time	t_{ZQINIT}	MIN	1	us
Long calibration time	t_{ZQCL}	MIN	360	ns
Short calibration time	t_{ZQCS}	MIN	90	ns
Calibration RESET Time	$t_{ZQRESET}$	MIN	Max (50ns, $3t_{CK}$)	ns
READ Parameters[4]				
DQS output access time from CK_t/CK_c	t_{DQSCK}	MIN	2500	ps
		MAX	5500	
DQSCK delta short [5]	$t_{DQSCKDS}$	MAX	190	ps
DQSCK delta medium [6]	$t_{DQSCKDM}$	MAX	435	ps
DQSCK delta long [7]	$t_{DQSCKDL}$	MAX	525	ps
DQS - DQ skew	t_{DQSQ}	MAX	115	ps
DQS Output High Pulse Width	t_{QSH}	MIN	t_{CH}(abs) - 0.05	$t_{CK(avg)}$
DQS Output Low Pulse Width	t_{QSL}	MIN	t_{CL}(abs) - 0.05	$t_{CK(avg)}$
DQ / DQS output hold time from DQS	t_{QH}	MIN	min(t_{QSH}, t_{QSL})	ps
Read preamble[8), 11)]	t_{RPRE}	MIN	0.9	$t_{CK(avg)}$
Read postamble[8), 12)]	t_{RPST}	MIN	0.3	$t_{CK(avg)}$
DQS low-Z from clock[8)]	$t_{LZ(DQS)}$	MIN	$t_{DQSCK(MIN)}$ - 300	ps
DQ low-Z from clock[8)]	$t_{LZ(DQ)}$	MIN	$t_{DQSCK,(MIN)}$ - 300	ps
DQS high-Z from clock[8)]	$t_{HZ(DQS)}$	MAX	$t_{DQSCK,(MAX)}$ - 100	ps
DQ high-Z from clock[8)]	$t_{HZ(DQ)}$	MAX	$t_{DQSCK,(MAX)}$ + (1.4 × $t_{DQSQ,(MAX)}$)	ps
WRITE Parameters[4]				
DQ and DM input hold time (Vref based)	t_{DH}	MIN	130	ps
DQ and DM input setup time (Vref based)	t_{DS}	MIN	130	ps
DQ and DM input pulse width	t_{DIPW}	MIN	0.35	$t_{CK(avg)}$
Write command to 1st DQS latching transition	t_{DQSS}	MIN	0.75	$t_{CK(avg)}$
		MAX	1.25	
DQS input high-level width	t_{DQSH}	MIN	0.4	$t_{CK(avg)}$
DQS input low-level width	t_{DQSL}	MIN	0.4	$t_{CK(avg)}$
DQS falling edge to CK setup time	t_{DSS}	MIN	0.2	$t_{CK(avg)}$
DQS falling edge hold time from CK	t_{DSH}	MIN	0.2	$t_{CK(avg)}$
Write postamble	t_{WPST}	MIN	0.4	$t_{CK(avg)}$
Write preamble	t_{WPRE}	MIN	0.8	$t_{CK(avg)}$
CKE Input Parameters				
CKE minimum pulse width (HIGH and LOW pulse width)	t_{CKE}	MIN	max(7.5ns, 3tCK)	ns
CKE input setup time	t_{ISCKE}[13)]	MIN	0.25	$t_{CK(avg)}$
CKE input hold time	t_{IHCKE}[14)]	MIN	0.25	$t_{CK(avg)}$
Command path disable delay	t_{CPDED}	MIN	2	$t_{CK(avg)}$
Command Address Input Parameters[4]				
Address and control input setup time	t_{ISCA}[15)]	MIN	130	ps
Address and control input hold time	t_{IHCA}[15)]	MIN	130	ps

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[Table 45] LPDDR3 AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
			1866	
CS_n input setup time	t_{ISCS} 15)	MIN	230	ps
CS_n input hold time	t_{IHCS} 15)	MIN	230	ps
Address and control input pulse width	t_{IPWCA}	MIN	0.35	$t_{CK(avg)}$
CS_n input pulse width	t_{IPWCS}	MIN	0.7	$t_{CK(avg)}$
Boot Parameters (10 MHz - 55 MHz) 16),17), 18)				
Clock Cycle Time	t_{CKb}	MAX	100	ns
		MIN	18	
CKE Input Setup Time	t_{ISCKEb}	MIN	2.5	ns
CKE Input Hold Time	t_{IHCKEb}	MIN	2.5	ns
Address and Control Input Setup Time	t_{ISb}	MIN	1150	ps
Address and Control Input Hold Time	t_{IHb}	MIN	1150	ps
DQS Output Data Access Time from CK_t/CK_c	t_{DQSCKb}	MIN	2.0	ns
		MAX	10.0	
Data Strobe Edge to Output Data Edge	t_{DQSQb}	MAX	1.2	ns
Mode Register Parameters				
MODE REGISTER WRITE command period	t_{MRW}	MIN	10	$t_{CK(avg)}$
MODE REGISTER READ command period	t_{MRR}	MIN	4	$t_{CK(avg)}$
Mode register set command delay	t_{MRD}	MIN	Max(14ns, 10tCK)	ns
Core Parameters 19)				
READ latency	RL	MIN	14	$t_{CK(avg)}$
WRITE latency (set A)	WL	MIN	8	$t_{CK(avg)}$
WRITE latency (set B)	WL	MIN	11	$t_{CK(avg)}$
ACTIVATE-to-ACTIVATE command period	t_{RC}	MIN	t_{RAS} + t_{RPab} (with all-bank precharge) t_{RAS} + t_{RPpb} (with per-bank precharge)	ns
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	t_{CKESR}	MIN	Max(15ns, 3t_{CK})	ns
SELF REFRESH exit to next valid command delay	t_{XSR}	MIN	Max (t_{RFCab} + 10ns, 2t_{CK})	ns
Exit power down to next valid command delay	t_{XP}	MIN	Max(7.5ns, 3t_{CK})	ns
CAS-to-CAS delay	t_{CCD}	MIN	4	$t_{CK(avg)}$
Internal READ to PRECHARGE command delay	t_{RTP}	MIN	Max(7.5ns, 4t_{CK})	ns
RAS-to-CAS delay	$t_{RCD(typ)}$	MIN	Max (18ns, 3t_{CK})	ns
Row precharge Time (single bank)	$t_{RPpb\ (typ)}$	MIN	Max (18ns, 3t_{CK})	ns
Row Precharge Time (all banks)	$t_{RPab\ (typ)}$	MIN	Max(21ns, 3t_{CK})	ns
Row active time	t_{RAS}	MIN	Max(42ns, 3t_{CK})	ns
		MAX	Min (9 × t_{REFI} × Refresh rate Multiplier, 70.2) 20)	us
WRITE recovery time	t_{WR}	MIN	Max(15ns, 4t_{CK})	ns
Internal WRITE-to READ command delay	t_{WTR}	MIN	Max(7.5ns, 4t_{CK})	ns
Active bank A to Active bank B	t_{RRD}	MIN	Max(10ns, 2t_{CK})	ns
Four bank ACTIVATE Window	t_{FAW}	MIN	Max(50ns, 8t_{CK})	ns
ODT Parameters				
Asynchronous R_{TT} turn-on delay from ODT input	t_{ODTon}	MIN	1.75	ns
		MAX	3.5	
Asynchronous R_{TT} turn-off delay from ODT input	t_{ODToff}	MIN	1.75	ns
		MAX	3.5	
Automatic R_{TT} turn-on delay after READ data	t_{AODTon}	MAX	t_{DQSCK} + 1.4 × $t_{DQSQ,max}$ + $t_{CK(avg,min)}$	ps

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[Table 45] LPDDR3 AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
			1866	
Automatic R_{TT} turn-off delay after READ data	$t_{AODToff}$	MIN	$t_{DQSCK,min}$ - 300	ps
R_{TT} disable delay from power down, self refresh	t_{ODTd}	MAX	12	ns
R_{TT} enable delay from power down and self refresh exit	t_{ODTe}	MAX	12	ns
CA Training Parameters				
First CA calibration Command after CA calibration mode is programmed	t_{CAMRD}	MIN	20	$t_{CK(avg)}$
First CA calibration Command after CKE is LOW	t_{CAENT}	MIN	10	$t_{CK(avg)}$
CA calibration Exit Command after CKE is HIGH	t_{CAEXT}	MIN	10	$t_{CK(avg)}$
CKE LOW after CA calibration mode is programmed	t_{CACKEL}	MIN	10	$t_{CK(avg)}$
CKE HIGH after the last CA calibration results are driven.	t_{CACKEH}	MIN	10	$t_{CK(avg)}$
Data out delay after CA training calibration command is programmed	t_{ADR}	MAX	20	ns
MRW CA exit command to DQ tri-state	t_{MRZ}	MIN	3	ns
CA calibration command to CA calibration command delay	t_{CACD}	MIN	$RU(t_{ADR}+2 \times t_{CK})$	$t_{CK(avg)}$
Write Leveling Parameters				
DQS_t/DQS_c delay after write leveling mode is programmed	$t_{WLDQSEN}$	MIN	25	ns
First DQS_t/DQS_c edge after write leveling mode is programmed	t_{WLMRD}	MIN	40	ns
Write leveling output delay	t_{WLO}	MAX	20	ns
Write leveling hold time	t_{WLH}	MIN	150	ps
Write leveling setup time	t_{WLS}	MIN	150	ps
Temperature De-Rating[18)]				
DQS output access time from CK_t/CK_c (derated)	t_{DQSCK}	MAX	5620	ps
RAS-to-CAS delay (derated)	t_{RCD}	MIN	t_{RCD} + 1.875	ns
ACTIVATE-to- ACTIVATE command period (derated)	t_{RC}	MIN	t_{RAS} (derated) + t_{RP} (derated)	ns
Row active time (derated)	t_{RAS}	MIN	t_{RAS} + 1.875	ns
Row precharge time (derated)	t_{RP}	MIN	t_{RP} + 1.875	ns
Active bank A to active bank B (derated)	t_{RRD}	MIN	t_{RRD} + 1.875	ns

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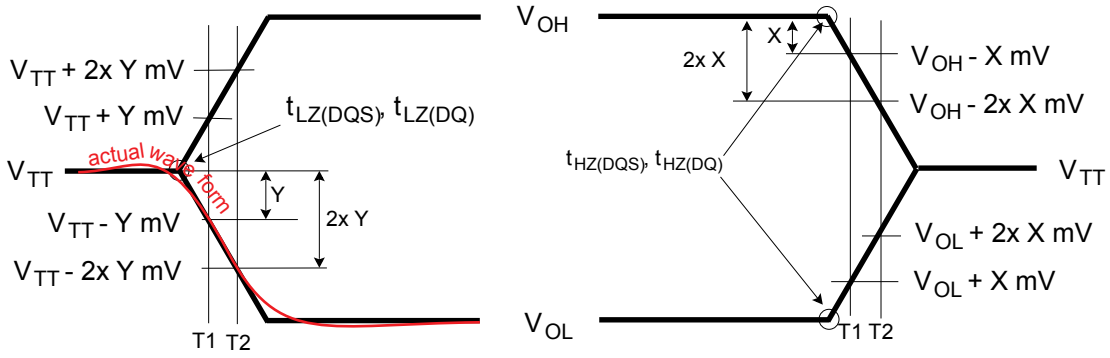
NOTE :

1) Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2) All AC timings assume an input slew rate of 2 V/ns for single ended signals.
3) Measured with 4 V/ns differential CK_t/CK_c slew rate and nominal VIX.
4) READ, WRITE, and Input setup and hold values are referenced to V_{REF}.
5) $t_{DQSCKDS}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. $t_{DQSCKDS}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10'C/s. Values do not include clock jitter.
6) $t_{DQSCKDM}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 1.6us rolling window. $t_{DQSCKDM}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10'C/s. Values do not include clock jitter.
7) $t_{DQSCKDL}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 32ms rolling window. $t_{DQSCKDL}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10'C/s. Values do not include clock jitter.
8) For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Operating and Timing Figure 10. LPDDR3: tDQSCKDM timing shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
9) Output Transition Timing



Start driving point = 2 x T1 - T2

End driving point = 2 x T1 - T2

10) The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.
11) Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge.
12) Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
13) CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK_t/CK_c crossing.
14) CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching a HIGH/LOW voltage level.
15) Input set-up/hold time for signal (CA[9:0], CS_n).
16) To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
17) The LPDDR3 device will set some mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition".
18) The output skew parameters are measured with default output impedance settings using the reference load.
19) The minimum tCK column applies only when tCK is greater than 6ns.
20) Refresh rate multiplier is specified by MR4, OP[2:0].

12.5 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the data sheet t_{IS}(base) and t_{IH}(base) value (see Table 46) to the Δt_{IS} and Δt_{IH} derating value (see Table 48) respectively.

Example: t_{IS} (total setup time) = t_{IS}(base) + Δt_{IS}

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)}$min. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $VIL_{(AC)}$max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to ac region', use nominal slew rate for derating value (see Figure 15). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 17).

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$max and the first crossing of $V_{REF(DC)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$min and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(DC)}$ region', use nominal slew rate for derating value (see Figure 16). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(DC)}$ level is used for derating value (see Figure 18).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC} (see Table 17).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$.

For slew rates in between the values listed in Table 48, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[Table 46] CA Setup and Hold Base-Values

unit [ps]	Data Rate	reference
	1866	
$t_{ISCA\ (base)}$	62.5	$V_{IH/L(ac)} = V_{REF(dc)}$+/-135mV
$t_{IHCA\ (base)}$	80	$V_{IH/L(dc)} = V_{REF(dc)}$+/-100mV

NOTE :
1) ac/dc referenced for 2V/ns CA slew rate and 4V/ns differential CK_t-CK_c slew rate.

[Table 47] CS_n Setup and Hold Base-Values

unit [ps]	Data Rate	reference
	1866	
$t_{ISCS\ (base)}$	162.5	$V_{IH/L(ac)} = V_{REF(dc)}$+/-135mV
$t_{IHCS\ (base)}$	180	$V_{IH/L(dc)} = V_{REF(dc)}$+/-100mV

NOTE :
1) ac/dc referenced for 2V/ns CS_n slew rate and 4V/ns differential CK_t-CK_c slew rate.

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[Table 48] Derating values t_{IS}/t_{IH} - ac/dc based AC150

Δt_{ISCA}, Δt_{IHCA}, Δt_{ISCS}, Δt_{IHCS} derating in [ps] AC/DC based AC150 Threshold -> $V_{IH(AC)}=V_{REF(DC)}+150mV$, $V_{IL(AC)}=V_{REF(DC)}-150mV$ DC100 Threshold -> $V_{IH(DC)}=V_{REF(DC)}+100mV$, $V_{IL(DC)}=V_{REF(DC)}-100mV$													
		CK_t, CK_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE :
1) Cell contents shaded in red are defined as 'not supported'.

[Table 49] Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition for CA

Slew Rate [V/ns]	tVAC [ps] @ 135mV 1866Mbps	
	min	max
> 4.0	40	-
4.0	40	-
3.5	39	-
3.0	36	-
2.5	33	-
2.0	29	-
1.5	21	-
< 1.5	21	-

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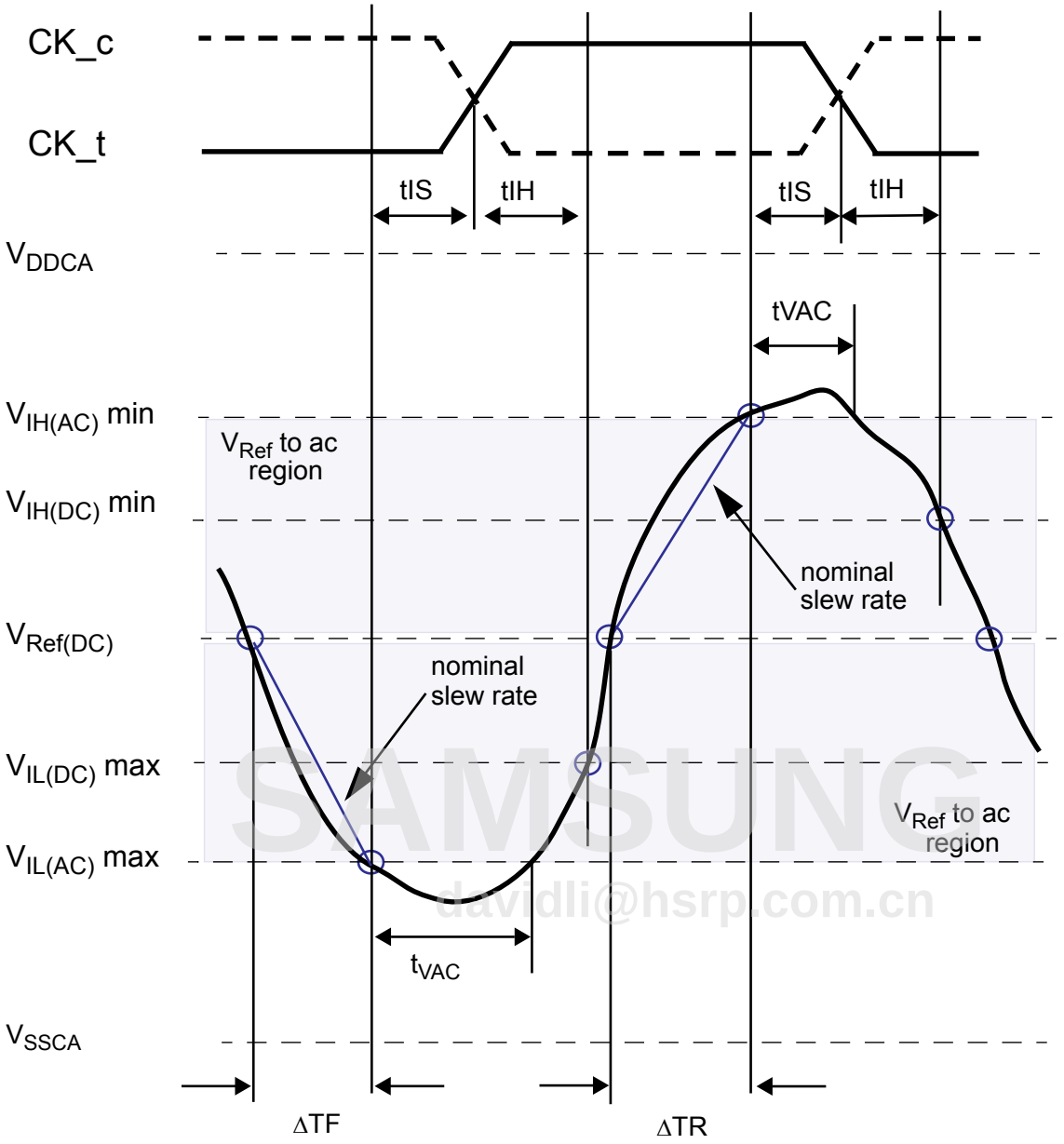

$$\text{Setup Slew Rate Falling Signal} = \frac{V_{Ref(DC)} - V_{IL(AC)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH\ (AC)}min - V_{Ref(DC)}}{\Delta TR}$$

Figure 15. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock.

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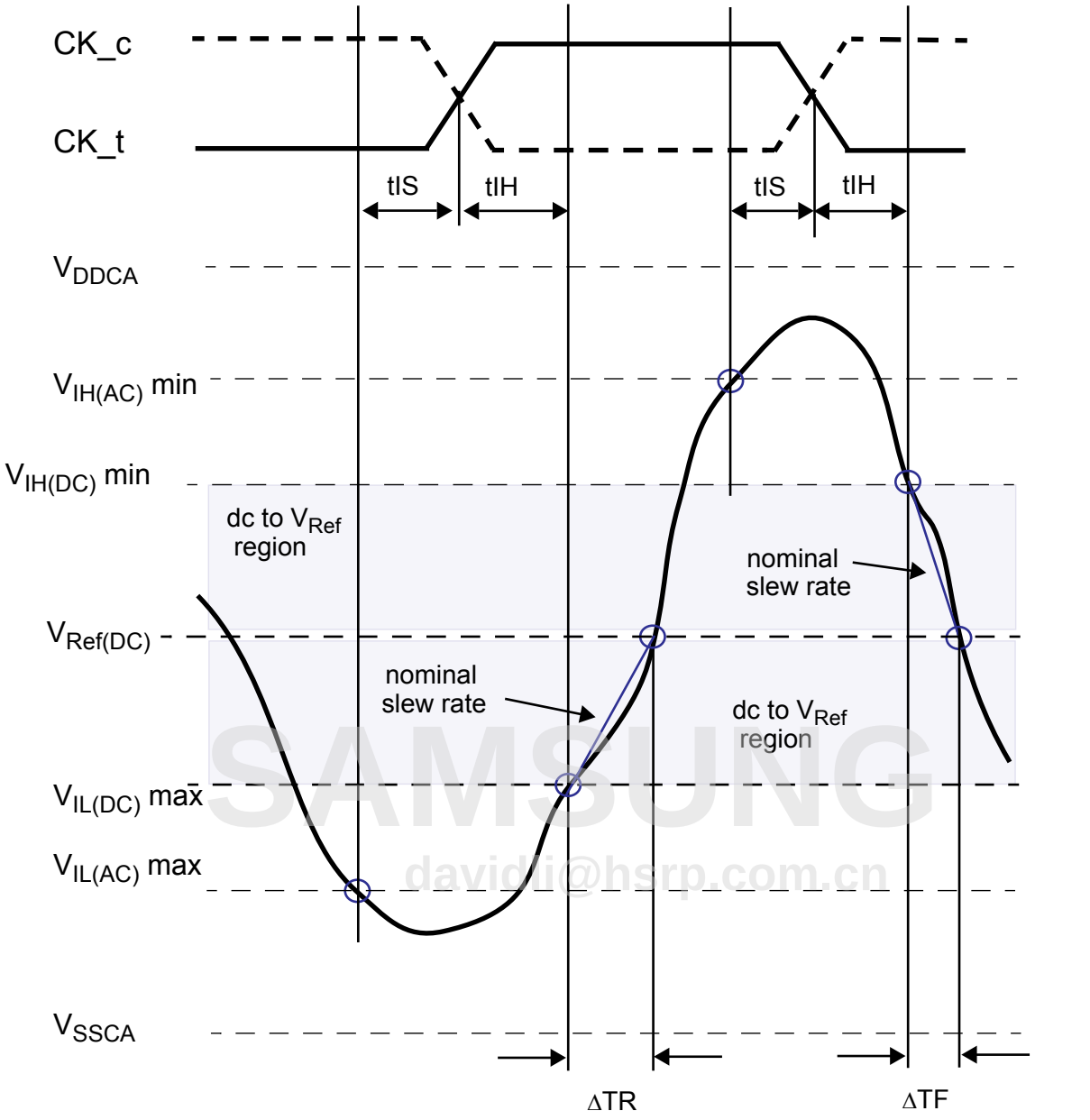

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH\ (DC)}min - V_{Ref(DC)}}{\Delta TF}$$

Figure 16. Illustration of nominal slew rate for hold time t_{IH} for CA and CS_n with respect to clock

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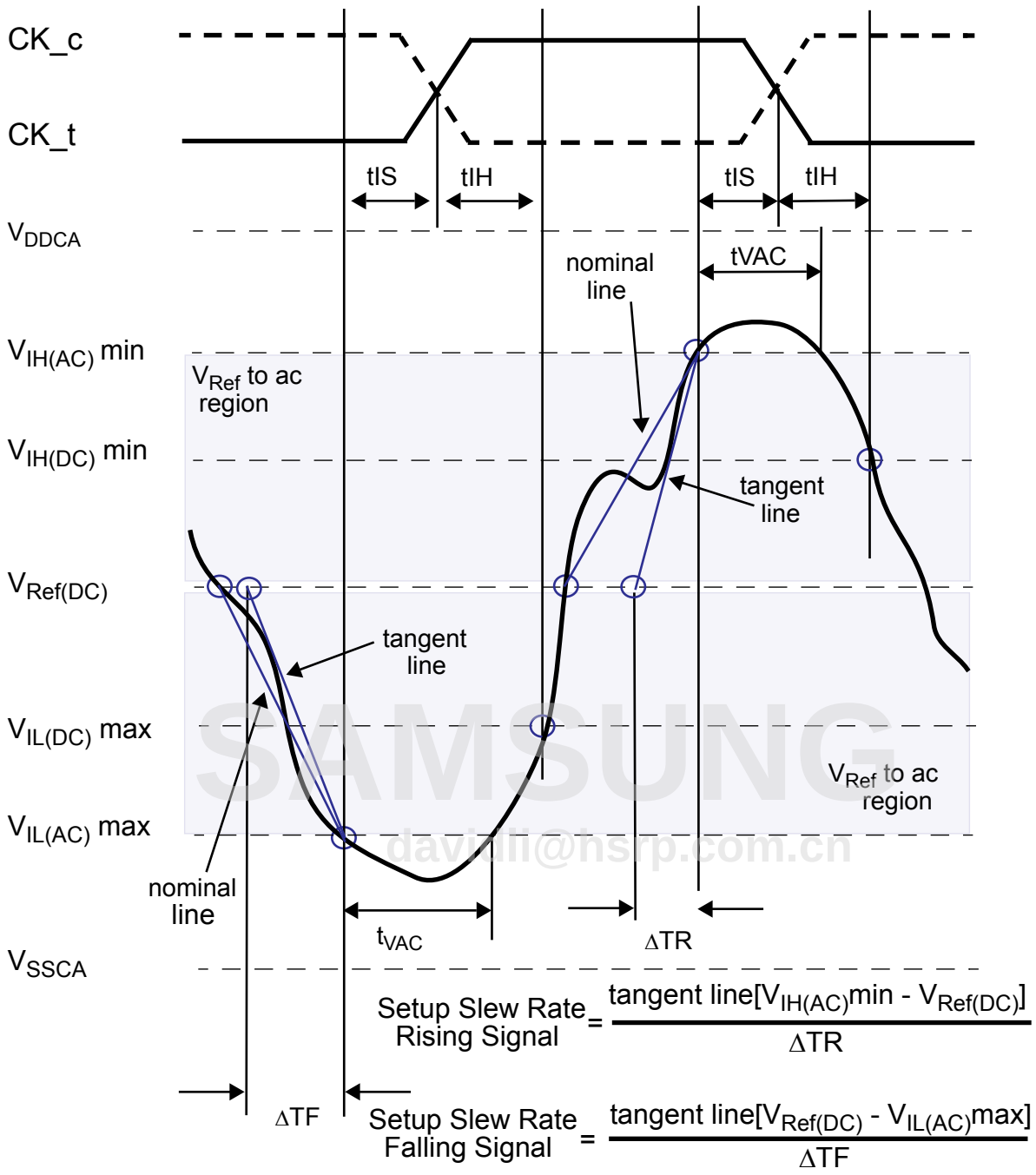
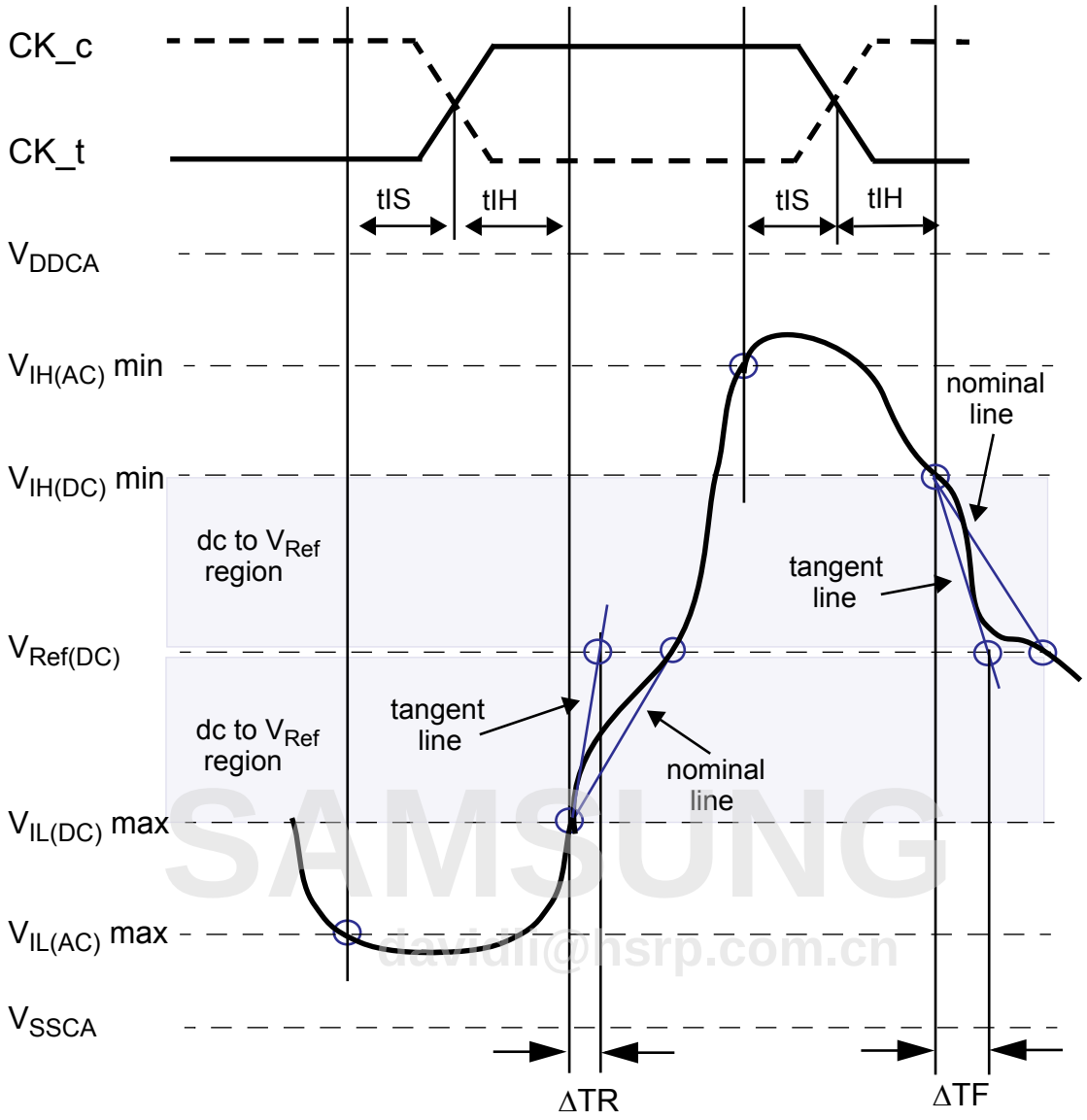


Figure 17. Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref(DC)} - V_{IL(DC)}\text{max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH(DC)}\text{min - } V_{Ref(DC)}\text{]}}{\Delta TF}$$

Figure 18. Illustration of tangent line for hold time t_{IH} for CA and CS_n with respect to clock

12.6 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS (base) and tDH(base) value (see Table 50) to the ΔtDS and ΔtDH (see Table 48) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)}$min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)}$max (see Figure 19). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 21).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$max and the first crossing of $V_{REF(DC)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$min and the first crossing of $V_{REF(DC)}$ (see Figure 20). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(DC)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{Ref(DC)}$ level is used for derating value (see Figure 22).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC} (see Table 17).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization.

[Table 50] Data Setup and Hold Base-Values

[ps]	Data Rate	reference
	1866	
$t_{DS(base)}$	62.5	$V_{IH/L(ac)} = V_{REF(dc)}$+/-135mV
$t_{DH(base)}$	80	$V_{IH/L(dc)} = V_{REF(dc)}$+/-100mV

NOTE :
1) ac/dc referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS_t-DQS_c slew rate and nominal V_{IX}.

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[Table 51] Derating values LPDDR3 t_{DS}/t_{DH} - ac/dc based AC150

ΔtDS, ΔtDH derating in [ps] AC/DC based AC150 Threshold -> $V_{IH(AC)}=V_{REF(DC)}$+150mV, $V_{IL(AC)}=V_{REF(DC)}$-150mV DC100 Threshold -> $V_{IH(DC)}=V_{REF(DC)}$+100mV, $V_{IL(DC)}=V_{REF(DC)}$-100mV													
		DQS_t, DQS_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE :
1) Cell contents shaded in red are defined as 'not supported'.

[Table 52] Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition for DQ, DM

Slew Rate [V/ns]	tVAC [ps] @ 135mV 1866Mbps	
	min	max
> 4.0	40	-
4.0	40	-
3.5	39	-
3.0	36	-
2.5	33	-
2.0	29	-
1.5	21	-
< 1.5	21	-

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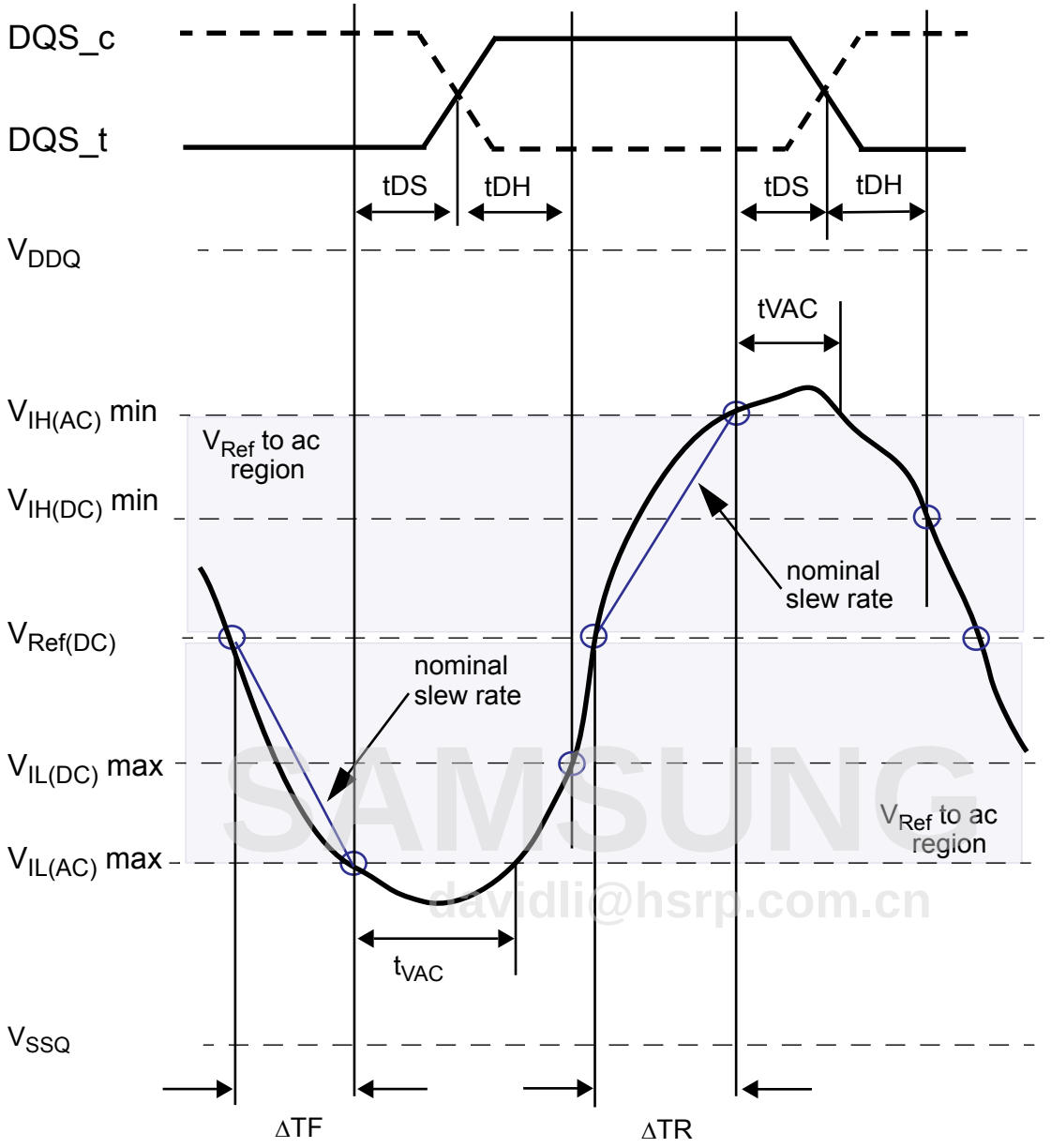

$$\text{Setup Slew Rate Falling Signal} = \frac{V_{Ref(DC)} - V_{IL(AC)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)}min - V_{Ref(DC)}}{\Delta TR}$$

Figure 19. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe

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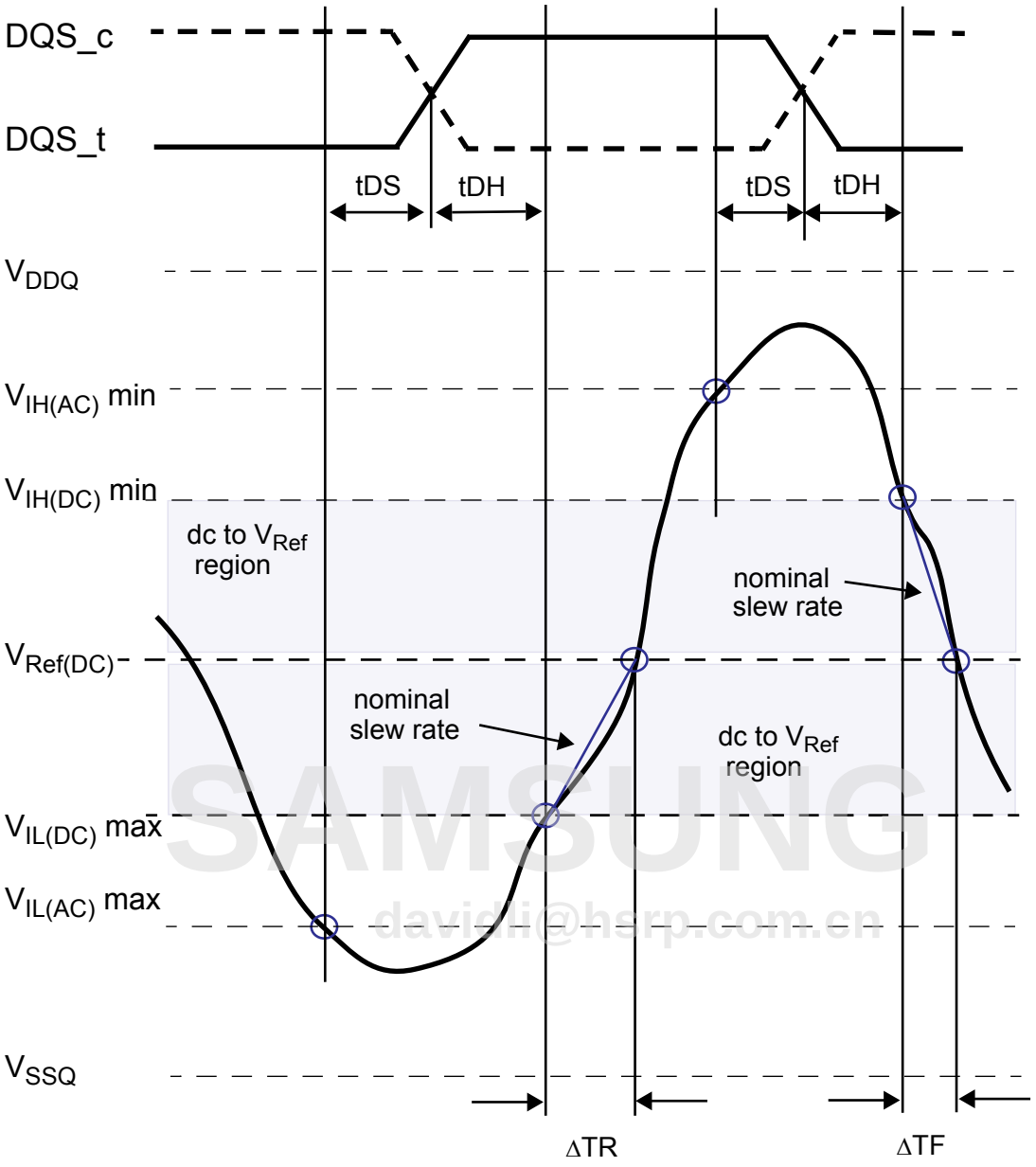

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{Ref(DC)}}{\Delta TF}$$

Figure 20. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

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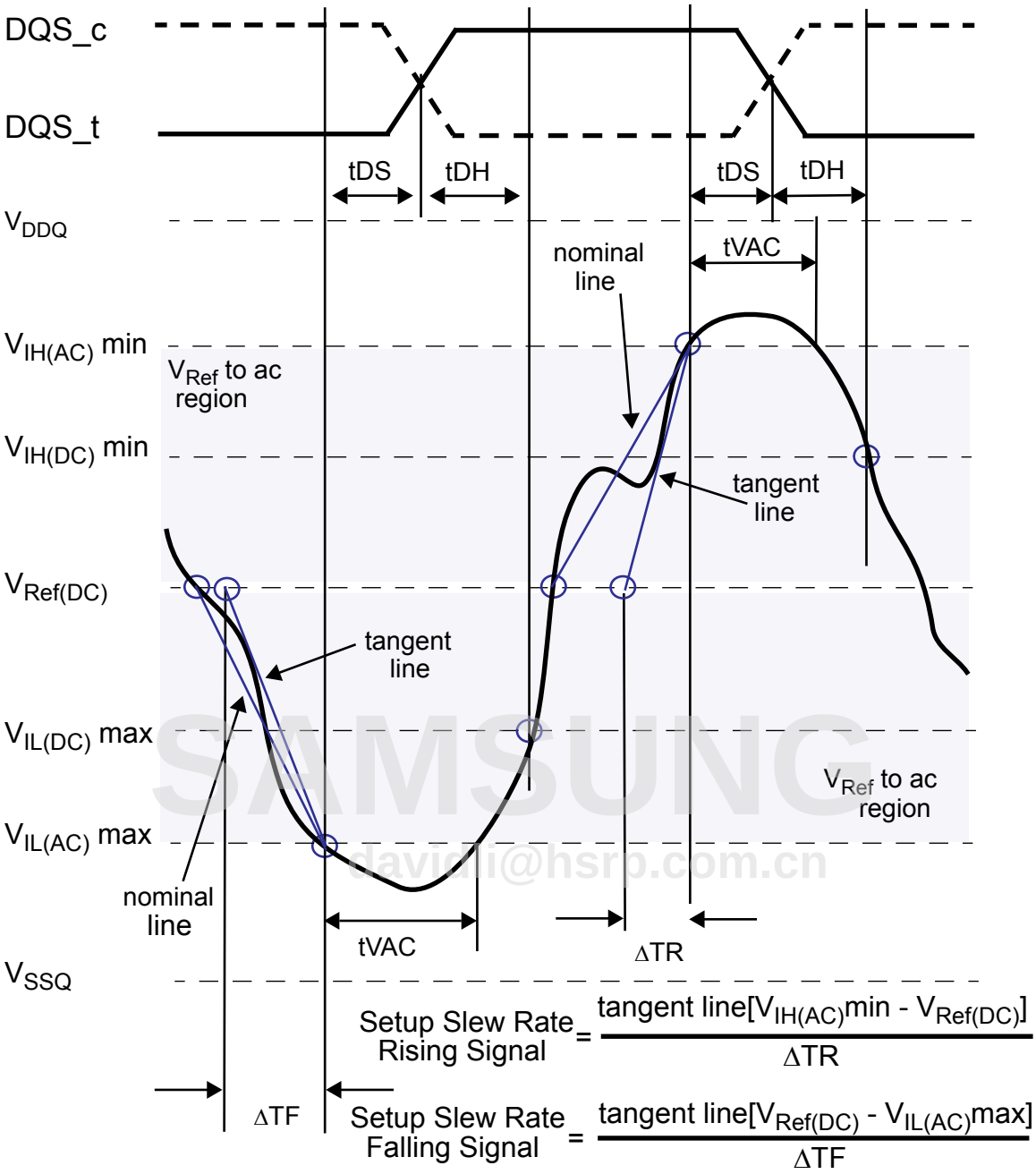
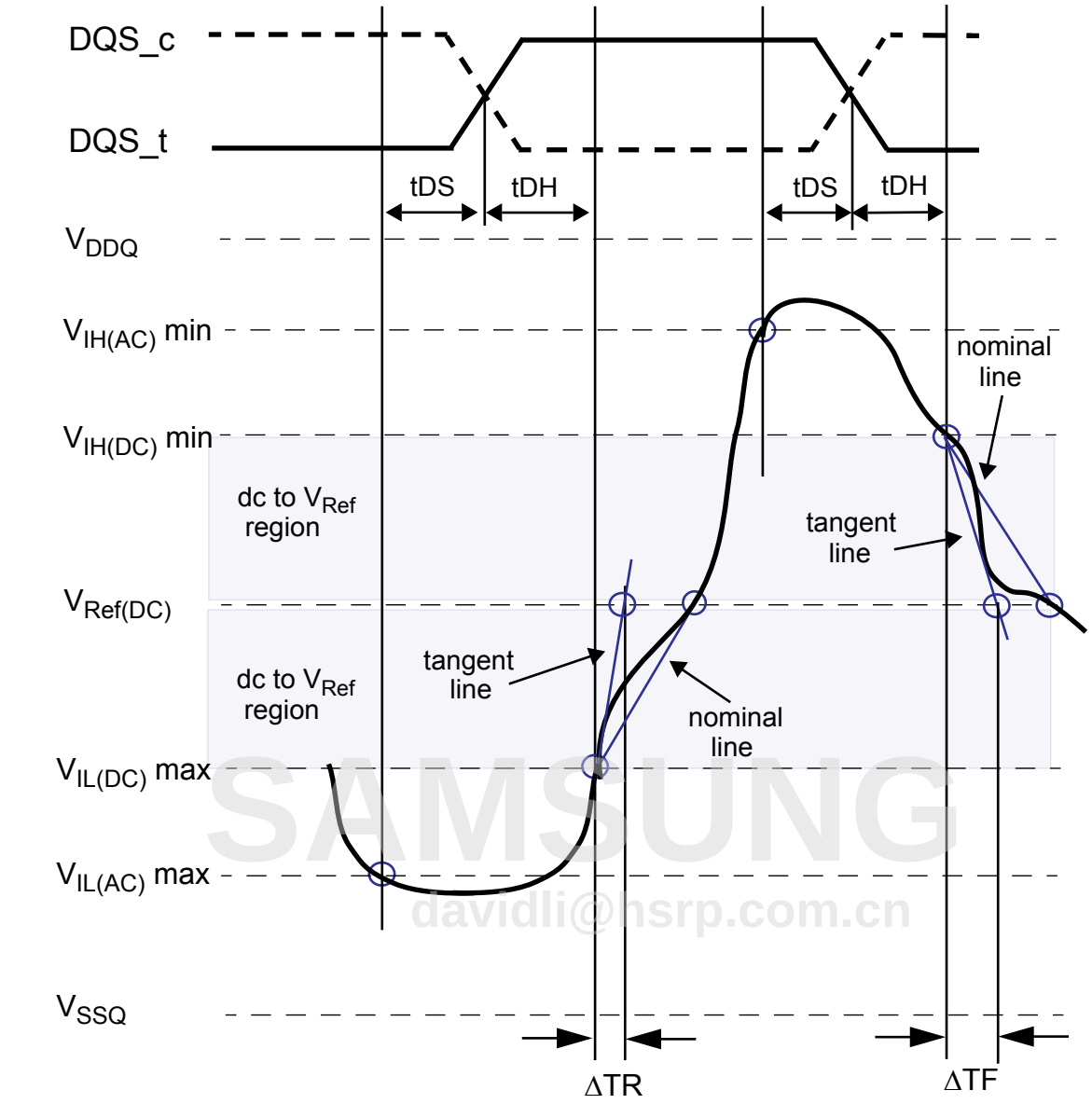


Figure 21. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref(DC)} - V_{IL(DC)}\text{max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH(DC)}\text{min - } V_{Ref(DC)}\text{]}}{\Delta TF}$$

Figure 22. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe

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LPDDR3 SDRAM Command Definitions and Timing Diagrams

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1.0 POWER-UP, INITIALIZATION, AND POWER-OFF

1.1 Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

• Voltage Ramp : While applying power (after Ta), CKE must be held LOW (≤ 0.2 x V_{DDCA}) and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.
Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK_t, CK_c, CS_n and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in Voltage Ramp Conditions table.

[Table 1] Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2-200mV
	VDD1 and VDD2 must be greater than VDDCA-200mV
	VDD1 and VDD2 must be greater than VDDQ-200mV
	VRef must always be less than all other supply voltages

NOTE :
1) Ta is the point when any power supply first reaches 300mV.
2) Noted conditions apply between Ta and power-off (controlled or uncontrolled).
3) Tb is the point at which all supply and reference voltages are within their defined operating ranges.
4) Power ramp duration t_{INIT0} (Tb - Ta) must not exceed 20ms.
5) The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Beginning at Tb, CKE must remain LOW for at least t_{INIT1}, after which CKE can be asserted HIGH. The Clock must be stable at least t_{INIT2} prior to the first CKE LOW-to-HIGH transition(Tc). CKE, CS_n and CA inputs must observe setup and hold requirements(t_{IS}, t_{IH}) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).
If any MRR commands are issued, the clock period must be within the range defined for tCKb. MRW commands can be issued at normal clock frequencies as long as all AC Timings are met. Some AC parameters (for example, t_{DQSCK}) could have relaxed timings (such as t_{DQSCKb}) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least t_{INIT3} (Td). The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{ZQINIT}.

•RESET command : After t_{INIT3} is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least t_{INIT4} while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during time t_{INIT4}.

•MRRs and Device Auto Initialization (DAI) polling: After t_{INIT4} is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. MRR commands are only valid at this time if the CA bus does not need to be trained. CA Training may only begin after time Tf. User may issue MRR command to poll the DAI bit which will indicate if device auto initialization is complete; once DAI bit indicates completion, SDRAM is in idle state. Device will also be in idle state after tINIT5(max) has expired (whether or not DAI bit has been read by MRR command).As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured.
After the DAI bit (MR0, DAI) is set to zero by the memory device(DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than t_{INIT5} after the RESET command. The controller must wait at least $t_{INIT5(MAX)}$ or until the DAI bit is set before proceeding.

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•ZQ Calibration: If CA Training is not required, the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10) after time Tf. If CA Training is required, the CA Training may begin at time Tf. See "Mode Register Write - CA Training Mode" for the CA Training command. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA Training. At the completion of CA Training (Tf'), the MRW initialization calibration(ZQ_CAL) command can be issued to the memory (MR10). This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after t_{ZQINIT}.

•Normal Operation: After t_{ZQINIT} (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.
After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in the LPDDR3 specification.

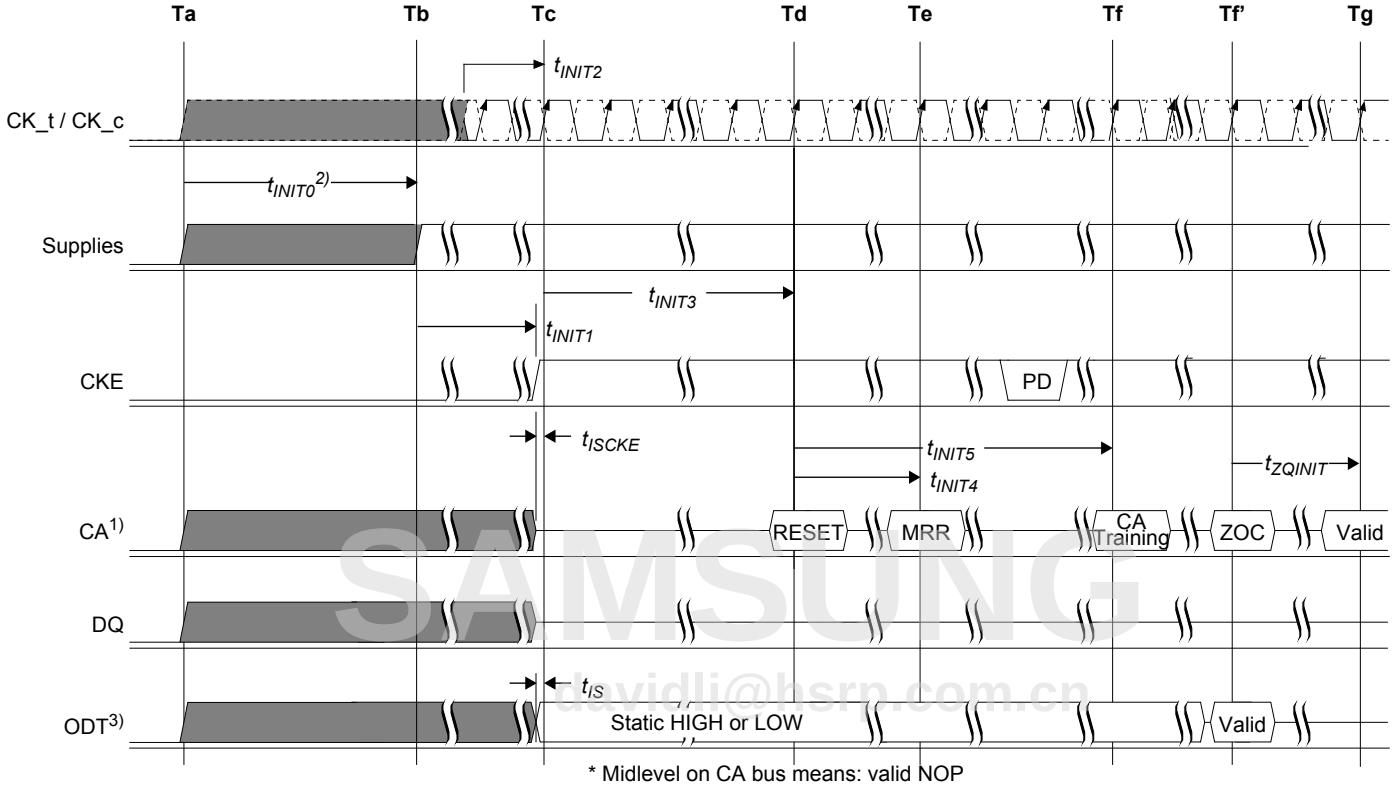

Figure 1: Voltage Ramp and Initialization Sequence

NOTE :
1) High-Z on the CA bus indicates NOP.
2) For t_{INIT} values, see Table 5.
3) After RESET command (time Te), RTT is disabled until ODT function is enabled by MRW to MR11 following Tg.
4) CA Training is optional.

[Table 2] Initialization Timing Parameters

Symbol	Value		Unit	Comment
	min	max		
t_{INIT0}	-	20	ms	Maximum voltage-ramp time
t_{INIT1}	100	-	ns	Minimum CKE LOW time after completion of voltage ramp
t_{INIT2}	5	-	t_{CK}	Minimum stable clock before first CKE HIGH
t_{INIT3}	200	-	µs	Minimum Idle time after first CKE assertion
t_{INIT4}	1	-	µs	Minimum Idle time after RESET command
t_{INIT5} 1)	-	10	µs	Maximum duration of device auto initialization
t_{ZQINIT}	1	-	µs	ZQ initial calibration
t_{CKb}	18	100	ns	Clock cycle time during boot

NOTE :
1) If DAI bit is not read via MRR, SDRAM will be in idle state after tINIT5(max) has expired.

1.1.1 Initialization After RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

1.2 Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK_t, CK_c, CS_n and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

[Table 3] Power Supply conditions

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}-200mV
Tx and Tz	V_{DD1} must be greater than V_{DDCA}-200mV
Tx and Tz	V_{DD1} must be greater than V_{DDQ}-200mV
Tx and Tz	V_{REF} must always be less than all other supply voltages

The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

1.2.1 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz(the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

[Table 4] Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	Min	Max		
t_{POFF}	-	2	s	Maximum Power-Off ramp time

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2.0 ACTIVATE COMMAND

The ACTIVATE command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 to BA2 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at t_{RCD} after the ACTIVATE command is issued. After a bank has been activated it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between ACTIVATE commands to different banks is t_{RRD}.

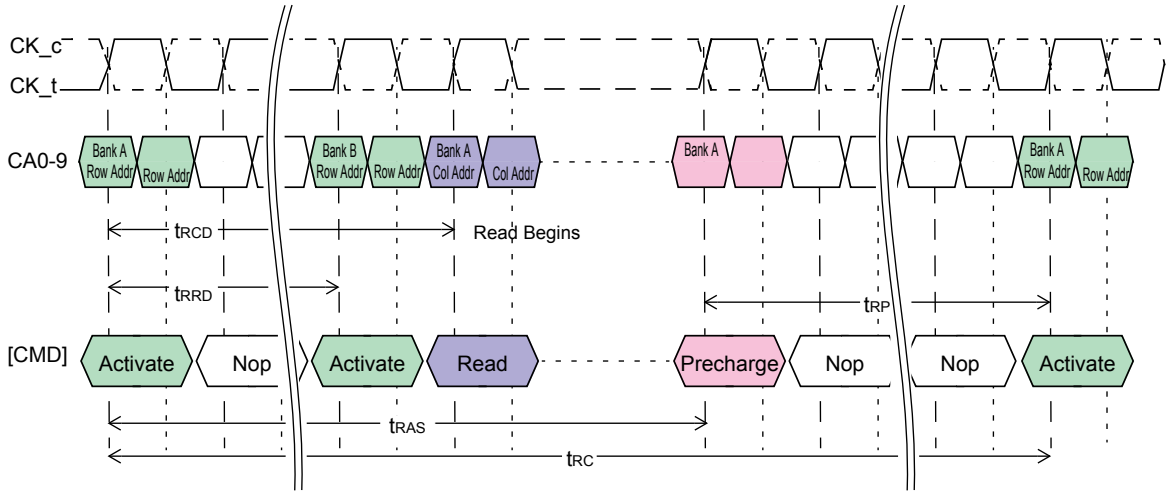

Figure 2: ACTIVATE command

NOTE :
1) A PRECHARGE-all command uses t_{RPab} timing, while a single-bank PRECHARGE command uses t_{RPpb} timing.
In this figure, t_{RP} is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

2.1 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR3 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

- **The 8-Bank Device Sequential Bank Activation Restriction :** No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting to clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(t_{FAW} / t_{CK}) is 10 clocks, and an ACTIVATE command is issued in clock *n*, no more than three further ACTIVATE commands can be issued at or between clock *n*+1 and *n*+9. REFpb also counts as bank activation for purposes of t_{FAW}. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceeds the t_{FAW} time.
- **The 8-Bank Device Precharge All Allowance :** t_{RP} for a PRECHARGE ALL command must equal t_{RPab}, which is greater than t_{RPpb}.

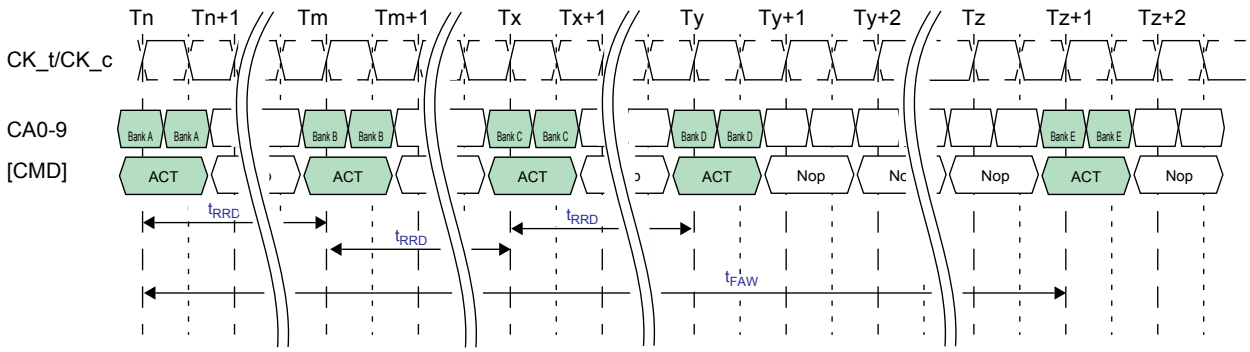

Figure 3: t_{FAW} Timing

3.0 LPDDR3 COMMAND INPUT SIGNAL TIMING DEFINITION

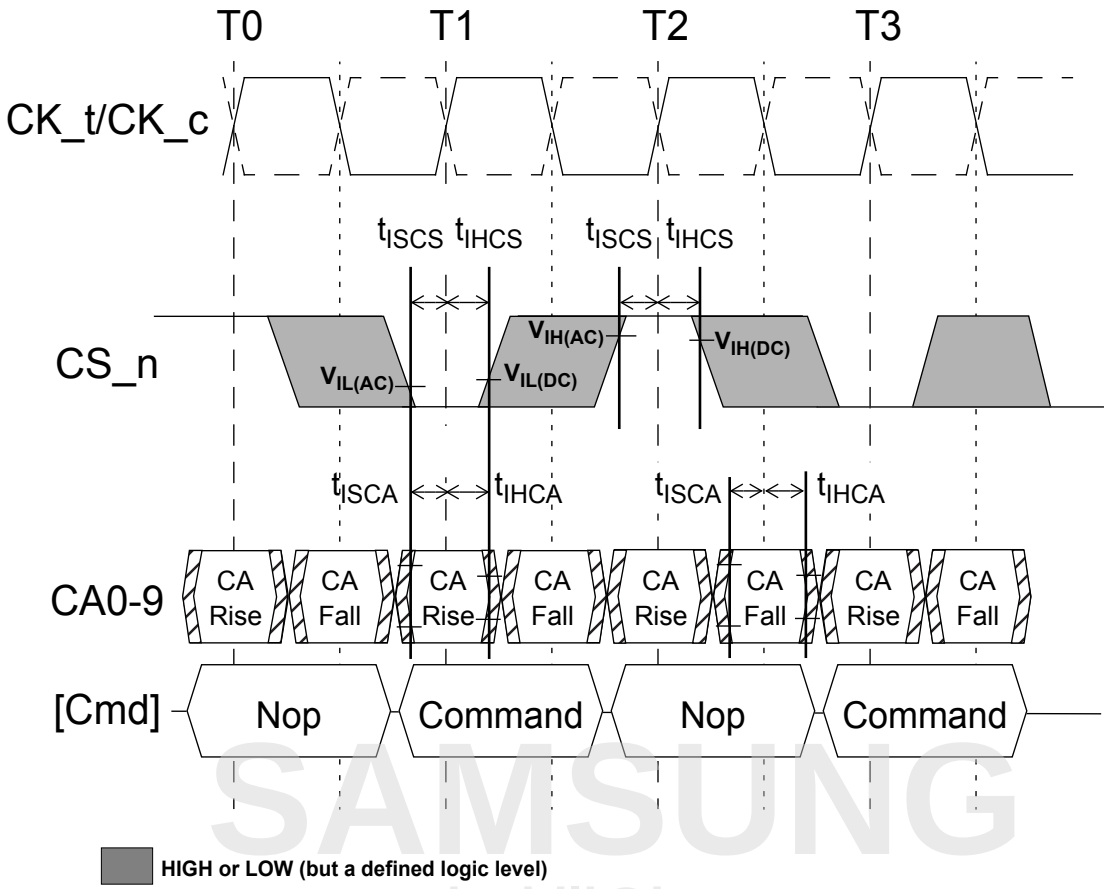

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Figure 4: Command Input Setup and Hold Timing

NOTE :
1) Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

3.1 LPDDR3 CKE Input Setup and Hold Timing

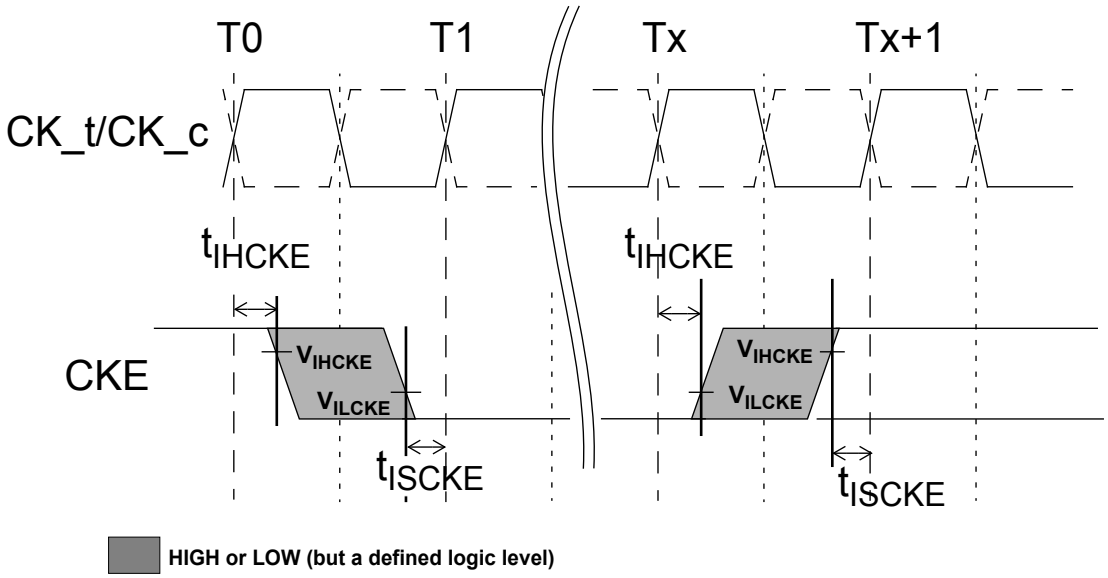

Figure 5: Command Input Setup and Hold Timing

NOTE :
1) After CKE is registered LOW, CKE signal level shall be maintained below V_{ILCKE} for tCKE specification (LOW pulse width).
2) After CKE is registered HIGH, CKE signal level shall be maintained above V_{IHCKE} for tCKE specification (HIGH pulse width).

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4.0 READ AND WRITE ACCESS MODES

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR3 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. Burst interrupts are not allowed.

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5.0 BURST READ OPERATION

The Burst READ command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs CA5r-CA6r and CA1f-CA9f determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid data is available RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock when the READ Command is issued. The data strobe output is driven LOW t_{RPRE} before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

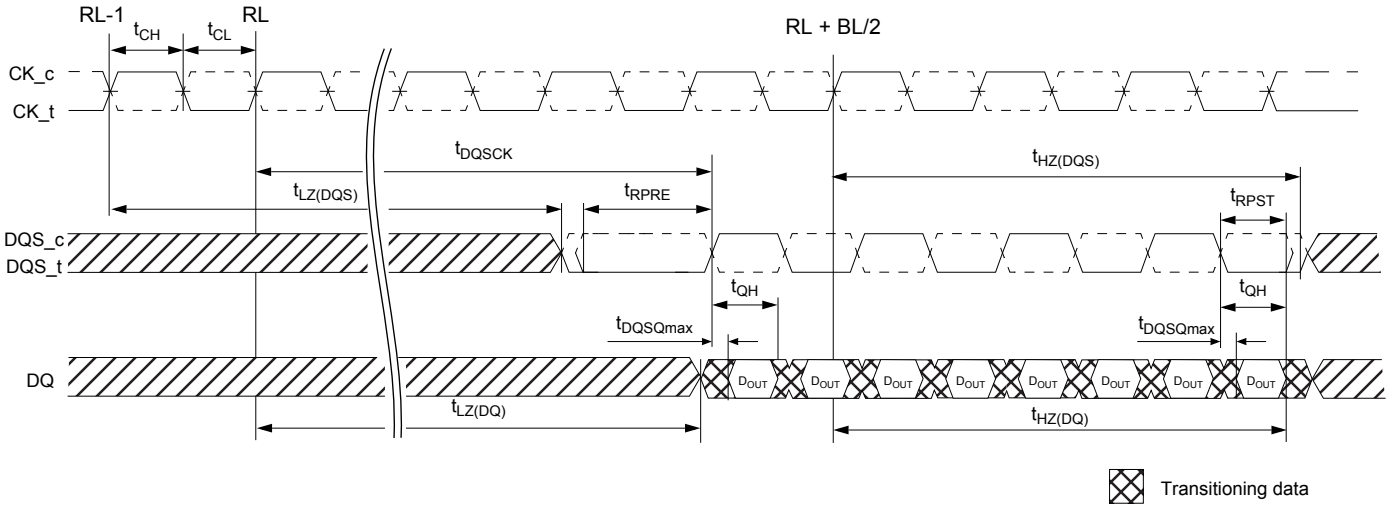


Figure 6: READ Output Timing

NOTE :
1) t_{DQSCK} can span multiple clock periods.
2) An effective burst length of 8 is shown.

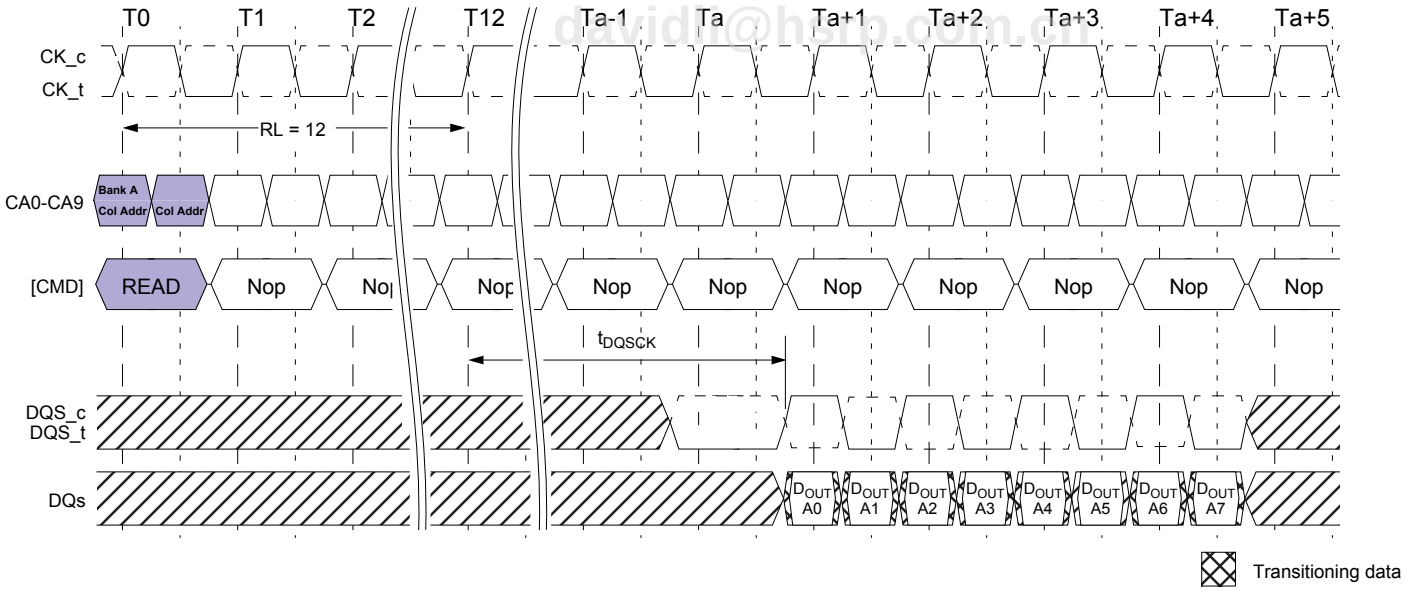


Figure 7: Burst read: RL = 12, BL = 8, t_{DQSCK} > t_{CK}

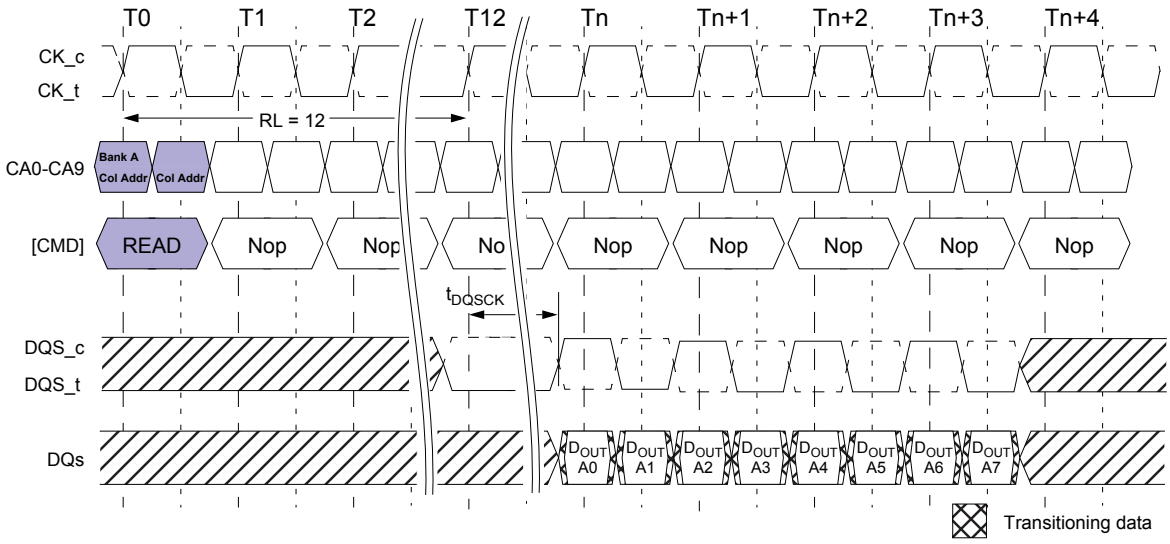
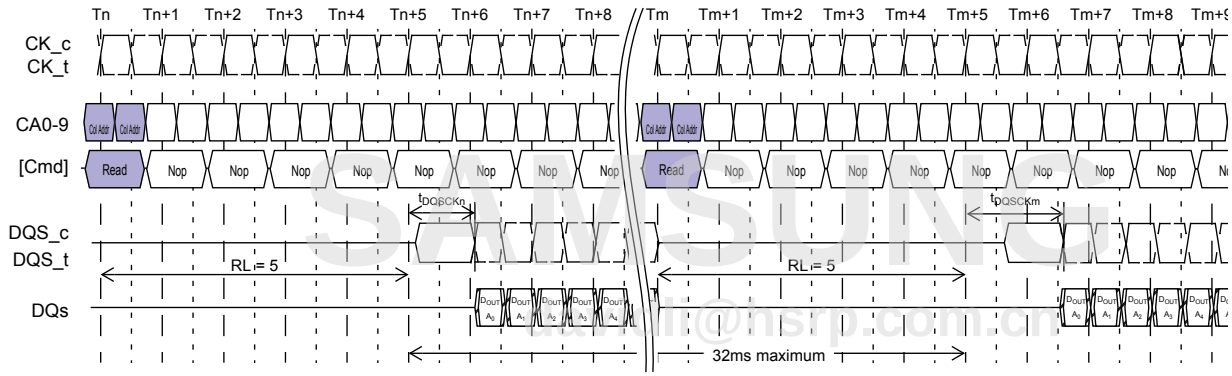


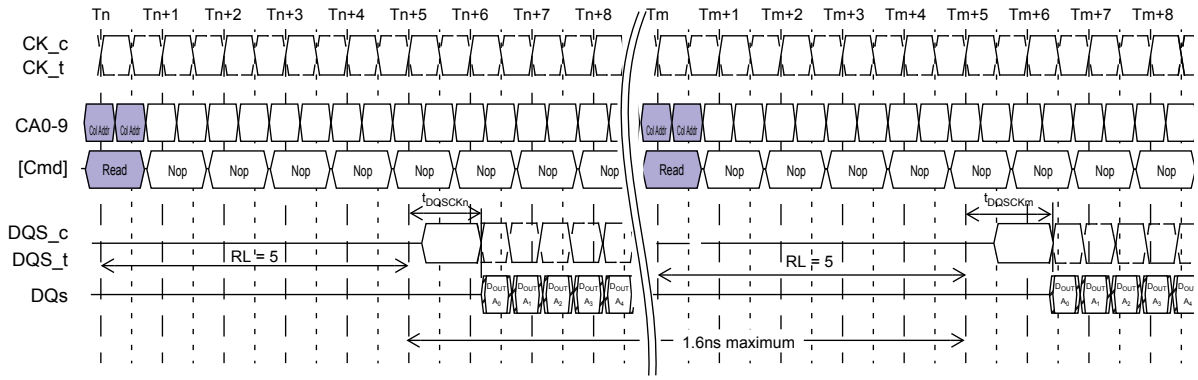
Figure 8: Burst read: RL = 12, BL = 8, $t_{DQSCK} < t_{CK}$



$$t_{DQSCKDL} = | t_{DQSCKn} - t_{DQSCKm} |$$

Figure 9: $t_{DQSCKDL}$ timing

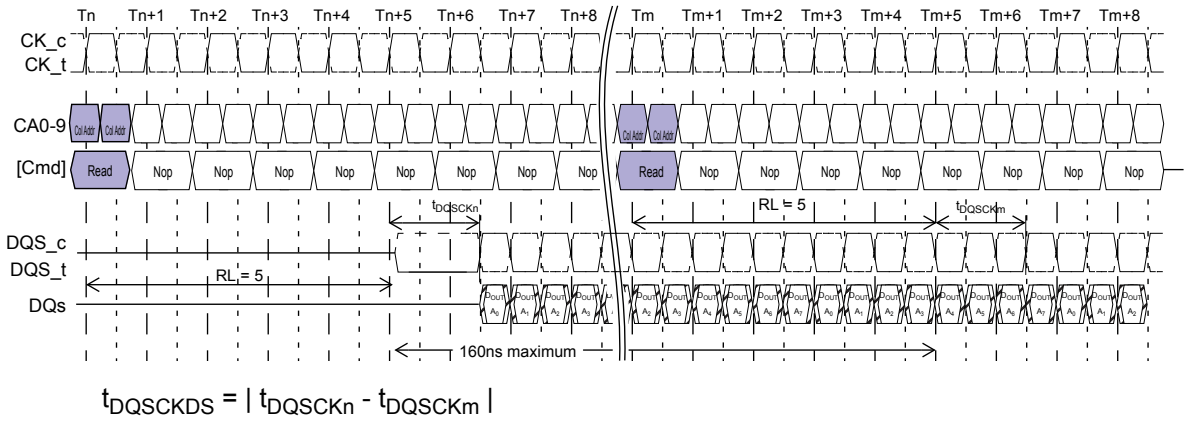
NOTE :
1) $t_{DQSCKDLmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn}, t_{DQSCKm}} pair within any 32ms rolling window.



$$t_{DQSCKDM} = | t_{DQSCKn} - t_{DQSCKm} |$$

Figure 10: LPDDR3: $t_{DQSCKDM}$ timing

NOTE :
1) $t_{DQSCKDMmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn},t_{DQSCKm}} pair within any 1.6us rolling window.



$$t_{DQSCKDS} = | t_{DQSCKn} - t_{DQSCKm} |$$

Figure 11: $t_{DQSCKDS}$ timing

NOTE :
1) $t_{DQSCKDSmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn}, t_{DQSCKm}} pair for reads within a consecutive burst within any 160ns rolling window.

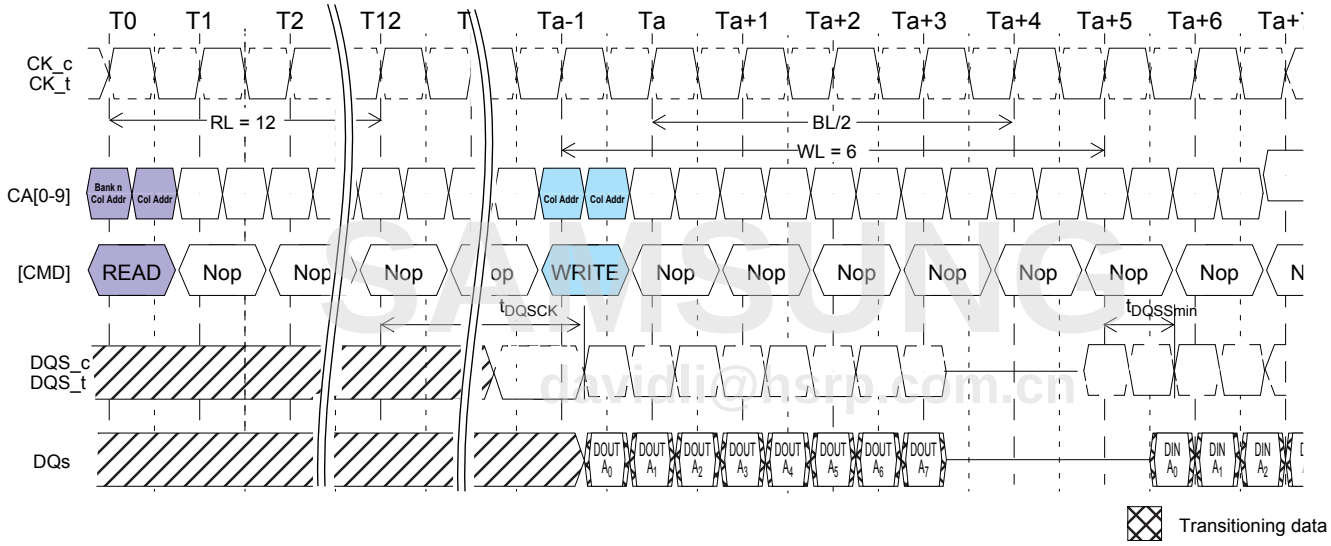


Figure 12: Burst Read Followed By Burst WRITE

The minimum time from the burst read command to the burst WRITE command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum READ-to-WRITE latency is RL + RU($t_{DQSCK(MAX)}$/t_{CK}) + BL/2 + 1 - WL clock cycles.

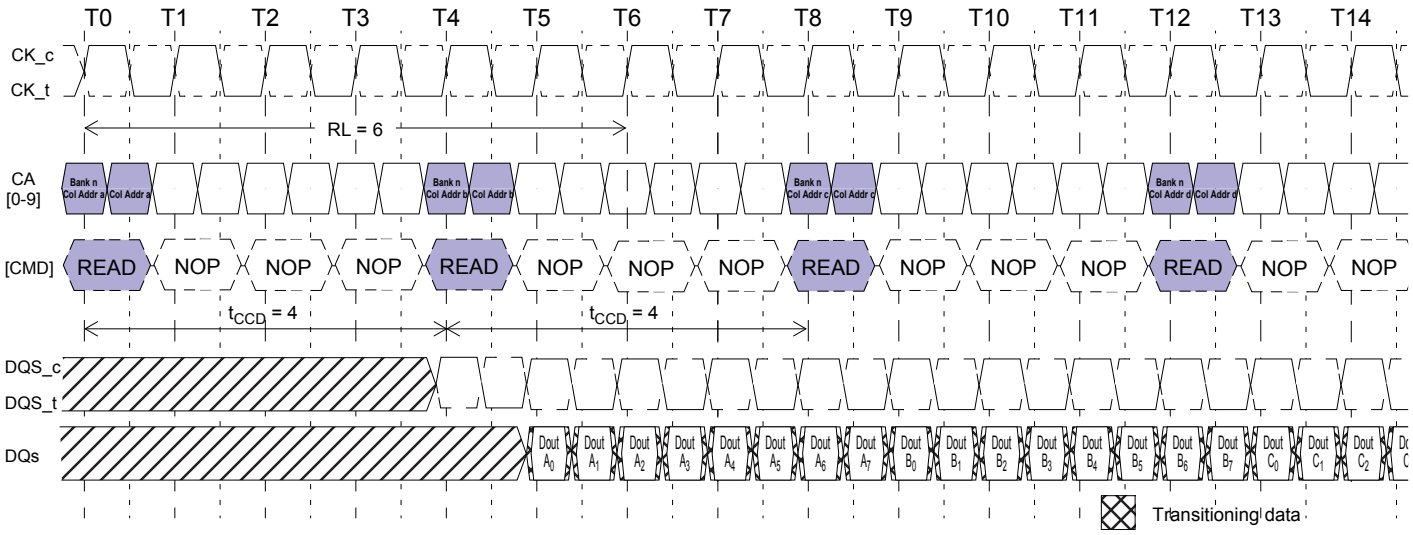


Figure 13: Seamless Burst Read:

The seamless burst READ operation is supported by enabling a READ command at every fourth clock cycle for BL = 8 operation.
This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

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6.0 BURST WRITE OPERATION

The Burst WRITE command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. Write Latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the t_{DQSS} delay is measured. The first valid data must be driven WL * t_{CK} + t_{DQSS} from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven for time t_{WPRE} prior to data input. The burst cycle data bits must be applied to the DQ pins t_{DS} prior to the associated edge of the DQS and held valid until t_{DH} after that edge.

Burst data is sampled on successive edges of the DQS until the 8-bit burst length is completed. After a burst WRITE operation, t_{WR} must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

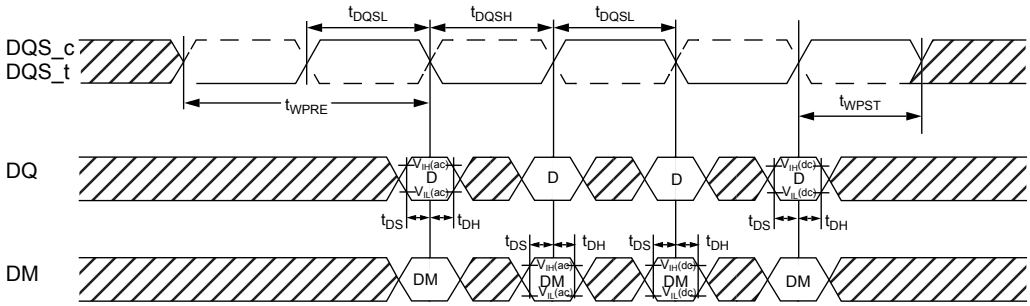

Figure 14: Data input (write) timing

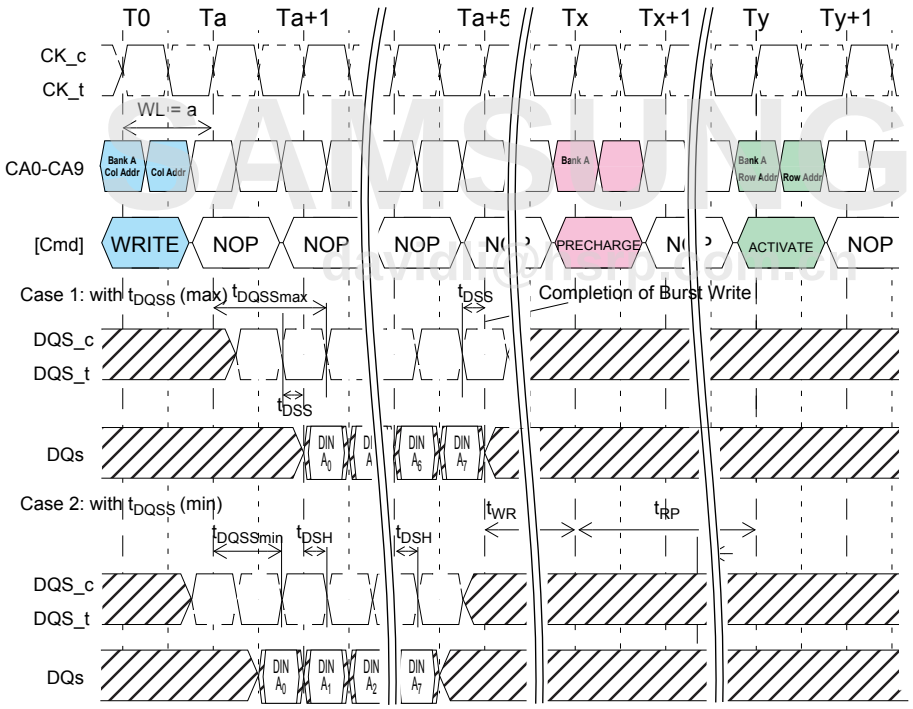

Figure 15: LPDDR3: Burst write

6.1 tWPRE Calculation

The method for calculating t_{WPRE} is shown in the following figure:

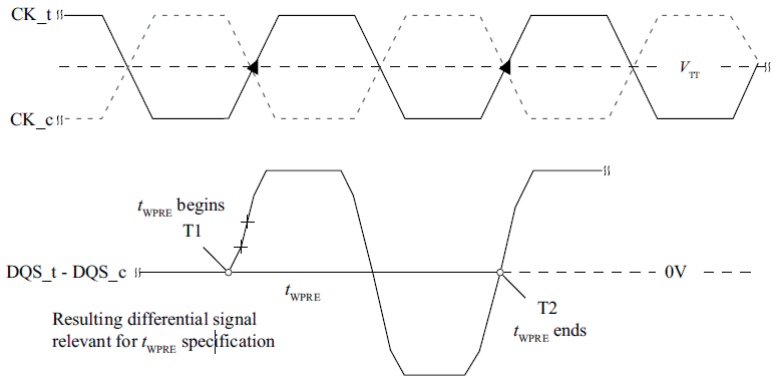

Figure 16: Method for Calculating t_{WPRE} Transitions and Endpoints

6.2 tWPST Calculation

The method for calculating t_{WPST} is shown in the follwing figure:

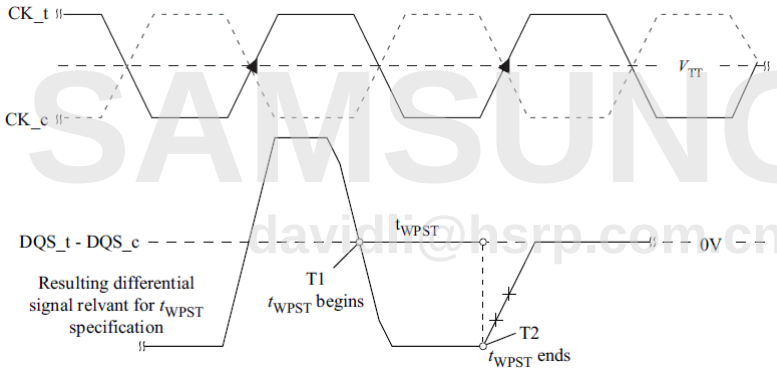

Figure 17: Method for Calculating t_{WPST} Transitions and Endpoints

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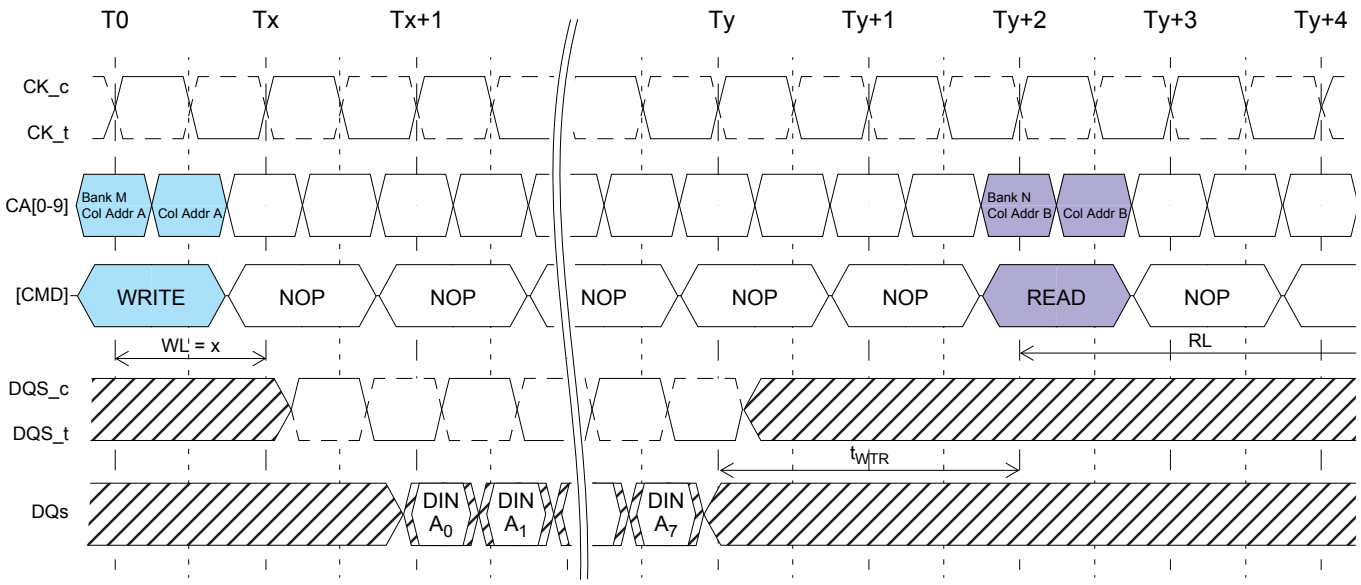

Figure 18: LPDDR3: Burst Write Followed By Burst Read

NOTE :
1) The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].
2) t_{WTR} starts at the rising edge of the clock after the last valid input datum.

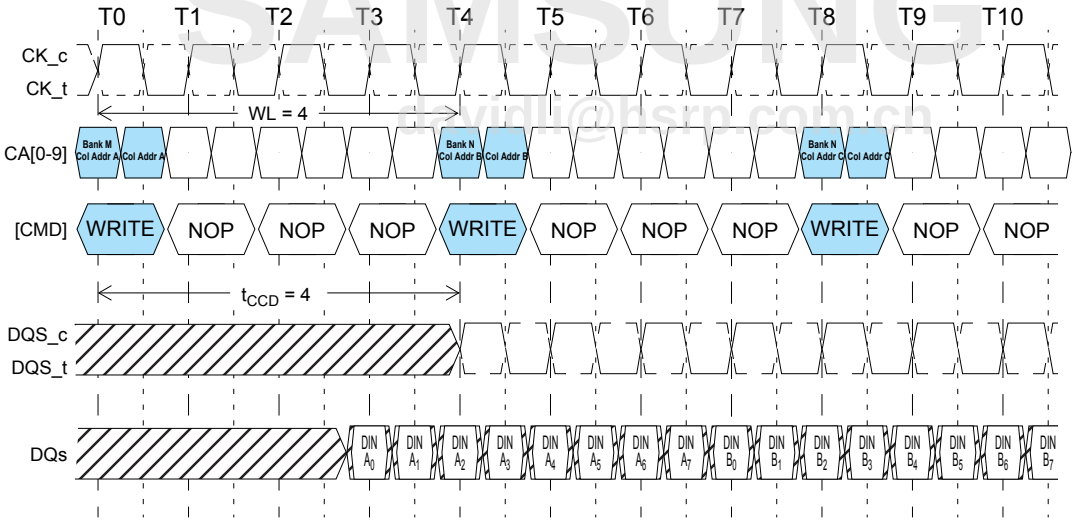

Figure 19: LPDDR3: Seamless burst write: WL = 4, t_{CCD} = 4

NOTE :
1) The seamless burst write operation is supported by enabling a write command every four clocks for BL = 8 operation. This operation is allowed for any activated bank.

7.0 WRITE DATA MASK

On LPDDR3 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on Mobile DDR SDRAMs. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data-mask loading is identical to data-bit loading to ensure matched system timing.

For data mask timing.

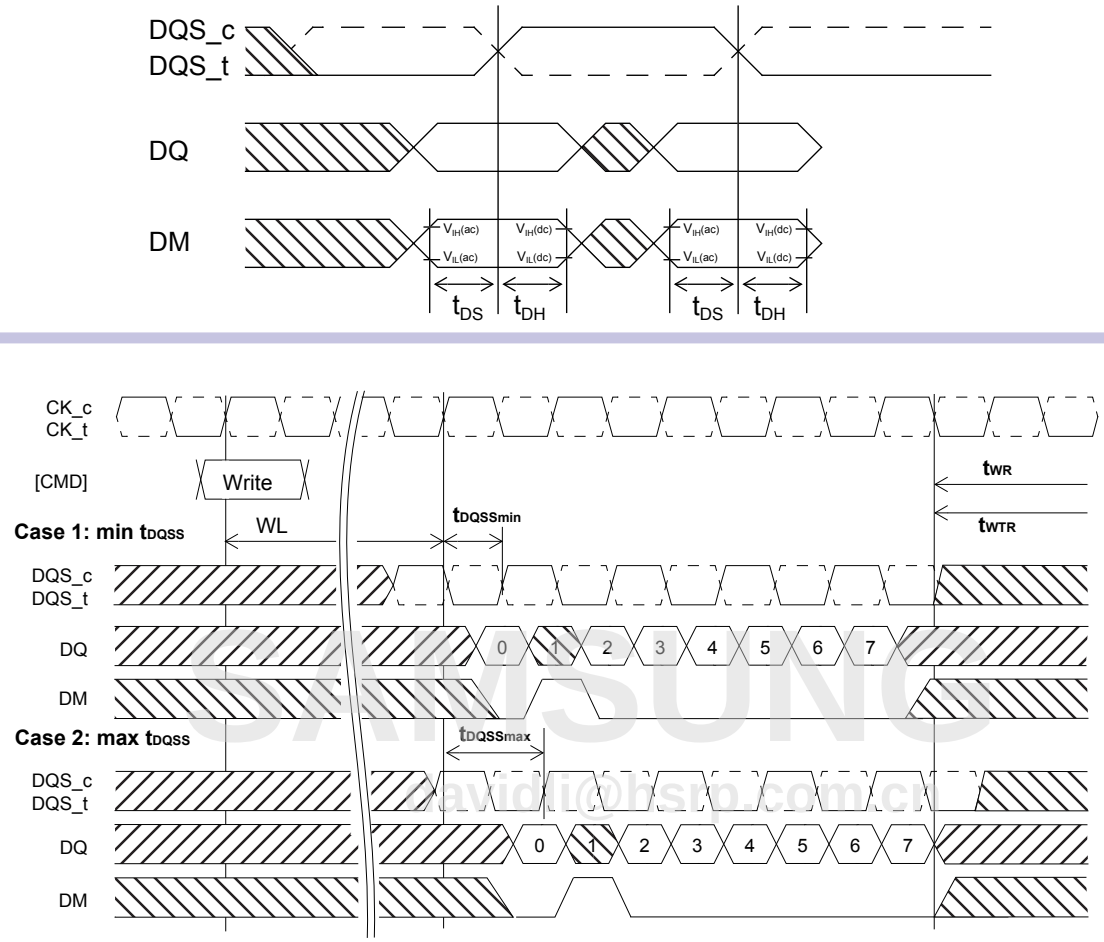

Figure 20: Data Mask Timing

NOTE :
1) For the data mask function, BL = 8 is shown; the second data bit is masked.

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8.0 PRECHARGE OPERATION

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE Command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharge bank(s) will be available for subsequent row access t_{RPab} after an all-bank PRECHARGE command is issued, or t_{RPpb} after a single-bank PRECHARGE command is issued.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row precharge time for an all-bank PRECHARGE (t_{RPab}) will be longer than the row PRECHARGE time for a single-bank PRECHARGE (t_{RPpb}). ACTIVATE to PRECHARGE timing is shown in Figure 24 Burst read followed by Precharge.

[Table 5] Bank Selection for PRECHARGE by Address Bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s)
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don't care	Don't care	Don't care	All banks

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8.1 Burst Read operation followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (t_{RP}) has elapsed. A PRECHARGE command cannot be issued until after t_{RAS} is satisfied. The minimum READ-to-PRECHARGE time must also satisfy a minimum analog time from the rising clock edge that initiates the last 8-bit prefetch of a READ command. tRPT begins BL/2-4 clock cycles after the READ command. For LPDDR3 READ-to-PRECHARGE timings see Table 5 Precharge & Auto Precharge clarification.

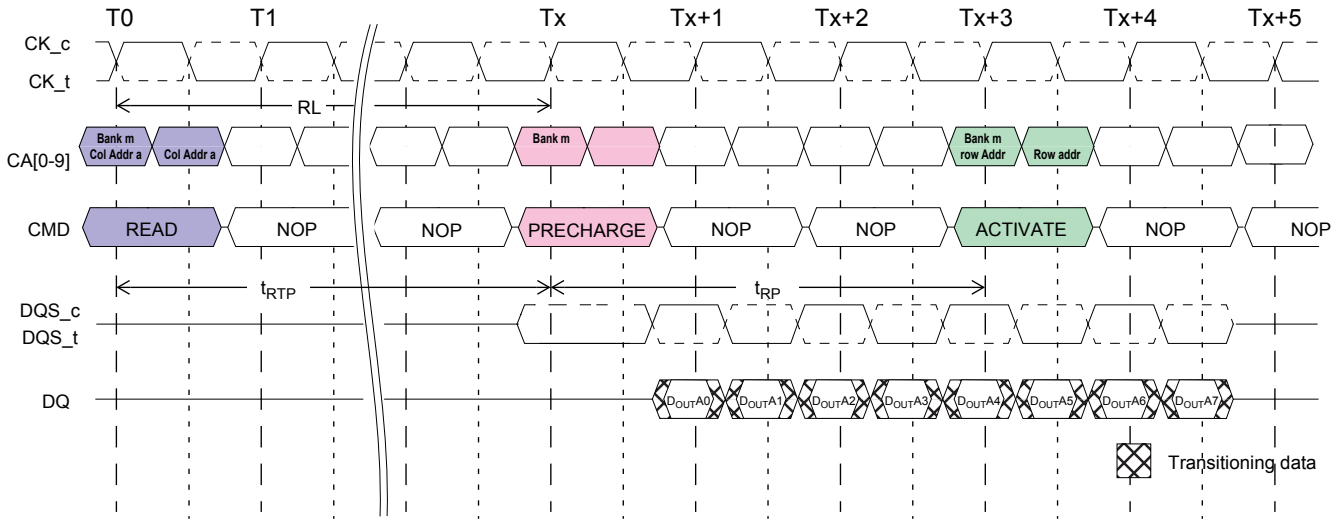

Figure 21: LPDDR3: Burst READ Followed by PRECHARGE

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8.2 Burst WRITE Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (tWR) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. A PRECHARGE command must not be issued prior to the tWR delay. For LPDDR3 WRITE-to-PRECHARGE timings see Table 2, “LPDDR3: PRECHARGE and Auto Precharge Clarification,”.

LPDDR3 devices write data to the array in prefetch multiples(prefetch = 8). An internal WRITE operation can only begin after a prefetch group has been completely latched, so tWR starts at prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(t_{WR}/t_{CK}) clock cycles.

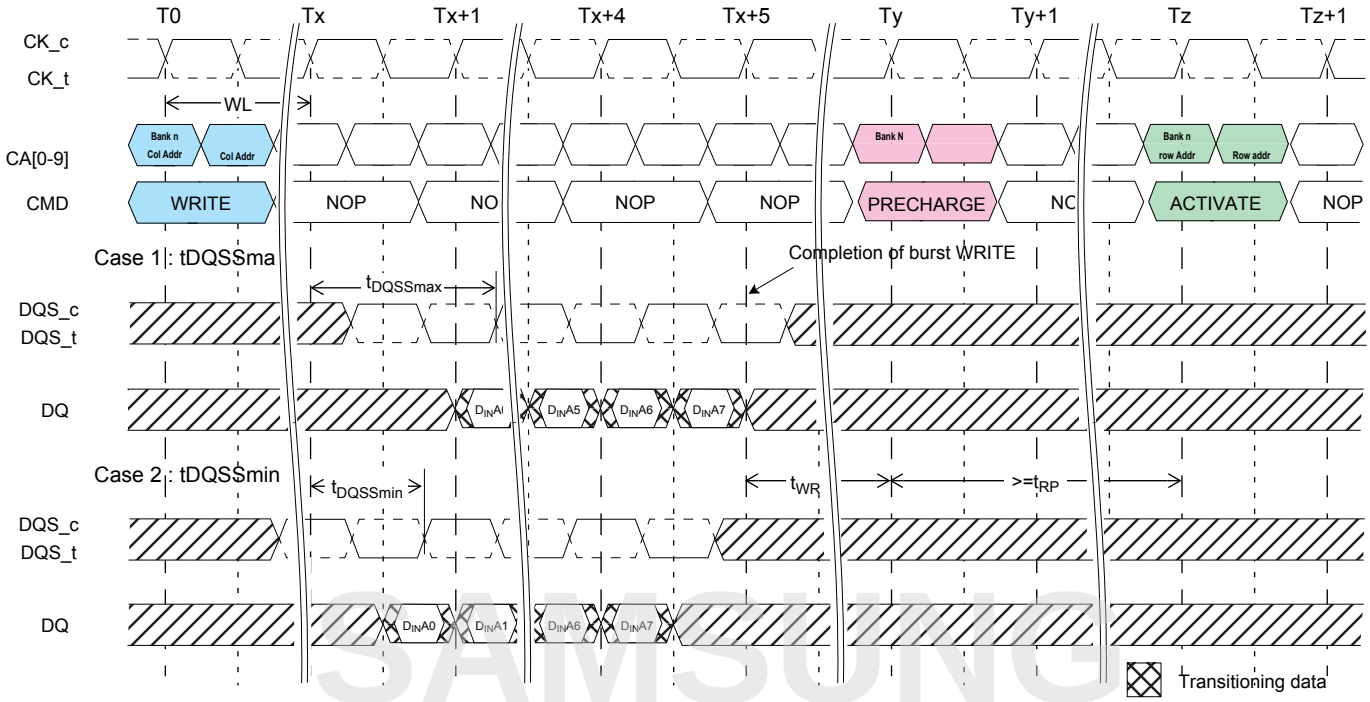

Figure 22: LPDDR3: Burst WRITE Followed by PRECHARGE

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8.3 Auto PRECHARGE operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or a WRITE command is issued to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency) thus improving system performance for random data access.

8.4 Burst READ with Auto-PRECHARGE

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto-precharge function is engaged.

LPDDR3 devices start an auto-precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(t_{RTP}/t_{CK}) clock cycles later than the READ with auto precharge command, whichever is greater. For LPDDR3 auto-precharge calculations see Table 5 Precharge & Auto Precharge clarification. Following an auto-precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

a) The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto-precharge begins.

b) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

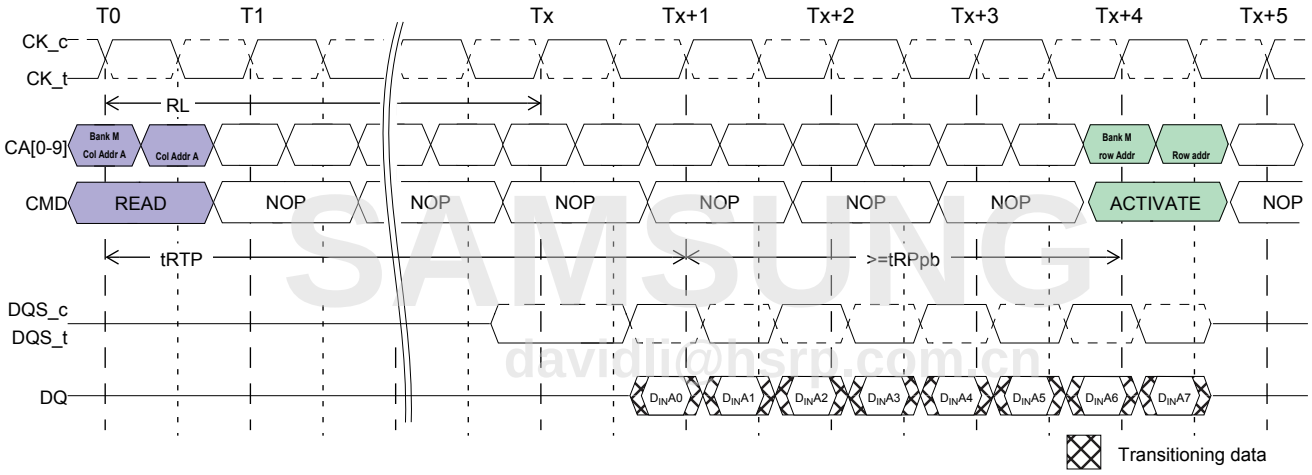

Figure 23: Burst READ with Auto-Precharge

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8.5 Burst WRITE with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge on the rising edge t_{WR} cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto-precharge begins.

The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

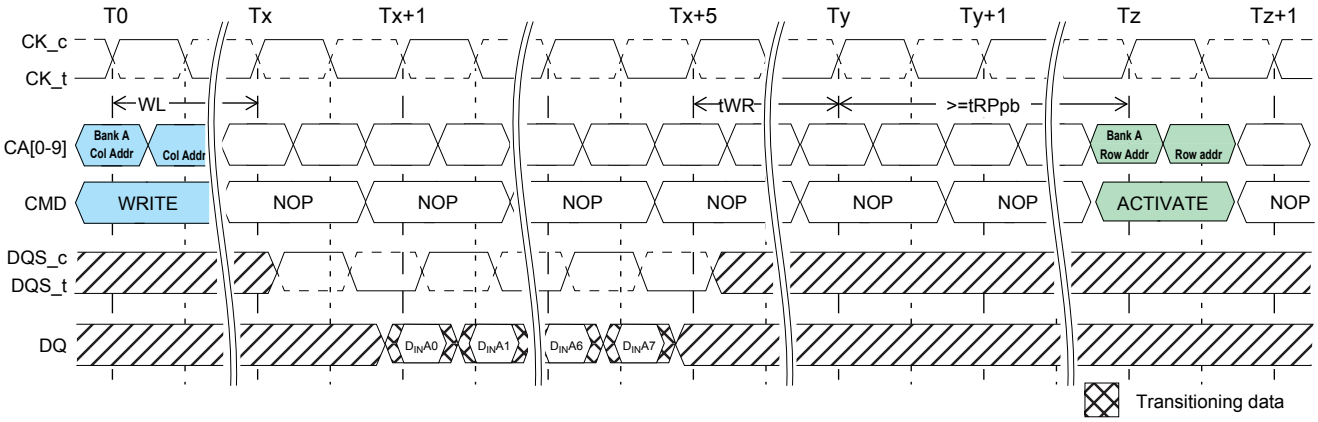

Figure 24: Burst WRITE with Auto Precharge

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[Table 6] PRECHARGE & Auto Precharge Clarification

From Command	To Command	Minimum Delay Between "From Command" to "To Command"	Unit	Notes
READ	PRECHARGE (to same Bank as READ)	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1
	PRECHARGE ALL	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1
READ w/ AP	PRECHARGE (to same Bank as READ w/ AP)	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1,2
	PRECHARGE ALL	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1
	ACTIVATE (to same Bank as READ w/ AP)	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4 + RU(t_{RPpb}/t_{CK})	clks	1
	WRITE or WRITE w/ AP (same bank)	Illegal	clks	3
	WRITE or WRITE w/ AP (different bank)	RL + BL/2 + RU($t_{DQSCKmax}/t_{CK}$) - WL + 1	clks	3
	READ or READ w/ AP (same bank)	Illegal	clks	3
	READ or READ w/ AP (different bank)	BL/2	clks	3
WRITE	PRECHARGE (to same Bank as WRITE)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
WRITE w/ AP	Precharge (to same Bank as Write w/ AP)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	PRECHARGE ALL	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	ACTIVATE (to same Bank as WRITE w/ AP)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPpb}/t_{CK})	clks	1
	WRITE or WRITE w/ AP (same bank)	Illegal	clks	3
	WRITE or WRITE w/ AP (different bank)	BL/2	clks	3
	READ or READ w/ AP (same bank)	Illegal	clks	3
	READ or READ w/ AP (different bank)	WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1	clks	3
PRECHARGE	PRECHARGE (to same Bank as PRECHARGE)	1	clks	1
	PRECHARGE ALL	1	clks	1
PRECHARGE All	PRECHARGE	1	clks	1
	PRECHARGE ALL	1	clks	1

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NOTE :
1) For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command, either one bank PRECHARGE or PRECHARGE ALL, issued to that bank. The PRECHARGE period is satisfied after t_{RP} depending on the latest PRECHARGE command issued to that bank.
2) Any command issued during the minimum delay time as specified in Table 6 is illegal.
3) After READ with AP, seamless READ operations to different banks are supported. After WRITE with AP, seamless WRITE operations to different banks are supported. READ and Write operations may not be truncated or interrupted.

9.0 REFRESH COMMAND

The Refresh command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command. A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met (see Table 7)

a) t_{RFCab} has been satisfied after the prior REFab command

b) t_{RFCpb} has been satisfied after the prior REFpb command

c) t_{RP} has been satisfied after the prior PRECHARGE command to that bank

d) t_{RRD} has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessable during per-bank REFRESH cycle time (t_{RFCpb}), however, other banks within the device are accessable and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the Idle state.

After issuing REFpb, these conditions must be met (see Table 7)

a) t_{RFCpb} must be satisfied before issuing a REFab command

b) t_{RFCpb} must be satisfied before issuing an ACTIVATE command to the same bank

c) t_{RRD} must be satisfied before issuing an ACTIVATE command to a different bank

d) t_{RFCpb} must be satisfied before issuing another REFpb command

An All Bank REFRESH command(REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

The REFab command must not be issued to the device until the following conditions have been met (see Table 7)

a) t_{RFCab} has been satisfied following the prior REFab command

b) t_{RFCpb} has been satisfied following the prior REFpb command

c) t_{RP} has been satisfied following the prior PRECHARGE commands

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When an all-bank refresh cycle has completed, all banks will be idle.

After issuing REFab:

a) t_{RFCab} latency must be satisfied before issuing an ACTIVATE command

b) t_{RFCab} latency must be satisfied before issuing a REFab or REFpb command.

[Table 7] REFRESH Command Scheduling Separation Requirements

Symbol	Minimum Delay From	To	Notes
t_{RFCab}	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
t_{RFCpb}	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	
t_{RRD}	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to different bank than the prior ACTIVATE command	

NOTE :
1) A bank must be in the Idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

In general, an all bank refresh command needs to be issued to the LPDDR3 SDRAM regularly every tREFI × Refresh Rate Multiplier interval.
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI × Refresh Rate Multiplier (see Figure 1). A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) , with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so
that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI × Refresh Rate Multiplier . At any given time, a maximum of 16 REF commands can be issued within 2 × tREFI × Refresh Rate Multiplier.

And for per bank refresh, a maximum 8 x 8 per bank refresh commands can be postponed or pulled in for scheduling
efficiency. At any given time, a maximum of 2 × 8 × 8 per bank refresh commands can be issued within 2 × tREFI × Refresh Rate Multiplier.

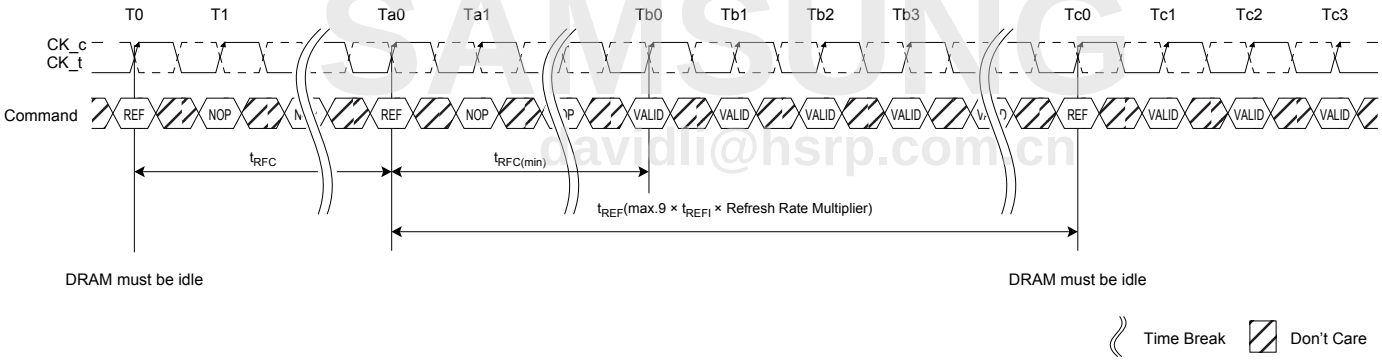

Figure 25: Refresh Command Timing

NOTE :
1) Only NOP commands allowed after Refresh command registered untill $t_{RFC(min)}$ expires.
2) Time interval between two Refresh commands may be extended to a maximum of 9 × tREFI × Refresh Rate Multiplier..

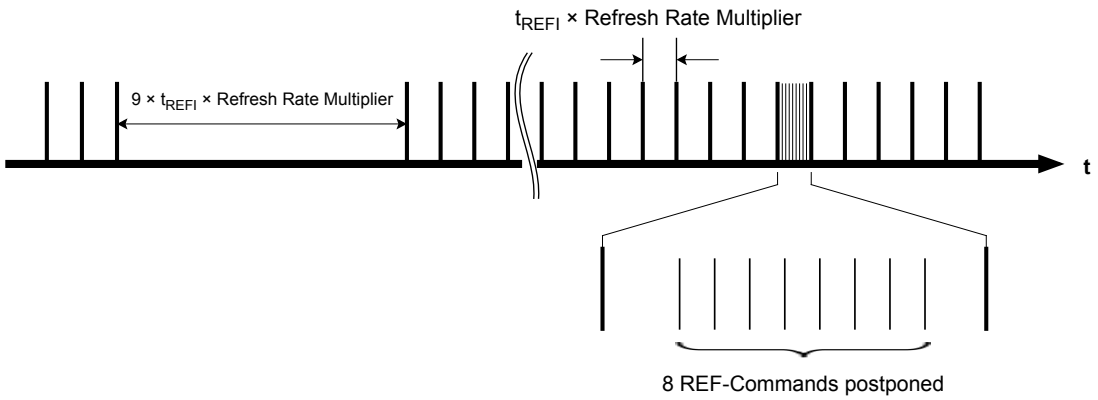

Figure 26: Postponing Refresh Commands

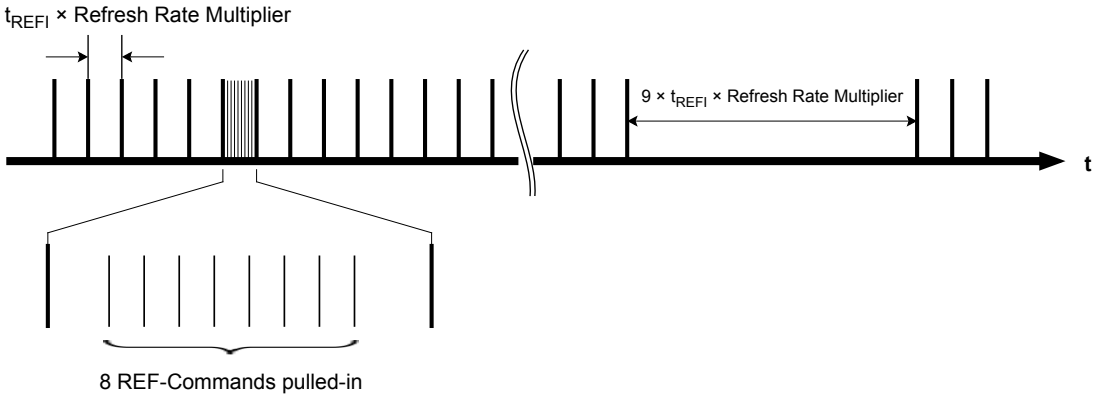

Figure 27: Pulling-in Refresh Commands

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9.1 Refresh Requirements

(1) Minimum number of Refresh commands:
LPDDR3 requires a minimum number, R, of Refresh (REFab) commands within any rolling refresh window (t_{REFW} = 32 ms @ MR4[2:0] = 011 or Tcase ≤ 85 °C). For t_{REFW} and t_{REFI} refresh multipliers at different MR4 settings, refer to the MR4 definition.

When using per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

(3) REFRESH Requirements and SELF REFRESH:
Self refresh mode may be entered with a maximum of eight refresh commands being postponed. After exiting selfrefresh mode with one or more refresh commands postponed, additional refresh commands may be postponed to the extent that the total number of postponed refresh commands (before and after the self refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REF commands does not change."

"The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the LPDDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self refresh mode."

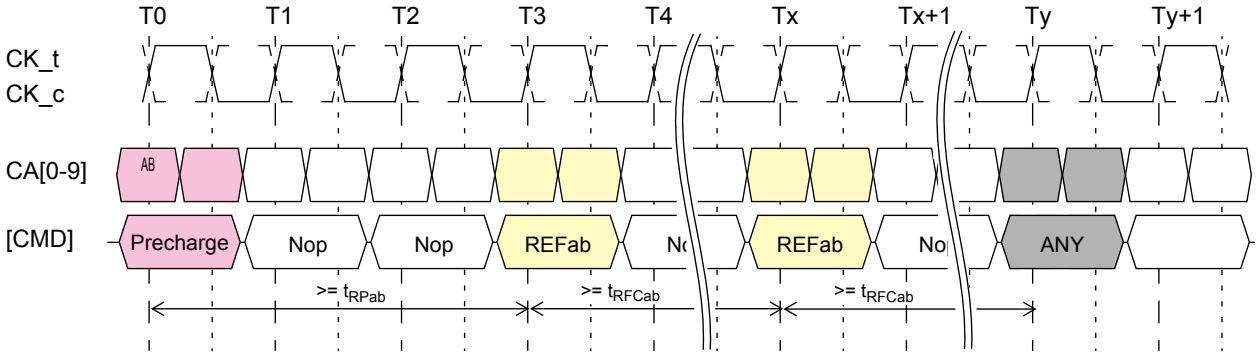

Figure 28: All Bank Refresh Operation

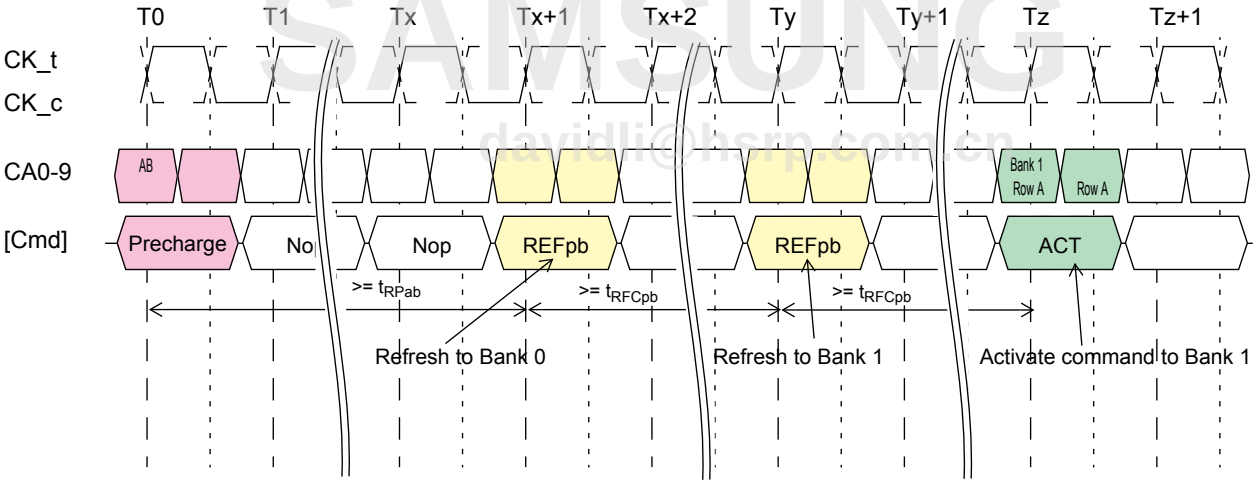

Figure 29: Per Bank Refresh Operation

NOTE :
1) In the beginning of this example, the REFpb bank is pointing to Bank 0.
2) Operations to banks other than the bank being refreshed are supported during the t_{RFCpb} period.

10.0 SELF REFRESH OPERATION

The Self Refresh command can be used to retain data in the LPDDR3 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SDRAM retains data without external clocking. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as tCPDED. CKE LOW will result in deactivation of input receivers after tCPDED has expired. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR3 SDRAM devices can operate in Self Refresh in both the standard or elevated Temperature Ranges. LPDDR3 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures.

Once the SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see Absolute Maximum DC Ratings). However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits (see Recommanded DC Operating Conditions). The SDRAM initiates a minimum of one all-bank refresh command internally within t_{CKESR} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the SDRAM must remain in Self Refresh mode is $t_{CKESR,min}$. The user may change the external clock frequency or halt the external clock t_{CPDED} after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 tCK prior to the positive clock-edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSR} for proper operation. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSR}. For the description of ODT operation and specifications during self-refresh entry and exit, see section On-Die Termination.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

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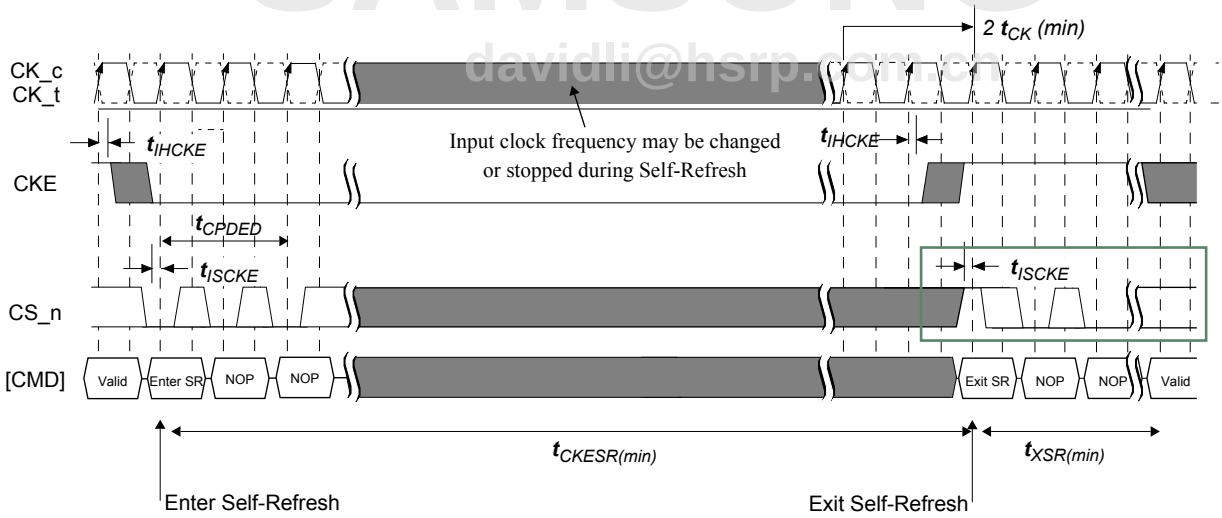

Figure 30: LPDDR3: Self-Refresh Operation

NOTE :
1) Input clock frequency may be changed or can be stopped or floated during self-refresh, provided that upon exiting self-refresh, the clock is stable and within specified limits for a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the speed grade in use.
2) Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3) t_{XSR} begins at the rising edge of the clock after CKE is driven HIGH.
4) A valid command may be issued only after t_{XSR} is satisfied. NOPs shall be issued during t_{XSR}.

10.1 Partial Array Self-Refresh(PASR)

10.1.1 PASR Bank Masking

The LPDDR3 SDRAM has 8 banks (additional banks may be required for higher densities). Each bank of an LPDDR3 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

10.2 PASR Segment Masking

A segment masking scheme may be used in lieu of or in combination with the bank masking scheme in LPDDR3 SDRAM. LPDDR3 devices utilize 8 segments per bank. For segment masking bit assignments, see Mode Register 17.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. 8 segments are used as listed in Mode Register 17. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. Programming of bits in the reserved registers has no effect on the device operation.

[Table 8] Example of Bank and Segment Masking use in LPDDR3 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

NOTE :
1) This table illustrates an example of an 8-bank LPDDR3 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

11.0 MODE REGISTER READ(MRR) COMMAND

The Mode Register Read (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f-CA0f and CA9r-CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL x tCK + tDQSCK + tDQSQ following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ Calibration function, where subsequent data beats contain valid content as described in the DQ Calibration specification. All DQS are oggled for the duration of the Mode Register READ burst.

The MRR command has a burst length of eight. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted.

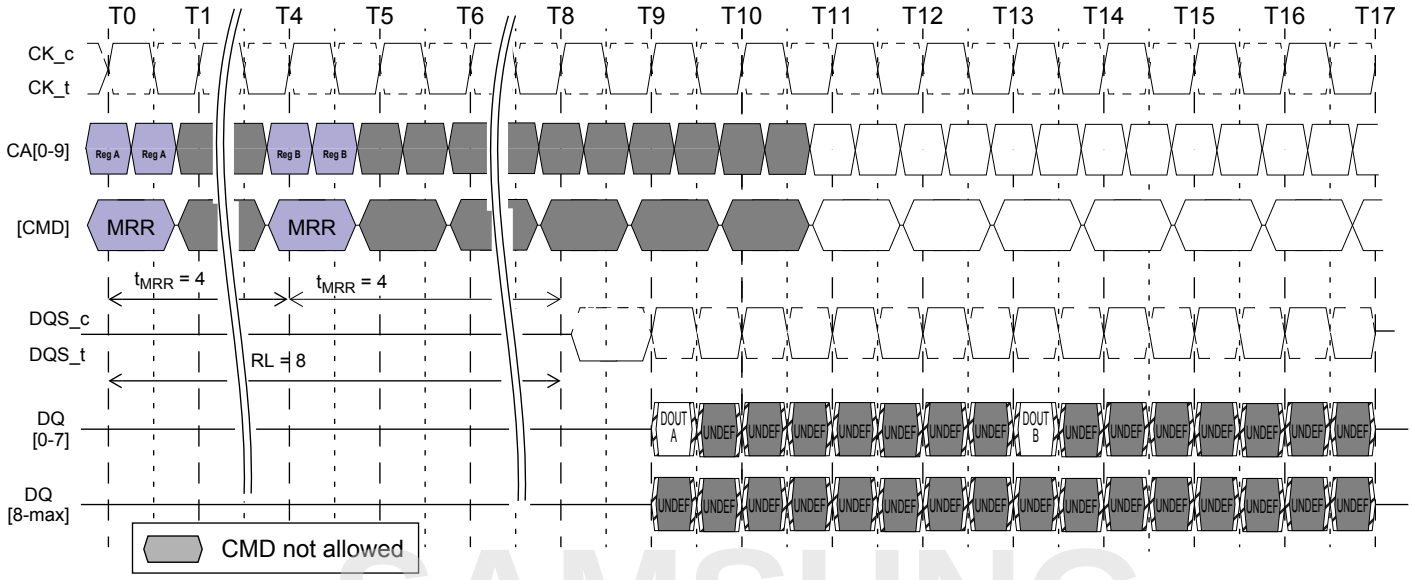

Figure 31: Mode Register Read timing example: RL = 8

NOTE :
1) MRRs to DQ calibration registers MR32 and MR40 are described in DQ calibration section.
2) Only the NOP command is supported during tMRR.
3) Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4) Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1 - WL clock cycles.
5) Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1clock cycles.
6) In this example, RL = 8 for illustration purposes only.

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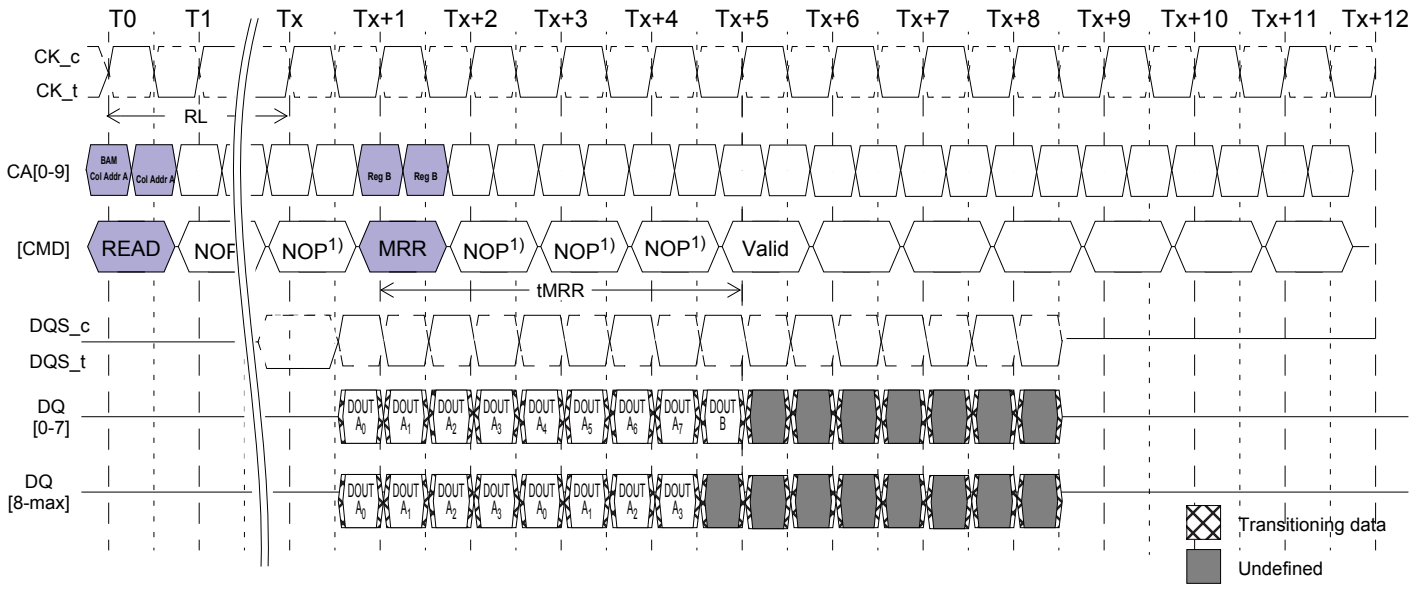

Figure 32: Read to MRR timing

NOTE :
1) Only the NOP command is supported during tMRR.
2) The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(t_{WTR}/t_{CK}) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR.

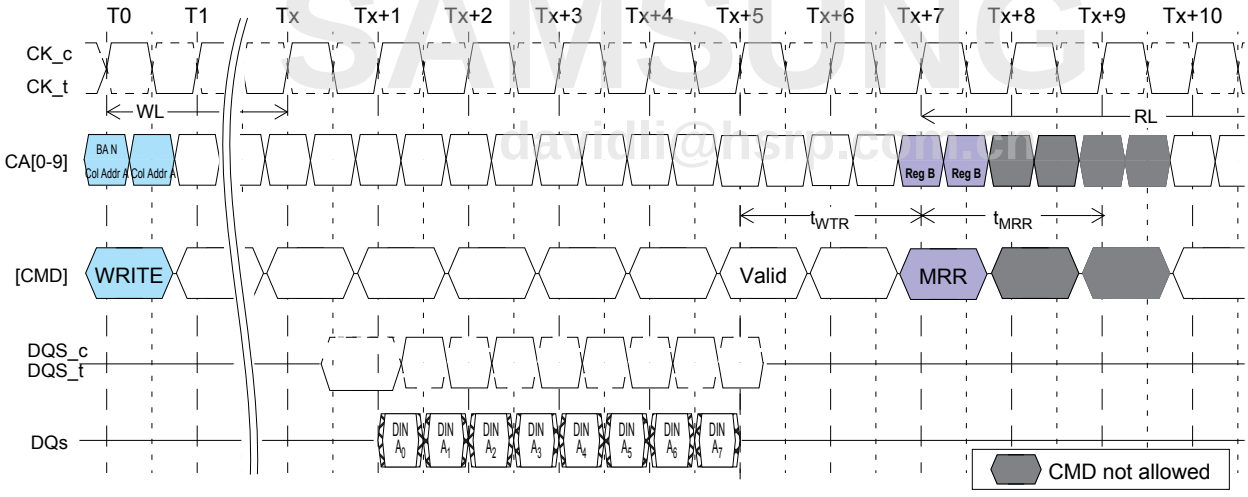

Figure 33: Burst Write Followed by MRR

NOTE :
1) The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].
2) Only the NOP command is supported during tMRR.

11.1 MRR Following Idle Power-Down State

Following the idle power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from standby, idle power-down mode.

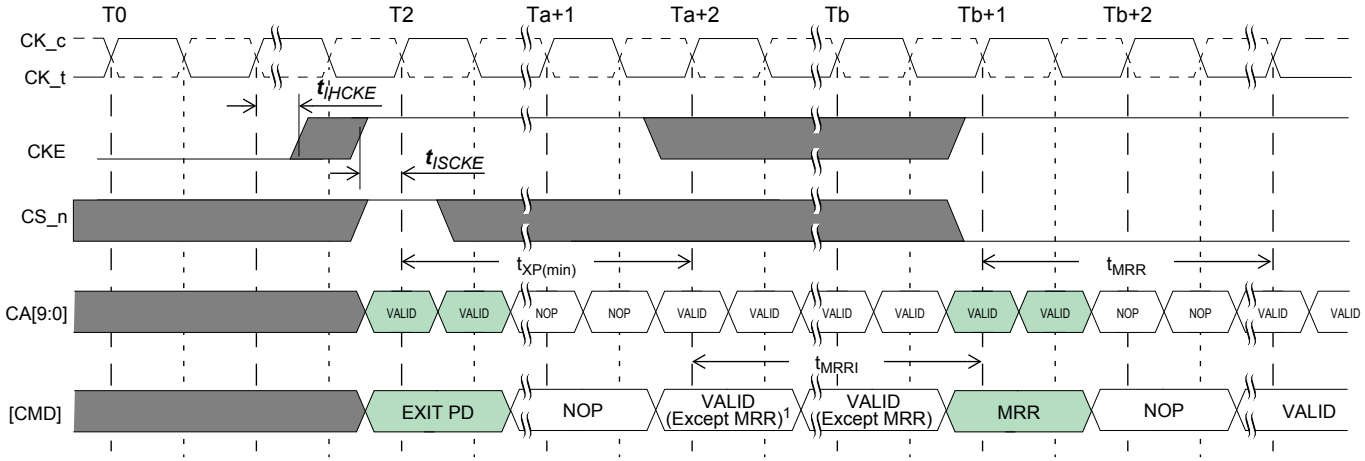

Figure 34: MRR Following Power-Down Idle State

NOTE :
1) Any valid command from the idle state except MRR
2) $t_{MMRI} = t_{RCD}$

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11.2 Temperature Sensor

LPDDR3 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER (See Operating Temperature Range) may be used to determine whether operating temperature requirements are being met.

LPDDR3 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification (See Operating Temperature Range) that applies for the Standard or elevated Temperature Ranges. For example, TCASE may be above 85°C when MR4[2:0] equals 011B. LPDDR3 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2C$$

[Table 9] Temperature Sensor

Parameter	Symbol	Max/Min	Value	Unit
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s
MR4 Read Interval	ReadInterval	Max	System Dependent	ms
Temperature Sensor Interval	t_{TSI}	Max	32	ms
System Response Delay	SysRespDelay	Max	System Dependent	ms
Device Temperature Margin	TempMargin	Max	2	°C

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For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$\frac{10C}{s} \times (ReadInterval + 32ms + 1ms) \leq 2C$$

In this case, ReadInterval shall be no greater than 167 ms.

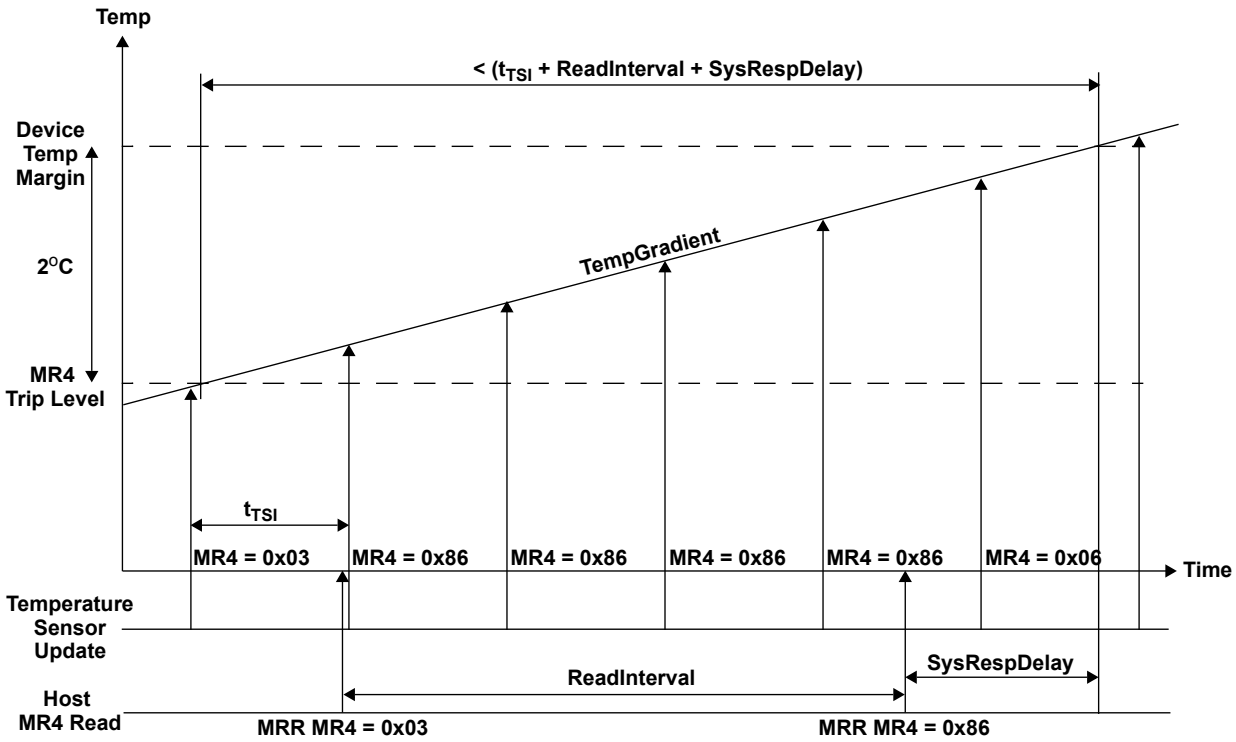

Figure 35: Temp Sensor Timing

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11.3 DQ Calibration

LPDDR3 devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For X16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For X32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

[Table 10] Data Calibration Pattern Description

Parameter	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Bit Time 4	Bit Time 5	Bit Time 6	Bit Time 7
Pattern "A" (MR32)	1	0	1	0	1	0	1	0
Pattern "B" (MR40)	0	0	1	1	0	0	1	1

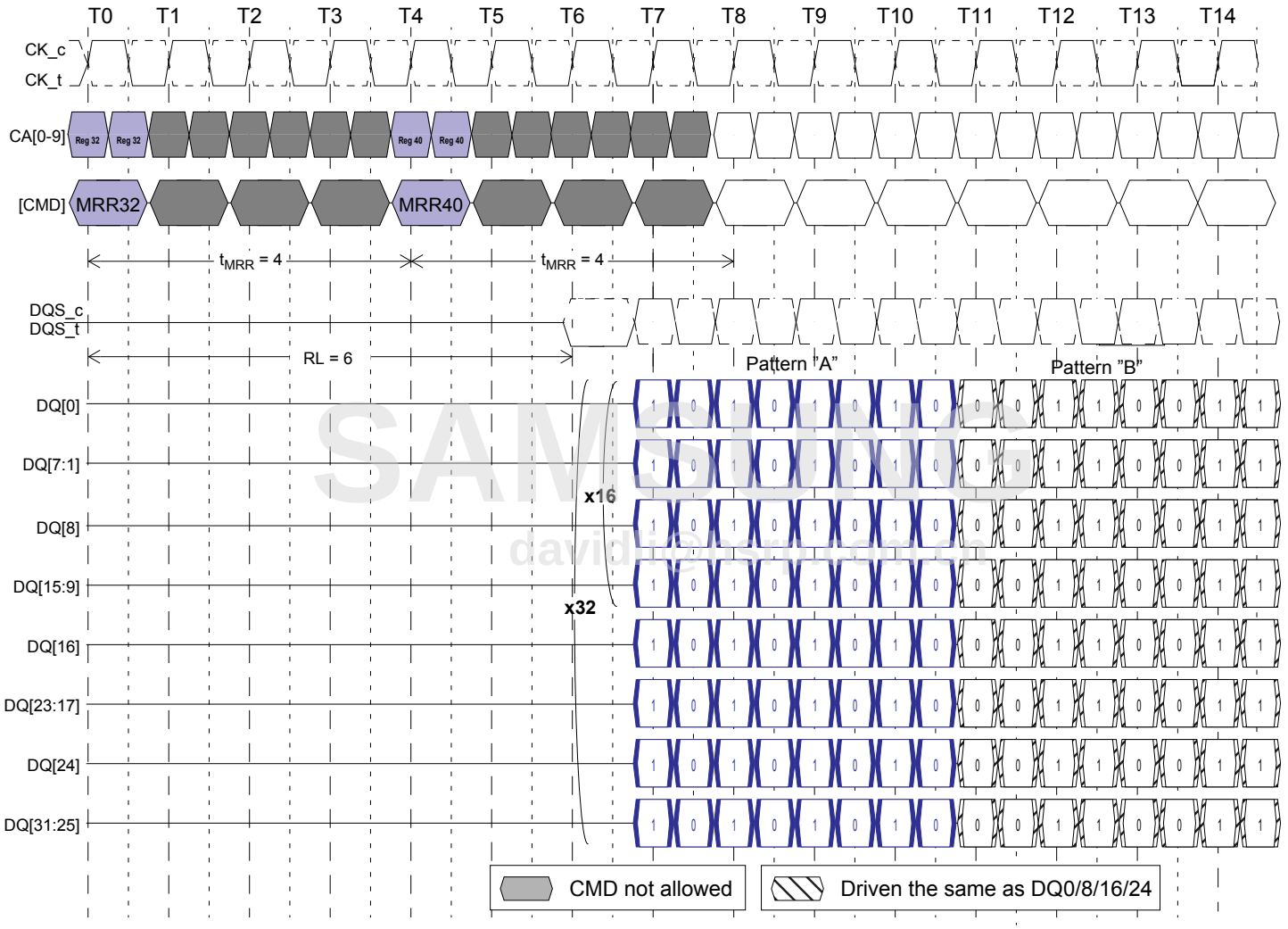

Figure 36: DQ Calibration timing

12.0 MODE REGISTER WRITE (MRW) COMMAND

The Mode Register Write (MRW) command is used to write configuration data to mode registers. The MRW command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by t_{MRW}. Mode Register WRITEs to read-only registers have no impact on the functionality of the device.

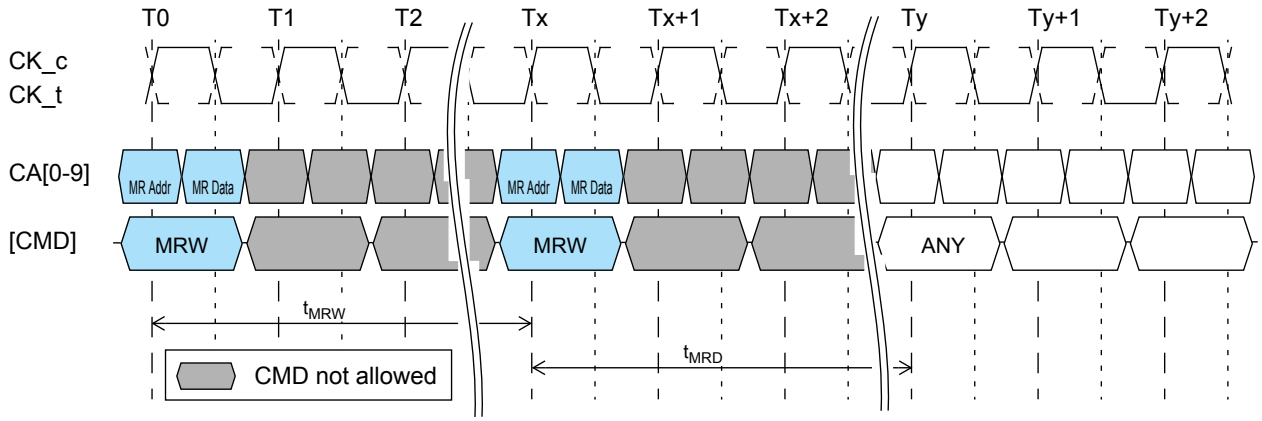

Figure 37: Mode Register Write Timing

NOTE :
1) At time Ty, the device is in the idle state.
2) Only the NOP command is supported during t_{MRW}.

12.1 Mode Register Write

MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE-ALL command.

12.2 MRW Reset

The MRW RESET command brings the device to the device auto-Initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

If the initialization is to be performed at-speed (greater than the recommended boot clock frequency), then CA Training may be necessary to ensure setup and hold timings. Since the MRW RESET command is required prior to CA Training it may be difficult to meet setup and hold requirements. User may however choose the OP code 0xFCh. This encoding ensures that no transitions are required on the CA bus between rising and falling clock edge. Prior to CA Training, it is recommended to hold the CA bus stable for one cycle prior to, and one cycle after, the issuance of the MRW RESET command to ensure setup and hold timings on the CA bus.

[Table 11] Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto-Init)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed

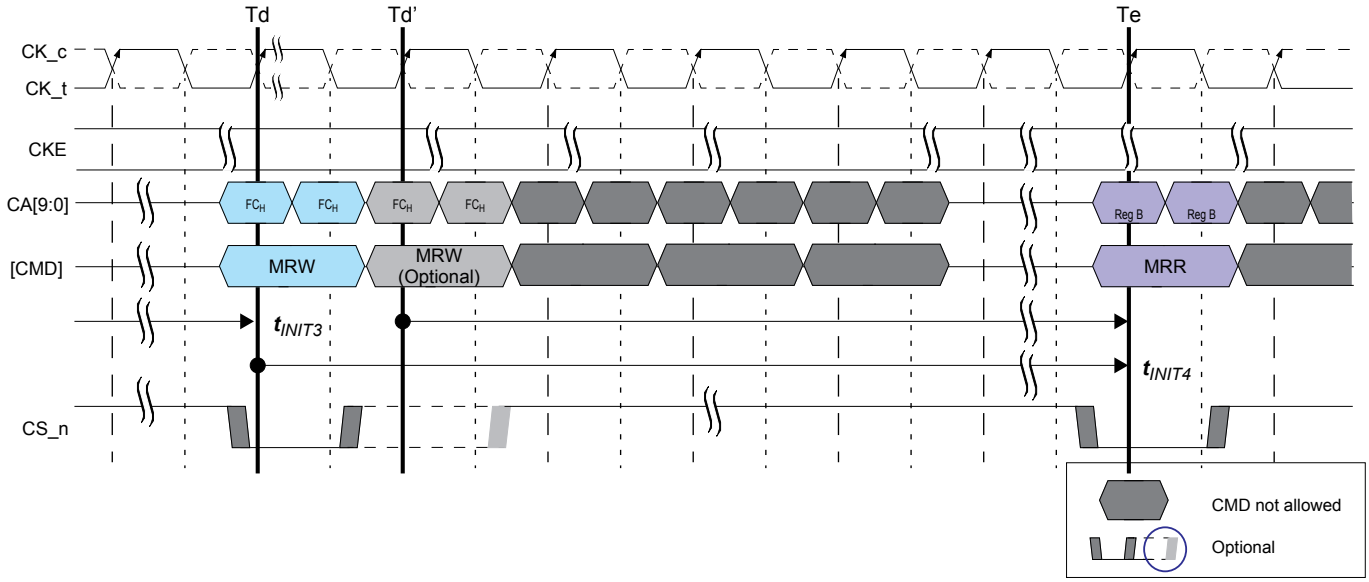

Figure 38: Mode Register Write Timing for MRW RESET

NOTE :
1) Optional MRW RESET command and optional CS_n assertion are allowed, When optional MRW RESET command is used, tINIT4 starts at Td'.

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12.3 Mode Register Write ZQ Calibration Command

The MRW command is used to initiate the ZQ Calibration command. This command is used to calibrate the ouput driver impedance and on-die termination across process, temperature, and voltage. LPDDR3 devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT is for initialization calibration, tZQRESET is for resetting ZQ to the default output impedance; tZQCL is for long calibration(s); and tZQCS is for short calibration(s).

The Initialization ZQ Calibration (ZQINIT) must be performed for LPDDR3. ZQINIT provides an output impedance accuracy of +/-15%. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of +/-15%. A ZQ Calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system. The ZQ Reset Command (ZQRESET) resets the output impedance calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to +/-30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQCorrection) of output impedance errors within tZQCS for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR3 devices are subject to temperature drift rate (Tdriftrate) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftate) + (VSens \times Vdriftrate)} = CalibrationInterval$$

where TSens = max (dRONdT) and VSens = max (dRONdV) define temperature and voltage sensitivities.

For example, if TSens = 0.75% / ^{o}C, VSens = 0.20% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

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A ZQ Calibration command can only be issued when the device is in the Idle state with all banks precharged. ODT shall be disabled via the mode register or the ODT pin prior to issuing a ZQ calibration command. No other activities can be performed on the data bus and the data bus shall be un-terminated during calibration periods (t_{ZQINIT}, t_{ZQCL} or t_{ZQCS}). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.

In systems sharing a ZQ resistor between devices, the controller must prevent t_{ZQINIT}, t_{ZQCS}, and t_{ZQCL} overlap between the devices. ZQ Reset overlap is acceptable.

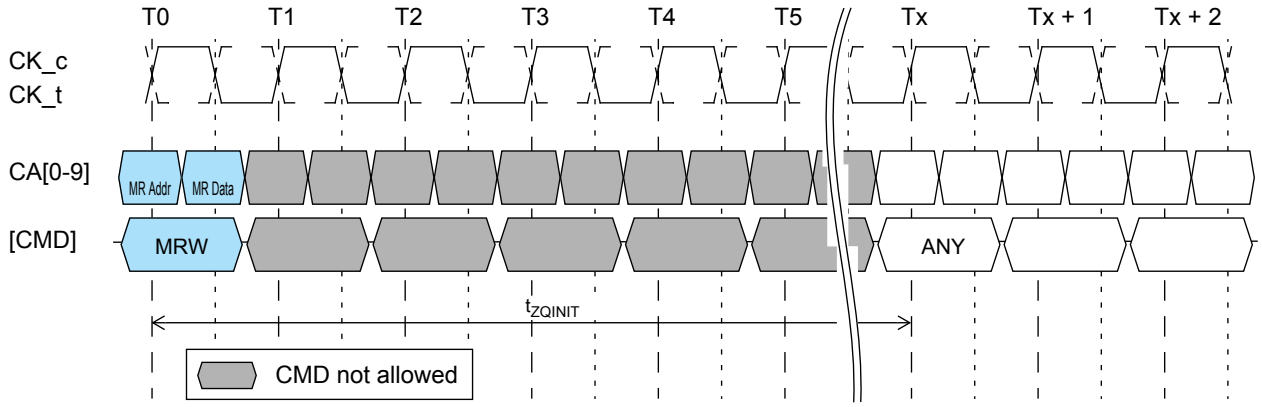

Figure 39: ZQ Initialization timing

NOTE :
1) Only the NOP command is supported during ZQ calibration.
2) CKE must be continuously registered HIGH during the calibration period.
3) All devices connected to the DQ bus should be high-Z during the calibration process.

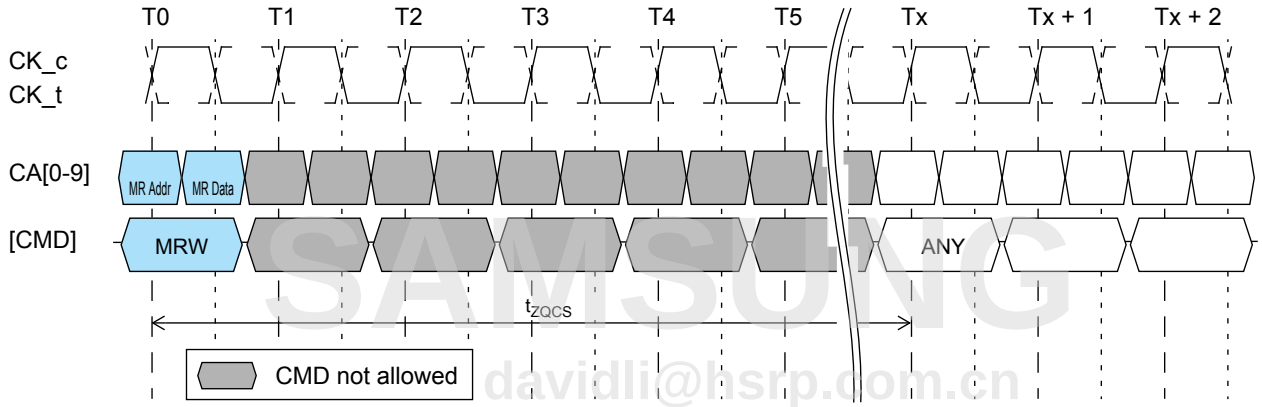

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Figure 40: ZQ Calibration Short timing

NOTE :
1) Only the NOP command is supported during ZQ calibration.
2) CKE must be registered HIGH continuously during the calibration period.
3) All devices connected to the DQ bus should be high-Z during the calibration process.

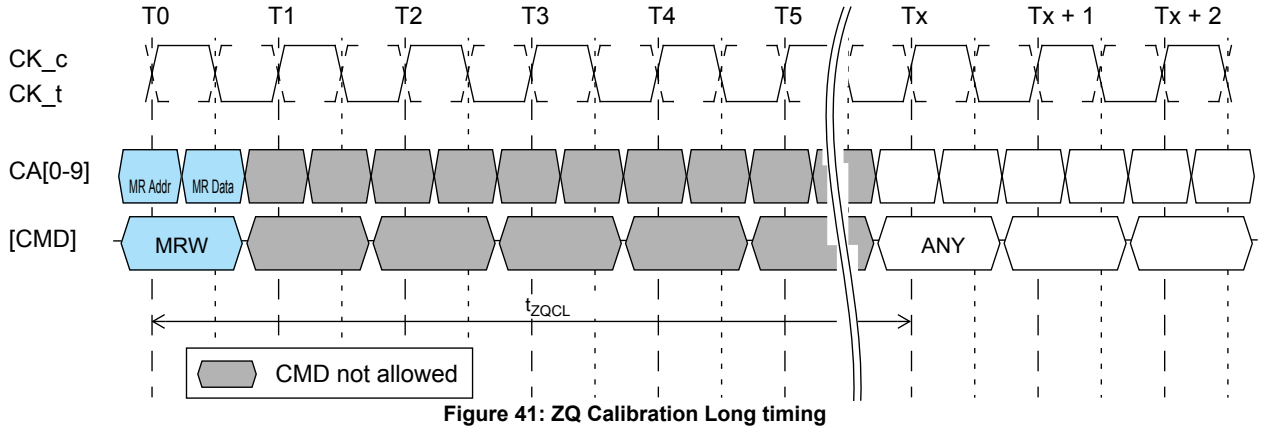

Figure 41: ZQ Calibration Long timing

NOTE :
1) Only the NOP command is supported during ZQ calibration.
2) CKE must be registered HIGH continuously during the calibration period.
3) All devices connected to the DQ bus should be high-Z during the calibration process.

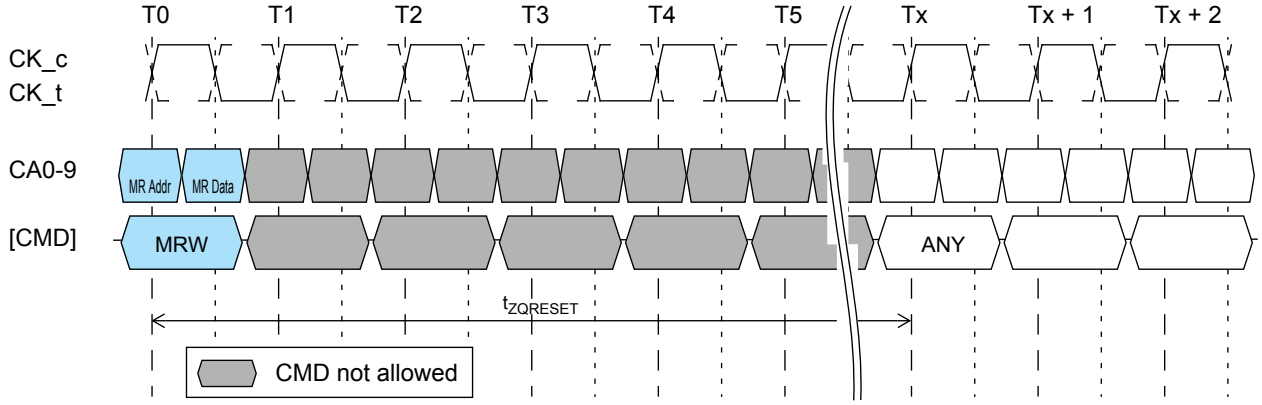

Figure 42: ZQ Calibration Reset timing

NOTE :
1) Only the NOP command is supported during ZQ calibration.
2) CKE must be registered HIGH continuously during the calibration period.
3) All devices connected to the DQ bus should be high-Z during the calibration process.

12.3.1 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, an RZQ +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (See "Input/output capacitance" on specific datasheet)

12.4 Mode Register Write - CA Training Mode

Because CA inputs operate as double data rate, it may be difficult for memory controller to satisfy CA input setup/hold timings at higher frequency. A CA Training mechanism is provided.

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12.4.1 CA Training Sequence

a) CA Training mode entry: Mode Register Write to MR41
b) CA Training session: Calibrate CA0, CA1, CA2, CA3, CA5, CA6, CA7 and CA8 (see Figure 12)
c) CA to DQ mapping change: Mode Register Write to MR48
d) Additional CA Training session: Calibrate remaining CA pins (CA4 and CA9) (see Figure 16)
e) CA Training mode exit: Mode Register Write to MR42

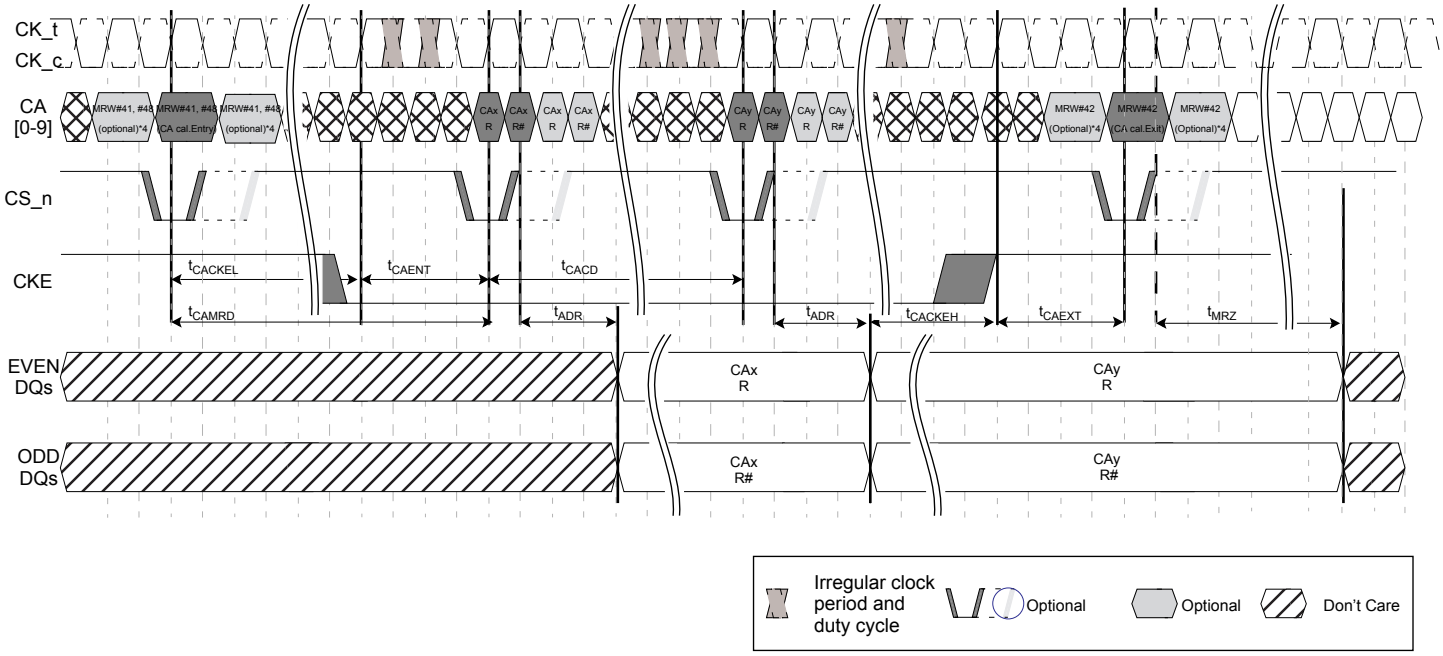

Figure 43: CA Training Timing chart

NOTE :
1) Unused DQ must be valid HIGH or LOW during data output period. Unused DQ may transition at the same time as the active DQ. DQS must remain static and not transition.
2) CA to DQ mapping change via MR 48 omitted here for clarity of the timing diagram. Both MR41 and MR48 training sequences must be completed before exiting the training mode (MR42). To enable a CA to DQ mapping change, CKE must be driven HIGH prior to issuance of the MRW 48 command.
3) Because data out control is asynchronous and will be an analog delay from when all the CA data is available, tADR and tMRZ are defined from CK_t falling edge.
4) It is recommended to hold the CA bus stable for one cycle prior to and one cycle after the issuance of the MRW CA training entry/exit command to ensure setup and hold timings on the CA bus.
5) Clock phase may be adjusted in CA training mode while CS_n is high and CKE is low resulting in an irregular clock with shorter/longer periods and pulse widths.
6) Optional MRW 41, 48, 42 command and CA calibration command are allowed. To complement these optional commands, optional CS_n assertions are also allowed. All timing must comprehend these optional CS_n assertions:
 a) t_{ADR} starts at the falling clock edge after the last registered CS_n assertion.
 b) t_{CACD}, t_{CACKEL}, t_{CAMRD} start with the rising clock edge of the last CS_n assertion.
 c) t_{CAENT}, t_{CAEXT} need to be met by the first CS_n assertion.
 d) t_{MRZ} will be met after the falling clock edge following the first CS_n assertion with exit (MRW#42) command.

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The LPDDR3 SDRAM may not properly recognize a Mode Register Write command at normal operation frequency before CA Training is finished. Special encodings are provided for CA Training mode enable/disable. MR41 and MR42 encodings are selected so that rising edge and falling edge values are the same. The LPDDR3 SDRAM will recognize MR41 and MR42 at normal operation frequency even before CA timing adjustment is finished.
Calibration data will be output through DQ pins. CA to DQ mapping is described in Table 16.
After timing calibration with MR41 is finished, users will issue MRW to MR48 and calibrate remaining CA pins (CA4 and CA9) using (DQ0/DQ1and DQ8/DQ9) as calibration data output pins (see Table 14).
CA Training timing values are specified in the AC Timing Table.

[Table 12] CA Training mode enable (MR41(29H, 0010 1001B), OP=A4H(1010 0100B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	H	L	L	H	L	H
Falling Edge	L	L	L	L	H	L	L	H	L	H

[Table 13] CA Training mode disable (MR42(2AH, 0010 1010B), OP=A8H(1010 1000B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	L	H	L	H	L	H
Falling Edge	L	L	L	L	L	H	L	H	L	H

[Table 14] CA to DQ mapping (CA Training mode enabled with MR41)

CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8	Clock edge
DQ0	DQ2	DQ4	DQ6	DQ8	DQ10	DQ12	DQ14	CK_t rising edge
DQ1	DQ3	DQ5	DQ7	DQ9	DQ11	DQ13	DQ15	CK_t falling edge

[Table 15] CA Training mode enable (MR48 (30H, 0011 0000B), OP=C0H(1100 0000B))

	CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	L	L	L	H	H
Falling Edge	L	L	L	L	L	L	L	H	H

[Table 16] CA to DQ mapping (CA Training mode is enabled with MR48)

CA4	CA9	Clock edge
DQ0	DQ8	CK_t rising edge
DQ1	DQ9	CK_t falling edge

NOTE :
1) Other DQs must have valid output (either HIGH or LOW).

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12.5 Mode Register Write - WR Leveling Mode

In order to provide for improved signal integrity performance, the LPDDR3 SDRAM provides a write leveling feature to compensate for timing skew, affecting timing parameters such as t_{DQSS}, t_{DSS}, and t_{DSH}.

The memory controller uses the write leveling feature to receive feedback from the SDRAM allowing it to adjust the clock to data strobe signal relationship for each DQS_t/DQS_c signal pair. The memory controller performing the leveling must have adjustable delay setting on DQS_t/DQS_c signal pair to align the rising edge of DQS signals with that of the clock signal at the DRAM pin. The DRAM asynchronously feeds back CLK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signals Delay established through this exercise ensures the t_{DQSS} specification can be met.

All DQS signals may have to be leveled independently. During Write Leveling operations each DQS signal latches the clock with a rising strobe edge and drives the result on all DQ[n] of its respective byte.

The LPDDR3 SDRAM enters into Write leveling mode when mode register MR2[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only NOP commands are allowed, or MRW command to exit write leveling operation. Upon completion of the write leveling operation, the DRAM exits from write leveling mode when MR2[7] is reset LOW.

The controller will drive DQS_t low and DQS_c high after a delay of tWLDQSEN. After time tWLMRD, the controller provides DQS Signal input which is used by the DRAM to sample the clock signal driven from the controller. The delay time tWLMRD(max) is controller dependent. The DRAM samples the clock input with the rising edge of DQS and provides asynchronous feedback on all the DQ bits after time tWLO. The controller samples this information and either increment or decrement the DQS_t and/or DQS_c delay settings and launches the next DQS_t/DQS_c pulse. The sample time and trigger time is controller dependent. Once the following DQS_t/DQS_c transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device. Figure47 describes the timing for the write leveling operation.

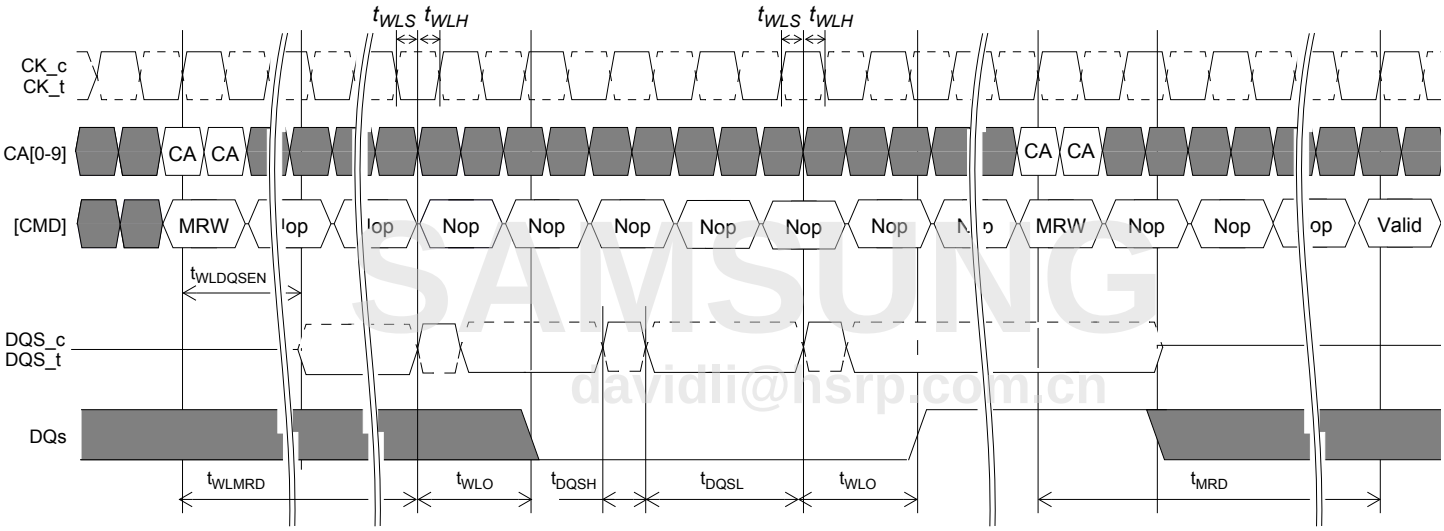

Figure 44: Write Leveling Timing

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13.0 On-Die Termination

ODT (On-Die Termination) is a feature of the LPDDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS_t, DQS_c and DM via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. Unlike other command inputs, the ODT pin directly controls ODT operation and is not sampled by the clock.
The ODT feature is turned off and not supported in Self-Refresh and Deep Power Down modes. ODT operation can optionally be enabled during CKE Power Down via a mode register. Note that if ODT is enabled during Power Down mode VDDQ may not be turned off during Power Down. The DRAM will also disable termination during read operations.
A simple functional representation of the DRAM ODT feature is shown in Figure 45.

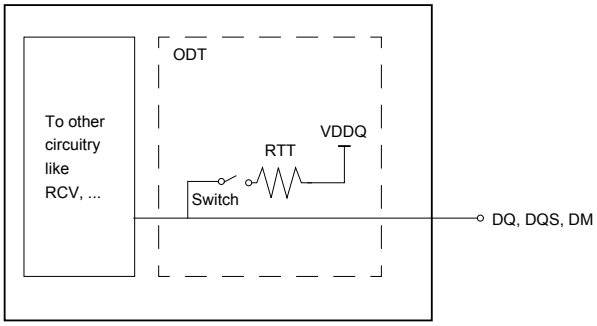

Figure 45: Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other mode register control information. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR11 is programmed to disable ODT, in self-refresh, in deep power down, in CKE power down (mode register option) and during read operations.

13.1 ODT Mode Register

The ODT Mode is enabled if MR11 OP<1:0> are non zero. In this case, the value of RTT is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP<1:0> are zero.
MR11 OP<2> determines whether ODT, if enabled through MR11 OP<1:0>, will operate during CKE power down.

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13.2 Asynchronous ODT

The ODT feature is controlled asynchronously based on the status of the ODT pin, except ODT is off when:.
- ODT is disabled through MR11 OP<1:0>
- DRAM is performing a read operation (RD or MRR)
- DRAM is in CKE Power Down and MR11 OP<2> is zero
- DRAM is in Self-Refresh or Deep Power Down modes.
- DRAM is in CA Training Mode.

In asynchronous ODT mode, the following timing parameters apply when ODT operation is controlled by the ODT pin: tODTon,min,max, tODToff,min,max.
Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured from ODT pin high.
Minimum RTT turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tODToff,max) is the point in time when the on-die termination has reached high impedance. tODToff,min and tODToff,max are measured from ODT pin low.

13.3 ODT During Read Operations (RD or MRR)

During read operations, LPDDR3 SDRAM will disable termination and disable ODT control through the ODT pin. After read operations are completed, ODT control is resumed through the ODT pin (if ODT Mode is enabled).

13.4 ODT During Power Down

When MR11 OP<2> is zero, termination control through the ODT pin will be disabled when the DRAM enters CKE power down. After a power down command is registered, termination will be disabled within a time window specified by tODTd,min,max. After a power down exit command is registered, termination will be enabled within a time window specified by tODTe,min,max.
Minimum RTT disable time (tODTd,min) is the point in time when the device termination circuit will no longer be controlled by the ODT pin. Maximum ODT disable time (tODTd,max) is the point in time when the on-die termination will be in high impedance.
Minimum RTT enable time (tODTe,min) is the point in time when the device termination circuit will no longer be in high impedance. The ODT pin shall control the device termination circuit after maximum ODT enable time (tODTe,max) is satisfied.
When MR11 OP<2> is enabled and MR11 OP<1:0> are non zero, ODT operation is supported during CKE power down with ODT control through the ODT pin.

13.5 ODT During Self Refresh

LPDDR3 SDRAM disables the ODT function during self refresh. After a self refresh command is registered, termination will be disabled within a time window specified by tODTd,min,max. After a self refresh exit command is registered, termination will be enabled within a time window specified by tODTe,min,max.

13.6 ODT During Deep Power Down

LPDDR3 SDRAM disables the ODT function during deep power down. After a deep power down command is registered, termination will be disabled within a time window specified by tODTd,min,max.

13.7 ODT During CA Training and Write Leveling

During CA Training Mode, LPDDR3 SDRAM will disable on-die termination and ignore the state of the ODT control pin. For ODT operation during Write Leveling mode, refer to the DRAM Termination Function In Write Leveling Mode Table for termination activation and deactivation for DQ and DQS_t/DQS_c.

[Table 17] DRAM Termination Function In Write Leveling Mode

ODT Pin	DQS_t/DQS_c termination	DQ termination
de-asserted	OFF	OFF
asserted	ON	OFF

If ODT is enabled, the ODT pin must be high, in Write Leveling mode.

[Table 18] ODT States Truth Table

	Write	Read/DQ Cal	ZQ Cal	CA Training	Write Level
DQ Termination	Enabled	Disabled	Disabled	Disabled	Disabled
DQS Termination	Enabled	Disabled	Disabled	Disabled	Enabled

NOTE :
1) ODT is enabled with MR11[1:0]=01b, 10b, or 11b and ODT pin HIGH. ODT is disabled with MR11[1:0]=00b or ODT pin LOW.

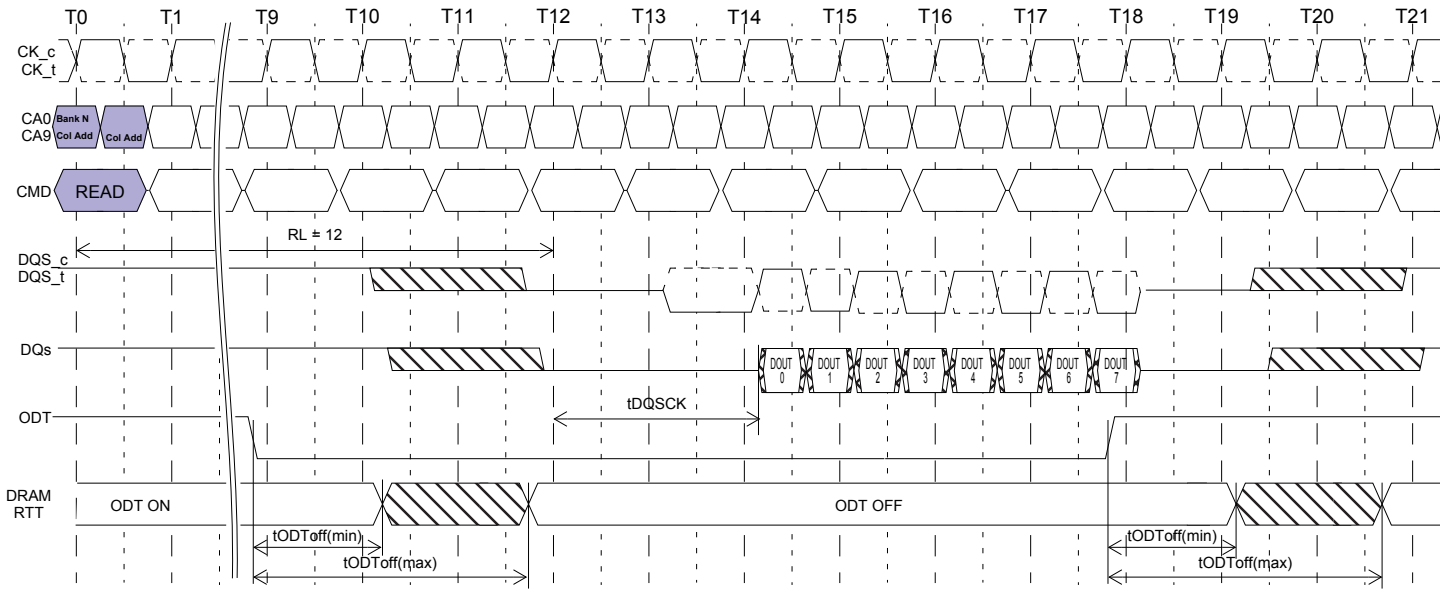

Figure 46: Asynchronous ODT Timing Example for RL = 12

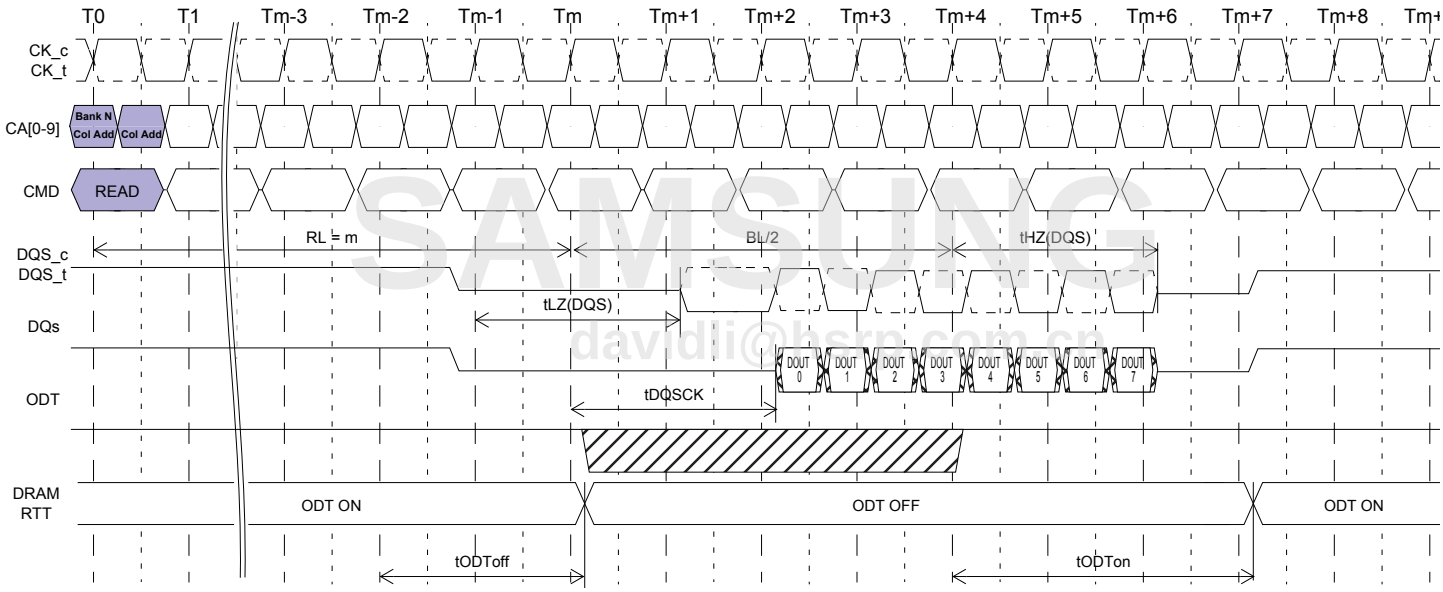

Figure 47: Automatic ODT Timing During READ Operation Example for RL = m

NOTE :
1) The automatic RTT turn-off delay, $t_{AODToff}$, is referenced from the rising edge of "RL-2" clock at Tm-2.
2) The automatic RTT turn-on delay, t_{AODTon}, is referenced from the rising edge of "RL+ BL/2" clock at Tm+4.

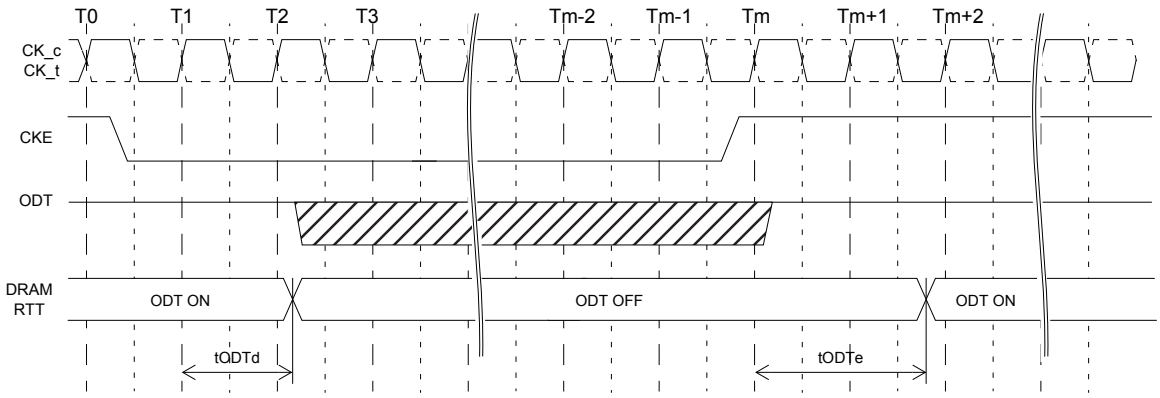

Figure 48: ODT Timing During Power Down, Self Refresh, Deep Power Down Entry/Exit Example

NOTE :
1) Upon exit of Deep Power Down mode, a complete power-up initialization sequence is required.

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14.0 POWER-DOWN

Power-down is entered synchronously when CKE is registered LOW and CS_n is HIGH at the rising edge of clock. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figures 51 Read to power-down entry.

Entering power-down deactivates the input and output buffers, excluding CKE. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW; this timing period is defined as t_{CPDED}. CKE LOW will result in deactivation of input receivers after t_{CPDED} has expired. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until tCKE,min is satisfied. V_{REFCA} must be maintained at a valid level during power down.

VDDQ can be turned off during power down. If VDDQ is turned off, V_{REFDQ} must also be turned off. Prior to exiting power down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until t_{CKE},min is satisfied. A valid, executable command can be applied with power-down exit latency t_{XP} after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. For the description of ODT operation and specifications during power-down entry and exit, see section On-Die Termination.

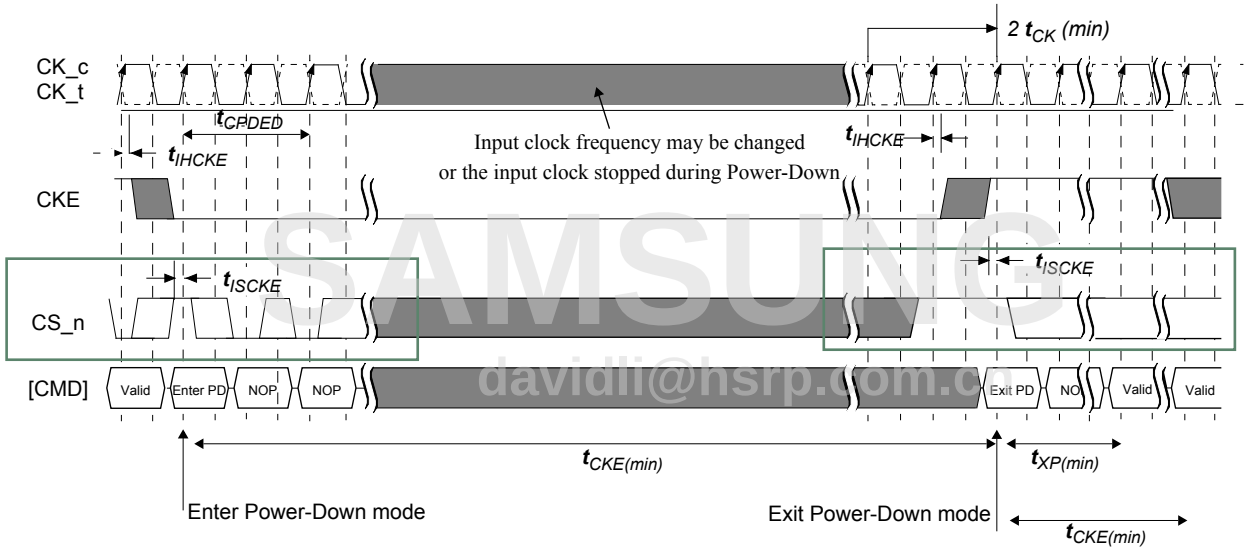

Figure 49: Basic power-down entry and exit timing

NOTE :
1) Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

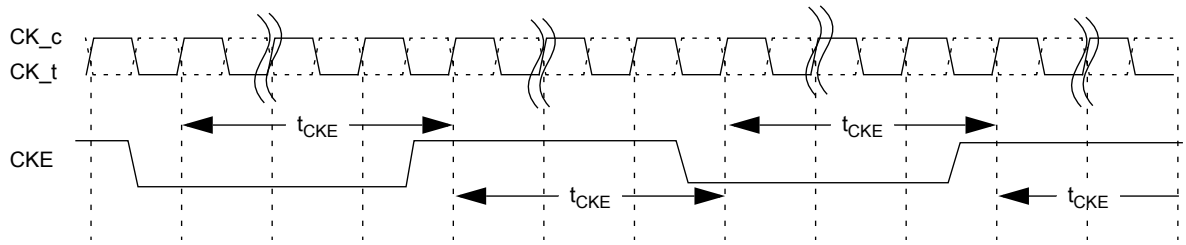

Figure 50: CKE-Intensive Environment

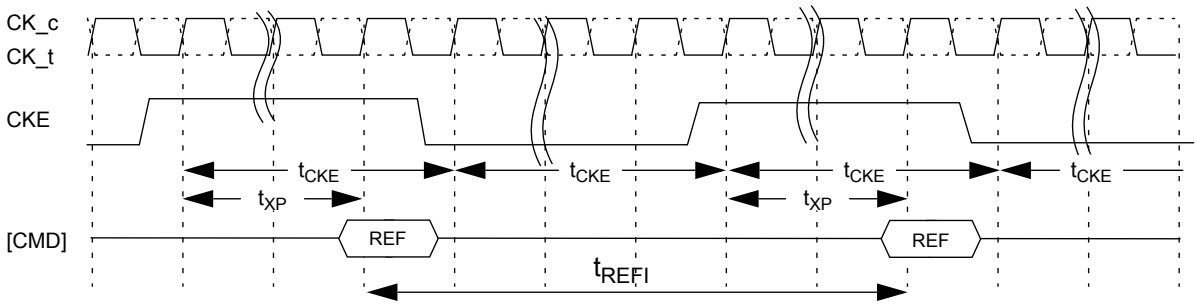

Figure 51: REFRESH-to-REFRESH Timing in CKE-Intensive Environments

NOTE :
1) The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

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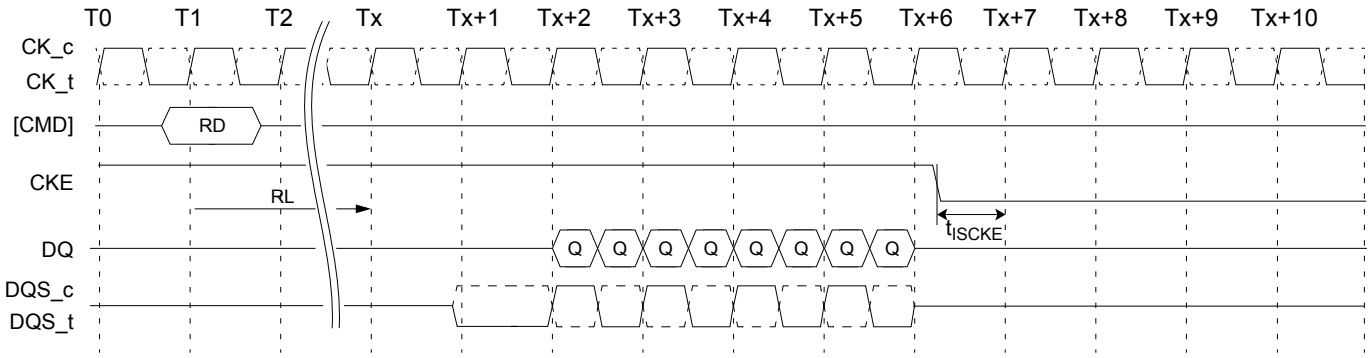

Figure 52: READ to Power-Down Entry

NOTE :
1) CKE must be held HIGH until the end of the burst operation.
2) CKE can be registered LOW at RL + RU($t_{DQSCK(MAX)}/t_{CK}$) + BL/2 + 1 clock cycles after the clock on which the READ command is registered.

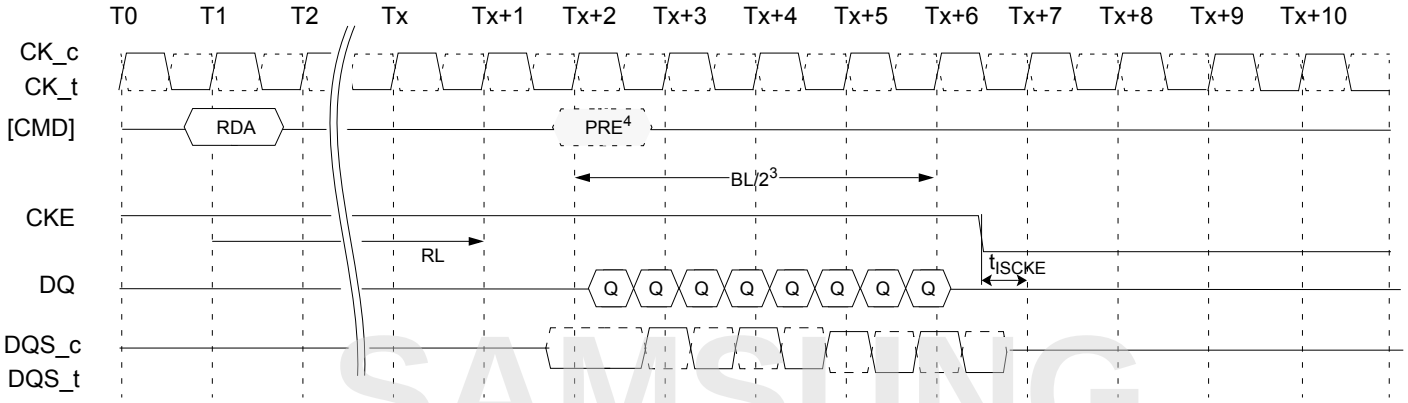

Figure 53: READ with Auto Precharge to Power-Down Entry

NOTE :
1) CKE must be held HIGH until the end of the burst operation.
2) CKE can be registered LOW at RL + RU(t_{DQSCK}/t_{CK})+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.
3) BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.
4) Start internal PRECHARGE.

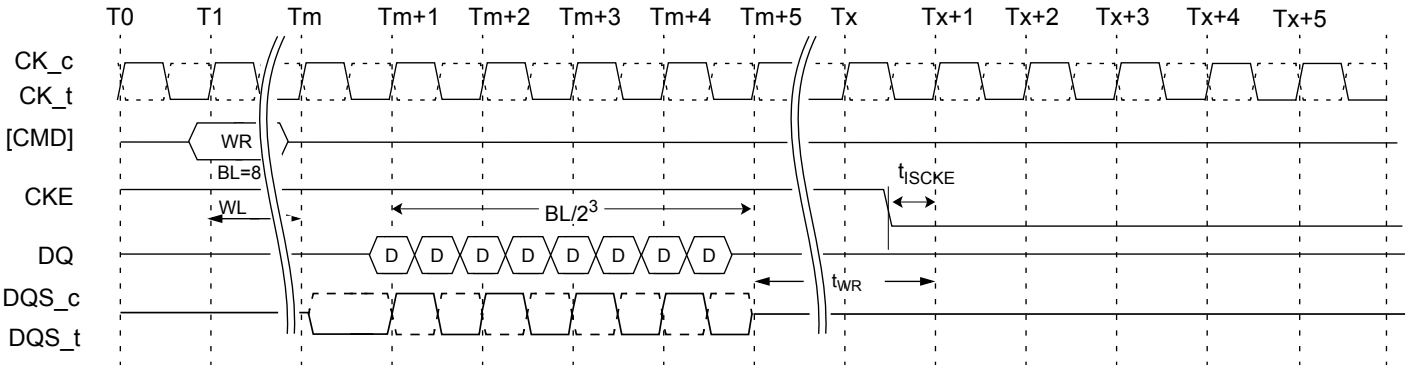

Figure 54: WRITE to Power-Down Entry

NOTE:
1) CKE can be registered LOW at WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) clock cycles after the clock on which the WRITE command is registered.

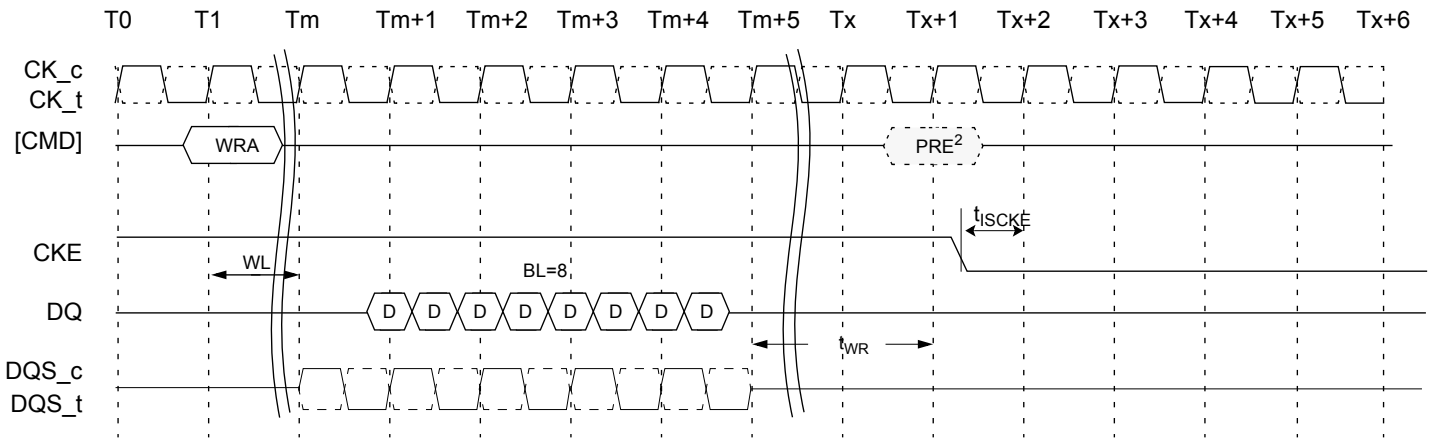

Figure 55: LPDDR3: WRITE with Auto Precharge to Power-Down Entry

NOTE :
1) CKE can be registered LOW at WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) + 1 clock cycles after the WRITE command is registered.
2) Start internal PRECHARGE.

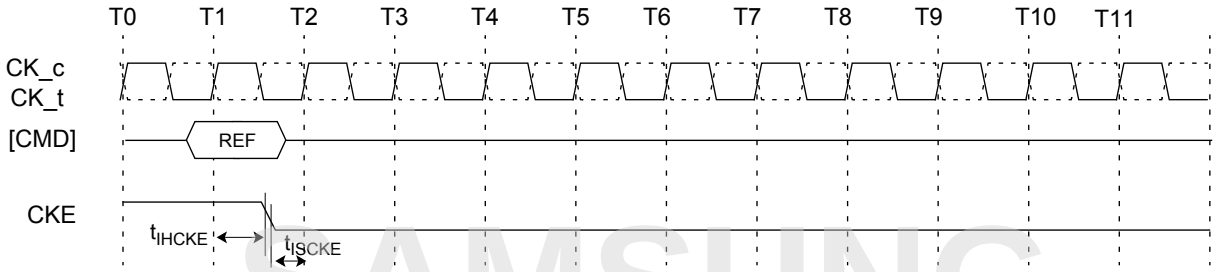

Figure 56: REFRESH Command to Power-Down Entry

NOTE :
1) CKE can go LOW t_{IHCKE} after the clock on which the REFRESH command is registered.

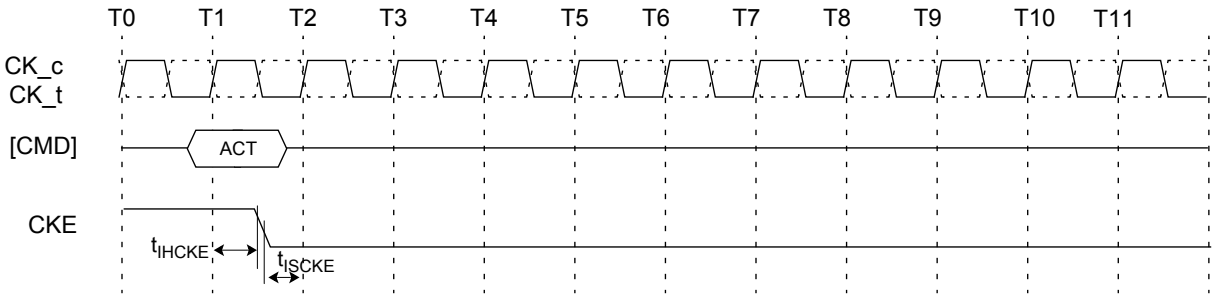

Figure 57: ACTIVATE Command to Power-Down Entry

NOTE:
1) CKE can go LOW at t_{IHCKE} after the clock on which the ACTIVATE command is registered.

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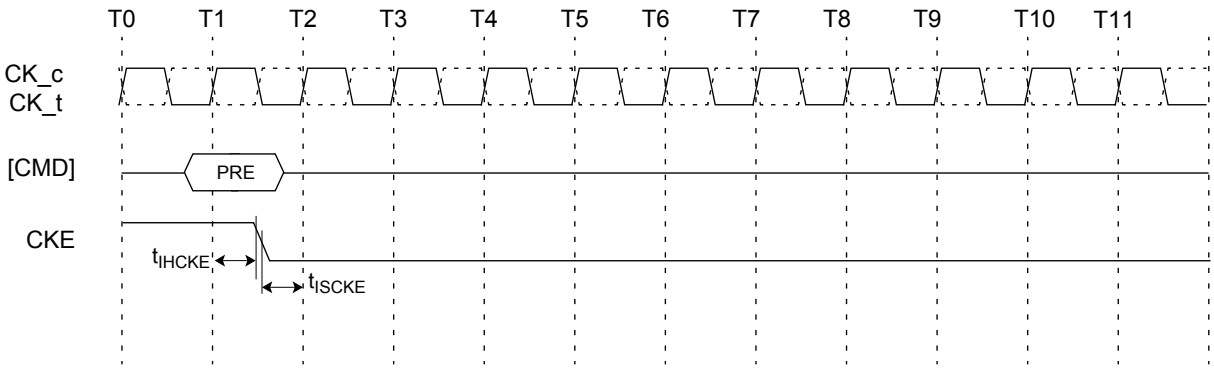

Figure 58: PRECHARGE Command to Power-Down Entry

NOTE :

1) CKE can go LOW tIHCKE after the clock on which the PRECHARGE command is registered.

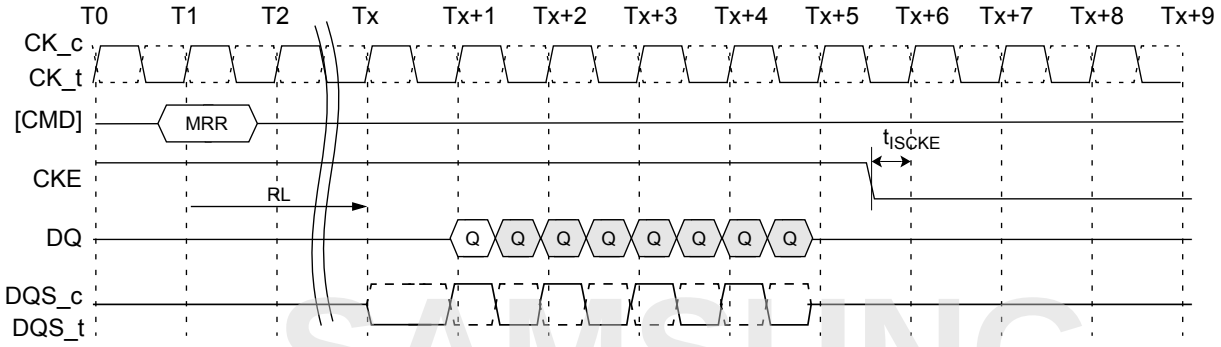

Figure 59: MRR to Power-Down Entry

NOTE :

1) CKE can be registered LOW RL + RU(t_{DQSCK}/t_{CK})+ BL/2 + 1 clock cycles after the clock on which the MRR command is registered.
2) CKE should be held high until the end of the burst operation.

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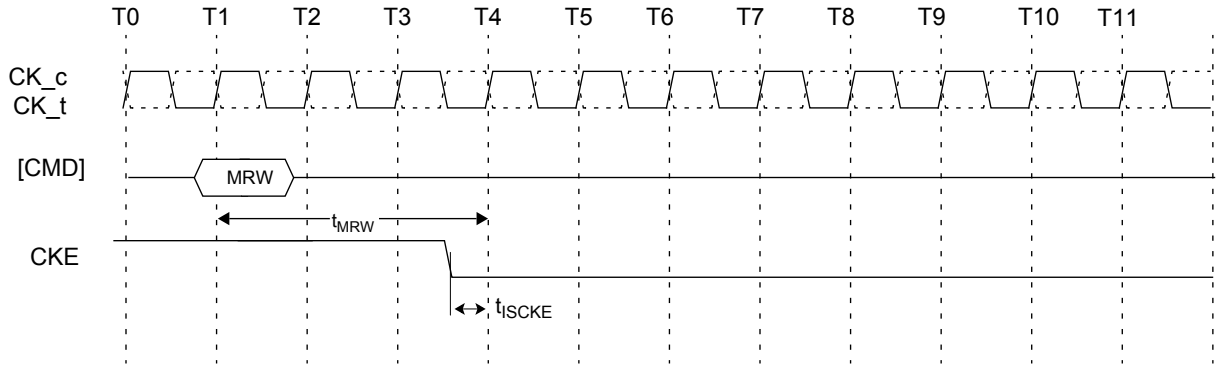

Figure 60: MRW to Power-Down Entry

NOTE :

1) CKE can be registered LOW t_{MRW} after the clock on which the MRW command is registered.

15.0 INPUT CLOCK STOP AND FREQUENCY CHANGE

LPDDR3 SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held or both are floated HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR3 devices support input clock frequency change during CKE HIGH under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR3 SDRAM is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2*tCK + tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS_n shall be held HIGH during clock clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to stopping the clock;
- The LPDDR3 SDRAM is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2*tCK + tXP.

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16.0 NO OPERATION COMMAND

The purpose of the No Operation command (NOP) is to prevent the LPDDR3 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

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