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Nyfea product specification

PRODUCT SPECIFICATION

Customer : _____

Product Name : Contactless Controller

Part NO : NF532

Issue Date : _____

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ChenTT	Zelig	

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1 General description

NF532 is an integrated 13.56 MHz contactless controller built around an embedded 80C51 microcontroller core. The device is intended to support six principal operating states:

- ISO/IEC 14443A/MIFARE Reader/Writer
- FeliCa Reader/Writer
- ISO/IEC 14443B Reader/Writer
- ISO/IEC 14443A/MIFARE card emulation for MIFARE Classic 1K and MIFARE Classic 4K
- FeliCa card emulation
- ISO/IEC 18092 / ECMA-340 Peer-to-Peer

For ISO/IEC 14443A/MIFARE operation, NF532 includes the receive demodulation and decoding functions needed to recover card or transponder responses. Framing, parity checking, and CRC error detection are handled by the contactless interface logic.

MIFARE Classic 1K and 4K card-emulation operation is supported, together with higher transfer-rate communication up to 424 kbit/s in both directions where the applicable protocol mode allows it.

The receive path also supports FeliCa-coded signaling. FeliCa framing and error checking are processed internally, with supported transfer rates up to 424 kbit/s.

For ISO/IEC 14443B Reader/Writer operation, layers 2 and 3 are supported except for anticollision. Anticollision and higher protocol layers are expected to be implemented by firmware.

In card-emulation operation, NF532 can respond by means of either the FeliCa or ISO/IEC 14443A/ MIFARE interface scheme. Load modulation may be produced by the internal transmitter path or through the LOADMOD output when an external active modulation circuit is employed. Secure-card implementations can additionally interface to a secure IC through the NFC-WI/S^{2}C connection.

NF532 also supports passive and active NFCIP-1 communication in accordance with ECMA-340 and ISO/IEC 18092. NFCIP-1 framing and error checking are carried out internally, with transfer rates up to 424 kbit/s.

For Reader/Writer and Card/PICC applications, an external antenna may be connected with the RF front end without requiring an additional active RF device.

Supported host interfaces are:

- SPI
- I^{2}C
- High-Speed UART (HSU)

An integrated low-dropout regulator supports direct battery-powered operation, and an internal power switch is provided for supplying an external secure IC.

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2 Features and benefits

- Embedded 80C51 core with 40 KB ROM and 1 KB RAM
- Integrated receive demodulation and decoding functions
- Buffered antenna drivers intended to minimize the number of external active components
- Integrated RF-level sensing
- Integrated data-mode detection
- ISO/IEC 14443A/MIFARE support
- ISO/IEC 14443B support in Reader/Writer mode
- Reader/Writer operating distance typically up to 50 mm, depending on antenna dimensions, tuning, supply conditions, and card technology
- NFCIP-1 operating distance typically up to 50 mm, subject to antenna and supply implementation
- Card-emulation distance typically around 100 mm under suitable antenna tuning and external-field conditions
- MIFARE Classic 1K/4K encryption support in Reader/Writer mode, including 212 kbit/s and 424 kbit/s higher-rate communication
- FeliCa communication at 212 kbit/s and 424 kbit/s
- Integrated NFCIP-1 RF interface up to 424 kbit/s
- Higher RF-interface rates may be implemented with suitable external analog circuitry
- SPI, I^2C, and High-Speed UART host interfaces
- Dedicated host interrupt signaling
- Hard-Power-Down and Soft-Power-Down operating states
- Host-interface wake-up capability from power-down through I^2C, HSU, or SPI
- Programmable timers
- Integrated crystal-oscillator circuitry
- 2.7 V to 5.5 V main supply operating range
- Switchable supply output for an external secure companion IC
- Dedicated GPIO resources for external control
- Antenna-detection support for production test
- ECMA-373 NFC-WI interface for connection with a secure IC

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3 Applications

- Mobile and portable equipment
- Consumer electronic products requiring 13.56 MHz contactless/NFC connectivity

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4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	battery supply voltage		2.7	-	5.5	V
ICVDD	LDO output voltage	VBAT> 3.4 V VSS= 0 V	[1] 2.7	3	3.4	V
PVDD	Supply voltage for host interface	VSS= 0 V	1.6	-	3.6	V
SVDD	Output voltage for secure IC interface	VSS= 0 V (SVDDSwitch Enabled)	DVDD-0.5	-	DVDD	V
IHPD	Hard-Power-Down current consumption	VBAT= 5 V	-	-	2	µA
ISPD	Soft-Power-Down current consumption	VBAT= 5 V, RF level detector on	-	-	45	µA
IDVDD	Digital supply current	VBAT= 5 V, SVDDswitch off	[1] -	25	-	mA
ISVDD	SVDDload current	VBAT= 5 V, SVDDswitch on	-	-	30	mA
IAVDD	Analog supply current	VBAT= 5 V	-	6	-	mA
ITVDD	Transmitter supply current	During RF transmission, VBAT= 5 V	-	60[3]	150[4]	mA
Ptot	Continuous total power dissipation	Tamb= -30 to +85° C	[2] -	-	0.5	W
Tamb	ambient temperature		-30	-	+85	° C

- [1] DVDD, AVDD and TVDD must always be at the same supply voltage.
- [2] The total current consumption is determined by the firmware version (various internal IC clock speed)
- [3] With an antenna tuned at 50 Ω at 13.56 MHz
- [4] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

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5 Ordering information

NF532 ordering codes and production package designations are product-specific items. They shall be finalized together with the released package drawing and manufacturing qualification data. The functional specification below sections is independent of the final commercial order code.

Table 2. Ordering information

Type number	Package	Description
NF532	TBD	Production order code and qualified package designation to be assigned before release.

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6 Block diagram

The block-level organization of NF532 is shown in Figure 1. The figure numbering is retained for direct engineering comparison with the compatibility reference.

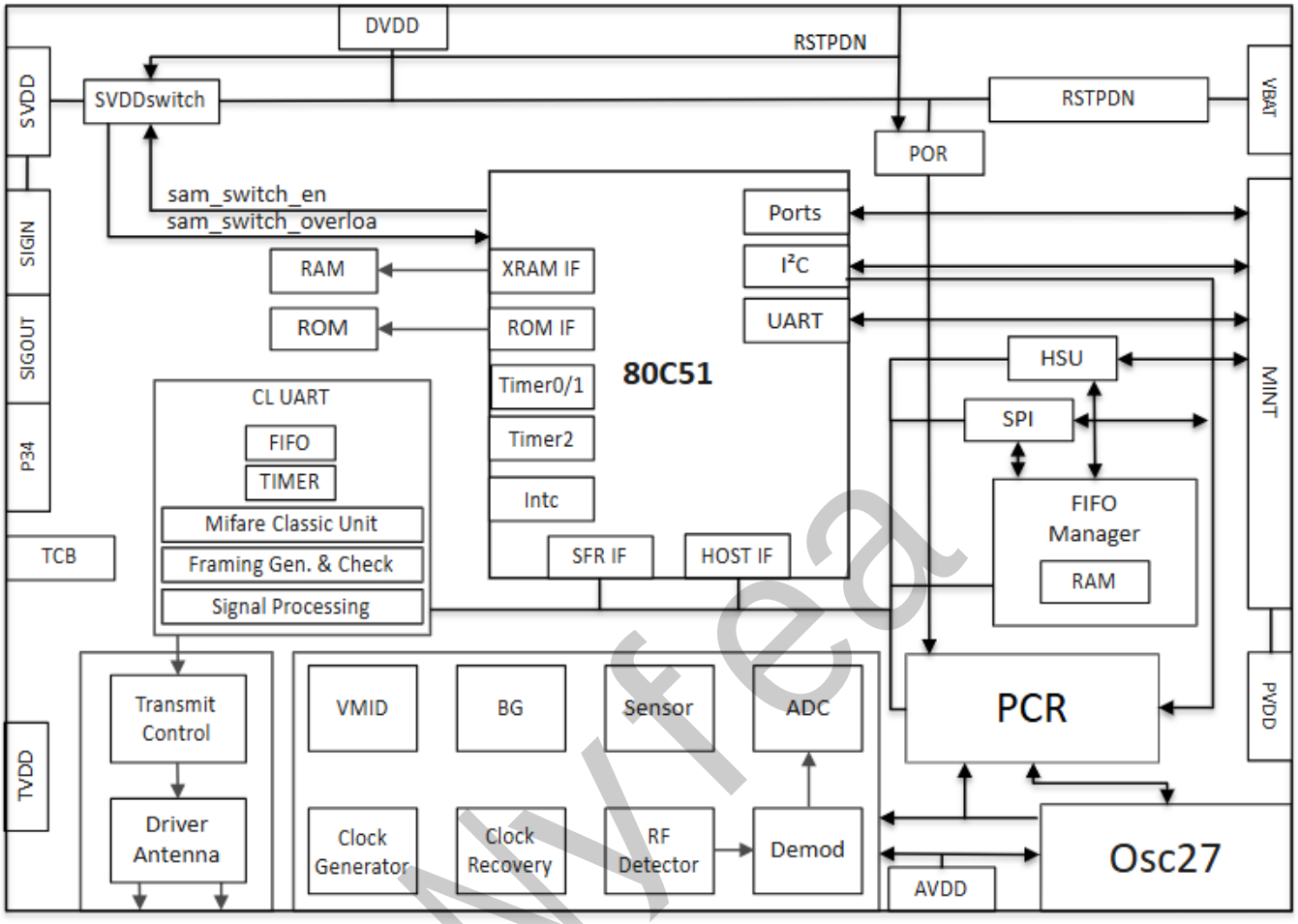


Fig 1. Block diagram of NF532

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7 Pinning information

7.1 Pinning

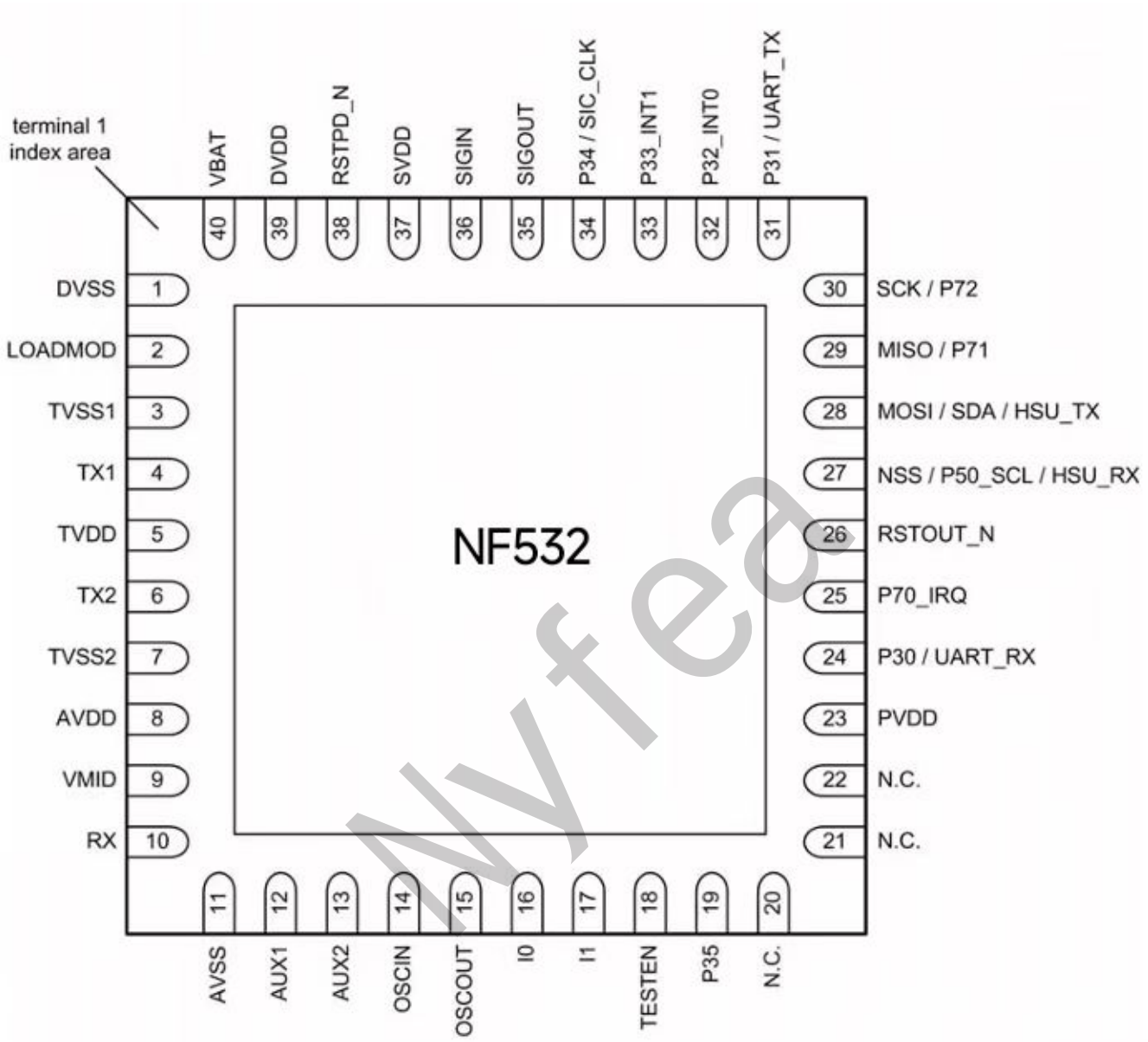


Fig 2. Pin configuration for HVQFN 40 (SOT618-1)

7.2 Pin description

Table 3. NF532 Pin description

Symbol	Pin	Type	Ref Voltage	Description
DVSS	1	PWR		Digital ground.
LOADMOD	2	O	DVDD	Load modulation signal.
TVSS1	3	PWR		Transmitter ground.
TX1	4	O	TVDD	Transmitter output 1: transmits modulated 13.56 MHz energy carrier.
TVDD	5	PWR		Transmitter power supply.
TX2	6	O	TVDD	Transmitter output 2: transmits modulated 13.56 MHz energy carrier.

Symbol	Pin	Type	Ref Voltage	Description
TVSS2	7	PWR		Transmitter ground.
AVDD	8	PWR		Analog power supply.
VMID	9	O	AVDD	Internally generated reference voltage to bias the receiving path
RX	10	I	AVDD	Receiver input.
AVSS	11	PWR		Analog ground.
AUX1	12	O	AVDD	Auxiliary output 1: analog and digital test signals.
AUX2	13	O	AVDD	Auxiliary output 2: analog and digital test signals.
OSCIN	14	I	AVDD	Crystal oscillator input: to oscillator inverting amplifier.
OSCOUT	15	O	AVDD	Crystal oscillator output: from oscillator inverting amplifier.
I0	16	I	DVDD	Host interface selector 0.
I1	17	I	DVDD	Host interface selector 1.
TESTEN	18	I	DVDD	Reserved for test: connect to ground for normal operation.
P35	19	IO	DVDD	General purpose IO.
N.C.	20			Not connected.
N.C.	21			Not connected.
N.C.	22			Not connected.
PVDD	23	PWR		Pad power supply.
P30 / UART_RX	24	IO	PVDD	General purpose IO / Debug UART receive input.
P70_IRQ	25	IO	PVDD	General purpose IO. Can be used as Interrupt request to host.
RSTOUT_N	26	O	PVDD	Reset indicator: when low, circuit is in reset state.
NSS / P50_SCL / HSU_RX	27	IO	PVDD	Host interface pin: SPI Not Slave Selected (NSS) or I^2C clock (SCL) or HSU receive (HSU_RX). Refer to Table 72 for details.
MOSI / SDA / HSU_TX	28	IO	PVDD	Host interface pin: SPI Master Out Slave In (MOSI) or I^2C data (SDA) or HSU transmit (HSU_TX). Refer to Table 72 for details.
MISO / P71	29	IO	PVDD	Host interface pin: SPI Master In Slave Out (MISO). Refer to Table 72 for details. Can be used as general purpose IO.
SCK / P72	30	IO	PVDD	Host interface pin: SPI serial clock. Refer to Table 72 for details. Can be used as general purpose IO.
P31 / UART_TX	31	IO	PVDD	General purpose IO/ Debug UART TX.
P32_INT0	32	IO	PVDD	General purpose IO / Interrupt source INT0.
P33_INT1	33	IO	PVDD	General purpose IO / Interrupt source INT1.
P34 / SIC_CLK	34	IO	SVDD	General purpose IO / Secure IC clock.
SIGOUT	35	O	SVDD	Contactless communication interface output: delivers a serial data stream in accordance with NFCIP-1 to a secure IC.
SIGIN	36	I	SVDD	Contactless communication interface input: accepts a serial data stream in accordance with NFCIP-1 and from a secure IC.
SVDD	37	O		Switchable output power for secure IC power supply with overload detection. Used as a reference voltage for secure IC communication.
RSTPD_N	38	I	PVDD	Reset and Power-Down: When low, internal current sources are switched off, the oscillator is disabled, and input pads are disconnected from the outside world. The internal reset phase starts on the negative edge on this pin.
DVDD	39	O		Internal digital power supply.
VBAT	40	PWR		Main external power supply.

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8 Functional description

8.1 80C51

NF532 uses an embedded 80C51 core as its local controller. Core-level behavior follows the standard 80C51 architecture; the implementation used here offers the next main resources:

- 6-clock CPU organization. A machine cycle holds six states, S1 through S6, and every instruction occupies no less than one machine cycle.
- ROM interface
- RAM interface for the internal IDATA and XRAM spaces (see Figure 4)
- Peripheral interface (PIF)
- Power-control logic for managing CPU power usage
- Clock-control logic used during shutdown and wake-up operation
- Port interface for I/O-pad configuration
- Interrupt controller
- Three timers
- Debug UART

Figure 3 summarizes the major blocks associated with the embedded 80C51 subsystem.

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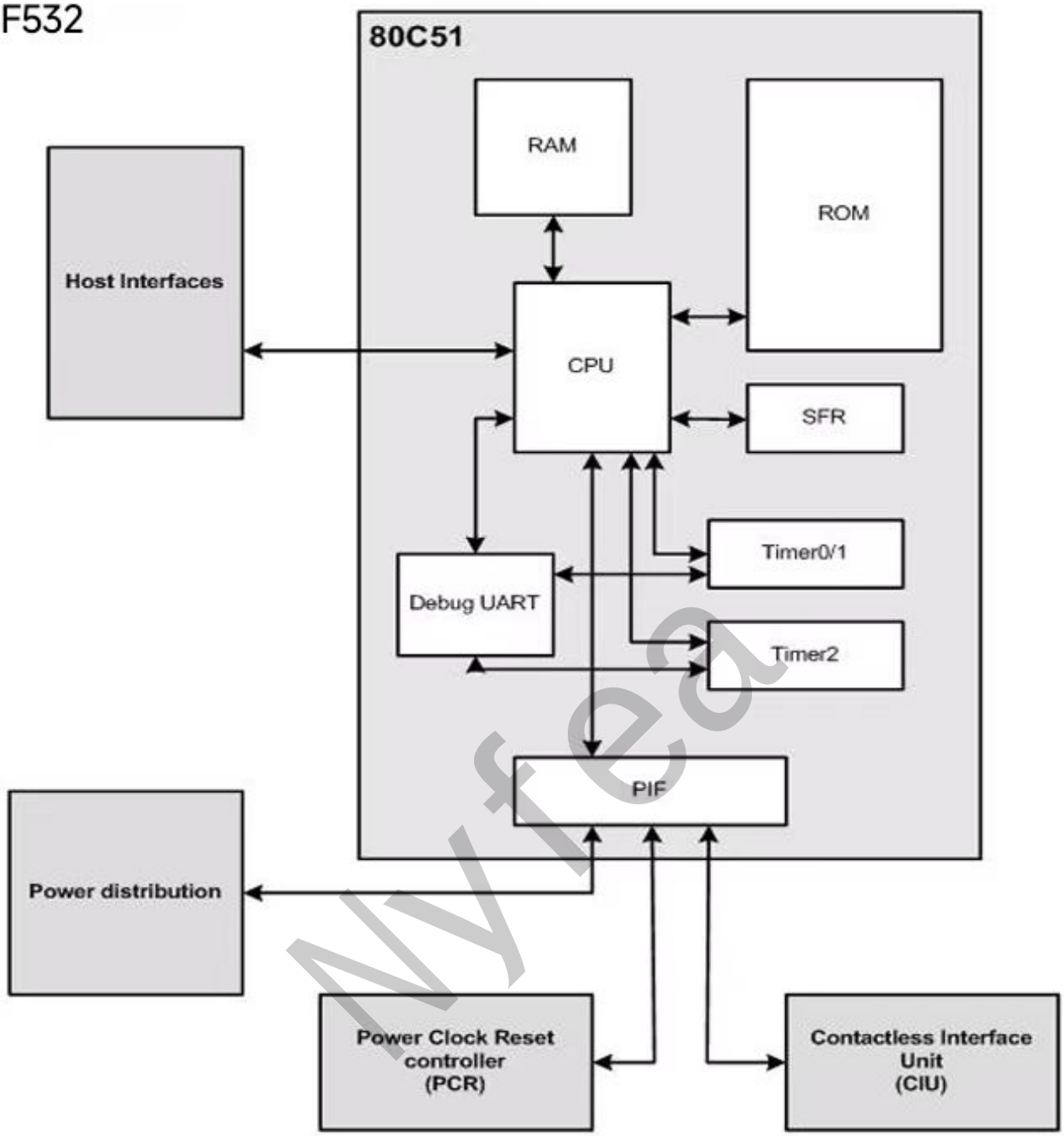


Fig 3. NF532 80C51 block description

8.1.1 NF532 memory map

NF532 uses two principal memory spaces: data memory and program memory. Figure 4 gives the associated map.

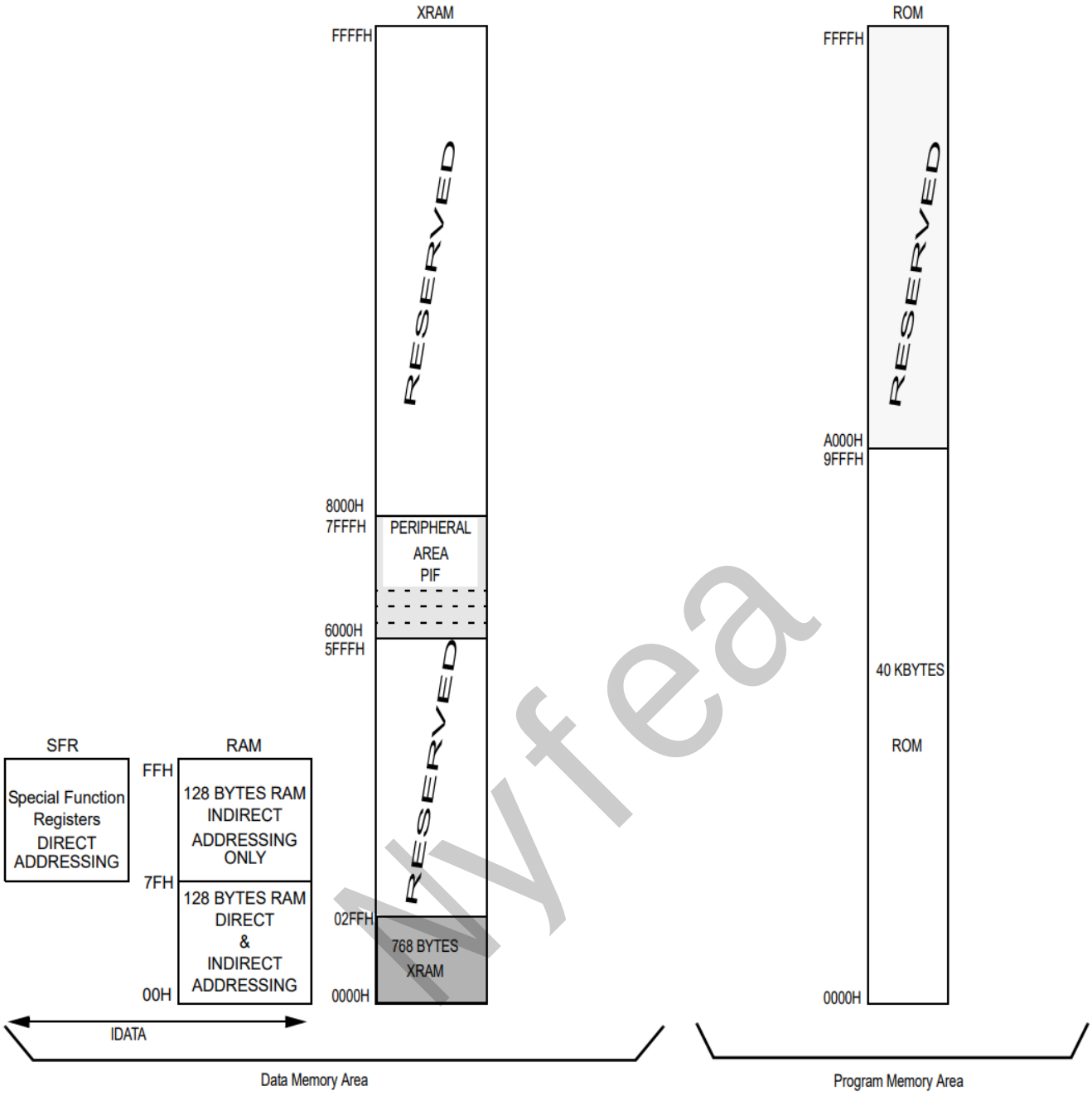


Fig 4. NF532 memory map overview

8.1.2 Data memory

The data-memory architecture holds two address spaces:

- 384-byte IDATA with byte-wide addressing
  - 258-byte RAM
  - 128-byte SFR
- 1 bank of 64 KB extended RAM (XRAM) with 2-byte-wide addressing

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8.1.2.1 IDATA memory

IDATA is organized as Lower IDATA RAM, Upper IDATA RAM, and the SFR space. Each access uses an 8-bit address, so a single addressing mode covers 256 locations. Direct and indirect addressing choose various targets in the upper half of the address range, allowing the full 384-byte IDATA/SFR organization to be reached.

- Direct addressing: the instruction carries the 8-bit operand address explicitly.
- Indirect addressing: the instruction names a register that holds the operand address.

Within 80h to FFh, direct accesses choose the SFR space while indirect accesses choose Upper IDATA RAM. Addresses 00h to 7Fh always choose Lower IDATA RAM. Table 4 summarizes this mapping.

Table 4. IDATA memory addressing

Address	Addressing mode	
	Direct	Indirect
00h to 7Fh	Lower IDATA RAM	Lower IDATA RAM
80h to FFh	SFRs	Upper IDATA RAM

Table 5 lists the SFR address map.

Table 5. SFR map of NFC controller

Ad - dress	Bit- address - able			By	te-address - able				Ad - dress
F8h	IP1		XRAMP		P3CFGA	P3CFGB			FFh
F0h	B				P7CFGA	P7CFGB		P7	F7h
E8h	IE1	CIU_Status2	CIU_FI - FOData	CIU_FIFO - Level	CIU_Water - Level	CIU_Con - trol	CIU_BitFram - ing	CIU_Coll	EFh
E0h	ACC								E7h
D8h	I^2CCON	I^2CSTA	I^2CDAT	I^2CADR				CIU_Status1	DFh
D0h	PSW	CIU_Command	CIU_CommIEn	CIU_DivIEn	CIU_CommIrq	CIU_DivIrq	CIU_Error		D7h
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	T2L	T2H			CFh
C0h									C7h
B8h	IP0								BFh
B0h	P3								B7h
A8h	IE0	SPIcontrol	SPIstatus	HSU_STA	HSU_CTR	HSU_PRE	HSU_CNT		AFh
A0h		FITEN	FDATA	FSIZE					A7h
98h	SOCON	SBUF	RWL	TWL	FIFOFS	FIFOFF	SFF	FIT	9Fh
90h									97h
88h	T01CON	T01MOD	T0L	T1L	T0H	T1H			8Fh
80h		SP	DPL	DPH				PCON	87h

8.1.2.2 XRAM memory

The XRAM memory is partitioned into 2 memory spaces:

- 0000h to 5FFFh: reserved for addressing embedded RAM. For the NF532, only accesses between 0000h and 02FF are valid.
- 6000h to 7FFFh: reserved for addressing embedded peripherals. This space is partitioned into 32 regions of 256 bytes each. Addressing may be carry outed by means of R0 or R1 and the XRAMP SFR.

The Table 6 depicts the mapping of internal peripherals into XRAM.

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Table 6. Peripheral mapping into XRAM memory space

Base Address	End Address	Description
6000h	60FFh	Reserved.
6100h	61FFh	IOs and miscellaneous registers configuration Refer to Section 8.2 “ General purpose IOs configurations ”
6200h	62FFh	Power Clock and Reset controller Refer to Section 8.5.7 “ PCR extension registers ”
6300h	633Fh	Contactless Unit Interface Refer to Section 8.6 “ Contactless Interface Unit (CIU) ”
6340h	FFFFh	Reserved

MOVX instructions are intended for XRAM access. Two addressing methods are accessible:

- 16-bit DPTR addressing: offers access across the complete XRAM address space.
- Paged addressing: XRAMP supplies the upper address byte, while R0 or R1 supplies the lower byte.

The Figure 5 illustrates both mechanisms.

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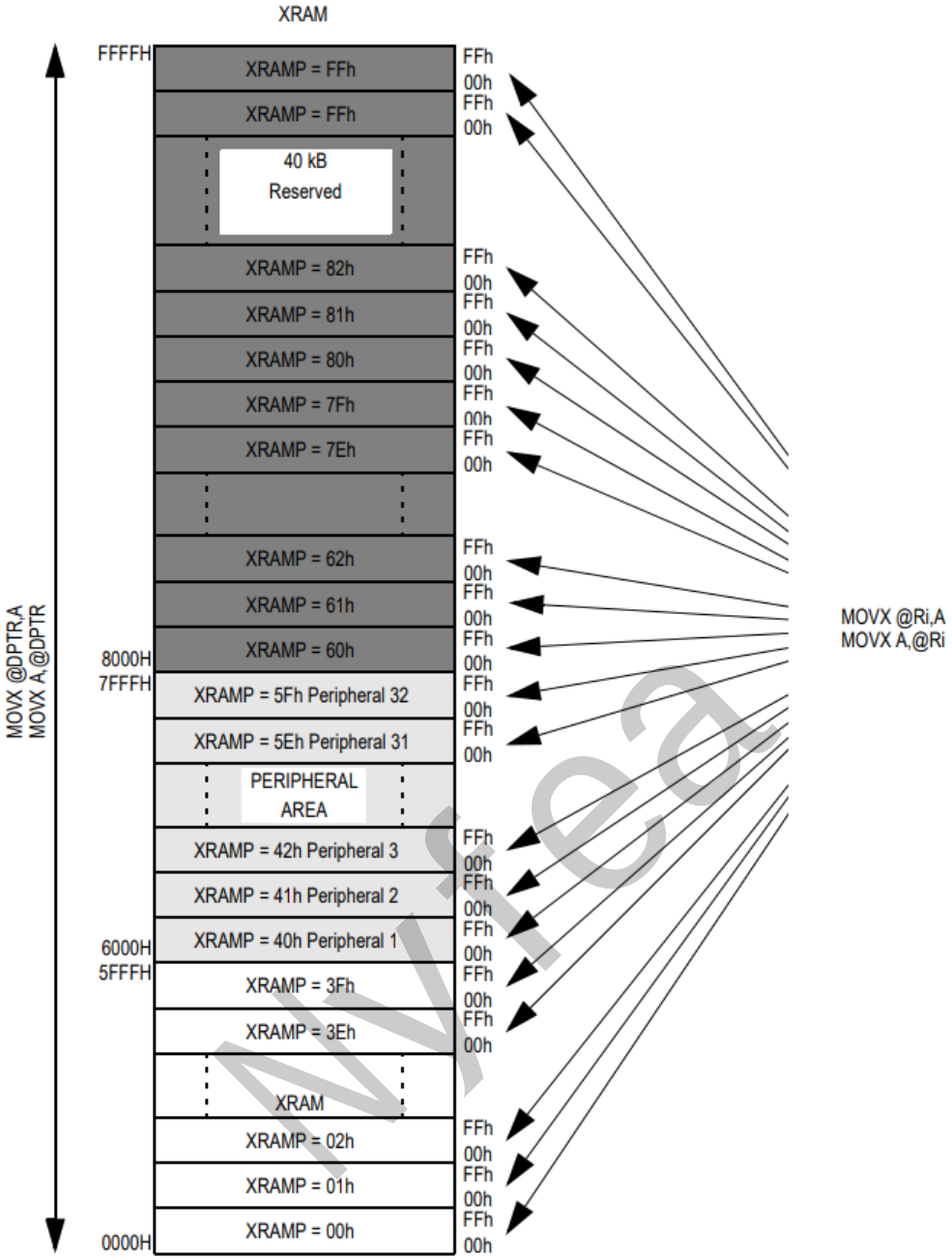


Fig 5. Indirect addressing of XRAM memory space

8.1.3 Program memory

Program addresses 0000h through 9FFFh map to the internal 40 KB ROM.

8.1.4 PCON module

The PCON SFR offers configuration of the CPU power-control function.

Table 7. PCON register (SFR: address 87h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SMOD			-			CPU_PD	-
Reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R/W	R/W

Table 8. Description of PCON bits

Bit	Symbol	Description
7	SMOD	**Serial MODe:** When this bit is set to 1, the baud rate of the Debug UART is doubled
6 to 3	-	Reserved.
1	CPU_PD	**Power-down:** When this bit is set to 1, the microcontroller goes in Power-down mode
0	Reserved	**Keep this bit at 0.**

8.1.5 Interrupt Controller

The interrupt controller provides:

- 13 interrupt sources
- Interrupt enable registers IE0 and IE1
- Interrupt priority registers IP0 and IP1
- Wake-up from Power-Down state

8.1.5.1 Interrupt vectors

The mapping between interrupt sources and interrupt vectors is shown in Table 9.

Table 9. Interrupt vector

Interrupt number	Interrupt vector	Interrupt sources	Incremental priority level (conflict resolution level)
0	0003h	External P32_INT0	Highest
1	000Bh	Timer0 interrupt	
2	0013h	External P33_INT1	
3	001Bh	Timer1 interrupt	
4	0023h	Debug UART interrupt	
5	002Bh	Timer2 interrupt	
6	0033h	NFC-WI interrupt	
7	003Bh	LDO overcurrent interrupt	
8	0043h	Reserved	
9	004Bh	CIU interrupt 1	
10	0053h	CIU interrupt 0	
11	005Bh	I^2C interrupt	
12	0063h	SPI, FIFO, or HSU interrupts	
13	006Bh	Reserved	
14	0073h	General Purpose IRQ	Lowest

8.1.5.2 Interrupt enable: IE0 and IE1 registers

Each interrupt source may be enabled or disabled independently by setting a bit in IE0 or IE1. In register IE0, a global interrupt enable bit may be cleared to 0 to disable all interrupts at once.

The 2 table belows describe IE0.

Table 10. Interrupt controller IE0 register (SFR: address A8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IE0_7	IE0_6	IE0_5	IE0_4	IE0_3	IE0_2	IE0_1	IE0_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 11. Description of IE0 bits

Bit	Symbol	Description
7	IE0_7	**Global interrupt enable** When this bit is set to 1, the interrupts may be enabled. When this bit is cleared to 0, all the interrupts are disabled.
6	IE0_6	**NFC-WI counter interrupt enable** When this bit is set to 1, NFC-WI interrupt is enabled. See Table 164.
5	IE0_5	**Timer2 interrupt enable** When this bit is set to 1, Timer2 interrupt is enabled. See Table 36.
4	IE0_4	**Debug UART interrupt enable** When this bit is set to 1, Debug UART interrupt is enabled. See Table 49.
3	IE0_3	**Timer1 interrupt enable** When this bit is set to 1, Timer1 interrupt is enabled. See Table 23.
2	IE0_2	**P33_INT1 interrupt enable** When this bit is set to 1, P33_INT1 pin interrupt is enabled. See Table 23. The polarity of P33_INT1 may be inverted (see Table 73).
1	IE0_1	**Timer0 interrupt enable** When this bit is set to 1, Timer0 interrupt is enabled. See Table 23.
0	IE0_0	**P32_INT0 interrupt enable** When this bit is set to 1, P32_INT0 pin interrupt is enabled. See Table 23.

The 2 following tables describe IE1.

Table 12. Interrupt controller IE1 register (SFR: address E8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IE1_7	-	IE1_5	IE1_4	IE1_3	IE1_2	-	IE1_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13. Description of IE1 bits

Bit	Symbol	Description
7	IE1_7	**General purpose IRQ interrupt enable.** Setting this bit to 1 enables interrupt function of P34, P35, P50_SCL and P71 in accordance with their respective enable and level control bits. See Table 19 , Table 137 andTable 143.
6	-	Reserved; keep this bit at 0
5	IE1_5	**FIFO, SPI and HSU interrupt enable.** Setting this bit to 1 enables FIFO interrupts, SPI interrupts, HSU interrupt. In HSU mode, the interrupt is when NSS is at 0. For the FIFO interrupts, see Table 112. For the SPI interrupts, see Table 122.
4	IE1_4	**I²C interrupt enable.** Setting this bit to 1 enables I^2C interrupt. See Table 77.
3	IE1_3	**CIU interrupt 0 enable.** Setting this bit to 1 enables CIU interrupt 0: CIU_IRQ_0. See Table 190.
2	IE1_2	**CIU interrupt 1 enable.** Setting this bit to 1 enables the CIU interrupt 1: CIU_IRQ_1. See Table 190 .
1	-	Reserved; keep this bit at 0.
0	IE1_0	LDO overcurrent interrupt enable. Setting this bit to 1 enables the LDO overcurrent detection interrupt. See Table 127.

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8.1.5.3 Interrupt prioritization: IP0 and IP1 registers

IP0 and IP1 assign each interrupt source to one of two priority classes. If two interrupt requests of various priority levels are accepted at the same time, the request with the high priority is serviced first. On the other hand, if the interrupts are of the same priority, precedence is resolved by comparing their respective conflict resolution levels (see Table 9 for details). The processing of a low priority interrupt can be interrupted by one with a high priority.

A RETI (Return From Interrupt) instruction jumps to the address immediately succeeding the point at which the interrupt was serviced. The instruction found at the return address is executed, prior to servicing any pending interrupts.

The 2 following tables describe IP0.

Table 14. Interrupt controller IP0 register (SFR: address B8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IP0_7	IP0_6	IP0_5	IP0_4	IP0_3	IP0_2	IP0_1	IP0_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 15. Description of IP0 bits

Bit	Symbol	Description
7	IP0_7	Reserved
6	IP0_6	When this bit is set to 1, NFC-WI interrupt is set to high priority.
5	IP0_5	When this bit is set to 1, Timer2 interrupt is set to high priority.
4	IP0_4	When this bit is set to 1, Debug UART interrupt is set to high priority.
3	IP0_3	When this bit is set to 1, Timer1 interrupt is set to high priority.
2	IP0_2	When this bit is set to 1, external P33_INT1 pin is set to high priority.
1	IP0_1	When this bit is set to 1, Timer0 interrupt is set to high priority.
0	IP0_0	When this bit is set to 1, external P32_INT0 pin is set to high priority.

The 2 following tables describe IP1.

Table 16. Interrupt controller IP1 register (SFR: address F8h) bit allocation

Bit	7	6	5	4	3	2	1 0
Symbol	IP1_7	-	IP1_5	IP1_4	IP1_3	IP1_2	-
Reset	0	0	0	0	0	0	00
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 17. Description of IP1 bits

Bit	Symbol	Description
7	IP1_7	When this bit is set to 1, General-purpose IRQ interrupt is set to high priority.
6	-	Reserved; keep this bit at 0.
5	IP1_5	When this bit is set to 1, combined SPI, FIFO and HSU interrupt is set to high priority.
4	IP1_4	When this bit is set to 1, I^2C interrupt is set to high priority.
3	IP1_3	When this bit is set to 1, CIU interrupt 0 is set to high priority.
2	IP1_2	When this bit is set to 1, CIU interrupt 1 is set to high priority.
1	-	Reserved; keep this bit at 0.
0	IP1_0	When this bit is set to 1, interrupt number 7 is set to high priority.

8.1.5.4 General purpose IRQ control

GPIRQ holds the controls for the general-purpose interrupt inputs.

Note: this GPIRQ function is an NF532-specific extension to the standard 8051 feature set.

Table 18. GPIRQ register (address 6107h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	gpirq_level_P71	gpirq_level_P50	gpirq_level_P35	gpirq_level_P34	gpirq_enable_P71	gpirq_enable_P50	gpirq_enable_P35	gpirq_enable_P34
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 19. Description of GPIRQ bits

Bit	Symbol	Description
7	gpirq_level_P71	**Selects the signal polarity on P71 to generate a GPIRQ interrupt event (assuming gpirq_enable_P71 is set).** When this bit is cleared to 0, an interrupt is generated if P71 is at 0. When this bit is set to 1, an interrupt is generated if P71 is at 1.
6	gpirq_level_P50	**Selects the signal polarity on P50 to generate a GPIRQ interrupt event (assuming gpirq_enable_P50 is set).** When this bit is cleared to 0, an interrupt is generated if P50_SCL is at 0. When this bit is set to 1, an interrupt is generated if P50_SCL is at 1.
5	gpirq_level_P35	**Selects the signal polarity on P35 to generate a GPIRQ interrupt event (assuming gpirq_enable_P35 is set).** When this bit is cleared to 0, an interrupt is generated if P35 is at 0. When this bit is set to 1, an interrupt is generated if P35 is at 1.
4	gpirq_level_P34	**Selects the signal polarity on P34 to generate a GPIRQ interrupt event (assuming gpirq_enable_P34 is set).** When this bit is cleared to 0, an interrupt is generated if P34 is at 0. When this bit is set to 1, an interrupt is generated if P34 is at 1. **Remark**:If hide_svdd_sig of the register control_rngpower is set and gpirq_enable_P34 is also set then this bit will be asserted independently of the level on the pad P34.
3	gpirq_enable_P71	Setting this bit to 1 enables pad P71 to generate a GPIRQ interrupt event~~. ~~[1]
2	gpirq_enable_P50	Setting this bit to 1 enables pad P50_SCL to generate a GPIRQ interrupt event~~. ~~[1]
1	gpirq_enable_P35	Setting this bit to 1 enables pad P35 to generate a GPIRQ interrupt event~~. ~~[1]
0	gpirq_enable_P34	Setting this bit to 1 enables pad P34 to generate a GPIRQ interrupt event~~. ~~[1]

[1] The bit IE1_7 of register IE1 (see Table 13) has also to be set to 1 to enable the associated CPU interrupt.

8.1.6 Timer0/1 description

Timer0 and Timer1 are general-purpose timer/counter blocks with the next capabilities:

- Configurable edge or level detection interrupts
- Timer or counter operation
- 4 timer/counter modes
- Baud rate generation for Debug UART

The module holds two 16-bit counters, Timer0 and Timer1. Either block can operate from the internal timing source or as an external event counter.

Four operating states are accessible:

- Mode 0: 13-bit timer/counter
- Mode 1: 16-bit timer/counter

- Mode 2: 8-bit timer/counter with programmable preload value
- Mode 3: two individual 8-bit timer/counters (Timer0 only)

In the 'timer' function, the timer/counter is incremented every machine cycle. The count rate is 1/6 of the CPU clock frequency (CPU_CLK).

In the 'counter' function, the timer/counter is incremented in response to a 1-to-0 transition on the input pins P34 / SIC_CLK (Timer0) or P35 (Timer1). In this operating state, the external input is sampled during state S5 of every machine cycle. If the associated pin is at 1 for a machine cycle, followed by 0 on the next machine cycle, the count is incremented. The new count value appears in the timer/counter in state S3 of the machine cycle following the one in which the transition was detected. The maximum count rate is 1/12 of the CPU_CLK frequency. There are no restrictions on the duty cycle of the external input signal but to ensure that a given level is sampled no less than once prior to it changes, it should be held for no less than one full machine cycle.

The overflow output 't1_ovf' of Timer1 may be used as a baud rate generator for the Debug UART. The Timer1 interrupt should be disabled for this case. For most applications which drive the Debug UART, Timer1 is configured for 'timer' operation and in auto-reload mode.

8.1.6.1 Timer0/1 registers

Six CPU-accessible SFRs implement the Timer0/1 register interface.

Table 20. Timer0/1 Special Function registers list

Name	Size [bytes]	Address Offset	Description	Access
T01CON	1	88h	Timer0/1 control register	R/W
T01MOD	1	89h	Timer0/1 mode register	R/W
T0L	1	8Ah	Lower byte of the Timer0 timer/counter	R/W
T1L	1	8Bh	Lower byte of the Timer1 timer/counter	R/W
T0H	1	8Ch	Upper byte of the Timer0 timer/counter	R/W
T1H	1	8Dh	Upper byte of the Timer1 timer/counter	R/W

The firmware carries out a register read in state S5 and a register write in state S6. The hardware writes bits TF0 and TF1 of the register T01CON during state S2 and state S4 respectively. The hardware writes bits IE0 and IE1 of the register T01CON during state S1 and reset these bits during state S2. The registers T0L, T0H, T1L, T1H are updated by the hardware during states S1, S2, S3 and S4 respectively. At the end of a machine cycle, the firmware load has overridden the hardware load as the firmware writes in state S6.

Table 21. Timer0/1 SFR registers CPU state access

		CPU STAT	E				
Register	Bit	S1	S2	S3	S4	S5	S6
T01CON	TF0		HW read			SW read	SW write
	TF1				HW read	SW read	SW write
	IE0 / IE1	HW write	HW reset			SW read	SW write
T0L		HW write				SW read	SW write
T0H			HW write			SW read	SW write
T1L				HW write		SW read	SW write
T1H					HW write	SW read	SW write

8.1.6.2 T01CON register

The register controls Timer0/1 and report its status.

Table 22. Timer0/1 T01CON register (SFR address 88h), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 23. Description of Timer0/1 T01CON register bits

Bit	Symbol	Description
7	TF1	**Timer1 overflow.** Set to 1 by hardware on a Timer1 overflow. The flag is cleared to 0 by the CPU after 2 machine cycles. The bit IE0_3 of register IE0 (see Table 11)has to be set to 1 to enable the corresponding CPU interrupt.
6	TR1	**Timer1 run control.** Controlled by firmware only. When this bit is set to 1, Timer1 is enabled.
5	TF0	**Timer0 overflow.** Set by hardware on a Timer0 overflow. The flag is cleared to 0 by the CPU after 2 machine cycles. The bit IE0_1 of register IE0 (see Table 11)has to be set to 1 to enable the corresponding CPU interrupt.
4	TR0	**Timer0 run control.** Controlled by firmware only. When this bit is set to 1, Timer0 is enabled.
3	IE1	**External Interrupt1 event.** Set to 1 by hardware when an external interrupt is detected on P33_INT1. The bit IE0_2 of register IE0 (see Table 11)has to be set to 1 to enable the corresponding CPU interrupt.
2	IT1	**External Interrupt1 control.** Controlled by firmware only. When this bit is set to 1, Interrupt1 triggers on a falling edge of P33_INT1. When this bit is cleared to 0, Interrupt1 triggers on a low level of P33_INT1.
1	IE0	**External Interrupt0 event.** Set to 1 by hardware when an external interrupt is detected on P32_INT0. The bit IE0_0 of register IE0 (see Table 11)has to be set to 1 to enable the corresponding CPU interrupt.
0	IT0	**External Interrupt0 control.** Controlled by firmware only. When this bit is set to 1, Interrupt0 triggered by a falling edge on P32_INT0. When this bit is cleared to 0, Interrupt0 triggered by a low level on P32_INT0.

8.1.6.3 T01MOD register

This register configures Timer0/1.

Table 24. Timer 0/1 T01MOD register (SFR address 89h), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GATE1	C/T1	M11	M10	GATE0	C/T0	M01	M00
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25. Description of T01MOD bits

Bit	Symbol	Description
7	GATE1	**Timer1 gate control.** Controlled by firmware only. When this bit is set to 1, Timer1 is enabled only when P33_INT1 is high and bit TR1 of register T01CON is set. When this bit is cleared to 0, Timer1 is enabled.
6	C/T1	**Timer1 timer/counter selector.** Controlled by firmware only. When this bit is set to 1, Timer1 operates as a counter. When this bit is cleared to 0, Timer1 operates as a timer.

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Bit	Symbol	Description
5 to 4	M[11:10]	**Timer1 mode.** Controlled by firmware only. • Mode 0: M11 = 0 and M10 = 0 — 8192 counter; T1L serves as a 5-bit prescaler. • Mode 1: M11 = 0 and M10 = 1 — 16-bit timer/counter; T1H and T1L are cascaded. • Mode 2: M11 = 1 and M10 = 0 — 8-bit auto-reload timer/counter; T1H stores the value reloaded into T1L whenever T1L overflows. • Mode 3: M11 = 1 and M10 = 1 — Timer1 is stopped (count frozen).
3	GATE0	**Timer0 gate control.** Controlled by firmware only. When this bit is set to 1, Timer0 is enabled only when P32_INT0 is high and bit TR0 of register T01CON is set. When this bit is cleared to 0, Timer0 is enabled.
2	C/T0	**Timer0 timer/counter selector.** Controlled by firmware only. When this bit is set to 1, Timer0 operates as a counter. When this bit is cleared to 0, Timer0 operates as a timer.
1 to 0	M[01:00]	**Timer0 mode.** Controlled by firmware only. • Mode 0: M01 = 0 and M00 = 0 — 8192 timer; T0L acts as a 5-bit prescaler. • Mode 1: M01 = 0 and M00 = 1 — 16-bit timer/counter; T0H and T0L are cascaded. • Mode 2: M01 = 1 and M00 = 0 — 8-bit auto-reload timer/counter; T0H stores the value reloaded into T0L whenever T0L overflows. • Mode 3: M01 = 1 and M00 = 1 — Timer0 is split into two 8-bit timer/counters, T0H and T0L. T0H is controlled by TR1; T0L is controlled by the normal Timer0 control expression {P32_INT0 OR (NOT GATE0)} AND TR0.

8.1.6.4 T0L and T0H registers

T0L and T0H hold the live Timer0 count value, with T0L providing the low byte and T0H the high byte.

Table 26. Timer0/1 T0L register (SFR address 8Ah), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T0L.7	T0L.6	T0L.5	T0L.4	T0L.3	T0L.2	T0L.1	T0L.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 27. Description of T0L bits

Bit	Symbol	Description
7 to 0	T0L.7 to T0L.0	Lower byte of the Timer0 timer/counter

Table 28. Timer0/1 T0H register (SFR address 8Ch), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T0H.7	T0H.6	T0H.5	T0H.4	T0H.3	T0H.2	T0H.1	T0H.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 29. Description of T0H bits

Bit	Symbol	Description
7 to 0	T0H.7 to T0H.0	Upper byte of the Timer0 timer/counter

8.1.6.5 T1L and T1H registers

T1L and T1H hold the active Timer1 count, with T1L as the low byte and T1H as the high byte.

Table 30. Timer0/1 T1L register (SFR address 8Bh), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T1L.7	T1L.6	T1L.5	T1L.4	T1L.3	T1L.2	T1L.1	T1L.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 31. Description of T1L bits

Bit	Symbol	Description
7 to 0	T1L.7 to T1L.0	Lower byte of the Timer1 timer/counter

Table 32. Timer0/1 T1H register (SFR address 8Dh), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T1H.7	T1H.6	T1H.5	T1H.4	T1H.3	T1H.2	T1H.1	T1H.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 33. Description of T1H bits

Bit	Symbol	Description
7 to 0	T1H.7 to T1H.0	Upper byte of the Timer1 timer/counter

8.1.6.6 Incrementer

The two 16-bit timer/counters are built around an 8-bit incrementer. The Timer0/1 are incremented in the CPU states S1 to S4; the overflow flags are set in CPU states S2 and S4.

- CPU state S1: TOL is incremented if Timer0 is set to:
  - timer operation
  - counter operation and when a 1-to-0 transition is detected on P34 / SIC_CLK input.
- CPU state S2: TOH is incremented if:
  - TOL overflows. The overflow flag TF0 in register T01CON is updated.
- CPU state S3: T1L is incremented if Timer1 is set to:
  - timer operation or
  - counter operation and when a 1-to-0 transition is detected on P35 input.
- CPU state S4: T1H is incremented if:
  - T1L overflows. The overflow flag TF1 in register T01CON is updated.

8.1.6.7 Overflow detection

For both the upper and lower bytes of the Timer0/1, an overflow is detected by comparing the incremented value of the most significant bit with its previous value. An overflow occurs when this bit changes from 1 to 0. An overflow event in the lower byte is clocked into a flip-flop and is employed in the next state as the increment enable for the upper byte. An overflow event in the upper byte will set the associated overflow bit in the T01CON register to 1. The upper byte overflow is also clocked into a flip-flop to produce the output signals ‘t0_ovf’ and ‘t1_ovf’.

The overflow flags TF0 and TF1, found in register T01CON, are loaded during states S2 and S4 respectively. The interrupt controller of the 80C51 scans all requests at state S2. Thus, an overflow of Timer0 or Timer1 is detected one machine cycle after it occurred. When the request is serviced, the interrupt routine sets the overflow flag to 0.

Execution of the interrupt routine begins on the fourth machine cycles following the timer overflow. When Timer0/1 receives the acknowledge from the CPU:

- the overflow flag TF0 in register T01CON is cleared to 0
- two machine cycles later, the overflow flag TF1 in register T01CON is cleared to 0

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If during the same machine cycle, an overflow flag is cleared to 0 due to a CPU acknowledge and set to 1 due to an overflow, the set to 1 is the strongest.

8.1.7 Timer2 description

Timer2 supports a subset of the standard Timer2 found in the 8052 microcontroller. Timer2 may be configured into 2 functional states via the T2CON and T2MOD registers:

- Mode1: Auto-reload up/down counting
- Mode2: Baud rate generation for Debug UART

Timer2 can operate either as a timer or as an event counter.

8.1.7.1 Timer2 registers

Timer2 holds six Special Function Registers (SFRs) which may be accessed by the CPU.

Table 34. Timer2 SFR register List

Name	Size [bytes]	SFR address	Description	Access
T2CON	1	C8h	Timer2 control register	R/W
T2MOD	1	C9h	Timer2 mode register	R/W
RCAP2L	1	CAh	Timer2 reload lower byte	R/W
RCAP2H	1	CBh	Timer2 reload upper byte	R/W
T2L	1	CCh	Lower byte of the Timer2 timer/counter	R/W
T2H	1	CDh	Upper byte of the Timer2 timer/counter	R/W

Timer2 registers may be written to by either hardware or firmware. If both the hardware and firmware attempt to update the registers T2H, T2L, RCAP2H or RCAP2L during the same machine cycle, the firmware write takes precedence. A firmware write occurs in state S6 of the machine cycle.

Each increment or decrement of Timer2 occurs in state S1 except when in baud rate generation mode and configured as a counter. In this operating state, Timer2 increments on each clock cycle. When configured as a timer, Timer2 is incremented every machine cycle. Since a machine cycle is made up of 6 clock periods, the count rate is 1/6 of the CPU clock frequency.

8.1.7.2 T2CON register

The register controls Timer2 and report its status.

Table 35. Timer2 T2CON register (SFR address C8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TF2	-	RCLK0	TCLK0	-	TR2	C/T2	-
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 36. Description of T2CON bits

Bit	Symbol	Description
7	TF2	Timer2 overflow Set to 1 by a Timer2 overflow. Set to 0 by firmware. TF2 is not set when in baud rate generation mode. The bit IE0_5 of register IE0 (see Table 11)has to be set to logic 1 to enable the corresponding CPU interrupt.
6	-	Reserved.

Bit	Symbol	Description
5	RCLK0	**Timer2 Debug UART Receive Clock selector**. Controlled by firmware only. When this bit is set to 1, Debug UART uses Timer2 overflow pulses. When this bit is cleared to 0, Debug UART uses overflow pulses from another source (e.g. Timer1 in a standard configuration).
4	TCLK0	**Timer2 Debug UART Transmit Clock selector**. Controlled by firmware only. When this bit is set to 1, Debug UART uses Timer2 overflow pulses. When this bit is cleared to 0, Debug UART uses overflow pulses from another source (e.g. Timer1 in a standard configuration).
3	-	Reserved.
2	TR2	**Timer2 Run control**. Controlled by firmware only. When this bit is set to 1, Timer2 is started. When this bit is cleared to 0, Timer2 is stopped.
1	C/T2	**Timer2 Counter/Timer selector**. Controlled by firmware only. When this bit is set to 1, Timer2 is set to counter operation. When set to logic0, Timer2 is set to timer operation.
0	-	Reserved. **This bit must be cleared to 0 by firmware.**

8.1.7.3 T2MOD register

This Special Function Register serves to configure Timer2.

Table 37. Timer2 T2MOD register (SFR address C9h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	T2RD	-	DCEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 38. Description of TMOD bits

Bit	Symbol	Description
7 to 3	-	Reserved.
2	T2RD	**Timer2 ReaD flag**. This bit may be updated by hardware or firmware. Hardware sets this bit to 1, if T2H is incremented between reading T2L and reading T2H. This bit is cleared to 0, on the trailing edge of next T2L read. This bit serves to indicate that the 16-bit Timer2 register is not read properly since the T2H part was incremented by hardware before it was read.
1	-	Reserved
0	DCEN	**Timer2 Down Count ENable**. Controlled by firmware only. When this bit is set, Timer2 may be configured (in auto_reload mode) as an up-counter. When this bit is reset, Timer2 may be configured (in auto-reload mode) as a down-counter.

8.1.7.4 T2L, T2H registers

T2L and T2H hold the active Timer2 count; T2L is the low byte and T2H is the high byte.

On the fly reading can give a wrong value since T2H may be changed after T2L is read and before T2H is read. This situation is shown by flag T2RD in T2MOD.

The two 8-bit registers operate together as a single 16-bit timer/counter.

Table 39. Timer2 T2L register (SFR address CCh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T2L.7	T2L.6	T2L.5	T2L.4	T2L.3	T2L.2	T2L.1	T2L.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 40. Description of T2L bits

Bit	Symbol	Description
7 to 0	T2L.7 to T2L.0	Lower byte of the Timer2 timer/counter

Table 41. Timer2 T2H register (SFR address CDh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T2H.7	T2H.6	T2H.5	T2H.4	T2H.3	T2H.2	T2H.1	T2H.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 42. Description of T2H bits

Bit	Symbol	Description
7 to 0	T2H.7 to T2H.0	Upper byte of the Timer2 timer/counter

8.1.7.5 RCAP2L, RCAP2H registers

RCAP2L and RCAP2H store the Timer2 reload value. During reload operation, their contents are transferred to T2L and T2H respectively.

Table 43. Timer2 RCAP2L register (SFR address CAh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	R2L.7	R2L.6	R2L.5	R2L.4	R2L.3	R2L.2	R2L.1	R2L.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 44. Description of RCAP2L bits

Bit	Symbol	Description
7 to 0	R2L.7 to R2L.0	Lower reload byte for Timer2

Table 45. Timer2 RCAP2H register (SFR address CBh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	R2H.7	R2H.6	R2H.5	R2H.4	R2H.3	R2H.2	R2H.1	R2H.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 46. Description of RCAP2H bits

Bit	Symbol	Description
7 to 0	R2H.7 to R2H.0	Upper reload byte for Timer2

8.1.8 Debug UART

The Debug UART offers a serial debug channel through the UART_RX and UART_TX pins.

8.1.8.1 Feature list

The Debug UART offers the next functions:

- Full duplex serial port
- Receive buffer to allow reception of a second byte while the first byte is being read out by the CPU
- Four modes of operation which support 8-bit and 9-bit data transfer at various baud rates
- Supports multi-processor communication

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- Baud rate may be controlled through Timer1 or Timer2 baud rate generator

8.1.8.2 Debug UART functional description

The serial port has a receive buffer: a second byte may be held while the previous one is read out of the buffer by the CPU. Nevertheless, if the first byte has still not been read by the time reception of the second byte is complete, one of the bytes is lost.

The receive and send data registers of the serial port are both accessed by firmware via the Special Function Register SOBUF. Writing to SOBUF writes the send register; reading from SOBUF accesses a physically separate receive register.

The serial port may operate in 4 modes. These modes are chosen by programming bits SM0 and SM1 in SOCON:

- Mode 0:
    - Serial data are accepted and transmitted through UART_RX. UART_TX outputs the shift clock. 8 bits are sent/received (LSB first)

Baud rate: fixed at 1/6 of the frequency of the CPU clock

- Mode 1:
    - 10 bits are sent through UART_TX or received through UART_RX: a start bit (0), 8 data bits (LSB first), and a stop bit (1)
    - Receive: The received stop bit is held into bit RB8 of register SOCON
    - Baud rate: variable (is determined by overflow of Timer1 or Timer2)
- Mode 2:
    - 11 bits are sent through UART_TX or received through UART_RX: start bit (0), 8 data bits (LSB first), a 9th data bit, and a stop bit (1)
    - Transmit: the 9th data bit is taken from bit TB8 of SOCON. As an example, the parity bit could be written into TB8.
    - Receive: the 9th data bit is held into RB8 of SOCON, while the stop bit has no effect
    - Baud rate: programmable to either 1/16 or 1/32 the frequency of the CPU clock
- Mode 3:
    - 11 bits are sent through UART_TX or received through UART_RX: a start bit (0), 8 data bits (LSB first), a 9th data bit, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all aspects except the baud rate
    - Transmit: as mode 2, the 9th data bit is taken from TB8 of SOCON
    - Receive: as mode 2, the 9th data bit is held into RB8 of SOCON
    - Baud rate: is determined by overflows of Timer1 or Timer2

The Debug UART initiates transmission and/or reception as follows.

- Transmission is initiated, in modes 0, 1, 2, 3, by any instruction that uses SOBUF as destination
- Reception is initiated, in mode 0, if RI and REN in SOCON are cleared to 0 and 1 respectively
- Reception is initiated in modes 1, 2, 3 by the incoming start bit if REN in SOCON is set to a 1

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The Debug UART holds 2 SFRs:

Table 47. Debug UART SFR register list

Name	Size [bytes]	SFR address	Description	Access
SOCON	1	0098h	Control and status register	R/W
SOBUF	1	0099h	Transmit and receive buffer	R/W

8.1.8.3 SOCON register

The Special Function Register SOCON is the control and status register of the Debug UART. This register holds the mode selection bits (SM2, SM1, SM0), the 9th data bit for send and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 48. Debug UART SOCON register (SFR: address 98h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49. Description of SOCON bits

Bit	Symbol	Description
7 to 6	SM (0:1)	**Mode selection bits 0 and 1.** Controlled by firmware only. The Debug UART provides four modes (see Table 50 “Debug UART modes”).
5	SM2	**Multi-processor communication enable.** Enables the multi-processor communication feature. Controlled by firmware only. • In modes 2 and 3: if SM2 = 1, RI is not activated and RB8/SOBUF are not loaded when the received 9th data bit is 0; if SM2 = 0, it does not affect RI or RB8. • In mode 1: if SM2 = 1, RI is not activated and RB8/SOBUF are not loaded when no valid stop bit is received; if SM2 = 0, it does not affect RI or RB8. • In mode 0, SM2 has no effect.
4	REN	**Serial reception enable.** Controlled by firmware only. Setting this bit to 1 enables reception.
3	TB8	**Transmit data bit.** Controlled by firmware only. In modes 2 and 3, TB8 is transmitted as the 9th data bit. In modes 0 and 1, TB8 is not used.
2	RB8	**Receive data bit.** Set by hardware and firmware.[1] When set: in modes 2 or 3, the received 9th data bit is stored in RB8; in mode 1, the received stop bit is stored in RB8; in mode 0, RB8 remains unchanged.
1	TI	**Transmit interrupt flag.**[3] TI must be cleared by firmware. In modes 2 or 3, hardware sets TI at the end of the 9th bit time; in modes 0 or 1, hardware sets TI at the end of the 8th bit time.
0	RI	**Receive interrupt flag.**[3] RI must be cleared by firmware. In modes 2 or 3, hardware sets RI one clock period after sampling the 9th data bit. In mode 1, RI is set one clock period after sampling the stop bit.[2] In mode 0, RI is set at the end of CPU state 1 of the 9th machine cycle after reception starts.

[1] If SM2 is 1, loading RB8 may be blocked; see the SM2 description above.

[2] If SM2 is 1, setting RI may be blocked; see the SM2 description above.

[3] IE0_4 in register IE0 must also be set to 1 to enable the associated CPU interrupt.

Remark: SOCON includes a locking mechanism that prevents firmware read-modify-write operations from overwriting fields while hardware is updating the register.

Table 50. Debug UART modes

Mode	SM0	SM1	Description	Baud rate
0	0	0	Shift register	fclk/6
1	0	1	8 bits Debug UART	Variable
2	1	0	9 bits Debug UART	fclk/64 or fclk/32
3	1	1	9 bits Debug UART	Variable

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8.1.8.4 SOBUF register

This register is implemented twice. Writing to SOBUF writes to the send buffer. Reading from SOBUF reads from the receive buffer. Only hardware can read from the send buffer and write to the receive buffer.

Table 51. Debug UART SOBUF Register (SFR: address 99h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				SOBU	F[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 52. Description of SOBUF bits

Bit	Symbol	Description
7 to 0	SOBUF[7:0]	Writing to SOBUF writes to the transmit buffer.
		Reading from SOBUF reads from the receive buffer.

8.1.8.5 Mode 0 baud rate

In mode 0, the baud rate is derived from the CPU states signals and thus:

- Baud rate in mode 0 (1)

The next table lists the baud rates in Debug UART mode 0.

Table 53. Baud rates in mode 0

Conditions	Min	Typ	Max	Unit
fCLK	6.78	13.56	27.12	MHz
Baud rate	1.13	2.26	4.52	Mb/s

8.1.8.6 Mode 2 baud rate

In mode 2, the baud rate is determined by the setting of bit SMOD from the SFR register PCON.

The next table lists the baud rates in Debug UART mode 2.

Table 54. Baud rates in mode 2

Conditions	Min	Typ	Max	Unit
fCLK	6.78	13.56	27.12	MHz
Baud rate (SMOD=0)	212	424	847.5	kb/s
Baud rate (SMOD=1)	424	847.5	1695	kb/s

8.1.8.7 Mode 1 and 3 baud rates

In modes 1 and 3, the baud rates are determined by the rate of timer1 and timer2 overflow bits: ‘t1_ovf’ and ‘t2_ovf’. The register bit TCLK0 from the register T2CON chooses if ‘t1_ovf’ or ‘t2_ovf’ should be used as a source when transmitting. The register bit RCLK0 from the register T2CON chooses if ‘t1_ovf’ or ‘t2_ovf’ should be used as a source when receiving. The timers interrupt should be disabled when used to define the Debug UART baud rates.

The data rate is also dependant on the setting of the bit SMOD from the SFR register PCON.

If over1rate is the equivalent ‘t1_ovf’ frequency and over2rate is the equivalent ‘t2_ovf’ frequency then:

See also Section 8.1.8.8 “Baud rates by means of Timer1 (Debug UART mode 1 and 3)”

See also Section 8.1.8.9 “Baud rates by means of Timer2 (Debug UART mode 1 and 3)”

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The next table shows the trigger choose:

Table 55. Trigger select

RCLKO	TCLKO	SMOD	receive trigger rate	transmit trigger rate
0	-	0	over1rate/32	-
0	-	1	over1rate/16	-
1	-	-	over2rate/16	-
-	0	0	-	over1rate/32
-	0	1	-	over1rate/16
-	1	-	-	over2rate/16

8.1.8.8 Baud rates using Timer1 (Debug UART mode 1 and 3)

The Timer1 interrupt should be disabled in this application. The Timer1 itself may be configured for either 'timer' or 'counter' operation, and in any of its 3 running modes. In the most typical applications, it is configured for 'timer' operation, in the auto-reload mode (Timer1 mode 2: high nibble of T01MOD = 0010b). In that case the baud rate is given by the formula:

When rewriting this formula, the setting for the Timer1 reload value T1H is calculated from the desired baud rate as follows:

One can achieve very low baud rates with Timer1 by leaving the Timer1 interrupt enabled, and configuring the timer to run as a 16-bit timer (high nibble of T01MOD = 0001b), and through the Timer1 interrupt to do a 16-bit firmware reload. Note: the frequency fclk is the internal microcontroller frequency. If there is no clock divider then fclk = fosc.

For details on programming Timer1 to function as baud rate generator for the Debug UART see Section 8.1.6 "Timer0/1 description".

The next table lists the maximum baud rates for by means of mode 2 of Timer1.

Table 56. Maximum baud rates using mode 2 of Timer1

Reload value	fCLK divided by	SMOD	Baud ra	te at fCLK		Unit
			6.78	13.56	27.12	MHz
FF	96	1	70.6	141.2	282.5	kb/s

The next table shows commonly used baud rates by means of mode 2 of Timer1 and a CLK frequency of 27.12 MHz.

Table 57. Baud rates using mode 2 of Timer1 with fCLK = 27.12 MHz

Reload value	fCLK divided by	SMOD	Baud rate at fCLK	Unit
FC	706	0	38.4	kb/s
F9	1412	0	19.2	kb/s
F1	2825	0	9.6	kb/s
E3	5650	0	4.8	kb/s
C5	11300	0	2.4	kb/s
8A	22600	0	1.2	kb/s

8.1.8.9 Baud rates using Timer2 (Debug UART mode 1 and 3)

Timer2 has a programming mode to function as baud rate generator for the Debug UART. In this mode the baud rate is given by formula:

When rewriting this formula, the setting for the Timer2 reload values T2RCH/L is calculated from the desired baud rate as follows:

Reload value T2RCH/L (8)

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For details on programming Timer2 to function as baud rate generator for the Debug UART (see Section 8.1.7 “Timer2 description”).

Note: the frequency fclk is the internal microcontroller frequency. If there is no clock divider then fclk = fosc.

The next table lists the maximum baud rates when by means of Timer2.

Table 58. Maximum baud rates using Timer2

Reload value T2RCH/L	fCLK divided by	Baud ra	te		Unit
		6.78	13.56	27.12	MHz
FFFF	16	424	847.5	1695	kb/s

8.2 General purpose IOs configurations

This chapter summarizes the various configurations for the IO pads:

P72, alternate function SCK P71, alternate function MISO P70_IRQ P35 P34, alternate function SIC_CLK P33_INT1 P32_INT0 P31, alternate function UART_TX P30, alternate function UART_RX

Note that in Hard Power Down mode, these ports are disconnected from their supply rail.

For a given port x, there are three configuration registers:

PxCFGA[n] PxCFGB[n] Px[n]

where x is 3 or 7 and n is the bit index.

At maximum 4 various controllable modes may be supported. These modes are defined with the next bits:

- PxCFGA[n]=0 and PxCFGB[n]=0: Open drain
- PxCFGA[n]=1 and PxCFGB[n]=0: Quasi Bidirectional (Reset mode)
- PxCFGA[n]=0 and PxCFGB[n]=1: input (High Impedance)
- PxCFGA[n]=1 and PxCFGB[n]=1: Push/pull output

Px[n] serves to write or read the port value.

Here is the list of the registers used for these GPIO configuration

Table 59. Timer0/1 Special Function registers List

Name	Size [bytes]	SFR address	Description	Access
P3CFGA	1	FCh	Port 3 configuration	R/W
P3CFGB	1	FDh	Port 3 configuration	R/W
P3	1	B0h	Port 3 value	R/W
P7CFGA	1	F4h	Port 7 configuration	R/W
P7CFGB	1	F5h	Port 7 configuration	R/W
P7	1	F7h	Port 7 value	R/W

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8.2.1 Pad configurations description

8.2.1.1 Open-drain

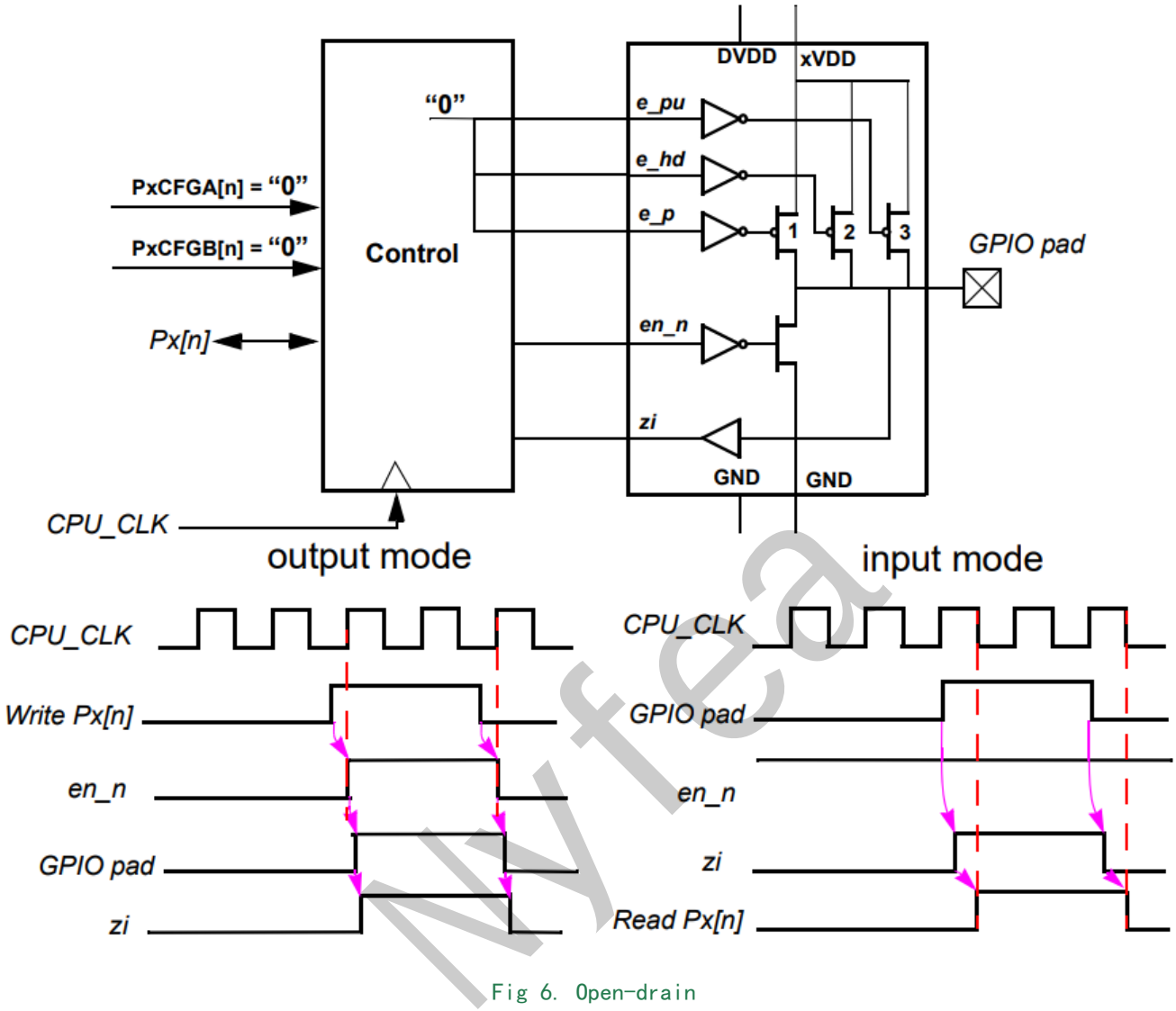


Fig 6. Open-drain

In open drain configuration, an external pull-up resistor is needed to output or read a 1. When writing polarity Px[n] to 0, the GPIO pad is pulled down to 0. When writing polarity Px[n] to 1 the GPIO pad is in High Impedance.

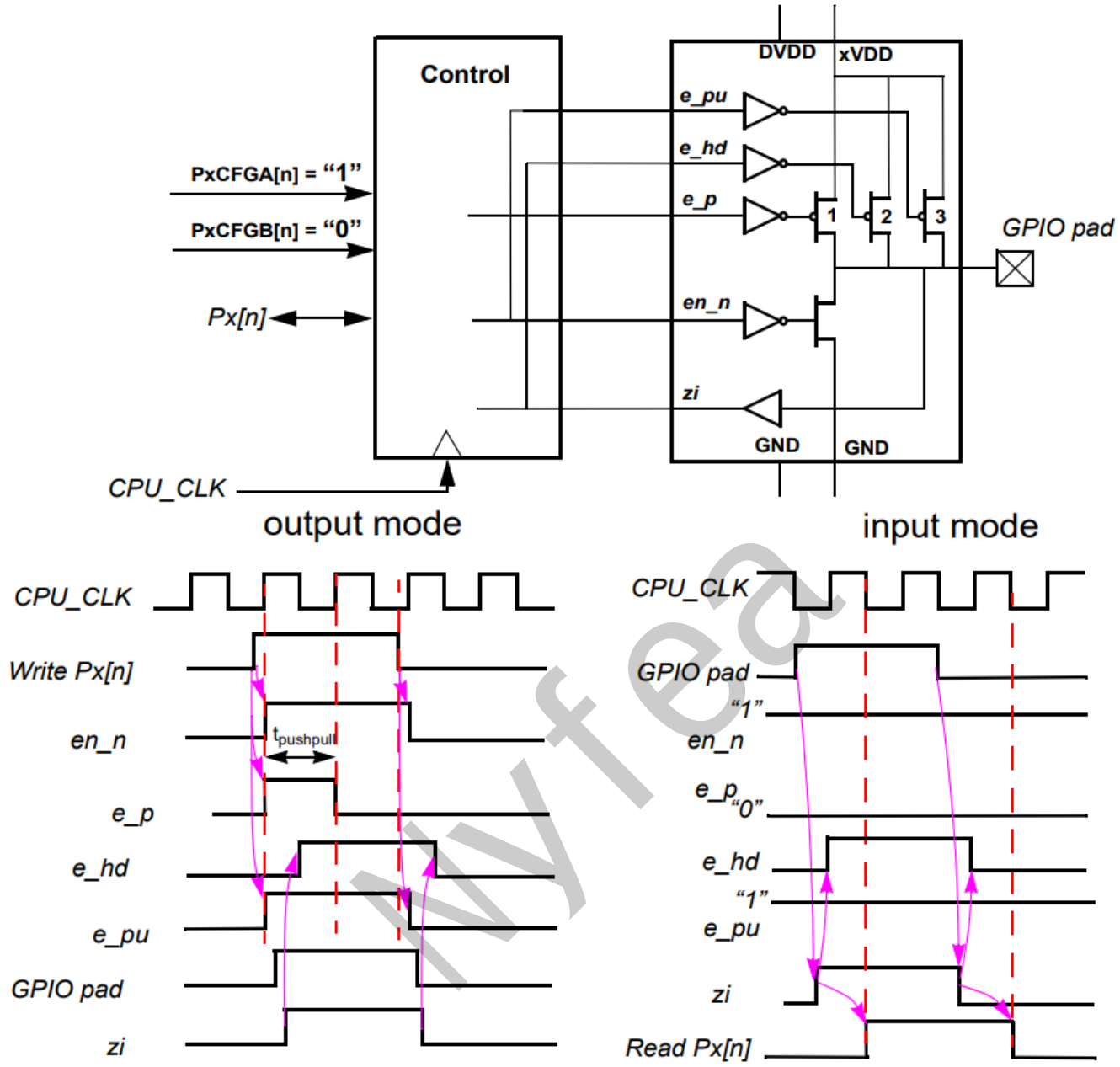


Fig 7. Quasi Bidirectional

In Quasi Bidirectional configuration, e_p is driven to 1 for only one CPU_CLK period when writing Px[n]. During the tpushpull time the pad drives a strong 1 at its output.

While zi (GPIO) is 1, the weak hold transistor (e_hd) is ON, which implements a latch function. Because of the weaker nature of this hold transistor, the pad cell can now act as an input as well.

A third very weak pull-up transistor (e_pu) ensures that an high impedance input is read as 1. e_pu is clocked and is at 1 while Px[n] is at 1.

On a transition from 0 to 1 externally driven on GPIO pad, when the voltage on the pad is at the supply voltage divided by 2, zi goes to 1, the pull-up e_hd is ON. e_hd is an asynchronous signal.

The maximum currents that may be sourced by the e_pu transistor is 80 mA and 500 mA by e_hd transistor.

8.2.1.3 Input

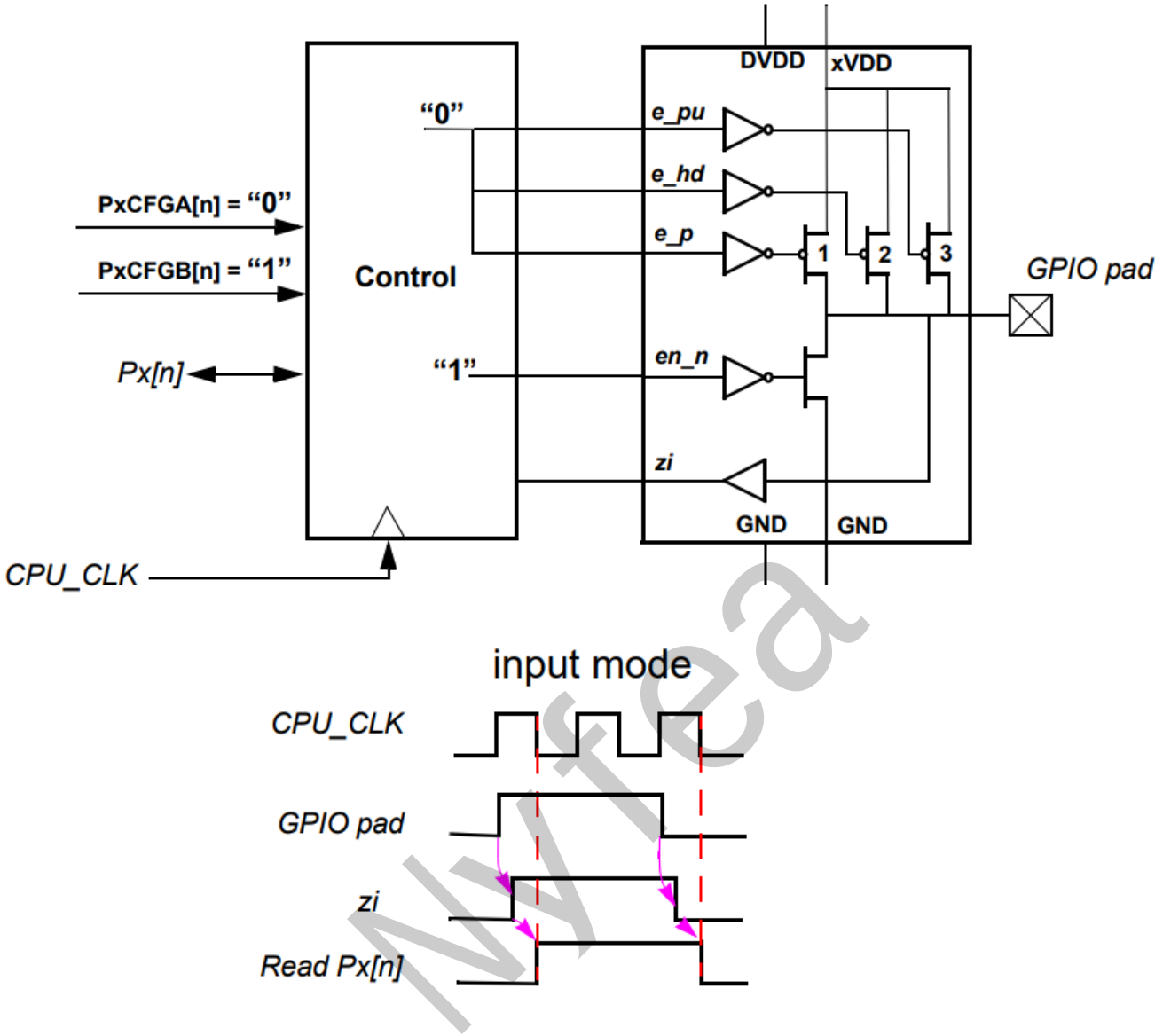


Fig 8. Input

In input configuration, no pull up or hold resistor are internally connected with the pad.

8.2.1.4 Push-pull output

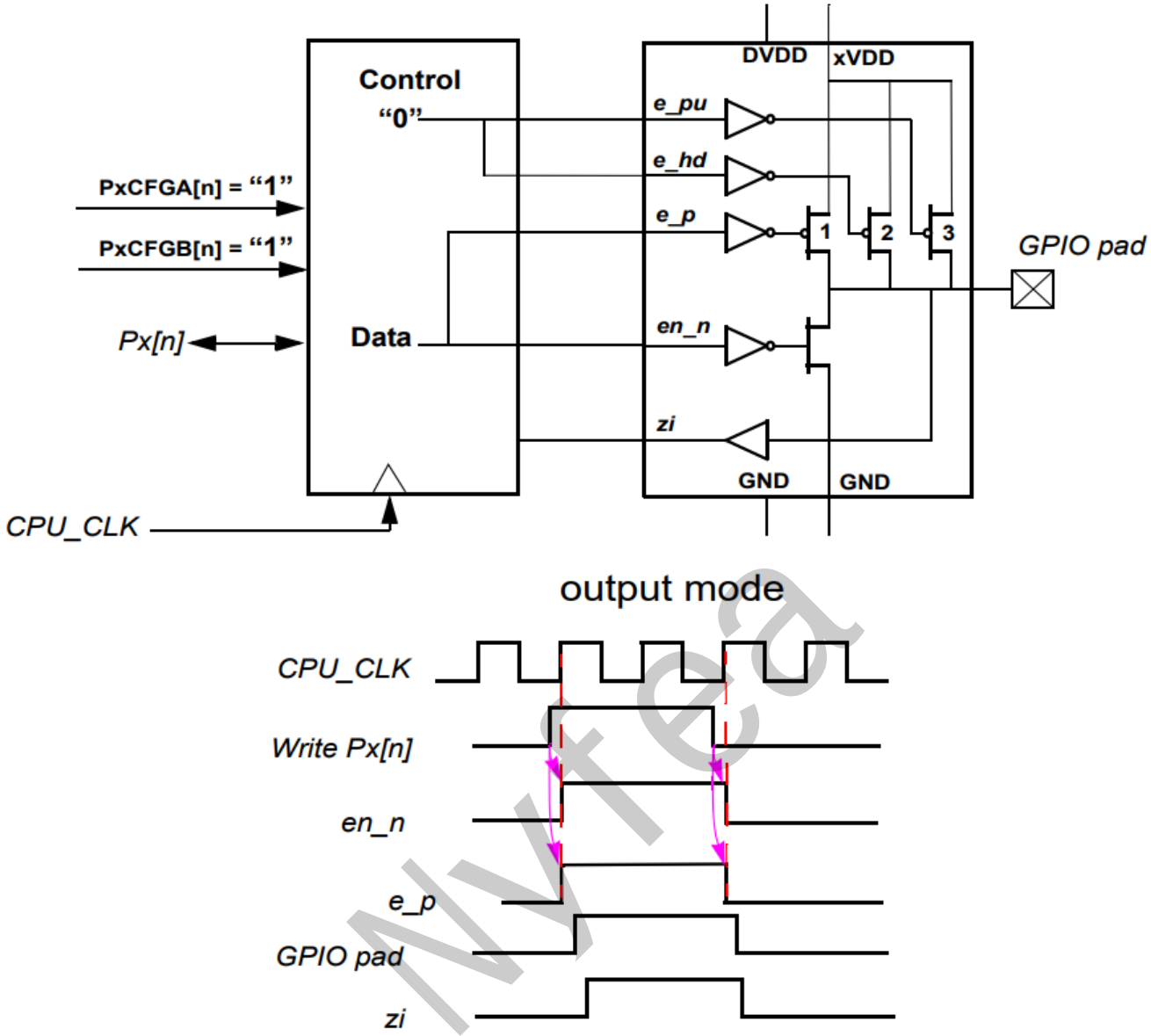


Fig 9. Push-pull output

In push-pull output, the output pin drives a strong 0 or a 1 continuously. The device can read back the pin output value.

8.2.2 GPIO registers description

8.2.2.1 P7CFGA register

Table 60. P7CFGA register (SFR: address F4h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	P7CFGA[2]	P7CFGA[1]	P7CFGA[0]
Reset	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R/W	R/W	R/W

Table 61. Description of P7CFGA bits

Bit	Symbol	Description
7 to 3	-	Reserved.

Bit	Symbol	Description
2	P7CFGA[2]	Out of SPI mode, and in conjunction with P7CFGB[2], it configures the functional mode of the P72 pin.
1	P7CFGA[1]	Out of SPI mode, and in conjunction with P7CFGB[1], it configures the functional mode of the P71 pin.
0	P7CFGA[0]	In conjunction with P7CFGB[0], it configures the functional mode of P70_IRQ pin.

Remark: When in Hard power down mode, the P72 to P70_IRQ pins are forced in quasi bidirectional mode. Referring to Figure 7, en_n = e_pu = "1", e_p = "0". And e_hd = "1" if P7x pin value is "1" and e_hd = "0" if P7x pin value is "0".

8.2.2.2 P7CFGB register

Table 62. P7CFGB register (SFR: address F5h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	P7CFGB[2]	P7CFGB[1]	P7CFGB[0]
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 63. Description of P7CFGB bits

Bit	Symbol	Description
7 to 3	-	Reserved.
2	P7CFGB[2]	Out of SPI mode, and in conjunction with P7CFGA[2], it configures the functional mode of the P72 pin.
1	P7CFGB[1]	Out of SPI mode, and in conjunction with P7CFGA[1], it configures the functional mode of the P71 pin.
0	P7CFGB[0]	In conjunction with P7CFGA[0], it configures the functional mode of P70_IRQ pin.

Remark: When in Hard power down mode, the P72 to P70_IRQ pins are forced in quasi bidirectional mode. Referring to Figure 7, en_n = e_pu = "1", e_p = "0". And e_hd = "1" if P7x pin value is "1" and e_hd = "0" if P7x pin value is "0".

8.2.2.3 P7 register

Table 64. P7 register (SFR: address F7h) bit allocation

Bit	7	6	5	4	3 2	1	0
Symbol	-	-	-	-	- P7[2]	P7[1]	P7[0]
Reset	1	1	1	1	1 1	1	1
Access	R	R	R	R	R R/W	R/W	R/W

Table 65. Description of P7 bits

Bit	Symbol	Description
7 to 3	-	Reserved.
2	P7[2]	**Out of SPI mode**:Writing to P7[2] writes the corresponding value to the P72 pin in accordance with the configuration mode defined by P7CFGA[2] and P7CFGB[2]. Reading from P7[2] reads the logic state of P72 pin.
1	P7[1]	**Out of SPI mode**:Writing to P7[1] writes the corresponding value to the P71 pin in accordance with the configuration mode defined by P7CFGA[1] and P7CFGB[1].
		Reading from P7[1] reads the logic state of P71 pin.

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Bit	Symbol	Description
0	P7[0]	**Writing to P7[0] writes**the corresponding value to the P70_IRQ pin in accordance with the configuration mode defined by P7CFGA[0] and P7CFGB[0].
		Reading from P7[0] reads the logic state of P70_IRQ pin.

8.2.2.4 P3CFGA register

Table 66. P3CFGA register (SFR: address FCh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	P3CFGA[	P3CFGA[	P3CFGA[	P3CFGA[	P3CFGA[	P3CFGA[
			5]	4]	3]	2]	1]	0]
Reset	1	1	1	1	1	1	1	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 67. Description of P3CFGA bits

Bit	Symbol	Description
7 to 6		Reserved.
5	P3CFGA[5]	In conjunction with P3CFGB[5], it configures the functional mode of P35.
4	P3CFGA[4]	In conjunction with P3CFGB[4], it configures the functional mode of P34.
3	P3CFGA[3]	In conjunction with P3CFGB[3], it configures the functional mode of P33_INT1.
2	P3CFGA[2]	In conjunction with P3CFGB[2], it configures the functional mode of P32_INT0[1]
1	P3CFGA[1]	In conjunction with P3CFGB[1], it configures the functional mode of P31
0	P3CFGA[0]	In conjunction with P3CFGB[0], it configures the functional mode of P30
[1] W is f	hen CPU_PD is orced to 1	set to 1(seeTable7onpage16), for P32_INT0 and referring toSection8.2.1 ,e_hd.

Remark: When in Hard power down mode, the P35 to P30 pins are forced in quasi bidirectional mode. Referring to Figure 7, en_n = e_pu = “1”, e_p = “0”. And e_hd = “1” if P3x pin value is “1” and e_hd = “0” if P3x pin value is “0”.

8.2.2.5 P3CFGB register

Table 68. P3CFGB register (SFR: address FDh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	P3CFGB[	P3CFGB[	P3CFGB[	P3CFGB[	P3CFGB[	P3CFGB[
			5]	4]	3]	2]	1]	0]
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 69. Description of P3CFGB bits

Bit	Symbol	Description
7 to 6		Reserved.
5	P3CFGB[5]	In conjunction with P3CFGA[5], it configures the functional mode of P35.
4	P3CFGB[4]	In conjunction with P3CFGA[4], it configures the functional mode of P34.
3	P3CFGB[3]	In conjunction with P3CFGA[3], it configures the functional mode of P33_INT1.
2	P3CFGB[2]	In conjunction with P3CFGA[2], it configures the functional mode of P32_INT0. [1]
1	P3CFGB[1]	In conjunction with P3CFGA[1], it configures the functional mode of P31.
0	P3CFGB[0]	In conjunction with P3CFGA[0], it configures the functional mode of P30.

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[1] When CPU_PD is set to 1(see Table 7), for P32_INT0 and referring to Section 8.2.1, e_hd is forced to 1.

Remark: When in Hard power down mode, the P35 to P30 pins are forced in quasi bidirectional mode. Referring to Figure 7, en_n = e_pu = "1", e_p = "0". And e_hd = "1" if P3x pin value is "1" and e_hd = "0" if P3x pin value is "0".

8.2.2.6 P3 register

Table 70. P3 register (SFR: address B0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	P3[5]	P3[4]	P3[3]	P3[2]	P3[1]	P3[0]
Reset	1	1	1	1	1	1	1	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 71. Description of P3 bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5	P3[5]	Writing to P3[5] writes the corresponding value to P35 pin in accordance with the configuration mode defined by P3CFGA[5] and P3CFGB[5]. Reading from P3[5] reads the logic state of P35 pin.
4	P3[4]	When P34 alternate function SIC_CLK is not used, writing to P3[4] writes the corresponding value to P34 pin in accordance with the configuration mode defined by P3CFGA[4] and P3CFGB[4]. Reading from P3[4] reads the logic state of P34 pin.
3	P3[3]	Writing to P3[3] writes the corresponding value to P33_INT1 pin according to the configuration mode defined by P3CFGA[3] and P3CFGB[3]. Reading from P3[3] reads the logic state of P33_INT1 pin.
2	P3[2]	Writing to P3[2] writes the corresponding value to P32_INT0 pin according to the configuration mode defined by P3CFGA[2] and P3CFGB[2]. Reading from P3[2] reads the logic state of P32_INT0 pin.
1	P3[1]	When the P31 pin alternate function UART_TX is not used, writing to P3[1] writes the corresponding value to P31 pin in accordance with the configuration mode defined by P3CFGA[1] and P3CFGB[1]. Reading from P3[1] reads the logic state of P31 pin.
0	P3[0]	When the P30 pin alternate function UART_RX is not used, writing to P3[0] writes the corresponding value to P30 pin in accordance with the configuration mode defined by P3CFGA[0] and P3CFGB[0]. Reading from P3[0] reads the logic state of P30 pin.

8.3 Host interfaces

NF532 must be able to support various kind of interfaces to communicate with the HOST. All the interfaces that have to be supported are exclusive.

- SPI interface
- I^2C interface: Standard and Fast modes
- High Speed UART (HSU): supporting specific high baud rates

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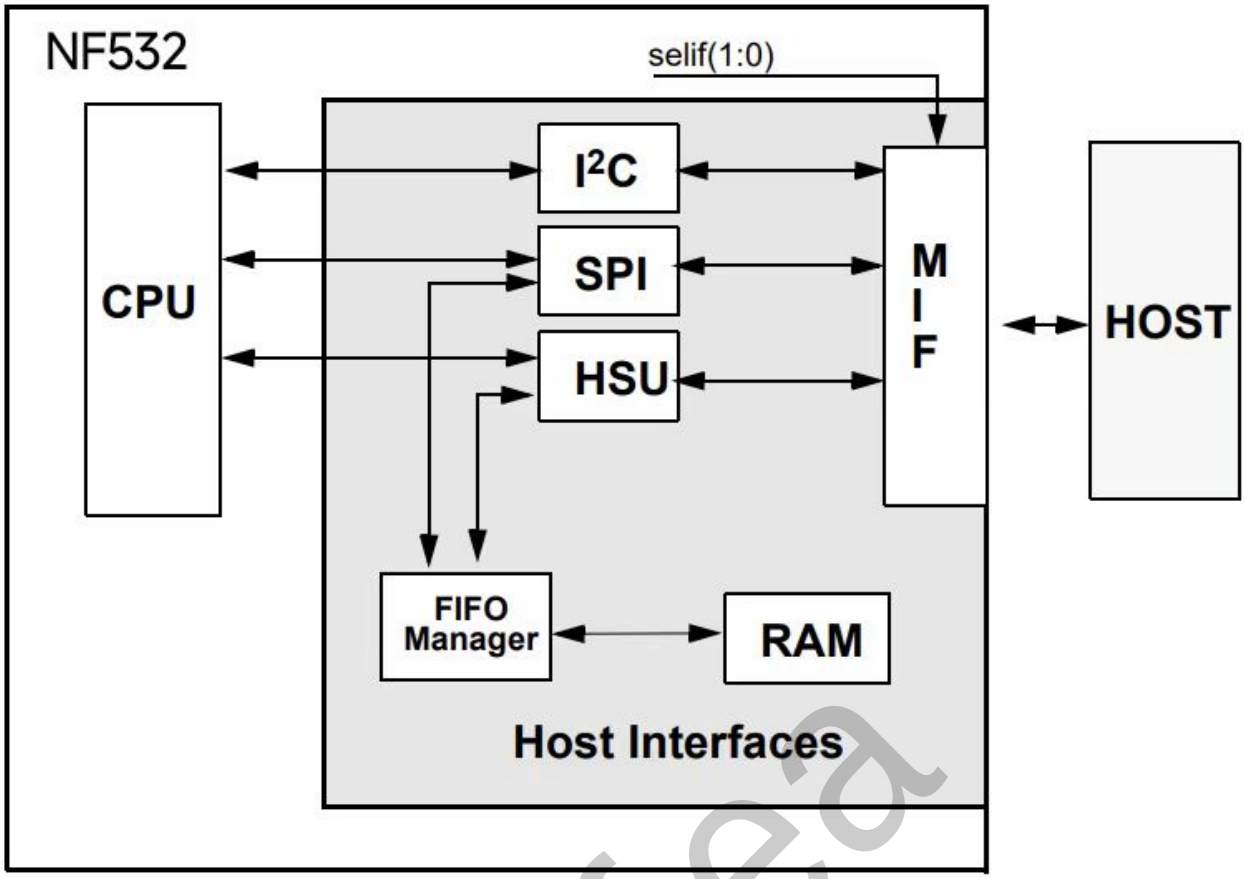


Fig 10. Host interface block diagram

8.3.1 Multi-InterFace (MIF) description

The Multi-InterFace (MIF) manages the configuration of the host interface pins, supplied by PVDD, in accordance with the selected links with the bits selif[1:0] of register Config_I0_I1 (see Table 74):

The firmware must copy the setting of the pads I0 and I1 to respectively selif[0] and selif[1].

Table 72. HOST interface selection

Selif [1:0]	00	01	10	11
Host interface selected	HSU	SPI	I²C	Reserved
Pin number				
27	HSU_RX	NSS	P50_SCL	-
28	HSU_TX	MOSI	SDA	-
29	P71	MISO	P71	-
30	P72	SCK	P72	-

8.3.1.1 MIF register

The Config I0_I1 register serves to choose the host interface. It manages also the polarity of P33_INT1.

Table 73. Config I0_I1 register (address 6103h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	int1_pol	-	pad_I1	-	pad_I0	enselif	Selif	[1:0]
Reset	0	0	X	0	X	0	0	0
Access	R/W	R	R/W	R	R/W	R/W	R/W	R/W

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Table 74. Description of Config IO_I1 bits

Bit	Symbol	Description
7	int1_pol	When set to 1, the value of the P33_INT1 pin is inverted.
6	-	Reserved.
5	pad_I1	When read, this bit gives the logic state of the I1 pin.
4	-	Reserved.
3	pad_I0	When read, this bit gives the logic state of the I0 pin.
2	enselif	When set to 1, the selif bits are valid and the selected MIF interface may drive the pins. Firmware must copy I0 and I1 to selif[0] and selif[1], respectively. When cleared to 0, the MIF cannot drive the I/O lines.
1:0	Selif[1:0]	Used by firmware to select the host-interface communication link; see Table 72.

8.3.1.2Configuration modes of the host interface pins

In I^2C mode, P50_SCL and SDA are configured in open-drain mode.

In HSU mode, HSU_RX is an input and HSU_TX uses push-pull output mode.

In SPI mode, NSS, MOSI and SCK are inputs; MISO uses push-pull output mode.

8.3.2 I^2C interface

It is recommended that the design refer the I^2 C standard for more information.

The I^2 C interface implements a Master/Slave I^2 C bus interface with integrated shift register, shift timing generation and Slave address recognition. I^2 C Standard mode (100 kHz SCLK) and Fast mode (400 kHz SCLK) are supported.

General Call +W is supported, not hardware General Call (GC +R).

The mains characteristics of the I^2 C module are:

- Support Master/Slave I^2 C bus
- Standard and Fast mode supported
- Wake-up of the NF532 on its own address
- Wake-up on General Call +W (GC +W)

The I^2C module is controlled through five registers:

Table 75. I^2C register list

Name	Size [bytes]	Address	Description	Access
I^2CCON	1	D8h (SFR)	Control register	R/W
I^2CSTA	1	D9h (SFR)	Status register	R/W
I^2CDAT	1	DAh (SFR)	Data register	R/W
I^2CADR	1	DBh (SFR)	Slave Address register	R/W
$i^2c\_wu\_control$	1	610Ah	Control register for the I^2C wake-up conditions	R/W

8.3.2.1 I^2C functional description

Four operating roles are supported by the I^2C interface:

- Master Transmitter
- Master Receiver
- Slave Receiver

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- Slave Transmitter

I²C transactions fall into two basic transfer directions:

- Data transfer from a Master transmitter to a Slave receiver. The first byte sent by the Master is the Slave address. Next follows multiple data bytes. The Slave returns an acknowledge bit after each received byte.
- Data transfer from a Slave transmitter to a Master receiver. The first byte (the Slave address) is sent by the Master. The Slave then returns an acknowledge bit. Next follows the data bytes sent by the Slave to the Master. The Master returns an acknowledge bit after each received byte except the last byte. At the end of the last received byte, a "not acknowledge" is returned.

For a given transaction environment, the I²C block can take either the Master or Slave role.

A typical NF532 system assigns the Master role to the host and operates the NF532 I²C interface as a Slave.

In the Slave mode, the I² C interface hardware looks for its own Slave address and the General Call address. If one of these addresses is detected, an interrupt is requested. When the NF532 microcontroller wishes to become the bus Master, the hardware waits until the bus is free before entering Master mode so that a possible Slave action is not interrupted. If bus arbitration is lost in the Master mode, the I² C interface switches to the Slave mode immediately and can detect its own Slave address in the same serial transaction.

8.3.2.2 Master transmitter mode

When operating as Master, the I²C block drives the serial clock and creates the START and STOP bus conditions. A Master transfer terminates either with STOP or with a repeated START. Because a repeated START immediately begins another transfer, bus ownership is retained.

I² C data are output through SDA while P50_SCL outputs the serial clock. The opening byte carries the 7-bit Slave address together with the transfer-direction bit. For this case the direction bit (R/W) is a 0 (W). I²C payload data are transferred one byte at a time. Each sent byte is followed by reception of an acknowledge bit. START and STOP conditions delimit the serial transaction.

In the Master transmitter mode, multiple data bytes may be transmitted to the Slave receiver. Before the Master transmitter mode may be entered, I² CCON must be initialized with the ENS1 bit set to 1 and the STA, STO and SI bits cleared to 0. ENS1 must be set to 1 to enable the I² C interface. If the AA bit is cleared to 0, the I² C interface will not acknowledge its own Slave address or the General Call address if they are present on the bus. This will prevent the I² C interface from entering a Slave mode.

The Master transmitter mode may now be entered by setting the STA bit. The I² C interface logic will then test the I² C bus and produce a start condition as soon as the bus becomes free. When a START condition is sent, the serial interrupt flag (SI) is set to 1, and the status code in the status register (I² CSTA) is 08h. This status code must be used to select the appropriate interrupt handler that writes I² CDAT with the Slave address and the direction bit (SLA+W). The SI bit in I² CCON must then be cleared to 0 before the serial transaction can continue.

When the Slave address and the direction bit have been transmitted and an acknowledgement bit has been accepted, the serial interrupt flag (SI) is set to 1 again, and multiple status codes may be reported in I²CSTA. The required firmware response for any of the status codes is detailed in Table 80. After a repeated start condition (state 10h), the I² C interface may switch to the Master receiver mode by loading I² CDAT with SLA+R.

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8.3.2.3 Master receiver mode

When operating as Master, the I²C block drives the serial clock and creates the START and STOP bus conditions. A Master transfer terminates either with STOP or with a repeated START. Because a repeated START immediately begins another transfer, bus ownership is retained.

The first byte transmitted holds the Slave address of the transmitting device (7-bit SLA) and the direction bit. For this case the direction bit (R/W) is 1 (R). I² C data are accepted via SDA while P50_SCL outputs the serial clock. I² C data are accepted 8 bits at a time. After each byte is accepted, an acknowledge bit is sent. START and STOP conditions are output to show the beginning and end of a serial transaction.

In the Master receiver mode, multiple data bytes are accepted from a Slave transmitter. Initialization follows the same sequence used for Master-transmitter operation. When the START condition has been transmitted, the interrupt handler must load I² CDAT with the 7-bit Slave address and the direction bit (SLA+R). The SI bit in I² CCON must then be cleared to 0 before the serial transaction can continue.

When the Slave address and the direction bit have been transmitted and an acknowledgement bit has been accepted, the serial interrupt flag (SI) is set to 1 again, and multiple status codes may occur in I²CSTA. The required firmware response for each of the status codes is detailed in Table 81. After a repeated start condition (state 10h), the I² C interface may switch to the Master transmitter mode by loading I² CDAT with SLA+W.

8.3.2.4 Slave receiver mode

I² C data and the serial clock are accepted through SDA and P50_SCL. After each byte is accepted, an acknowledge bit is sent. START and STOP are detected as the transaction boundaries. Hardware carries out address matching after the Slave address and direction bit have been accepted.

In the Slave receiver mode, multiple data bytes are accepted from a Master transmitter. To initiate the Slave receiver mode, I² CADR must be written with the 7-bit Slave address to which the I² C interface will respond when addressed by a Master. Also the least significant bit of I² CADR should be set to 1 if the interface should respond to the General Call address (00h). The control register, I² CCON, should be initialized with ENS1 and AA set to 1 and STA, STO, and SI cleared to 0 to enter the Slave receiver mode. Setting the AA bit will enable the logic to acknowledge its own Slave address or the General Call address and ENS1 will enable the interface.

When I² CADR and I² CCON have been initialized, the I² C interface waits until it is addressed by its own Slave address followed by the direction bit which must be '0' (W) for the I² C interface to operate in the Slave receiver mode. After its own Slave address and the W bit have been accepted, the serial interrupt flag (SI) is set to 1 and a valid status code may be read from I² CDAT. This status code should be used to select the appropriate interrupt handler, and the appropriate action to be taken for each of the status codes is detailed in Table 82. The Slave receiver mode may also be entered if arbitration is lost while the I² C interface is in the Master mode.

If the AA bit is cleared to 0 during a transfer, the I² C interface will return a not acknowledge (1) to SDA after the next incoming data byte. While AA is cleared to 0, the I² C interface does not respond to its own Slave address or a General Call address. Nevertheless, the I² C bus is still monitored and address recognition may be resumed at any time by setting AA. Consequently, the AA bit may be used to temporarily isolate the I² C interface from the I² C bus.

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8.3.2.5 Slave transmitter mode

The first byte follows the same handling used in Slave-receiver operation. Nevertheless, in this mode, the direction bit will show that the transfer direction is reversed. I^2C data are sent via SDA while the serial clock is input through P50_SCL. START and STOP are detected as the transaction boundaries.

In the Slave transmitter mode, multiple data bytes are sent to a Master receiver. Data transfer is initialized as in the Slave receiver mode. When I^2C CADR and I^2C CCON have been initialized, the I^2C interface waits until it is addressed by its own Slave address followed by the direction bit which must be '1' (R) for the I^2C interface to operate in the Slave transmitter mode. After its own Slave address and the R bit have been accepted, the serial interrupt flag (SI) is set to 1 and a valid status code may be read from I^2C CSTA. This status code serves to select the appropriate interrupt handler, and the appropriate action to be taken for each of these status codes is detailed in Table 83. The Slave transmitter mode may also be entered if arbitration is lost while the I^2C interface is in the Master mode.

If the AA bit is cleared to 0 during a transfer, the I^2C interface will send the last byte of the transfer and enter state C0h or C8h. the I^2C interface is switched to the unaddressed Slave mode and will ignore the Master receiver if it continues the transfer. Thus the Master receiver receives all '1' s as I^2C data. While AA is cleared to 0, the I^2C interface does not respond to its own Slave address or a General Call address. Nevertheless, the I^2C bus is still monitored, and address recognition may be resumed at any time by setting AA. Consequently, the AA bit may be used to temporarily isolate the I^2C interface from the I^2C bus.

8.3.2.6 I^2C wake-up mode

The dedicated I^2C wake-up block is applicable only while the interface is configured for Slave operation.

This wake-up circuitry is separate from the main I^2C peripheral and is provided specifically to bring NF532 out of Soft-Power-Down.

Prior to Soft-Power-Down entry, firmware shall complete the next setup:

- Enable the block and choose the wake-up conditions (see Table 90).
- Enable the I^2C wake-up event in the PCR (see Table 143)

While NF532 is in Soft-Power-Down, the wake-up block monitors I^2C bus activity. If it recognizes its own address and the command type is valid (read only, write only, or both depending on settings in register i^2c_wu_control, see Table 90), the wake-up block will produce an acknowledge, stretch P50_SCL, configure the I^2C interface in Slave Transmitter or Slave Receiver mode depending on the command. Finally, i^2c_on is set to 1, which initiates the wake-up sequence (see Section 8.5 "Power clock and reset controller").

When the microcontroller has been woken up, the firmware must identify the wake-up source and must disable the wake-up block (see Table 90) to use I^2C. It is now the I^2C peripheral which stretches P50_SCL.

To enable wake-up on GC +W, the LSB bit of I^2C CADR should be set to 1 (see Table 88). The wake-up block and the wake-up on a write command should be enabled before entering Soft-Power-Down mode. When the wake-up on GC +W condition is recognized, the behavior is the same as described above.

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8.3.2.7 I²CCON register

This 8-bit SFR is readable and writable by the CPU. Two bits are affected by the Serial IO (the I² C interface) hardware: the SI bit is set to 1 when a serial interrupt is requested, and the STO bit is cleared to 0 when a STOP condition is present on the I² C bus. The STO bit is also cleared to 0 when ENS1 = '0'.

Table 76. I²CCON register (SFR: address D8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CR[2]	ENS1	STA	STO	SI	AA	CR[	1:0]
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77. Description of I²CCON bits

Bit	Symbol	Description
7	CR[2]	**Selects the serial clock frequency in Master mode.** Together with CR[1:0], this bit determines the clock rate (serial clock frequency) when the I²C interface is in a Master mode. Special attention has to be made on the I²C bit frequency in case of dynamic switching of the CPU clock frequency.
6	ENS1	**Serial IO enable.** When ENS1 bit is to 0, SDA and P50_SCL are in high impedance. The logic state of SDA and P50_SCL is ignored, the I²C interface is in the "not addressed" Slave state, and the STO bit in I²CCON is forced to 0. No other bits are affected. When ENS1 is 1, the I²C interface is enabled, assuming selif[1:0] bits are 10b (see Table 72). ENS1 should not be used to temporarily release the I²C interface from the I²C bus since, when ENS1 is cleared to 0, the I²C bus status is lost. The AA flag should be used instead.
5	STA	**START control.** When the STA bit is set to 1 to enter Master mode, the I²C interface hardware checks the status of the I²C bus and generates a START condition if the bus is free. If the bus is not free, then the I²C interface waits for a STOP condition (which will free the bus) and generates a START condition after a delay of a half clock period of the internal serial clock generator. If STA is set to 1, while the I²C interface is already in a Master mode and one or more bytes are transmitted or received, the I²C interface transmits a repeated START condition. STA may be set to 1 at any time. This includes the case when the I²C interface is the addressed Slave. When the STA bit is cleared to 0, no START condition or repeated START condition is generated.
4	STO	**STOP control.** When the STO bit is set to 1, while the I²C interface is in Master mode, a STOP condition is transmitted to the I²C bus. When the STOP condition is detected on the bus, the I²C interface hardware automatically sets STO to 0. In Slave mode, STO may be set to 1 to recover from an error condition. For this case, no STOP condition is transmitted to the I²C bus. However, the I²C interface hardware behaves as if a STOP condition has been received and switches to the defined "not addressed" Slave Receiver mode. If the STA and STO bits are both set to 1, the STOP condition is transmitted to the I²C bus if the I²C interface is in Master mode (in Slave mode, the I²C interface generates an internal STOP condition which is not transmitted). The I²C interface then transmits a START condition. When the STO bit is cleared to 0, no STOP condition is generated.
3	SI	**Serial interrupt flag.** When SI is set to 1, then if the serial interrupt from the I²C interface port is enabled, the CPU will receive an interrupt. SI is set by hardware when any one of 25 of the possible 26 states of the I²C interface are entered. The only state that does not cause SI to be set to 1 is state F8h, which indicates that no relevant state information is available. While SI is set by hardware to 1, P50_SCL is held in 0 when the SCL line is 0, and P50_SCL is held in high impedance when the SCL line is 1. SI must be cleared to 0 by firmware. When the SI flag is cleared to 0, no serial interrupt is requested, and there is no stretching of the SCL line via P50_SCL. The bit IE1_4 of register IE1 (see Table 13) has also to be set to 1 to enable the corresponding I²C interrupt to the CPU.

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Bit	Symbol	Description
2	AA	**Assert Acknowledge flag.** If AA is set to 1, an acknowledge (low level to SDA) is returned during the acknowledge clock pulse on the P50_SCL line when: • The "own Slave address" has been received. • The general call address has been received while the general call bit (GC) in I²CADR is set. • A data byte has been received while the I²C interface is in Master Receiver mode. • A data byte has been received while the I²C interface is in the addressed Slave Receiver mode. When the I²C interface is in the addressed Slave Transmitter mode, state C8h will be entered after the last serial bit is transmitted. When SI is cleared to 0, the I²C interface leaves state C8h, enters the Not-addressed Slave Receiver mode, and the SDA line remains at 1. In state C8h, AA may be set to 1 again for future address recognition. When the I²C interface is in the Not-addressed Slave mode, its own Slave address and the general call address are ignored. Consequently, no acknowledge is returned, and a serial interrupt is not requested. Thus, the I²C interface may be temporarily released from the I²C bus while the bus status is monitored. While the I²C interface is released from the bus, START and STOP conditions are detected, and I²C data are shifted in. Address recognition may be resumed at any time by setting AA to 1. If AA is set to 1 when the I²C own Slave address or the general call address has been partly received, the address is recognized at the end of the byte transmission.
1 to 0	CR[1:0]	**Selects the serial clock frequency in Master mode.** See the selection table below.

CR2	CR1	CR0	CPU_CLK division factor	I²C bit frequency
0	0	0	10	CPU_CLK/10
0	0	1	20	CPU_CLK/20
0	1	0	30	CPU_CLK/30
0	1	1	40	CPU_CLK/40
1	0	0	80	CPU_CLK/80
1	0	1	120	CPU_CLK/120
1	1	0	160	CPU_CLK/160
1	1	1	(256-T1 reload value)*12 24...3072	CPU_CLK/3072...CPU_CLK/24

8.3.2.8 I²CSTA register

I² CSTA is an 8-bit read-only special function register. The three least significant bits are always at 0. The five most significant bits hold the status code. There are 26 possible status codes. When I² CSTA holds F8h, no relevant state information is accessible and no serial interrupt is requested. Reset initializes I² CSTA to F8h. All other I² CSTA values correspond to defined I² C interface states. When each of these states is entered, a serial interrupt is requested (SI = '1'), this can happen in any CPU cycle, and a valid status code is present in I² CSTA. This status code will stay present in I² CSTA until SI is cleared to 0 by firmware.

Note that I² CSTA changes one CPU_CLK clock cycle after SI changes, so the new status may be visible in the same machine cycle SI changes or possibly (in one out of six CPU states) the machine cycle after that. This should not be a problem since you should not read I² CSTA prior to either polling SI or entry of the interrupt handler (which in itself takes multiple machine cycles).

Table 78. I²CSTA register (SFR: address D9h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				ST[7:0]				
Reset	1	1	1	1	1	0	0	0
Access	R	R	R	R	R	R	R	R

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Table 79. Description of I²CSTA bits

Bit	Symbol	Description
7 to 0	ST[7:0]	**Encoded status bit for the different functional mode.** Several Status codes are returned in a certain mode (Master Transmitter, Master Receiver, Slave Transmitter, Slave Receiver) plus some miscellaneous status codes that may be returned at any time.

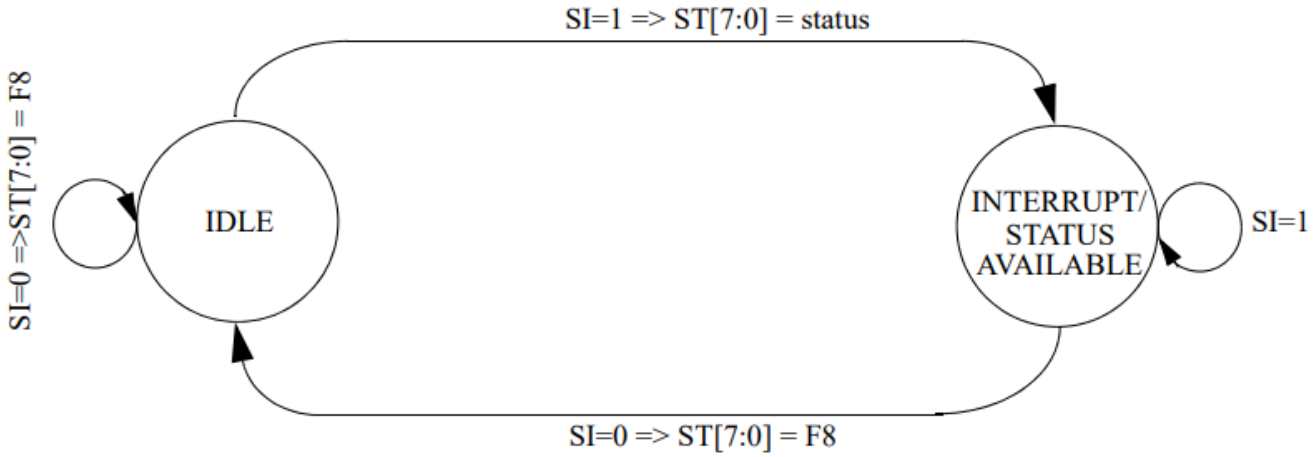


Fig 11. I²C state machine of status behavior

Table 80. I²C Master Transmitter Mode status code

Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
08h	A START condition has been transmitted	Load SLA+W	X	0	0	X	SLA+W is transmitted ACK is received
10h	A repeated START condition has been transmitted	Load SLA+W	X	0	0	X	As above
		Load SLA+R	X	0	0	X	SLA+W is transmitted; the I²C interface switches to MST/(TRX or REC) mode
18h	SLA+W has been transmitted; ACK has been received	Load data byte	0	0	0	X	Data byte is transmitted; ACK bit is received
		No I²CDAT action	1	0	0	X	Repeated START is transmitted
		No I²CDAT action	0	1	0	X	STOP condition is transmitted; STO flag is cleared to 0
		No I²CDAT action	1	1	0	X	STOP condition followed by a START condition is transmitted; STO flag is cleared to 0
20h	SLA+W has been transmitted; NOT ACK has been received	Load data byte	0	0	0	X	Data byte is transmitted; ACK bit is received
		No I²CDAT action	1	0	0	X	Repeated START is transmitted
		No I²CDAT action	0	1	0	X	STOP condition is transmitted; STO flag is cleared to 0
		No I²CDAT action	1	1	0	X	STOP condition followed by a START condition is transmitted; STO flag is cleared to 0
28h	Write data byte in I²CDAT has been transmitted; ACK has been received	Load data byte	0	0	0	X	Data byte is transmitted; ACK bit is received
		No I²CDAT action	1	0	0	X	Repeated START is transmitted
		No I²CDAT action	0	1	0	X	STOP condition is transmitted; STO flag is cleared to 0
		No I²CDAT action	1	1	0	X	STOP condition followed by a START condition is transmitted; STO flag is cleared to 0

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Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
30h	Write data byte in I²CDAT has been transmitted; NOT ACK has been received	Load data byte	0	0	0	X	Data byte is transmitted; ACK bit is received
		No I²CDAT action	1	0	0	X	Repeated START is transmitted
		No I²CDAT action	0	1	0	X	STOP condition is transmitted; STO flag is cleared to 0
		No I²CDAT action	1	1	0	X	STOP condition followed by a START condition is transmitted; STO flag is cleared to 0
38h	Arbitration lost in SLA+R/W or Data bytes	No I²CDAT action	0	0	0	X	I²C bus will be released; a Slave mode will be entered
		No I²CDAT action	1	0	0	X	A START condition is transmitted when the bus becomes free

Table 81. I²C Master Receiver Mode status codes

Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
08h	A START condition has been transmitted	Load SLA+W	X	0	0	X	SLA+W is transmitted, ACK is received
10h	A repeated START condition has been transmitted	Load SLA+W	X	0	0	X	As above
		Load SLA+R	X	0	0	X	SLA+W is transmitted; the I²C interface switches to MST/(TRX or REC) mode
38h	Arbitration lost in SLA+R/W or Data bytes	No I²CDAT action	0	0	0	X	I²C bus will be released; a Slave mode will be entered
		No I²CDAT action	1	0	0	X	A START condition is transmitted when the bus becomes free
40h	SLA+R has been transmitted; ACK has been received	No I²CDAT action	0	0	0	0	Data byte is received; NOT ACK bit is returned
		No I²CDAT action	0	0	0	1	Data byte is received; ACK bit is returned
48h	SLA+R has been transmitted; NOT ACK has been received	No I²CDAT action	1	0	0	X	Repeated START condition is transmitted
		No I²CDAT action	0	1	0	X	STOP condition is transmitted; STO flag is cleared to 0
		No I²CDAT action	1	1	0	X	STOP condition followed by a START condition is transmitted; STO flag is cleared to 0
50h	Read data byte has been received; ACK has been returned	Read data byte or	0	0	0	0	Data byte is received; NOT ACK bit is returned
		Read data byte	0	0	0	1	Data byte is received; ACK bit is returned
58h	Read data byte has been received; NOT ACK has been returned	Read data byte	1	0	0	X	Repeated START condition is transmitted
		Read data byte	0	1	0	X	STOP condition is transmitted; STO flag is cleared to 0
		Read data byte	1	1	0	X	STOP condition followed by a START condition is transmitted; STO flag is cleared to 0

Table 82. I²C Slave Receiver Mode status codes

Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
60h	Own SLA+W has been received; ACK has been returned	No I²CDAT action	X	0	0	0	Data byte is received and NOT ACK is returned
		No I²CDAT action	X	0	0	1	Data byte is received and ACK is returned

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Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
68h	Arbitration lost in SLA+R/W as Master; Own SLA+W has been received, ACK returned	No I²CDAT action	X	0	0	0	Data byte is received and NOT ACK is returned
		No I²CDAT action	X	0	0	1	Data byte is received and ACK is returned
70h	General call address (00h) has been received; ACK has been returned	No I²CDAT action	X	0	0	0	Data byte is received and NOT ACK is returned
		No I²CDAT action	X	0	0	1	Data byte is received and ACK is returned
78h	Arbitration lost in SLA+R/W as Master; General call address has been received, ACK has been returned	No I²CDAT action	X	0	0	0	Data byte is received and NOT ACK is returned
		No I²CDAT action	X	0	0	1	Data byte is received and ACK is returned
80h	Previously addressed with own SLA; Write data byte has been received; ACK has been returned	Read data byte	X	0	0	0	Data byte is received and NOT ACK is returned
		Read data byte	X	0	0	1	Data byte is received and ACK is returned
90h	Previously addressed with General Call; Write data byte has been received; ACK has been returned	Read data byte	X	0	0	0	Data byte is received and NOT ACK is returned
		Read data byte	X	0	0	1	Data byte is received and ACK is returned
88h	Previously addressed with own SLA; Write data byte has been received; NOT ACK has been returned	Read data byte	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		Read data byte	0	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition is transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1. A START condition is transmitted when the bus becomes free
98h	Previously addressed with General Call; Write data byte has been received; NOT ACK has been returned	Read data byte	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		Read data byte	0	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition is transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1. A START condition is transmitted when the bus becomes free
A0h	A STOP condition or repeated START condition has been received while still addressed as SLV/(REC or TRX)	Read data byte	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address

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Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
		Read data byte	0	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode; No recognition of own SLA or General call address. A START condition is transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1. A START condition is transmitted when the bus becomes free

Table 83. I²C Slave Transmitter Mode status codes

Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
A8h	Own SLA+R has been received; ACK has been returned	Load data byte	X	0	0	0	Last data byte is transmitted and ACK bit is received
		Load data byte	X	0	0	1	Data byte is transmitted; ACK is received
B0h	Arbitration lost in SLA+R/W as Master; Own SLA+R has been received. ACK has been returned	Load data byte	X	0	0	0	Last data byte is transmitted and ACK bit is received
		Load data byte	X	0	0	1	Data byte is transmitted; ACK is received
B8h	Read data byte in I²CDAT has been transmitted; ACK has been received	Load data byte	X	0	0	0	Last data byte is transmitted and ACK bit is received
		Load data byte	X	0	0	1	Data byte is transmitted; ACK is received
C0h	Read data byte in I²CDAT has been transmitted; NOT ACK has been received	No I²CDAT action	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		No I²CDAT action	0	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1.
		No I²CDAT action	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition is transmitted when the bus becomes free
		No I²CDAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1. A START condition is transmitted when the bus becomes free
C8h	Last read data byte in I²CDAT has been transmitted (AA is cleared to 0); ACK has been received	No I²CDAT action	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		No I²CDAT action	0	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1.
		No I²CDAT action	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition is transmitted when the bus becomes free
		No I²CDAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA is recognized; General call address is recognized if I²CADR[0] is set to 1. A START condition is transmitted when the bus becomes free

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Table 84. I²C Miscellaneous status codes

Status Code ST[7:0]	Status of the I²C Bus and the I²C interface Hardware	Application firmware Response To/from I²CDAT	STA	STO	SI	AA	Next Action Taken By the I²C interface Hardware
00h	Bus error	No I²CDAT action	X	1	0	X	Hardware will enter the "not addressed" Slave mode
F8h	No information available	No I²CDAT action	--	--	--	--	--

8.3.2.9 I²CDAT register

I² CDAT holds a byte of I² C data to be transmitted or a byte which has just been received. The CPU has read/write access to this 8-bit SFR while it is not in the process of shifting a byte. This occurs when the I² C interface is in a defined state and the serial interrupt flag SI is set to 1. Data in I² CDAT stays stable as long as SI is set to 1. The first bit to be transmitted is the MSB (bit 7), and, after a byte has been accepted, the first bit of incoming data is located at the MSB of I² CDAT. While data is being shifted out, data on the bus is at the same time being shifted in; I² CDAT always holds the last data byte present on the bus. Thus, in the event of lost arbitration, the transition from Master Transmitter to Slave Receiver is made with the correct data in I² CDAT.

Table 85. I²CDAT register (SFR: address DAh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				I²CD	AT[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 86. Description of I²CDAT bits

Bit	Symbol	Description
7 to 0	I²CDAT[7:0]	**I²C data.** Eight bits to be transmitted or just received. A 1 in I²CDAT corresponds to a 1 on the I²C bus, and a 0
		corresponds to a 0 on the bus. I²C data shift through I²CDAT from right to left.

I² CDAT[7:0] and the ACK flag form a 9-bit shift register which shifts in or shifts out an 8-bit byte, followed by an acknowledge bit. The ACK flag is controlled by the I² C interface hardware and cannot be accessed by the CPU. I² C data are shifted through the ACK flag into I² CDAT on the rising edges of clock pulses on P50_SCL. When a byte has been shifted into I² CDAT, the I² C data are accessible in I² CDAT, and the acknowledge bit is returned by the control logic during the ninth clock pulse. I² C data are shifted out from I² CDAT via a buffer on the falling edges of clock pulses on P50_SCL.

When the CPU writes to I² CDAT, the buffer is written with the contents of I² CDAT[7] which is the first bit to be transmitted to the SDA line. After nine serial clock pulses, the eight bits in I² CDAT will have been transmitted to the SDA line, and the acknowledge bit is present in ACK. Note that the eight transmitted bits are shifted back into I² CDAT.

8.3.2.10 I²CADR register

This 8-bit SFR is readable and writable by the CPU. I² CADR is not affected by the I² C interface hardware. The contents of this register is irrelevant when the I² C interface is in a Master mode. In the Slave modes, the seven most significant bits must be written with the microcontroller's own Slave address, and, if the least significant bit is set to 1, the General Call address (00h) is recognized; otherwise it has no effect.

Table 87. I²CADR register (SFR: address DBh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				SA[6:0]				GC

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Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 88. Description of I²CADR bits

Bit	Symbol	Description
7 to 1	SA[6:0]	**Slave address.** These bits correspond to the 7-bit Slave address which is recognized on the incoming data stream from the I²C bus. When the Slave address is detected and the interface is enabled, a serial interrupt SI is generated to the CPU.
0	GC	**General call.** When this bit is set to 1, will cause the I²C logic to watch for the general call address to be transmitted on the I²C bus. If a general call address is detected and this bit is set to 1, SI is set to 1.

8.3.2.11 I²C_wu_control register

The wake-up block has to be enabled before the device enters Soft-Power-Down mode. The choice of the wake-up conditions is made within the register I² C_wu_control. Read and Write conditions may be set together.

Table 89. I²C_wu_control register (address 610Ah) bit allocation

Bit	7	6	5	4	3 2	1	0
Symbol	-	-	-	-	- i²c_wu_en_wr	i²c_wu_en_rd	i²c_wu_en
Reset	0	0	0	0	0 0	0	0
Access	R	R	R	R	R R/W	R/W	R/W

Table 90. Description of I²C_wu_control bits

Bit	Symbol	Description
7 to 3	-	Reserved.
2	i²c_wu_en_wr	When this bit is set to 1, the wake-up is valid for write commands
1	i²c_wu_en_rd	When this bit is set to 1, the wake-up is valid for read commands
0	i²c_wu_en	When this bit is set to 1, enable the I²C wake-up conditions.
		The bit i²c_wu_en of register PCR Wakeupen (see Table 144)has also to be set to 1 to enable the corresponding NF532 wake-up.

8.3.3 FIFO manager

This block is designed to manage a RAM as a FIFO to optimize the data exchange between the CPU and the HOST.

8.3.3.1 FIFO manager functional description

The RAM used for the FIFO is shared between the SPI and HSU interfaces. Indeed, these interfaces cannot be used at the same time. The selection of the interface used is done by firmware. The FIFO manager block is the common part between the SPI and the HSU interfaces. It is made up of a Data register, a Status register and also some registers to define the characteristics of the FIFO. These registers are addressed by the CPU as SFRs.

The RAM used as a FIFO is partitioned into two part: a receive part and a send part.

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This block also manages the possible conflicts existing around the FIFO between the CPU and the interfaces. Indeed, a request coming from the interface (TR_req or RCV_req) may be simultaneous with a request to access to the data register coming from the CPU.

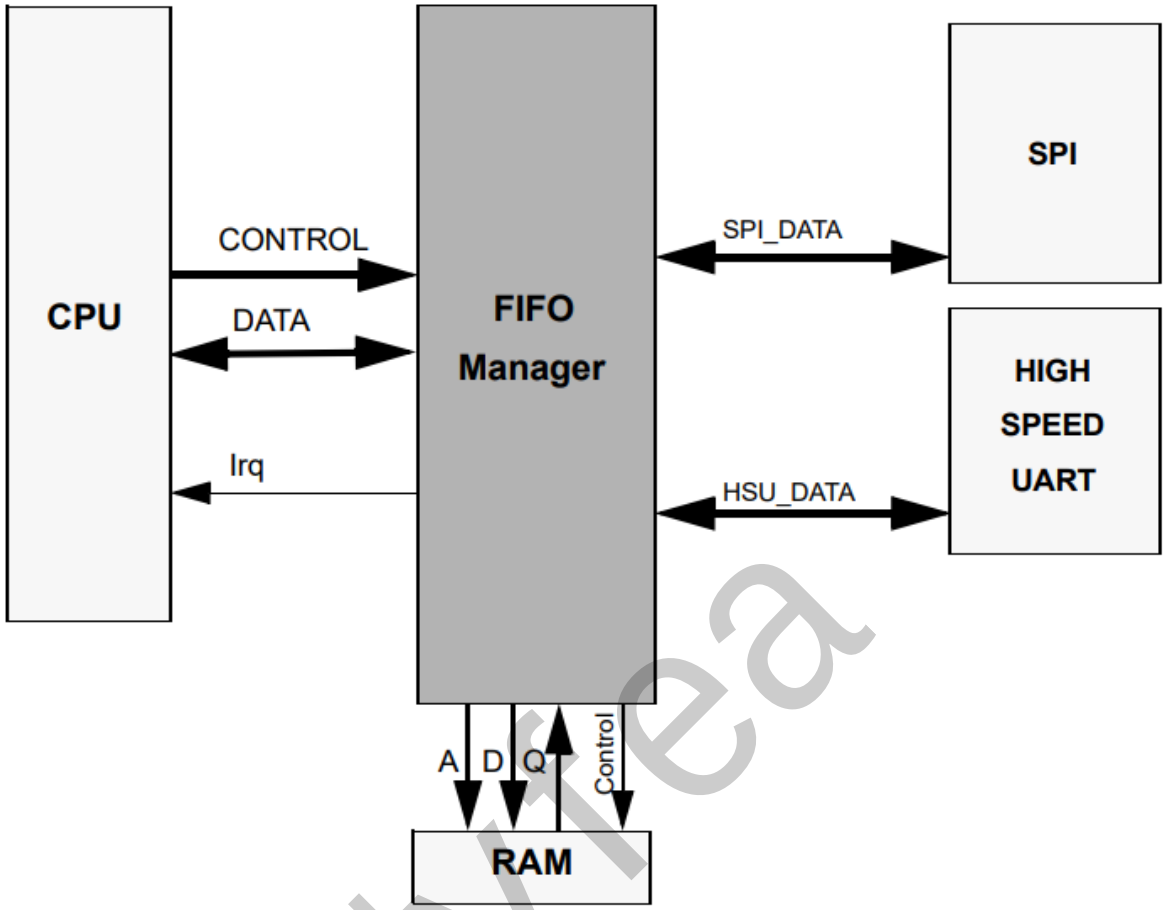


Fig 12. FIFO manager block diagram

9 SFR registers are needed to manage the FIFO manager.

Table 91. Fifo manager SFR register list

Name	Size [bytes]	SFR Address	Description	Access
RWL	1	9Ah	FIFO Receive Waterlevel: Controls the threshold of the FIFO in reception	R/W
TWL	1	9Bh	FIFO Transmit Waterlevel: Controls the threshold of the FIFO in transmission	R/W
FIFOFS	1	9Ch	FIFO Transmit FreeSpace: Status of the number of characters which can still be loaded in the FIFO	R/W
FIFOFF	1	9Dh	FIFO Receive Fullness: Status of the number of received characters in the FIFO	R/W
SFF	1	9Eh	Global Status/Error messages	R
FIT	1	9Fh	Interrupt Source	R/W
FITEN	1	A1h	Interrupt Enable and Reset FIFO	R
FDATA	1	A2h	Data reception/transmission buffer	R/W
FSIZE	1	A3h	Control the size of the FIFO in Reception	R/W

8.3.3.2 RWL register

This register specifies the warning level of the Receive FIFO for the CPU. It implies a FIFO buffer overflow.

Table 92. RWL register (SFR: address 9Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				RWaterl	evel[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 93. Description of RWL bits

Bit	Symbol	Description
7 to 0	RWaterlevel[7:0]	Overflow threshold of the Receive FIFO to set a warning

8.3.3.3 TWL register

This register specifies the warning level of the Transmit FIFO for the CPU. It implies a FIFO buffer underflow.

Table 94. TWL register (SFR: address 9Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				TWaterl	evel[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 95. Description of TWL bits

Bit	Symbol	Description
7 to 0	TWaterlevel[7:0]	Underflow threshold of the Transmit FIFO to set a warning

8.3.3.4 FIFOFS register

This register reports the number of bytes that the CPU can still load into the FIFO until the Transmit FIFO is full.

Table 96. FIFOFS register (SFR: address 9Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol			T	ransmitFre	espace[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 97. Description of FIFOFS register bits

Bit	Symbol	Description
7 to 0	TransmitFreespace[7:0]	Freespace into the FIFO

8.3.3.5 FIFOFF register

This register reports the number of bytes already received and written into the Receive FIFO.

Table 98. FIFOFF register (SFR: address 9Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				ReceiveFu	llness[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 99. Description of FIFOFF bits

Bit	Symbol	Description
7 to 0	ReceiveFullness[7:0]	Number of bytes received in the FIFO

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8.3.3.6 SFF register

The register bits serve to allow the CPU to monitor the state of the FIFO. The primary purpose is to detect completion of data transfers.

Table 100. SFF register (SFR: address 9Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFO_EN	-	TWLL	TFF	TFE	RWLH	RFF	RFE
Reset	0	0	1	0	1	0	0	1
Access	R/W	R	R	R	R	R	R	R

Table 101. Description of SFF bits

Bit	Symbol	Description
7	FIFO_EN	**Fifo Enable**:Set to 1 this bit enables the FIFO manager clock (CPU_CLK). Set to 0 the clock remains low.
6	-	Reserved.
5	TWLL	**Transmit WaterlLevelLow**:This bit is set to 1 when the number of bytes stored into the Transmit FIFO is equal or smaller than the threshold TWaterlevel.
4	TFF	**Transmit FIFO Full**:This is set to 1 if the transmit part of the FIFO is full. It is cleared to 0 when a transfer is completed.
3	TFE	**Transmit FIFO Empty**:This bit indicates when the transmit part of the FIFO is empty.
		It is cleared to 0 when the CPU writes a character in the data register.
2	RWLH	**Receive WaterLevel High**: This bit is set to 1 when the number of bytes stored into the Receive FIFO is greater or equal to the threshold RWaterlevel.
1	RFF	**Receive FIFO Full**:This bit is set to 1 if the receive part of the FIFO is full. It is cleared to 0 by reading the FDATA register.
0	RFE	**Receive FIFO Empty**:This bit indicates when the receive part of the FIFO is empty.
		Set to 1, when the Receive FIFO is empty.
		Set to 0, when the Receive FIFO contains at least 1 byte.

8.3.3.7 FIT register

The FIT register holds 6 read-write bits which are logically OR-ed to produce an interrupt going to the CPU.

Table 102. FIT register (SFR: address 9Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Reset	-	WCOL_	TWLL_	TFF_	RWLH_	ROVR_	RFF_
			IRQ	IRQ	IRQ	IRQ	IRQ	IRQ
Reset	0	0	0	0	0	0	0	0
Access	W	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 103. Description of FIT bits

Bit	Symbol	Description
7	Reset	**Reset**. Writing 1 causes bits written as 1 in the same command to be cleared to 0 in this register.
6	-	Reserved.
5	WCOL_IRQ	**Write collision IRQ**. Set when the transmit side of the FIFO is already full (TFF = 1) and the CPU writes another character to the data register.
4	TWLL_IRQ	**Transmit WaterLevelLow IRQ**. Set when the number of bytes in the Transmit FIFO is equal to or below TWater-level.
3	TFF_IRQ	**Transmit FIFO Full IRQ**. Set when the transmit side of the FIFO is full.

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Bit	Symbol	Description
2	RWLH_IRQ	**Receive WaterLevel High IRQ**. Set when the number of bytes in the Receive FIFO is greater than or equal to RWaterlevel.
1	ROVR_IRQ	**Read overrun IRQ**. Indicates that the receive side of the FIFO was full when another transfer completed, causing the new incoming data to be lost.
0	RFF_IRQ	**Receive FIFO Full IRQ**. Set when the receive side of the FIFO is full.

8.3.3.8 FITEN register

The FITEN register enables or disables the interrupt requests to the CPU. It is also used to reset the contents of the Receive and Transmit FIFO.

Table 104. FITEN register (SFR: address A1h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TFLUSH	RFLUSH	EN_ WCOL_ IRQ	EN_ TWLL_ IRQ	EN_ TFF_ IRQ	EN_ RWLH_ IRQ	EN_ ROVR_ IRQ	EN_ RFF_ IRQ
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 105. Description of FITEN bits

Bit	Symbol	Description
7	TFLUSH	When set to 1, resets the Transmit FIFO pointer. TFLUSH and RFLUSH must not be asserted at the same time.
6	RFLUSH	When set to 1, resets the Receive FIFO pointer. RFLUSH and TFLUSH must be asserted one after the other, not simultaneously.
5	EN_WCOL_IRQ	**Enable Write Collision IRQ**. When set to 1, WCOL_IRQ is enabled. IE1_5 must also be set to 1 to enable the corresponding CPU interrupt.
4	EN_TWLL_IRQ	**Enable Transmit WaterLevelLow IRQ**. When set to 1, TWLL_IRQ is enabled. IE1_5 must also be set to 1 to enable the corresponding CPU interrupt.
3	EN_TFF_IRQ	**Enable Transmit FIFO Full IRQ**. When set to 1, TFF_IRQ is enabled. IE1_5 must also be set to 1 to enable the corresponding CPU interrupt.
2	EN_RWLH_IRQ	**Enable Receive WaterLevel High IRQ**. When set to 1, RWLH_IRQ is enabled. IE1_5 must also be set to 1 to enable the corresponding CPU interrupt.
1	EN_ROVR_IRQ	**Enable Read Overrun IRQ**. When set to 1, ROVR_IRQ is enabled. IE1_5 must also be set to 1 to enable the corresponding CPU interrupt.
0	EN_RFF_IRQ	**Enable Receive FIFO Full IRQ**. When set to 1, RFF_IRQ is enabled. IE1_5 must also be set to 1 to enable the corresponding CPU interrupt.

8.3.3.9 FDATA register

FDATA provides the CPU access point for transmitted and received data bytes. Each data written in the data register is pushed into the Transmit FIFO. Each data read from the data register is popped from the Receive FIFO.

Table 106. FDATA register (SFR: address A2h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				FDAT	A[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 107. Description of FDATA bits

Bit	Symbol	Description
7 to 0	FDATA[7:0]	Writing to FDATA writes to the transmit buffer.
		Reading from FDATA reads from the receive buffer.

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8.3.3.10 FSIZE register

This register specifies the size of the Receive FIFO. The maximum size is 182 bytes. The free space not used by the Receive FIFO in the RAM is allocated to Transmit FIFO.

Table 108. FSIZE register (SFR: address A3h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				Receive	Size[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109. Description of FSIZE bits

Bit	Symbol	Description
7 to 0	ReceiveSize[7:0]	Size of the Receive FIFO

8.3.4 HIGH SPEED UART (HSU)

The High Speed UART (HSU) offers a high speed link to the host (up to 1.288 Mbit/s).

The HSU is a full duplex serial port. The serial port has a Receive-buffer: in conjunction with the FIFO manager, the reception of multiple bytes may be carry outed without strong CPU real time constraints. Nevertheless, if the Receive FIFO still has not been read by the CPU, and the number of receive bytes is greater than the Receive FIFO size then the new incoming bytes is lost.

The HSU receive and send data registers are both accessed by firmware in the FIFO manager FDATA register. Writing to FDATA writes the send register, reading from FDATA accesses the separate receive register.

The characteristics of the UART are the next:

- Full duplex serial port
- Receive buffer to allow reception of byte while the previous bytes are held into the FIFO manager
- 8-bit data transfers
- Programmable baud rate generator by means of prescaler for transmission and reception
- Based on 27.12 MHz clock frequency
- Dedicated protocol preamble filter
- Wake-up generator

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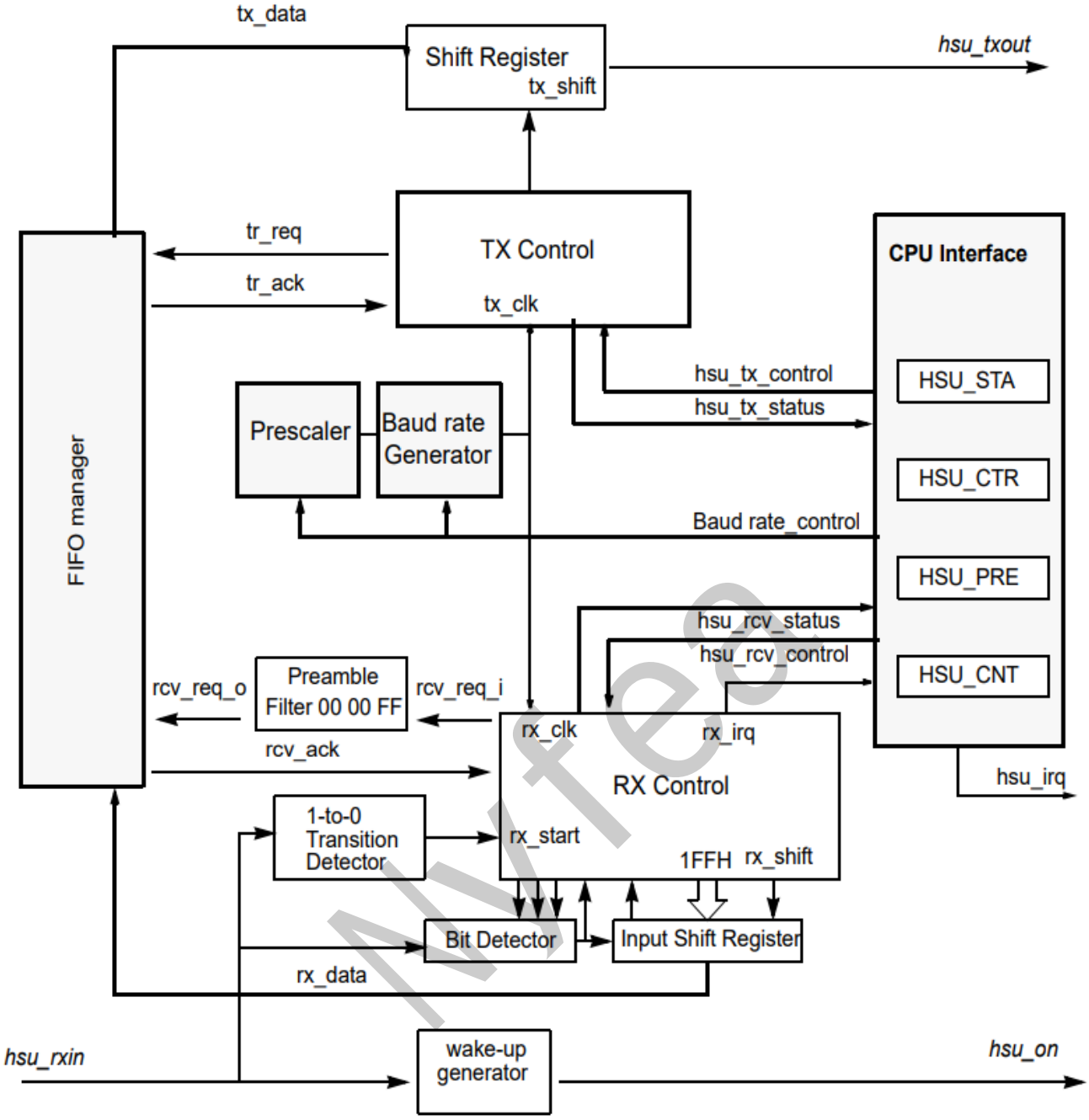


Fig 13. HSU block diagram

The HSU contains 4 SFRs:

Table 110. HSU SFR register list

Name	Size [bytes]	SFR Address	Description	Access
HSU_STA	1	ABh	HSU STAtus register	R/W
HSU_CTR	1	ACh	HSU ConTRol register	R/W
HSU_PRE	1	ADh	HSU PREscaler for baud rate generator	R/W
HSU_CNT	1	AEh	HSU CouNTer for baud rate generator	R/W

8.3.4.1 Mode of operation

The HSU supports only one operational mode, which has the next characteristics:

- Start bit:
  - Start bit is detected when a 0 is asserted on the HSU_RX line.
- 8 data bits:
  - The data bits are sent or received LSB first.
- Stop bit:
  - During reception, the Stop bit(s) is detected when all the data bits are accepted and when Stop bit(s) is sampled to 1. The number of Stop bits is programmable. It may be 1 or 2.
  - During Transmission, after the complete data bit transmission, a variable number of Stop bit(s) is sent. This number is programmable from 1 to 4.

8.3.4.2 HSU Baud rate generator

To reach the high-speed transfer rate, the HSU has its own baud-rate generator. The baud rate generator contains a prescaler and a counter. The prescaler is located prior to the counter. The purpose of the prescaler is to divide the frequency of the count signal to enlarge the range of the counter (at the cost of a lower resolution). The division factor of the prescaler equals 2 to the power HSU_PRE[8:0] (Table 113), resulting in division factors ranging from 1 (20) to 256 (28). The combination of these 2 blocks specifies the bit duration and the bit sampling.

8.3.4.3 HSU preamble filter

Received characters are sent to the FIFO manager after three consecutive characters have been accepted: 00 00 FF. When the frame is finished, and prior to a new frame arrives, firmware shall write a 1 in the start_frame bit of the HSU_CTR register to re-activate the preamble filter. If firmware does not write a 1 then all characters of the frame are sent to the FIFO manager (including the preamble).

8.3.4.4 HSU wake-up generator

The wake-up generator is a 3-bit counter which counts on every rising edge of the HSU_RX pin. When the counter reaches 5, the hsu_on signal is set to 1 to wake-up the NF532. This block is useful in Soft-Power-Down mode. The firmware shall reset this counter just prior to going in Soft-Power-Down by writing a 1 in the hsu_wu_en bit into the HSU_CTR register.

8.3.4.5 HSU_STA register

The SFR HSU_STA is the status register of the HSU.

Table 111. HSU_STA register (SFR: address ABh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	set_bit	-	-	disable_	irq_rx_	irq_rx_fer	irq_rx_	irq_rx_fer
				preamb	over_en	_ en	over	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Table 112. Description of HSU_STA bits

Bit	Symbol	Description
7	set_bit	When cleared to 0 during write operation, the bits set to 1 in the write command are written to 0 in the register. When set to 1 during write operation, the bits set to 1 in the write command are written to 1 in the register.

Bit	Symbol	Description
6 to 5	-	Reserved
4	disable_preamb	**Preamble filter disable.** When this bit is set to 1, this bit disables the preamble filtering, it means that HSU_RX line transmit any received bytes to the FIFO manager.
3	irq_rx_over_en	**FIFO overflow interrupt enable.** When this bit is set to 1, this bit enables the interrupt generation when the bit irq_rx_over is set to 1. The bit IE1_5 of register IE1 (see Table 13)has also to be set to 1 to enable the corresponding CPU interrupt.
2	irq_rx_fer_en	**Framing error interrupt enable.** When this bit is set to 1, this bit enables the interrupt generation when the bit irq_rx_fer is set to 1. The bit IE1_5 of register IE1 (see Table 13)has also to be set to 1 to enable the corresponding CPU interrupt.
1	irq_rx_over	**Receive FIFO overflow interrupt.** Set to 1 when the FIFO manager is full (rcv_ack is cleared to 0) and when HSU shift register is ready to send another byte to the FIFO manager.
0	irq_rx_fer	**Framing error interrupt.** Set to 1 when a framing error has been detected. Framing error detection is based on Stop bit sampling. When Stop bit is expected at 1 but is sampled at 0, this bit is set to 1.

8.3.4.6 HSU_CTR register

This register offers the controls for the configuration of the HSU.

Table 113. HSU_CTR register (SFR: address ACh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	hsu_wu_	start_frame	tx_stop	bit[1:0]	rx_stopbit	tx_en	rx_en	soft_reset_n
	en							
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 114. Description of HSU_CTR bits

Bit	Symbol	Description
7	hsu_wu_en	**HSU wake-up enable.** When set to 1 this bit re-activates the NSS / SCL / HSU_RX rising-edge counter. When the counter is 5 then a signal hsu_on is activated. This signal is one of the possible wake-up events from Soft-Power-Down mode in the PCR block. The firmware shall set this bit to 1 just before requesting a Soft-Power-Down mode. The bit HSU_on_en of register PCR Wakeupen (see Table 144) has also to be set to 1 to enable the corresponding NF532 wake-up.
6	start_frame	**Enables the preamble filter for next frame.** When set to 1 this bit indicates that a new frame is coming. This re-activates the preamble filter (when enabled), meaning that the first “00 00 FF” characters will not be sent to the FIFO manager.
5:4	tx_stopbit[1:0]	**Specifies the number of stop bit during transmission.** These 2 bits define the number of Stop bit(s) inserted at the end of the transmitted frame. The number of Stop bit(s) transmitted is equal to tx_stopbit +1.
3	rx_stopbit	**Specifies the number of stop bit during reception.** This bit defines the number of Stop bit(s) inserted at the end of the received frame. The number of Stop bit(s) expected in reception is equal to rx_stopbit +1.
2	tx_en	**Enables the transmission of HSU.** When set to 1 this bit enables the transmission of characters. When this bit is cleared to 0, the transmission is disabled only after the completion of the current transmission.
1	rx_en	**Enables the reception of the HSU.** When set to 1 this bit enables the reception of characters. When this bit is cleared to 0, the reception is disabled only after the completion of the current reception.

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Bit	Symbol	Description
0	soft_reset_n	**HSU Reset.** When this bit is cleared to 0, this bit disables the clock of the HSU_RX control, HSU_TX control and baud rate generator modules.

8.3.4.7 HSU_PRE register

This register configures the baud rate generator prescaler. The prescaler enlarges the range of the counter (at the cost of a lower resolution). The division factor of the prescaler ranges from 1 (20) to 256 (28).

Table 115. HSU_PRE register (SFR: address ADh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				hsu_pres	caler[7:0]			
Reset	0	0	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 116. Description of HSU_PRE bits

Bit	Symbol	Description
7 to 0	hsu_prescaler[7:0]	In conjunction with HSU_CNT, specifies the HSU baud rate.
		Baud rate = fclk/ ((hsu_prescaler +1) * hsu_counter)

8.3.4.8 HSU_CNT register

This register configures the baud rate generator counter.

Table 117. HSU_CNT register (SFR: address AEh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				hsu_cou	nter[7:0]			
Reset	0	1	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 118. Description of HSU_CNT bits

Bit	Symbol	Description
7 to 0	hsu_counter[7:0]	In conjunction with HSU_PRE, specifies the HSU baud rate.
		Baud rate = fclk/ ((hsu_prescaler +1) * hsu_counter)

Here is a table of recommendation for some data rates:

Table 119. Recommendation for HSU data rates

Targeted data rate	HSU_CNT value	HSU_PRE value	Real HSU freq	Min recommended Host HSU freq	Max recommended Host HSU freq
9 600	0x71	0x18	9 516	9 326	9 706
19 200	0x9D	0x08	19 193	18 810	19 576
38 400	0x65	0x06	38 359	37 592	39 126
57 600	0x9D	0x02	57 579	56 428	58 730
115 200	0xEB	0x00	115 404	113 096	117 712
230 400	0x76	0x00	229 831	225 234	234 427
460 800	0x3B	0x00	459 661	450 467	468 854
921 600	0x1D	0x00	935 172	916 468	953 875
1 288 000	0x15	0x00	1 291 429	1 265 600	1 317 257

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8.3.5 Serial Parallel Interface (SPI)

The SPI has the next features:

- Compliant with Motorola de-facto Serial Peripheral Interface (SPI) standard
- Synchronous, Serial, Half-Duplex communication, 5 MHz max
- Slave configuration
- 8 bits bus interface

Through the SPI interface, the host can either access the FIFO manager (acting as data buffer) or the SPI status register. This selection is made through the hereafter described protocol.

The SPI interface is managed by 2 SFRs.

Table 120. SPI SFR register list

Name	Size	SFR	Description	R/W
	[bytes]	address		
SPIcontrol	1	A9h	SPI control bits	R/W
SPIstatus	1	AAh	SPI Status/Error bits	R

8.3.5.1 Shift register pointer

A shift register serves to address the SPI interface. The setting loaded in this register is either the first byte of the FIFO manager or the SPI status register.

The first byte received from the host will hold the address of the register to access (SPI status or FIFO manager FDATA) and also whether it is a SPI write or read. This character is managed by hardware.

The bits used to define these operations are the 2 LSBs of the first byte.

Table 121. SPI operation

Bit 1	Bit 0	Operation
0	0	No effect
0	1	FIFO manager write access
1	0	SPI Status register read access
1	1	FIFO manager read access

STATUS or DATA (Decoded output of First byte)

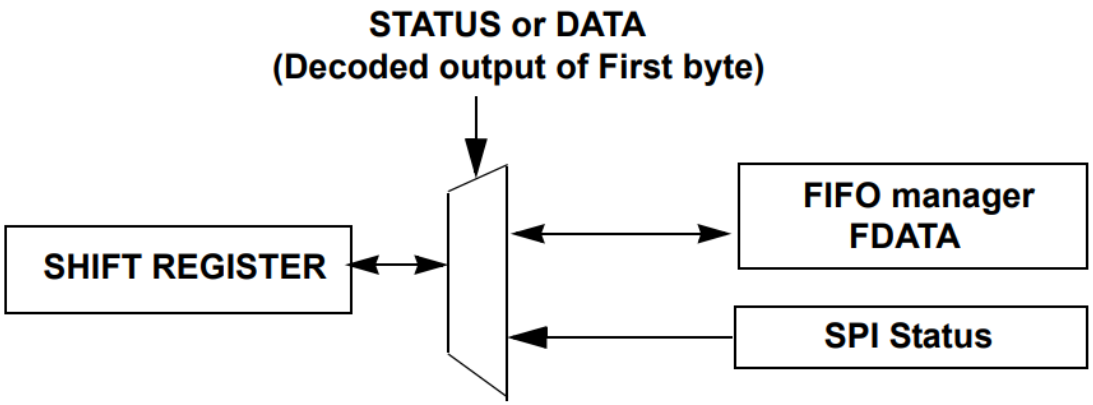


Fig 14. Memory manager shift register management

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8.3.5.2 Protocol

Once the FIFO is full enough (see FIFO manager thresholds in Table 91), the CPU sets bit READY in the SPI Status register to 1. Polling the SPI Status register, the host is informed of the READY flag and can start the data transfer.

The protocol used is based on:

- ADDRESS / DATA protocol for status data exchanges
- ADDRESS / DATA / DATA / DATA... for data transfers

An exchange begins on the falling edge of NSS and follows the diagram described below.

8.3.5.3 SPI status register read

There is for that case no read request going to the FIFO manager. The contents of the status register is loaded in the SPI shift register.

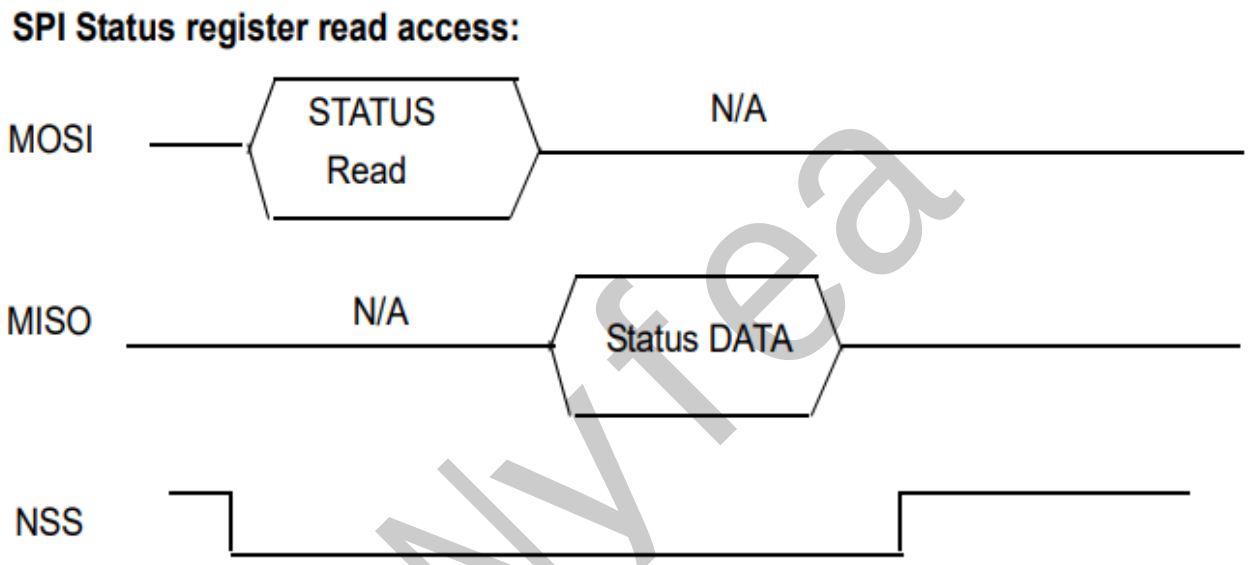


Fig 15. SPI Status register read access

8.3.5.4 FIFO manager read access

Bytes are loaded from the FIFO manager into the SPI shift register and sent back to the host.

Remark: for proper operation, the firmware should write an additional byte in the FIFO manager (FDATA). This byte is not transmitted.

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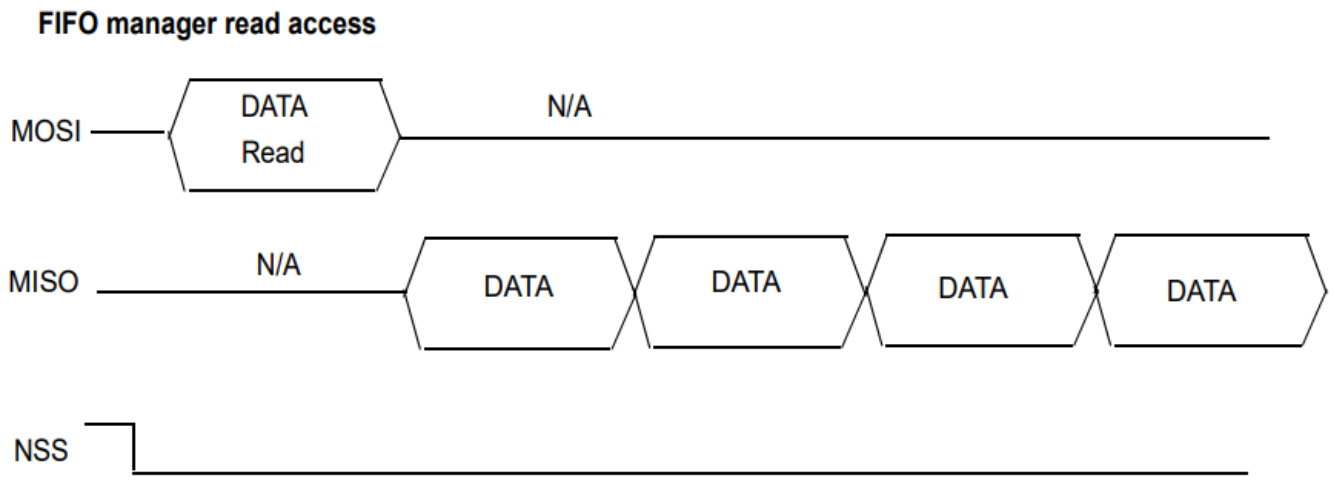


Fig 16. SPI FIFO manager read access

8.3.5.5 FIFO manager write access

MISO is maintained at 0. Once a byte is accepted, a write request is sent to the FIFO manager and the byte is loaded from SPI shift register into Receive FIFO of the FIFO manager.

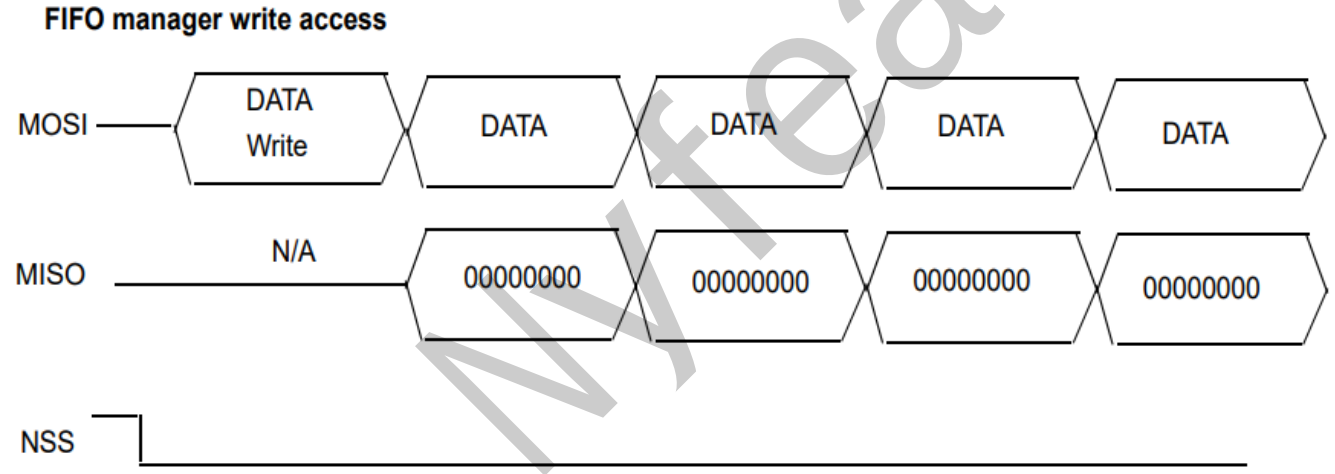


Fig 17. SPI FIFO manager write access

8.3.5.6 SPIcontrol register

SPIcontrol register holds programmable bits used to control the function of the SPI block. This register has to be set prior to any data transfer.

Table 122. SPIcontrol register (SFR: address A9h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	Enable	-	CPHA	CPOL	IE1	IE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R	R/W	R/W	R/W	R/W

Table 123. Description of SPIcontrol bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5	Enable	**SPI enable**:Setting this bit to 1 enables the SPI interface assuming that selif[1:0] are set to 01b.

Bit	Symbol	Description
4	-	Reserved.
3	CPHA	**Clock PHAse**:This bit controls the relationship between the data and the clock on SPI transfers. When cleared to 0: Data is always sampled on the first clock edge of SCK. When set to 1: Data is always sampled on the second clock edge of SCK.
2	CPOL	**Clock POLarity**:This bit controls the polarity of SCK clock. When this bit is set to 1, SCK starts from 0 else starts from 1.
1	IE1	**Interrupt Enable 1**:When this bit is set to 1, the hardware interrupt generated by TR_FE in SPIstatus register is enabled. The bit IE1_5 of register IE1 (see Table 13)has also to be set to 1 to enable the corresponding CPU interrupt.
0	IE0	**Interrupt Enable 0**:When this bit is set to 1, the hardware interrupt generated by RCV_OVR in SPIstatus register is enabled. The bit IE1_5 of register IE1 (see Table 13)has also to be set to 1 to enable the corresponding CPU interrupt.

Remark: The figure below explains how bits CPOL and CPHA may be used.

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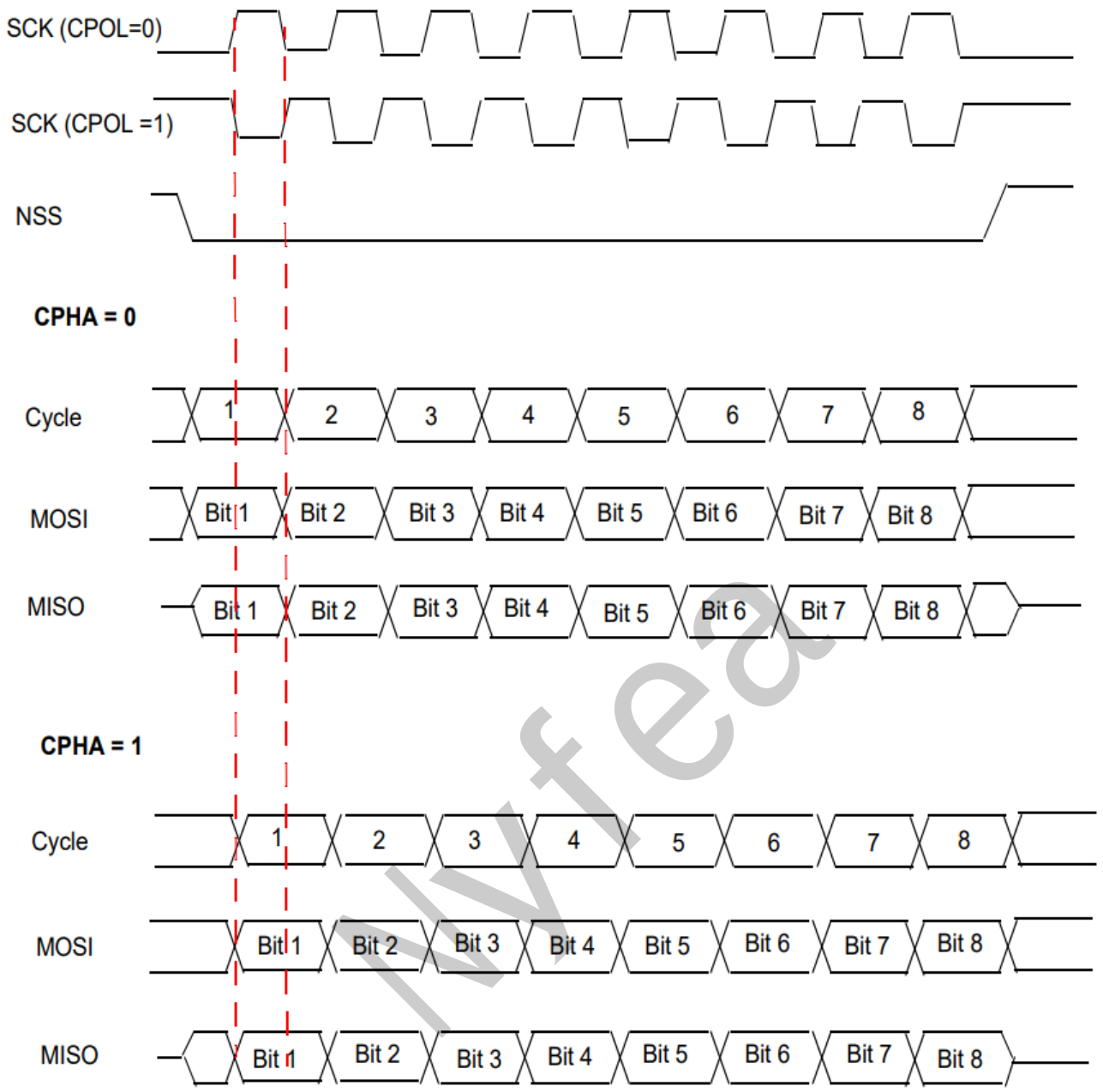


Fig 18. SPI Data transfer format

8.3.5.7 SPIstatus register

The SPIstatus register is byte addressable. It holds bits which serve to monitor the state of the SPI interface, including normal functions, and exception conditions. The primary purpose of this register is to detect completion of a data transfer. The staying bits in this register are exception condition indicators.

Table 124. SPIstatus register (SFR: address AAh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	TR_FE	RCV_OVR	-	READY
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

Table 125. Description of SPIstatus bits

Bit	Symbol	Description
7 to 4	-	Reserved.
3	TR_FE	**Transmit FIFO Empty**:Set to 1 when the host attempts to read a new byte and FIFO manager is empty. An interrupt may be generated if enabled (see IE1 bit in register SPIcontrol). It is cleared to 0 by firmware.
2	RCV_OVR	**Receive Overrun**:Set to 1 when the host attempts to write a new byte and FIFO manager is full, or has not yet processed the previous byte. An interrupt may be generated if enabled (see IE0 bit in register SPIcontrol) It is cleared to 0 by firmware.
1	-	**Reserved; keep this bit at 0.**
0	READY	**Ready flag. The firmware set READY to 1 to inform the host when NF532 is ready to send data.**

8.4 Power management

Figure 19 “Power management scheme” depicts the internal and external power distribution management. Power is supplied to the NF532 via pins VBAT and PVDD. VBAT is driven by the battery and serves to supply the all blocks excluding the host interface. PVDD is connected with the host’s power supply and powers the NF532’s host interface. No specific sequencing is needed between the two supply rails: VBAT may be present without PVDD and vice versa.

An internal low drop-out (LDO) voltage regulator produces DVDD and SVDD, which serve to supply the internal digital logic and the secure IC respectively. DVDD is also routed externally to supply AVDD (analog power) and TVDD (send power). DVDD, AVDD and TVDD must be separately decoupled.

When another host interface than SPI is employed, the NF532 may be used with reduced functionalities; all functionalities, except those related to the PVDD supplied pins (like host interfaces) when:

PVDD < 0.4V

- 5.5V > VBAT > 2.7V
- 3.6V > RSTPD_N > VBAT * 0.65

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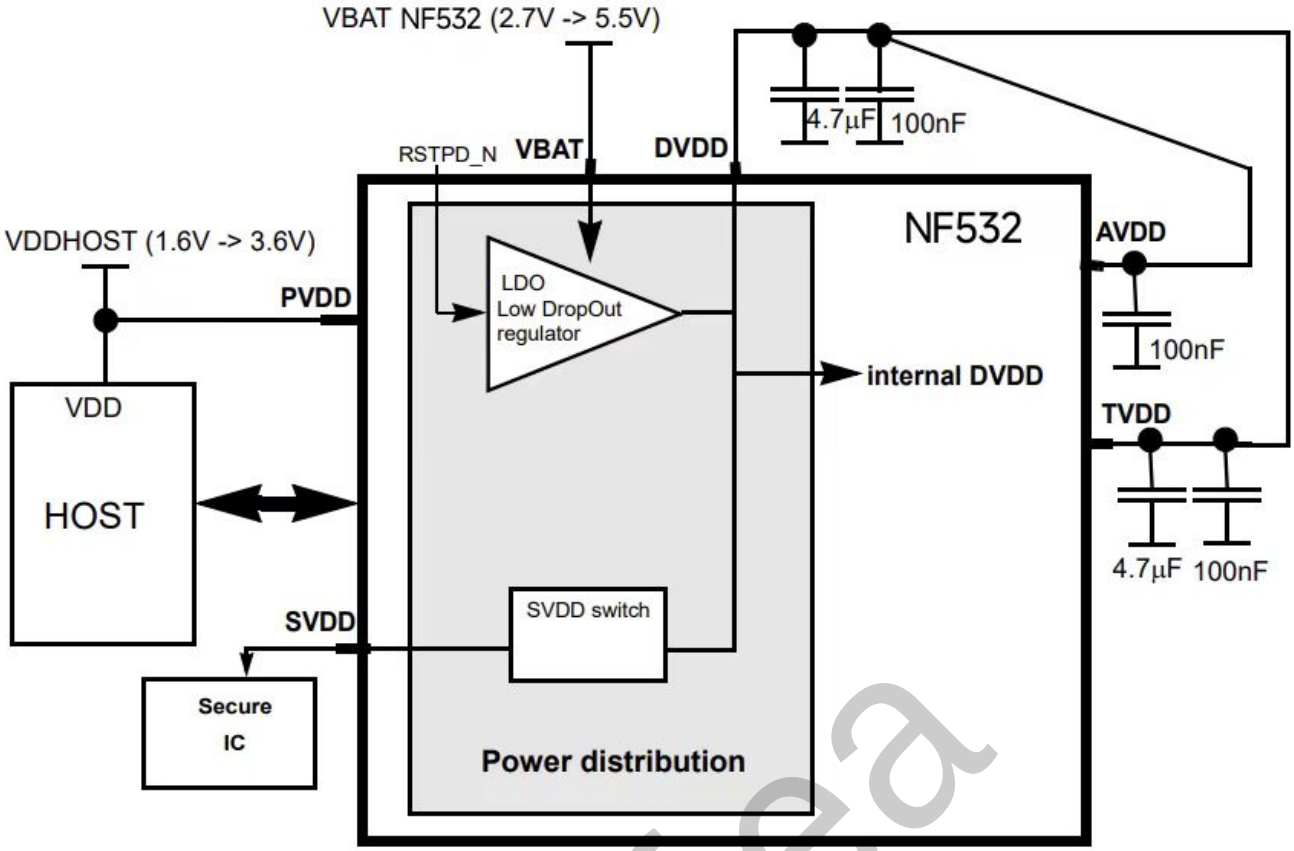


Fig 19. Power management scheme

8.4.1 Low drop-out voltage regulator

8.4.1.1 LDO block diagram

The regulator serves to reduce the VBAT voltage to the typical voltage rating of the NF532. It acts as a 3.0 V linear regulator with resistive feed-back, as long as the VBAT voltage is above 3.4 V. It is designed to cope with a maximum fluctuation of 400 mV on the VBAT line (due to voltage bursts exhibited by the battery).

If VBAT falls below 3.4 V, the output of the regulator tracks VBAT with a variable delta. It continues to reject any noise on the VBAT line via the use of an internal band-gap reference.

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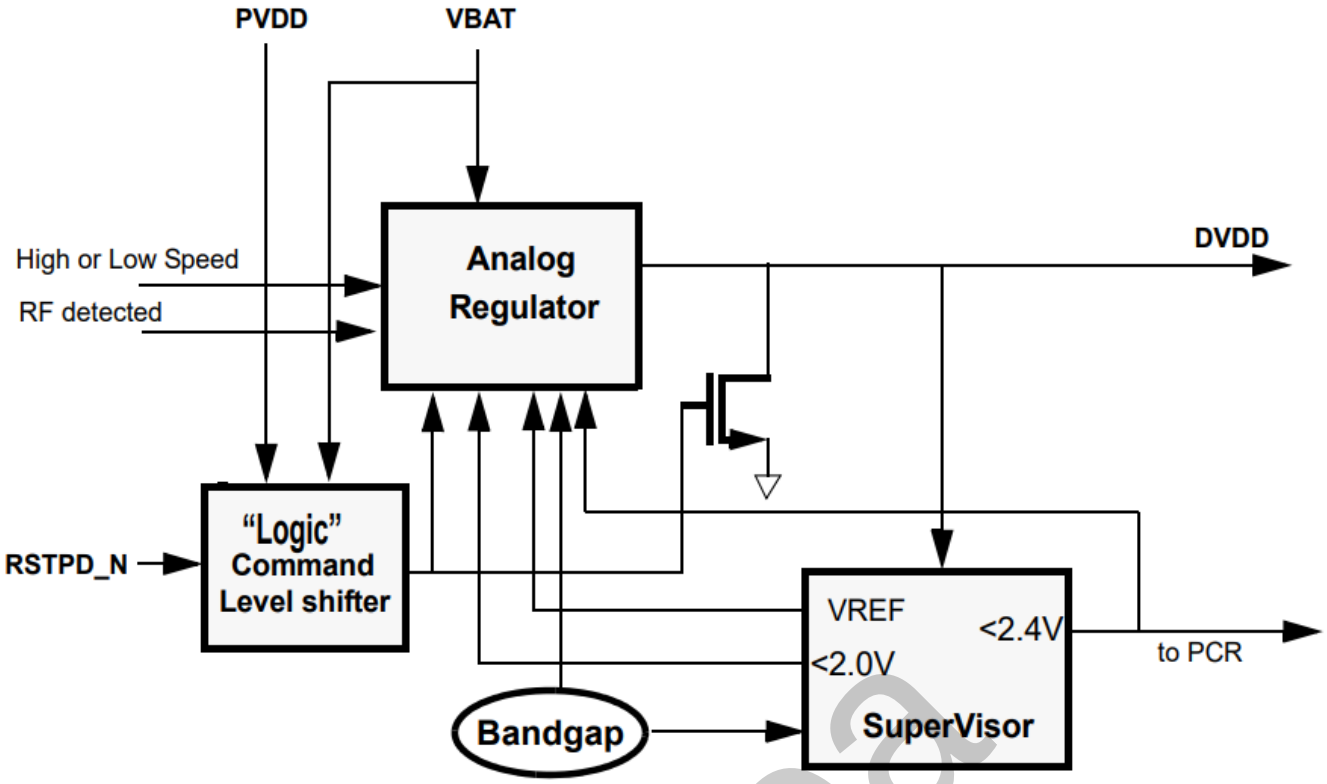


Fig 20. LDO block diagram

8.4.1.2 LDO with offset

The LDO produces DVDD. When RSTPD_N is high, and PVDD is above 1.6 V, this voltage is defined by:

- VBAT > 3.4V: DVDD is fixed at 3V and bursts on VBAT up to 400 mV are suppressed.
- 3.4V > VBAT > 2.5V: DVDD follows VBAT with an offset, which decreases with VBAT from 400mV at 3.4V to 0mV at 2.5V.
- 2.5V > VBAT > 2.35V: DVDD=VBAT.
- 2.35V > VBAT=DVDD and the NF532 is in reset.

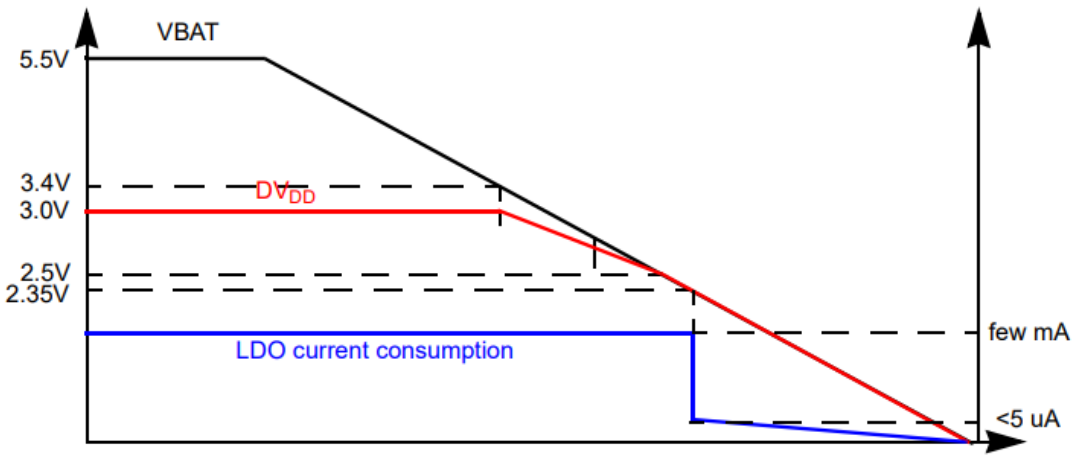


Fig 21. Graph of DVDD versus VBAT with offset

When the NF532 is in Soft-Power-Down mode, bursts rejection is no longer present and the behavior then becomes:

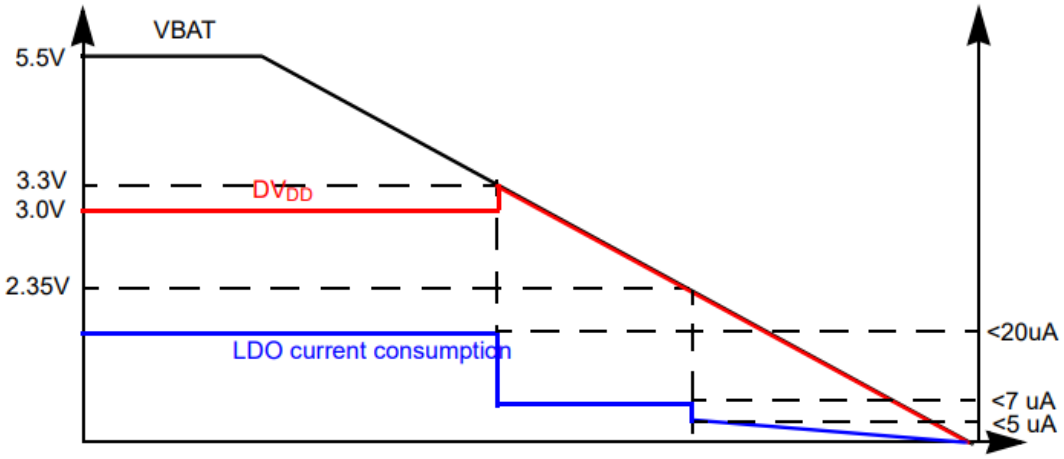


Fig 22. Graph of DVDD versus VBAT in Soft-Power-Down mode with offset

8.4.1.3 LDO without offset

The LDO produces DVDD but any voltage fluctuation on VBAT is not compensated for. When RSTPD_N is high and PVDD is above 1.6 V, this voltage is defined by:

- VBAT > 3.0V: DVDD = 3 V.
- 3.0V > VBAT > 2.35V: DVDD = VBAT.
- 2.35V > VBAT=DVDD and the NF532 is in reset.

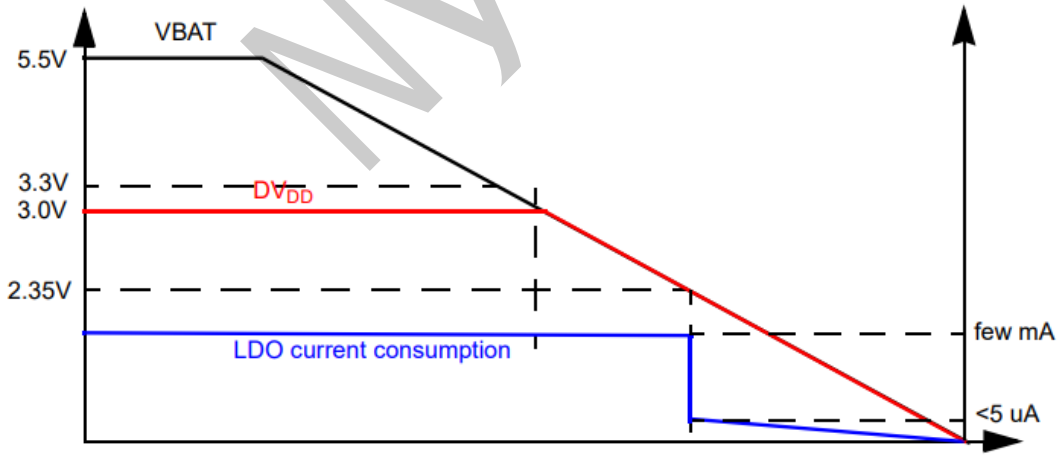


Fig 23. Graph of DVDD versus VBAT without offset

When in Soft-Power-Down mode, the behavior is the same as that with offset. See Figure 22.

8.4.1.4 LDO overcurrent detection

The LDO integrates an overcurrent detector. When the current on VBAT exceeds a programmable threshold, an error bit is set. See Table 126. If IE1_0 is set to 1 (see Table 13), an 80C51 interrupt is asserted when an overcurrent is detected.

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8.4.1.5 LDO register

Table 126. LDO register- (address 6109h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	overcurrent_	sel_overc	urrent[1:0]	enoffset	soft_	control_
			status	-			highspeedreg	highspeedreg
Reset	0	0	0	0	0	1	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 127. Description of LDO bits

Bit	Symbol	Description
7 to 6	-	Reserved
5	overcurrent_status	Set to 1 by NF532 when overcurrent is detected. The bit IE1_0 of register IE1 (see Table 13)has also to be set to 1 to enable the corresponding CPU interrupt.
4 to 3	sel_overcurrent[1:0]	**Select overcurrent threshold.** 00: 300 mA 01: 210 mA
		10: 180 mA 11: 150 mA
2	enoffset	**Enable of the LDO offset.** When this bit is set to 1, offset is present.
1	soft_highspeedreg	**Control the LDO regulation speed.** When this bit is cleared to 0, the bandwidth of LDO is reduced to filter bursts on VBAT. When this bit is set to 1, the bandwidth is increased to establish DVDD supply quickly.
0	control_highspeedreg	**Select the control source of the LDO regulation speed.** When set to 1, LDO bandwidth controlled by soft_highspeedreg. When this bit is cleared to 0, LDO bandwidth controlled by output of RF level detector. When RF is detected, bandwidth is reduced.

8.4.2 SVDD switch

The SVDD switch serves to control power to the secure IC. The switch is controlled by register Control_switch_rng (address 6106h). The switch is enabled with bit sic_switch_en. When disabled, the SVDD pin is tied to ground. A current limiter is incorporated into the switch. Current consumption exceeding 40 mA triggers the limiter and the status bit sic_switch_overload is set.

Register Control_switch_rng also controls the random generator within the Contactless Interface Unit (CIU).

Table 128. Control_switch_rng register (address 6106h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	hide_svdd_	sic_switch_	sic_switch_	-	cpu_need_	random_	-
		sig	overload	en		rng	dataready	
Reset	0	1	0	0	0	0	0	1
Access	R	R/W	R	R/W	R	R/W	R/W	R

Table 129. Description of Control_switch_rng bits

Bit	Symbol	Description
7	-	Reserved.
6	hide_svdd_sig	**Configures internal state of input signals SIGIN and P34 when idle.** This bit may be used to avoid spikes on SIGIN and P34 when the SVDD switch is enabled or disabled. When this bit is cleared to 0, internal state of SIGIN and P34 are driven by pads SIGIN and P34 respectively. When this bit is set to 1, internal state of SIGIN is cleared to 0 and internal state of P34 is set to 1.

Bit	Symbol	Description
5	sic_switch_overload	**Indicates state of SVDD switch current limiter.** When this bit is cleared to 0, indicates that current consumption through SVDD switch does not exceed limit (40mA). When this bit is set to 1, the SVDD switch current limiter is activated.
4	sic_switch_en	**Enables or disables power to SVDD switch.** When this bit is cleared to 0, SVDD switch is disabled and SVDD output is tied to the ground. When this bit is set to 1, the SVDD switch is enabled and the SVDD output delivers power to secure IC and internal pads (SIGIN, SIGOUT and P34).
3	-	Reserved.
2	cpu_need_rng	**Forces random number generator into running mode.** When set to 0, random number generator is under control of Contactless Interface Unit. When this bit is set to 1, random number generator is forced to run.
1	random_dataready	**Indicates availability of random number.** When this bit is set to 1, a new random number is available. Automatically cleared to 0 when register data_rng (address 6105h) is read.
0	-	Reserved.

8.5 Power clock and reset controller

The PCR controller is responsible for the clock generation, power management and reset mechanism within the NF532.

8.5.1 PCR block diagram

The block diagram shows the relationship between the PCR, other embedded blocks and external signals.

PCR block diagram

Table 130. NF532 clock source characteristics

Clock name	Frequency MHz	Tolerance	Clock source	Comments
OSC_CLK27	27.12	±14 kHz	OSC 27.12	Output of OSC 27
CPU_CLK	27.12/13.56/6.78	±500 ppm	OSC 27.12	Default is 6.78 MHz
HSU_CLK	27.12	±14 kHz	OSC 27.12	

8.5.2 27.12 MHz crystal oscillator

The 27.12 MHz clock applied to the NF532 is the time reference for the embedded microcontroller. Consequently stability of the clock frequency is an important factor for reliable operation. It is recommended that the design adopt the circuit shown in Figure 24.

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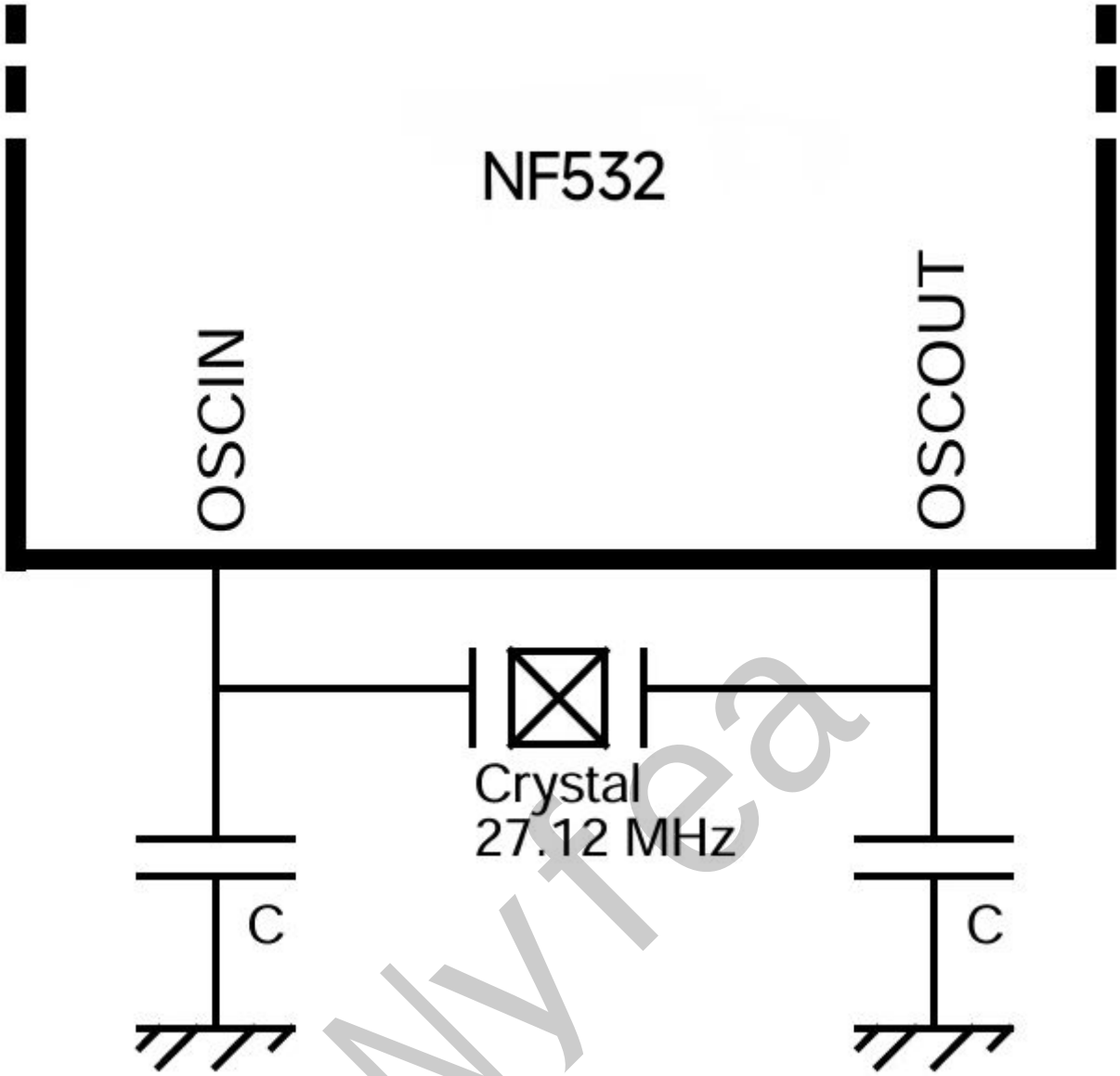


Fig 24. 27.12 MHz crystal oscillator connection

8.5.3 Reset modes

The possible reset mechanisms are listed below:

- Supply rail variation

When DVDD falls below 2.4 V , the POR (Power-On-Reset) asserts an internal reset signal. The Power Sequencer disables all clocks. When DVDD rises above 2.4V, the POR deasserts the internal reset signal and the Power Sequencer begins the power-up sequence. Once the NF532 is out of reset, the RSTOUT_N pin is driven high.

- Glitch on DVDD

When DVDD falls below 2.35 V for greater than 1 ms, the POR asserts an internal reset signal. The power sequencer begins the Power-down sequence. The NF532 goes into reset and the RSTOUT_N signal is driven low.

- Hard Power Down mode (HPD)

When RSTPD_N is cleared to 0, the NF532 goes into Hard Power Down (HPD) mode. The NF532 goes into reset and the RSTOUT_N signal is driven low. The power usage is at the minimum. DVDD is tied to ground and ports are disconnected from their supply rails.

When in Hard Power Down mode, the GPIO pins are forced in quasi bidirectional mode. Referring to Figure 7, en_n = e_pu = “1”, e_p = “0”. e_hd = “1” if GPIO pin value is “1” and e_hd = “0” if GPIO pin value is “0”.

8.5.4 Soft-Power-Down mode (SPD)

To initiate the Soft-Power-Down mode with minimal power usage, the firmware should:

- Configure I/Os to minimize power usage. Be careful that for P32_INT0, referring to Section 8.2.1 “Pad configurations description”, e_hd is forced to 1.
- Shut down unused functions
  - Contactless Interface Unit with bit Power-down of SFR register D1h, see Table 179.
  - Disable the SVDD switch, see Table 129
  - Power down the RF level detector if RF wake-up is not enabled, see Table 287.
- Enable relevant wake-up sources
- Disable unwanted interrupts
- Assert bit CPU_PD in register PCON, see Table 7

When bit CPU_PD is set, all clocks are stopped and the LDO is put into Soft-Power-Down mode. Finally, the Power Sequencer goes into Stopped state.

8.5.5 Low power modes

There are 2 various low power modes.

- Hard-Power-Down mode (HPD): controlled by the pin RSTPD_N. The NF532 goes ”
- into reset and power usage is at a minimum, see Section 8.5.3 “Reset modes.
- Soft-Power-Down mode (SPD): controlled by firmware. See Section 8.5.4 “Soft-Power-Down mode (SPD)” to optimize the power usage in this mode.

Table 131. Current consumption in low power modes

Mode	Conditions	Maximum current consumption
Hard-Power-Down	RSTPD_N is cleared to 0	2μA
Soft-Power-Down with no RF detector	Sequence of Section 8.5.4 is applied	40μA
Soft-Power-Down	Sequence of Section 8.5.4 is applied	45μA
with RF detector active		

8.5.6 Remote wake-up from SPD

The NF532 may be woken up from a Soft-Power-Down mode when an event occurs on one of the wake-up sources, which has been enabled. There are eight wake-up sources:

- P32_INT0
- P33_INT1
- RF field detected (RF_DETECT)

- HSU wake-up (HSU_ON)
- I^2C wake-up (I^2C_ON)
- SPI wake-up (SPI_ON)
- NFC_WI counters
- GPIRQ: P34, P35, P50_SCL, P71.

When one of these signals is asserted, if its associated enable bit is set (see Table 144), the Power Sequencer begins the wake-up sequence. The wake-up event can only be serviced if the Power Sequencer is in the Stopped state, which means the NF532 is fully entered in Soft-Power-Down mode.

Figure 25 illustrates the wake-up mechanism, with an event on P33_INT1 as an example. CPU_CLK is active T1 after the falling edge of P33_INT1 and the NF532 is ready. T1 is determined by the choice of crystal oscillator and its layout. For devices such as TAS-3225A, TAS-7 or KSS2F, T1 is a maximum of 2ms. Exit from the Power-down mode is signaled by CPU_PD going low one clock cycle later.

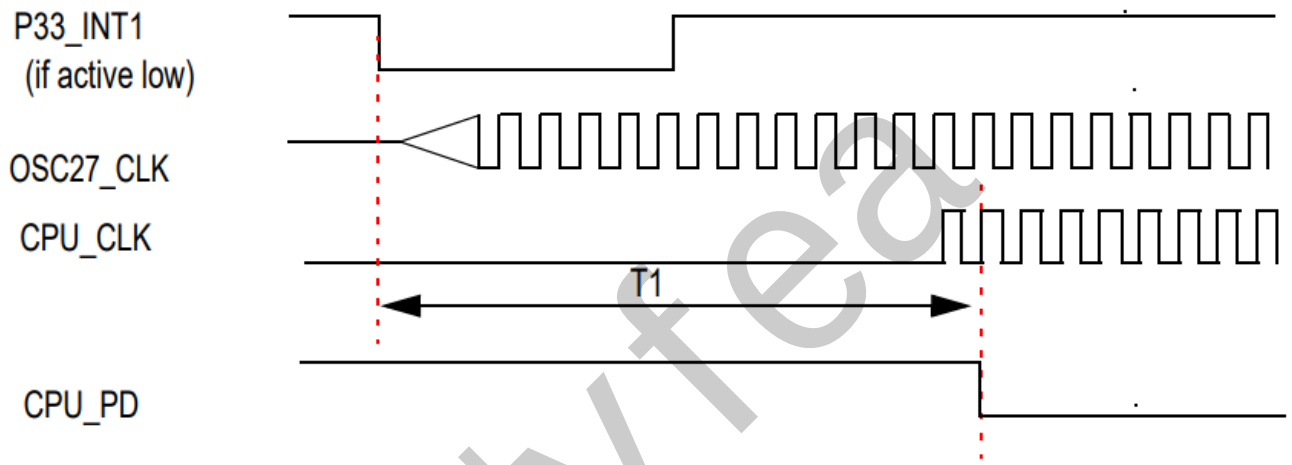


Fig 25. Remote wake-up from Power-down with P33 as wake-up source

8.5.7 PCR extension registers

The PCR is controlled via multiple registers given in Table 132:

Table 132. PCR registers

Name	Size [bytes]	Address offset	Description	Reset	R/W
CFR	1	6200h	Clock Frequency Register	02	R/W
CER	1	6201h	Clock Enable Register	0E	R/W
ILR	1	6202h	Interrupt Level Register	40	R/W
Control	1	6203h	Control	C0	R/W
Status	1	6204h	Status	00	R
Wakeupen	1	6205h	Wake-up Enable	00	R/W

8.5.8 PCR register description

8.5.8.1 CFR register

The Clock Frequency Register serves to choose the frequency of the CPU and its associated peripherals. The clock frequency may be changed dynamically by writing to this register at any time.

Table 133. PCR CFR register- (address 6200h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	cpu_fr	eq[1:0]
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R/W	R/W

Table 134. Description of PCR CFR bits

Bit	Symbol	Description	
7 to 2	-	Reserved	
1 to 0	cpu_frq[1:0]	Select CPU cloc	k frequency.
		cpu_frq[1:0]	**CPU clock frequency**
		00	27.12 MHz
		01	13.56 MHz
		10	6.78 MHz
		11	27.12 MHz

8.5.8.2 CER register

The Clock Enable Register serves to enable or disable the clock of the HSU (frequency is fixed at 27.12 MHz). The clock may be switched on or off at any time.

Table 135. PCR CER register (address 6201h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	hsu_enable	-	-	-
Reset	0	0	0	0	1	1	1	0
Access	R	R	R	R	R/W	R	R	R

Table 136. Description of PCR CER bits

Bit	Symbol	Description
7 to 4	-	Reserved.
3	hsu_enable	**Enable HSU clock.** When 1, HSU is enabled. When 0, HSU is disabled.
2 to 0	-	Reserved.

8.5.8.3 ILR register

The Interrupt Level Register serves to program the level of the external interrupts. Firmware can write to this register at any time.

Table 137. PCR ILR register (address 6202h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	porpulse_	-	enable_pdselif	-	gpirq_level	int1_level	int0_level
		latched						
Reset	0	1	0	0	0	0	0	0
Access	R	R/W	R	R/W	R	R/W	R/W	R/W

Table 138. Description of PCR ILR bits

Bit	Symbol	Description
7	-	Reserved
6	porpulse_latched	**Indicates that a reset has been generated.** When this bit is set to 1, indicates that the system has been reset. The firmware can write a “0” during the firmware reset sequence.
5	-	Reserved

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Bit	Symbol	Description
4	enable_pdselif	**Indicates that a reset has been generated. When this bit is set to 1, P33_INT1 directly controls state of host interface pins:** • If P33_INT1 is set to 1, host interface output pins are driven in accordance with selected interface protocol • If P33_INT1 is cleared to 0, host interface output pins are set into high-impedance state When this bit is cleared to 0, P33_INT1 does not control host interface pins. Their state is determined by selected interface protocol.
		enable_pdselif **P33_INT1** **State of host interface pins**
		0 x Active
		1 0 High Impedance
		1 1 Active
3	-	Reserved.
2	gpirq_level	**Selects gpirq interrupt level.** When this bit is set to 1, wake-up condition is true when gpirq is high. When this bit is cleared to 0, wake-up condition is true when gpirq is low.
1	int1_level	**Selects P33_INT1 interrupt level.** When this bit is set to 1, wake-up condition is true when P33_INT1 is low. When this bit is cleared to 0, wake-up condition is true when P33_INT1 is high.
0	int0_level	**Selects P32_INT0 interrupt level.** When this bit is set to 1, wake-up condition is true when P32_INT0 is high.
		When this bit is cleared to 0, wake-up condition is true when P32_INT0 is low.

8.5.8.4 PCR Control register

The Control register serves to carry out a firmware reset and clear wake-up conditions in the Status register.

Table 139. PCR Control register (address 6203h) bit allocation

Bit	7	6	5	4	3	2 1	0
Symbol	-	-	-	-	-	- clear_wakeup_cond	soft_reset
Reset	1	1	0	0	0	0 0	0
Access	R	R	R	R	R	R R/W	R/W

Table 140. Description of PCR Control bits

Bit	Symbol	Description
7 to 2	-	Reserved.
1	clear_wakeup_cond	**Clears value of wakeupcond in Status register.** When set to 1, wake-up conditions stored in PCR Status register are set to 0. Bit is cleared to 0 automatically by hardware.
0	soft_reset	**Initiates a firmware reset.** When this bit is set to 1, system goes into firmware reset mode. Bit is cleared to 0 automatically by hardware after performing firmware reset sequence.

8.5.8.5 PCR Status register

The PCR Status register stores the logic state of the 8 wake-up events, reported within 7 flags.

Remark: The following status bits are not masked by the associated enable bit of the PCR Wakeupen register (see Table 143). But if not enabled, the event does not wake-up the NF532.

Remark: Be careful when handling the status register, not all the status events are latched. Consequently it be possible that the status register does not show any wake-up event when reading this register after wake-up.

Remark: There is no priority management. More than one wake-up event may be signalled in the register. Consequently it may not be possible to detect the source of the wake-up event by reading this register.

Table 141. PCR Status register (address 6204h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	i²c_wu	gpirq_wu	SPI_wu	HSU_wu	CIU_wu	-	int1_wu	int0_wu
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

An event on a given wake-up condition is flagged by a 1 in the associated bit field.

Table 142. Description of PCR Status bits

Bit	Symbol	Description
7	i²c_wu	**I²C wake-up event (own address)**. Set to 1 when NF532 wakes because its own I²C address is detected.[1]
6	gpirq_wu	**GPIRQ wake-up event**. Set to 1 when NF532 wakes from a GPIRQ event (GPIRQ at 0).[2]
5	SPI_wu	**SPI wake-up event**. Set to 1 when NF532 wakes from an SPI event (NSS at 0).[2]
4	HSU_wu	**HSU wake-up event**. Set to 1 when NF532 wakes from an HSU event (five rising edges on HSU_RX).[1]
3	CIU_wu	**Contactless wake-up event**. Set to 1 when NF532 wakes from an RF-detect or NFC-WI contactless event.[1][2]
2	-	Reserved.
1	int1_wu	**P33_INT1 wake-up event**. Set to 1 when the system wakes from a P33_INT1 interrupt.[2]
0	int0_wu	**P32_INT0 wake-up event**. Set to 1 when the system wakes from a P32_INT0 interrupt.[2]

[1] This wake-up event is latched. Firmware must clear the status after reading it by writing 1 to clear_wakeup_cond in PCR Control.

[2] This event is not latched while no CPU clock is available; the status reflects the event only if it remains active until the CPU clock is accessible.

8.5.8.6 PCR Wakeupen register

Register Wakeupen enables the selection of various wake-up events.

Table 143. PCR Wakeupen register (address 6205h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	i²c_wu_	GPIRQ_	SPI_on_	HSU_on_	CIU_wu_	-	int1_en	int0_en
	en	wu_en	en	en	en			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Table 144. Description of PCR Wakeupen bits

Bit	Symbol	Description
7	i²c_wu_en	**I²C wake-up enable**. Setting this bit to 1 allows an I²C event—specifically recognition of the device's own address—to wake the NF532. See Table 90 for the corresponding event enable.
6	GPIRQ_wu_en	**General-purpose IRQ wake-up enable**. When this bit is 1, a GPIRQ event can wake the NF532.
5	SPI_on_en	**SPI wake-up enable**. When this bit is 1, an SPI event can wake the NF532.
4	HSU_on_en	**HSU wake-up enable**. When this bit is 1, an HSU event can wake the NF532. See Table 114 for the corresponding event enable.
3	CIU_wu_en	**Contactless Interface Unit wake-up enable**. Setting this bit to 1 allows an RF-detection or NFC-WI event from the CIU to wake the NF532.

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Bit	Symbol	Description
2	-	Reserved.
1	int1_en	**P33_INT1 wake-up enable.** When this bit is 1, an event on P33_INT1 can wake the NF532.
0	int0_en	**P32_INT0 wake-up enable.** When this bit is 1, an event on P32_INT0 can wake the NF532.

8.6 Contactless Interface Unit (CIU)

The NF532 CIU is a modem for contactless communication at 13.56 MHz. It supports 6 various operating states

- ISO/IEC 14443A/MIFARE Reader/Writer.
- FeliCa Reader/Writer.
- ISO/IEC 14443B Reader/Writer
- ISO/IEC 14443A/MIFARE Card 1K or MIFARE 4K card emulation mode
- FeliCa Card emulation
- ISO/IEC 18092, ECMA 340 NFCIP-1 Peer-to-Peer

The CIU implements a demodulator and decoder for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The CIU handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The CIU supports MIFARE Classic 1K or MIFARE Classic 4K card emulation mode. The CIU supports contactless communication by means of MIFARE Higher data rates up to 424 kbit/s in both directions.

The CIU can demodulate and decode FeliCa coded signals. The CIU digital part handles the FeliCa framing and error detection. The CIU supports contactless communication by means of FeliCa Higher data rates up to 424 kbit/s in both directions.

The CIU supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision which must be implemented in firmware as well as upper layers.

In card emulation mode, the CIU is able to answer to a Reader/Writer command either in accordance with the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The CIU produces the load modulation signals, either from its transmitter or from the LOADMOD pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC through the NFC-WI/S^2 C interface.

Compliant to ECMA 340 and ISO/IEC 18092 NFCIP-1 Passive and Active communication modes, the CIU offers the possibility to communicate to another NFCIP-1 compliant device, at data rates up to 424 kbit/s. The CIU handles the complete NFCIP-1 framing and error detection.

The CIU transceiver may be connected with an external antenna for Reader/Writer or Card/PICC modes, without any additional active component.

8.6.1 Feature list

- Frequently accessed registers placed in SFR space
- Highly integrated analog circuitry to demodulate and decode incoming data
- Buffered transmitter drivers to minimize external components to connect an antenna.
- Integrated RF level detector
- Integrated data mode detector

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- Typical operating distance of 50 mm in ISO/IEC 14443A/MIFARE or FeliCa in Reader/Writer mode depending on the antenna size, tuning and power supply
- Typical operating distance of 50 mm in NFCIP-1 mode depending on the antenna size, tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE card or FeliCa card operation mode of about 100 mm depending on the antenna size, tuning and the external field strength
- Supports MIFARE Classic 1K or MIFARE Classic 4K encryption in Reader/Writer mode
- Supports MIFARE higher data rate at 212 kbit/s and 424 kbit/s
- Supports contactless communication in accordance with the FeliCa scheme at 212 kbit/s and 424 kbit/s
- Support of the NFC-WI/S^2 C interface
- 64 byte send and receive FIFO-buffer
- Programmable timer
- CRC Co-processor
- Internal self test and antenna presence detector
- 2 interrupt sources
- Adjustable parameters to optimize the transceiver carry outance in accordance with the antenna characteristics

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8.6.2 Simplified block diagram

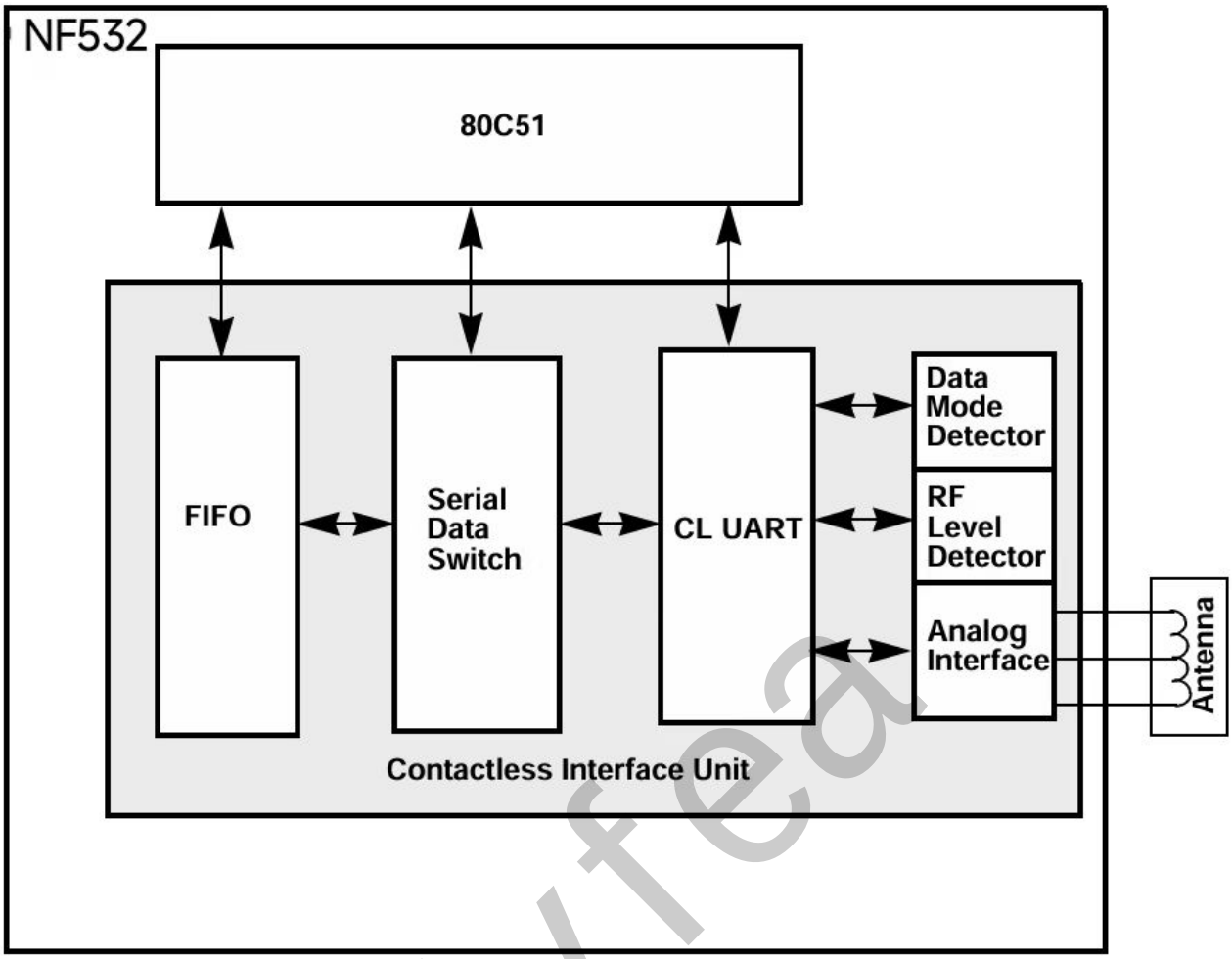


Fig 26. Simplify Contactless Interface Unit (CIU) block diagram

The Analog Interface handles the modulation and demodulation of the analog signals in accordance with the Card emulation mode, Reader/Writer mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The data mode detector detects a ISO/IEC 14443-A MIFARE, FeliCa or NFCIP-1 mode to prepare the internal receiver to demodulate signals, which are sent to the NF532.

The NFC-WI/S^2 C interface supports communication to secure IC. It also supports digital signals for data rates above 424 kbit/s.

The CL UART handles the protocol requirements for the communication schemes in co-operation with the appropriate firmware. The FIFO buffer allows a convenient data transfer from the 80C51 to the CIU and vice versa.

8.6.3 Reader/Writer modes

All showd modulation indices and modes in this chapter are system parameters. Consequently, beside the IC settings a suitable antenna tuning is needed to achieve the optimal carry outance.

8.6.3.1 ISO/IEC 14443A Reader/Writer

The diagram below summarizes the communication on a physical level, the communication overview in the Table 145 summarizes the physical parameters.

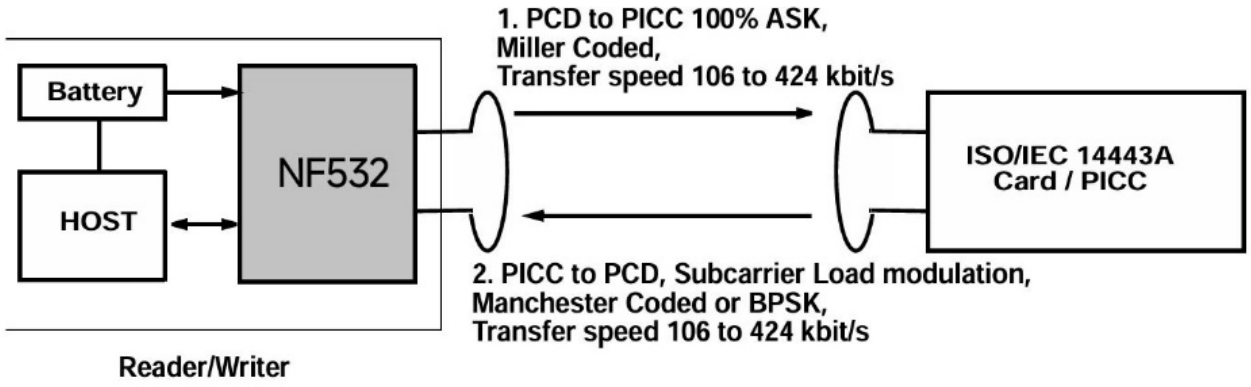


Fig 27. ISO/IEC 14443A/MIFARE Reader/Writer communication diagram

Table 145. Communication overview for ISO/IEC 14443A/MIFARE Reader/Writer

Communicatio	n scheme	ISO/IEC 14443A MIFARE	MIFARE Higher Bau	d Rate
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		128 ---------- 944s ≈	64 ---------- 472s ≈	32 ---------- 236s ≈
		13,56MHz _,_μ	13,56MHz _,_μ	13,56MHz _,_μ
NF532 to	Modulation	100% ASK	100% ASK	100% ASK
PICC/Card	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PICC/Card to NF532	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	Manchester coding	BPSK	BPSK

The internal CRC co-processor calculates the CRC value according the data coding and framing specified in the ISO/IEC 14443A part 3, and handles parity generation internally in accordance with the data rate.

With appropriate firmware, the NF532 can handle the complete ISO/IEC 14443A/MIFARE protocol.

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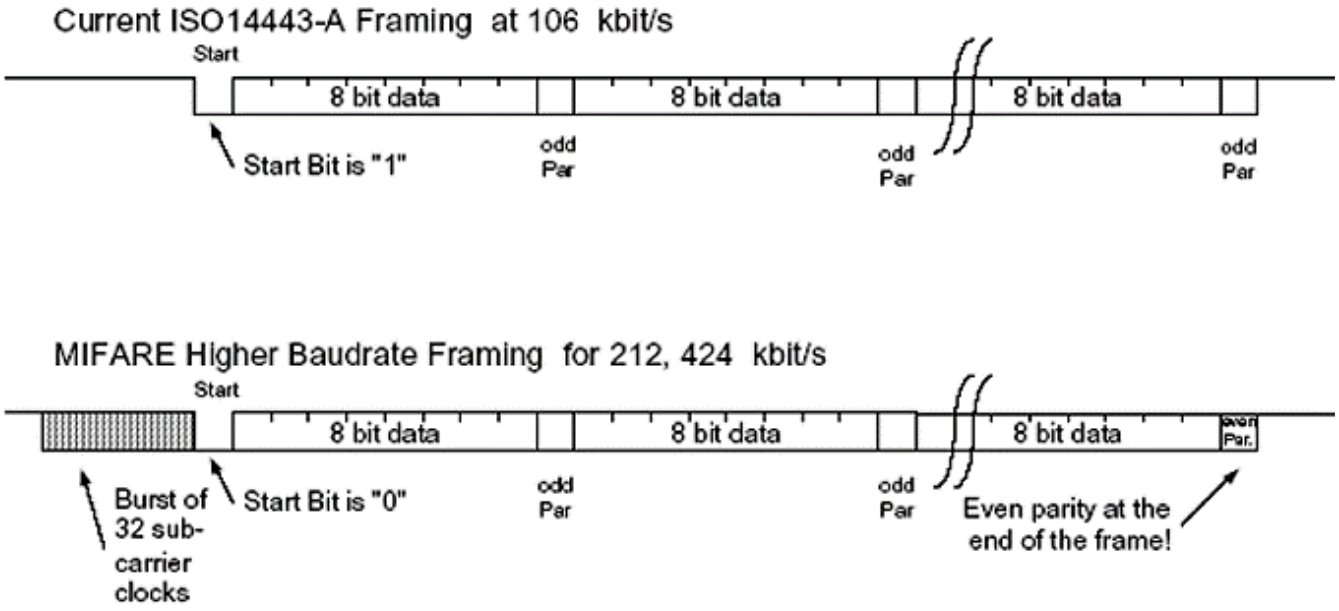


Fig 28. Data coding and framing according to ISO/IEC 14443A

8.6.3.2 FeliCa Reader/Writer

The diagram below summarizes the communication at the physical level. Table 146 summarizes the physical parameters.

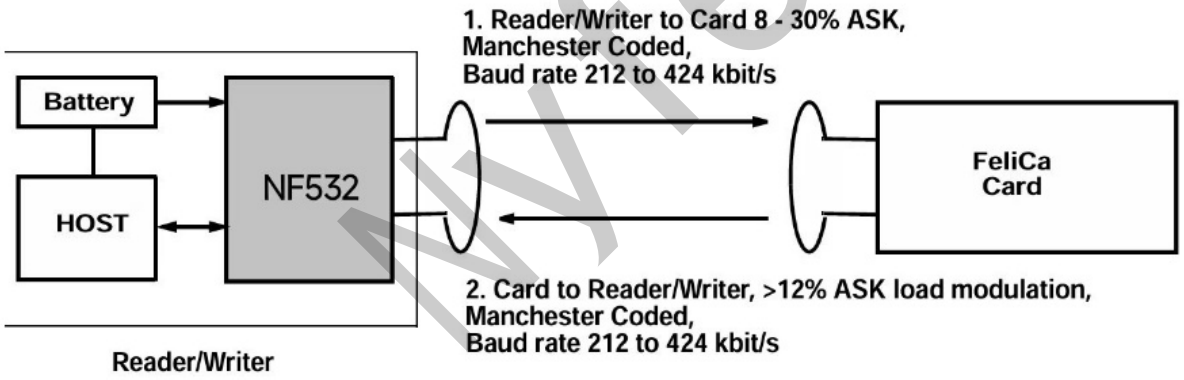


Fig 29. FeliCa Reader/Writer communication diagram

Table 146. Communication overview for FeliCa Reader/Writer

Communication	scheme	FeliCa	FeliCa higher baud rate
Baud rate		212 kbit/s	424 kbit/s
Bit length		64 ---------- 472s ≈	32 ---------- 236s ≈
		13,56MHz _, _µ	13,56MHz _, _µ
NF532 to	Modulation	8 - 30% ASK	8 - 30% ASK
PICC/Card	Bit coding	Manchester coding	Manchester coding
PICC/Card to	Modulation	>12% ASK	>12% ASK
NF532	Bit coding	Manchester coding	Manchester coding

With appropriate firmware, the NF532 can handle the FeliCa protocol.

The FeliCa Framing and coding must comply with the next table:

Table 147. FeliCa Framing and Coding

Preamble	SYNC	LEN	n-Data	CRC
00h 00h 00h 00h 00h 00h	B2h 4Dh			

To enable the FeliCa communication a 6-byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2-byte SYNC bytes (B2h, 4Dh) are sent to synchronize the receiver.

The following LEN byte reports the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done in accordance with the FeliCa definitions with the MSB first.

To send data on the RF interface, the 80C51 has to send the LEN and data bytes to the CIU. The Preamble and SYNC bytes are produced by the CIU automatically and must not be written to the FIFO. The CIU carries out internally the CRC calculation and adds the result to the frame.

The starting value for the CRC Polynomial is 2 null bytes: (00h), (00h)

Example of frame:

Table 148. FeliCa framing and coding

Preamble					SYNC		LEN	2 Data	Bytes	CRC	
00 00	00	00	00	00	B2	4D	03	AB	CD	90	35

8.6.3.3 ISO/IEC 14443B Reader/Writer

The CIU supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision which must be implemented in firmware as well as upper layers.

The diagram below summarizes the communication at the physical level. Table 149 summarizes the physical parameters.

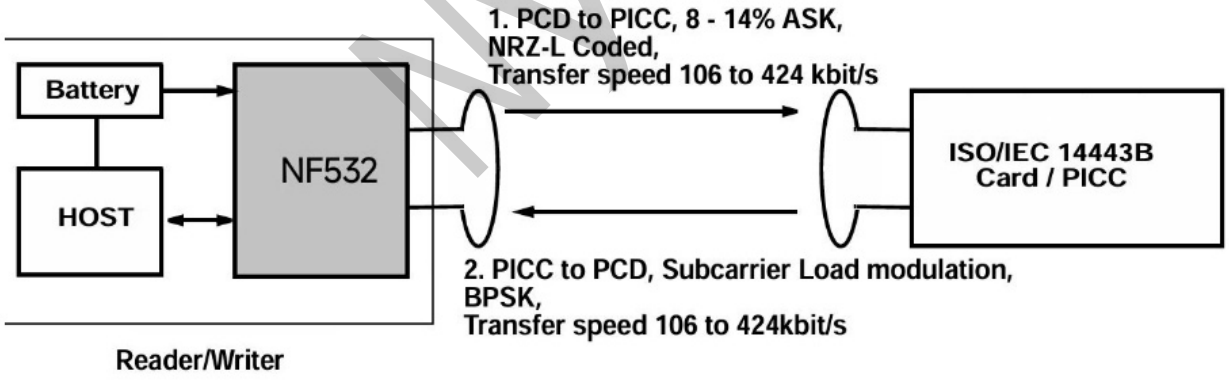


Fig 30. ISO/IEC 14443B Reader/Writer communication diagram

With appropriate firmware, the NF532 can handle the ISO/IEC 14443B protocol.

Table 149. Communication overview for ISO/IEC 14443B Reader/Writer

Communicatio	n scheme	ISO/IEC 14443B	Type B higher baud	rate
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		128 ———————————— 944s ≈	64 ———————————— 472s ≈	32 ———————————— 236s ≈
		13,56MHz _, _μ	13,56MHz _, _μ	13,56MHz _, _μ

Communicatio	n scheme	ISO/IEC 14443B	Type B higher baud	rate
NF532 to	Modulation	8 -14% ASK	8 -14% ASK	8 -14% ASK
PICC/Card	Bit coding	NRZ-L	NRZ-L	NRZ-L
PICC/Card to NF532	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	BPSK	BPSK	BPSK

8.6.4 ISO/IEC 18092, ECMA 340 NFCIP-1 operating mode

A NFCIP-1 communication takes place between 2 devices:

- Initiator: produces RF field at 13.56 MHz and begins the NFCIP-1 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or with a self produced and self modulated RF field for Active Communication mode.

The NFCIP-1 communication variousiates between Active and Passive communication modes.

- Active Communication mode means both the initiator and the target are through their own RF field to send data
- Passive Communication mode means that the Target answers to an Initiator command in a load modulation scheme. The Initiator is active in terms of generating the RF field.

To fully support the NFCIP-1 standard the NF532 supports the Active and Passive Communications mode at the data rates 106 kbit/s, 212 kbit/s and 424 kbit/s as specified in the NFCIP-1 standard

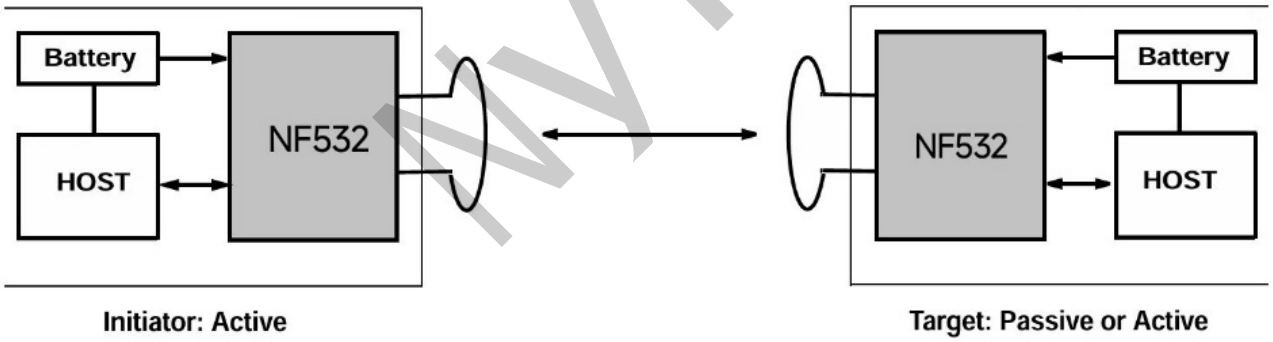


Fig 31. NFCIP-1 mode

With appropriate firmware, the NF532 can handle the NFCIP-1 protocol, for all communication modes and data rates, for both Initiator and Target.

8.6.4.1 ACTIVE Communication mode

Active Communication Mode means both the Initiator and the Target are through their own RF field to send data.

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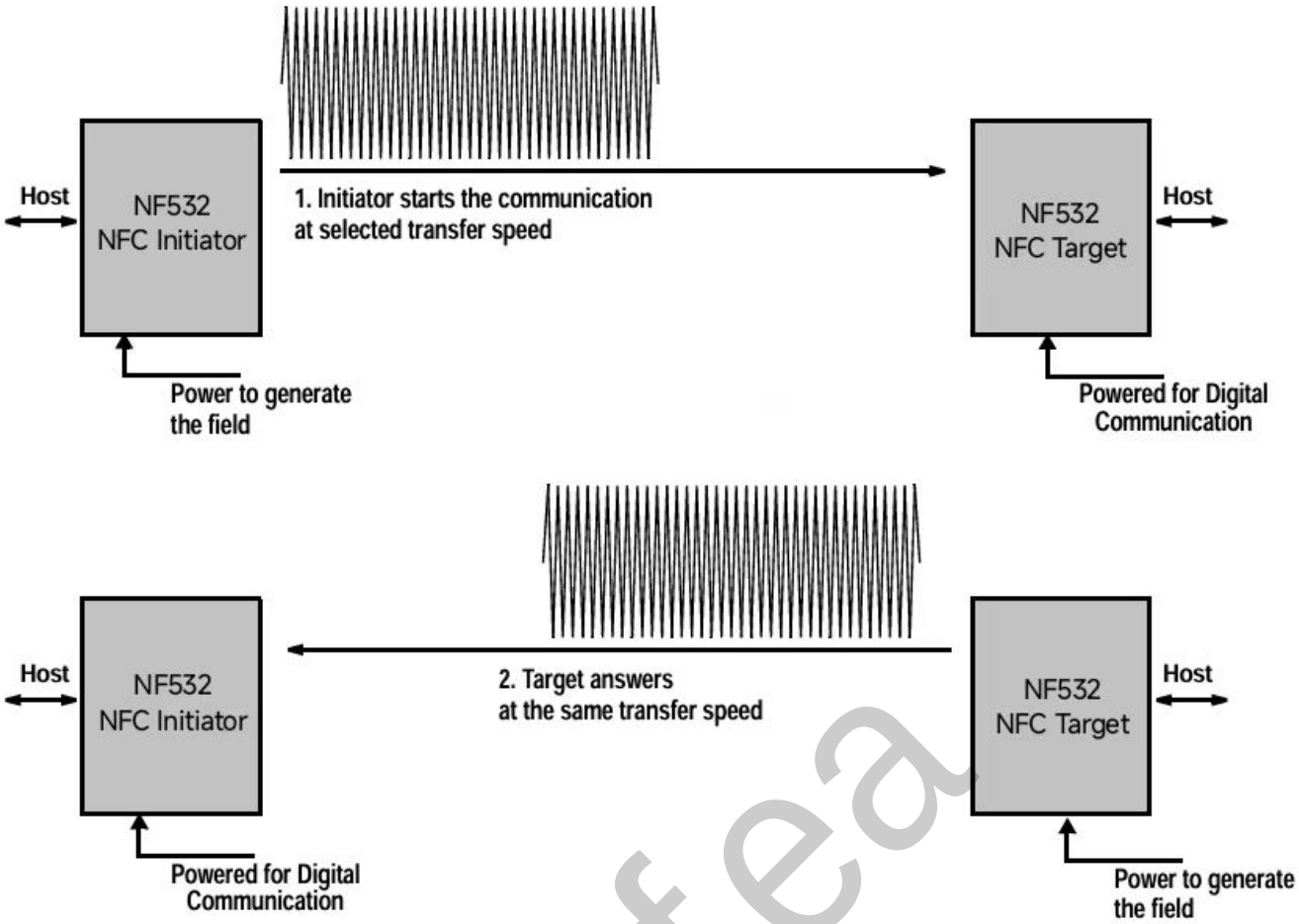


Fig 32. Active NFC mode

The table below gives an overview of the active communication modes:

Table 150. Communication overview for NFC Active Communication mode

Communication	scheme	ISO/IEC 18092, ECM	A 340, NFCIP-1	
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		128 944s ≈	64 472s ≈	32 236s ≈
		13,56MHz _, _μ	13,56MHz _, _μ	13,56MHz _, _μ
Initiator to Target	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded
Target to Initiator	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded

8.6.4.2 PASSIVE Communication mode

Passive Communication Mode means that the target answers to an Initiator command in a load modulation scheme.

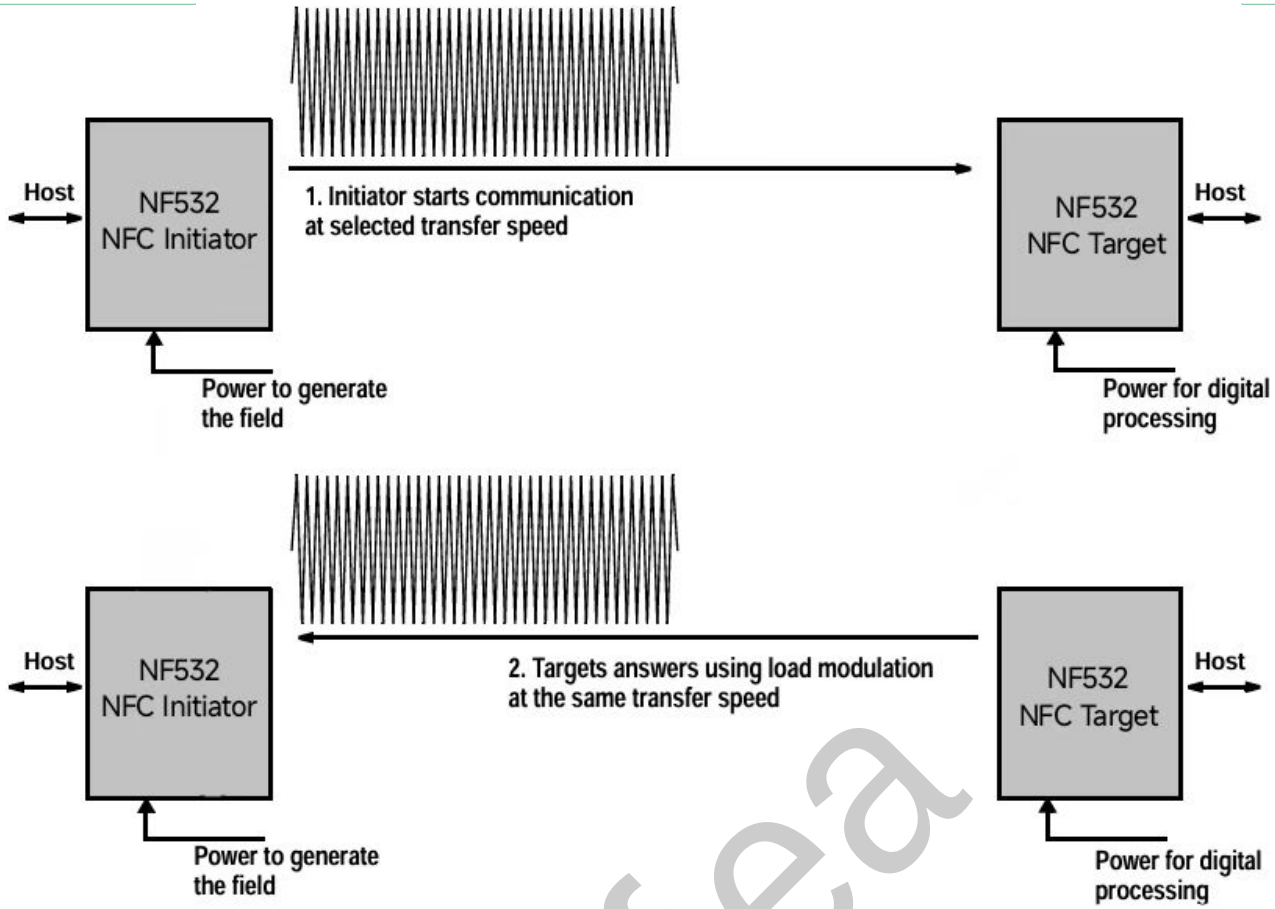


Fig 33. Passive NFC mode

The table below gives an overview of the active communication modes:

Table 151. Communication overview for NFC Passive Communication mode

Communicatio	n scheme	ISO/IEC 18092, ECM	A 340, NFCIP-1	
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		128 944s ≈	64 472s ≈	32 236s ≈
		13,56MHz _, _μ	13,56MHz _, _μ	13,56MHz _, _μ
NF532 to	Modulation	100% ASK	100% ASK	100% ASK
PICC/Card	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PICC/Card to NF532	Modulation	Subcarrier load modulation	>12% ASK	>12% ASK
	Subcarrier frequency	13.56 MHz/16	No subcarrier	No subcarrier
	Bit coding	Manchester coding	Manchester coding	Manchester coding

8.6.4.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are specified in the NFCIP-1 standard: ISO/IEC 18092 or ECMA 340.

8.6.4.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely specified in this document. For detailed explanation of the protocol refer to the ISO/IEC 18092 / ECMA340 NFCIP-1 standard. Nevertheless the datalink layer is in accordance with the next policy:

- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction.
- Speed should not be changed during a data transfer

In order not to disturb current infrastructure based on 13.56 MHz general rules to start NFC communication are specified in the next way:

- Per default NFCIP-1 device is in target mode, meaning its RF field is switched off.
- The RF level detector is active.
- Only if application needs the NFCIP-1 device shall switch to Initiator mode.
- Initiator shall only switch on its RF field if no external RF field is detected by RF Level detector during a time of TIDT.
- The initiator carries out initialization in accordance with the selected mode.

8.6.5 Card operating modes

The NF532 may be addressed like a FeliCa or ISO/IEC 14443A/MIFARE card. Consequently, the NF532 can produce an answer in a load modulation scheme in accordance with the ISO/IEC 14443A/MIFARE or FeliCa interface description.

Remark: The NF532 does not support a secure storage of data. This has to be handled by a dedicated secure IC or a host. The secure IC is optional.

Remark: The NF532 can not be powered by the field in this mode and needs a power supply.

8.6.5.1 ISO/IEC 14443A/MIFARE card operating mode

With appropriate firmware, the NF532 can handle the ISO/IEC 14443A including the level 4, and the MIFARE protocols.

The diagram below summarizes the communication at the physical level. Table 152 summarizes the physical parameters.

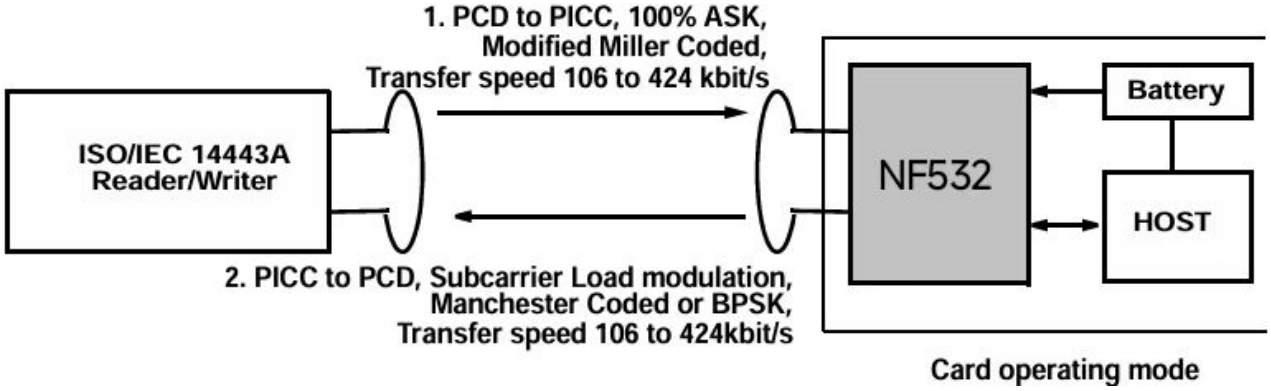


Fig 34. ISO/IEC 14443A/MIFARE card operating mode communication diagram

Table 152. Communication overview for ISO/IEC 14443A/MIFARE Card operating mode

Communicatio	n scheme	ISO/IEC 14443A MIFARE	MIFARE higher bau	d rate
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		128 _____ 944s ≈	64 _____ 472s ≈	32 _____ 236s ≈
		13,56MHz _,_μ	13,56MHz _,_μ	13,56MHz _,_μ
Reader/Writer	Modulation	100% ASK	100% ASK	100% ASK
to NF532	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
NF532 to Reader/Writer	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	Manchester coding	BPSK	BPSK

8.6.5.2 FeliCa Card operating mode

With appropriate firmware, the NF532 can handle the FeliCa protocol.

The diagram below summarizes the communication at the physical level. Table 153 summarizes the physical parameters.

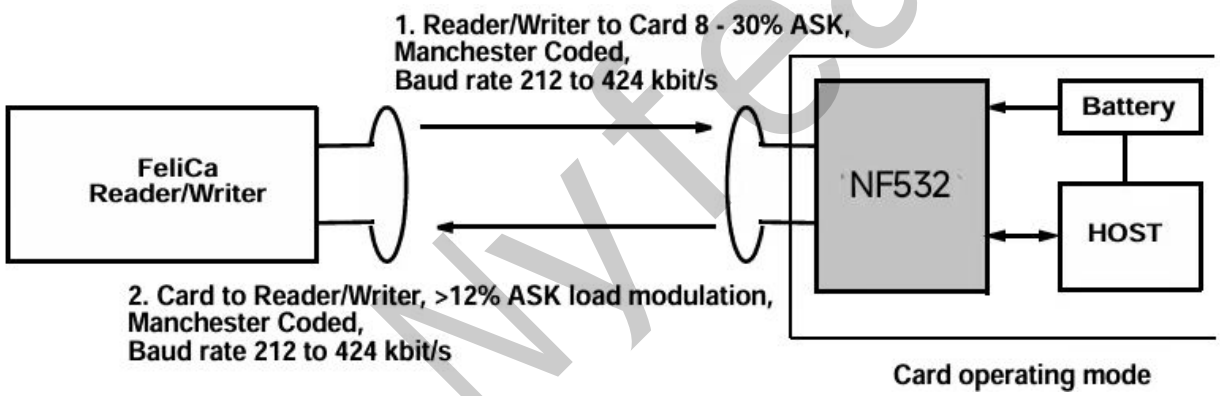


Fig 35. FeliCa card operating mode communication diagram

Table 153. Communication overview for FeliCa Card operating mode

Communication s	cheme	FeliCa	FeliCa higher baud rate
Baud rate		212 kbit/s	424 kbit/s
Bit length		64 _____ 472s ≈	32 _____ 236s ≈
		13,56MHz _,_μ	13,56MHz _,_μ
Reader/Writer to	Modulation	8 - 30% ASK	8 - 30% ASK
NF532	Bit coding	Manchester coding	Manchester coding
NF532 to	Modulation	>12% ASK	>12% ASK
Reader/Writer	Bit coding	Manchester coding	Manchester coding

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8.6.6 Overall CIU block diagram

The NF532 supports various contactless communication modes. The CIU supports the internal 80C51 for the various selected communication schemes such as Card Operation mode, Reader/Writer Operating mode or NFCIP-1 mode up to 424 kbit/s. The CIU produces bit- and byte-oriented framing and handles error detection in accordance with these various contactless protocols.

Higher data rates up to 3.39 Mbit/s may be handled by the digital part of the CIU. To modulate and demodulate the data an external circuit has to be connected with the communication interface pins SIGIN/SIGOUT.

Remark: The size and tuning of the antenna have an important impact on the achievable operating distance.

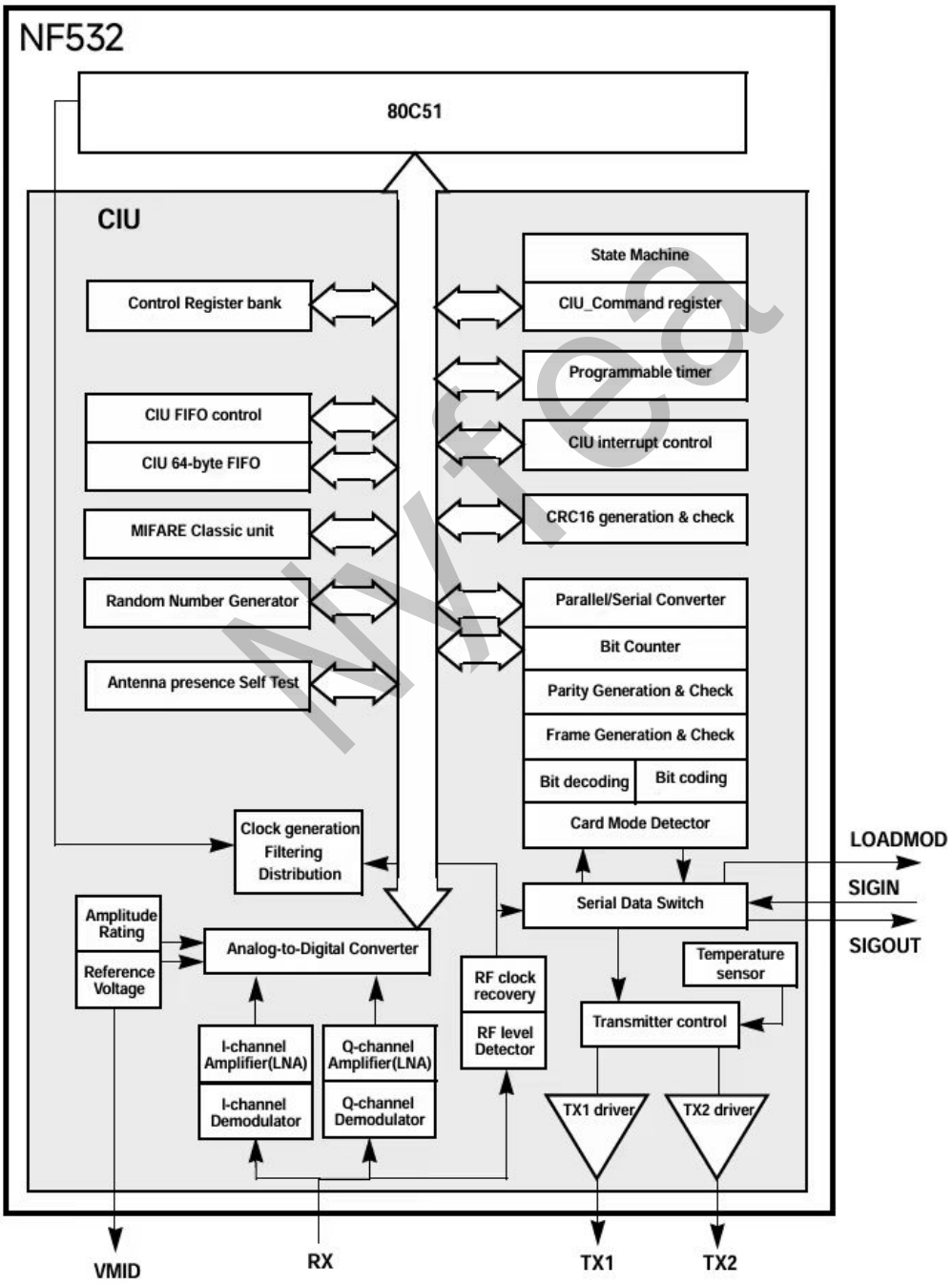


Fig 36. CIU detailed block diagram

8.6.7 Transmitter control

The signals delivered by the transmitter are on pins TX1 and pin TX2. The supply and grounds of the transmitter drivers are TVDD, TVSS1 and TVSS2.

The signals delivered are the 13.56 MHz energy carrier modulated by an envelope signal. It may be used to drive an antenna directly, with a few passive components for matching and filtering, see Section 13 “Application information”. The signals on TX1 and TX2 may be configured by the register CIU_TxControl, see Table 212.

The modulation index may be set by adjusting the impedance of the drivers. The impedance of the p-driver may be configured by the registers CIU_CWGsP and CIU_ModGsP. The impedance of the n-driver may be configured by the registers CIU_GsNOn and CIU_GsNOff. Furthermore, the modulation index is determined by the antenna design and tuning.

Remark: It is recommended that the design use a modulation index in the range of 8% for the FeliCa and NFCIP-1 communication scheme at 212 and 424 kbit/s.

The registers CIU_TxMode and CIU_TxAuto control the data rate and framing during the transmission and the setting of the antenna driver to support the various requirements at the various modes and data rates.

In the next tables, these abbreviations are employed:

- RF: 13. 56 MHz clock derived from 27.12 MHz quartz divided by 2
- RF_n: inverted 13.56 MHz clock
- GsPMos: Conductance of the transmitter PMOS
- GsNMos: Conductance of the transmitter NMOS
- CWGsP: PMOS conductance value for Continuous Wave (see Table 249)
- ModGsP: refers to ModGsP[5:0], PMOS conductance value for Modulation (see Table 250)
- CWGsNOn: refers to CWGsP[5:0], NMOS conductance value for Continuous Wave (see Table 247)
- ModGsNOn: NMOS conductance value for Modulation when generating RF field (see Table 247)
- CWGsNOff: NMOS conductance value for Continuous Wave when no RF is produced by the NF532 itself (see Table 239)
- ModGsNOff: NMOS conductance value for modulation when load Modulation (see Table 239)

Remark: If only 1 driver is switched on, the settings for ModGsNOn and CWGsNOn are intended for both drivers.

Table 154. Settings for TX1

TX1 RFEn	Force 100ASK	In-vTx1 RFON	In-vTx1 RFOFF	Envel-ope	TX1	GsP-Mos	GsNMos	Remarks
0	X	X	0	0	0		ModGs-NOff	If TX1RFEN is cleared to 0, the pin TX1 is cleared to 0 or 1 depending on
				1	0		CWGsNOff	InvTx1RFOFF. The bit Force 100ASK has no effect. Envelope modulates the transconductance value
			1	0	1	ModG-sP		.
				1	1	CWGsP		

TX1 RFEn	Force 100ASK	In - vTx1 RFON	In - vTx1 RFOFF	Envel - ope	TX1	GsP - Mos	GsNMos	Remarks
1	0	0	X	0 1	RF RF	ModG - sP CWGsP	ModGsNON CWGsNON	If TX1RFEN is set to 1, the RF phase of TX1 is depending on InvTx1RFON. The bit Force100ASK has effect; when Envelope is set to loic 0 TX1 is ulled to round
	0	1	X	0	RF_n	ModG - sP	ModGsNON	g , p g.
				1	RF_n	CWGsP	CWGsNON	
	1	0	X	0	0		ModGsNON	
				1	RF	CWGsP	CWGsNON	
	1	1	X	0	0		ModGsNON	
				1	RF_n	CWGsP	CWGsNON	

1 1 X Table 155. Settings for TX2 TX2 Force TX2CW RFEn 100ASK 0 X 0 X

TX2 RFEn	Force 100ASK	TX2CW	In - VTx2 RFON	In - vTx2 RFOFF	Envel - ope	TX2	GsP - Mos	GsNMos	Remarks
0	X	0	X	0	0 1	0 0		ModGs - NOff CWGsNOff	If Tx2RFEn is cleared to 0, the pin TX2 is forced to 0 or 1 depending on the InvTx2RFOFF bit. The bit ForceASK100 has no effect. The signal Enveloe modulates the transconductance value
				1	0	1	ModG - sP		p
					1	1	CWGsP		
		1	X	0	0 1	0 0		CWGsNOff CWGsNOff	When Tx2CW bit is set, the transconductance values are al - ways CWGsP or CWGsNOff
				1	0	1	CWGsP		
					1	1	CWGsP		

Table 155. Settings for TX2 …continued

TX2 RFEn	Force 100ASK	TX2CW	In - VTx2 RFON	In - vTx2 RFOFF	Envel - ope	TX2	GsP - Mos	GsNMos	Remarks
1	0	0	0	X	0	RF	ModG - sP	ModGsNOn	When TX2RFEn is set to 1 and Force100ASK cleared to 0, the
					1	RF	CWGsP	CWGsNOn	phase of TX2 is depending on InvTx2RFON. If Tx2CW bit is set to loic 1 the transconductance values are alwas CWGsP or
			1	X	0	RF_n	ModG - sP	ModGsNOn	g , y CWGsNOn, independent of Envelope.
					1	RF_n	CWGsP	CWGsNOn	
		1	0	X	X	RF	CWGsP	CWGsNOn	
			1	X	X	RF_n	CWGsP	CWGsNOn	
	1	0	0	X	0 1	0 RF	CWGsP	ModGs - NOn CWGsNOn	If TX2RFEn is set to 1 and TX2CW to 0, the bit Force100ASK has effect; when Envelope is cleared to 0, TX2 is pulled to ground.
			1	X	0	0		ModGsNOn	
					1	RF_n	CWGsP	CWGsNOn	
		1	0	X	X	RF	CWGsP	CWGsNOn	
			1	X	X	RF_n	CWGsP	CWGsNOn	

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8.6.8 RF level detector

The RF level detector is integrated to fulfill NFCIP-1 protocol requirements (e.g. RF collision avoidance).

Furthermore the RF level detector may be used to wake-up the NF532 and to produce an interrupt.

The sensitivity of the RF level detector is adjustable in a 4-bit range through the bits RFLevel in register CIU_RFCfg (see Table 245). The sensitivity itself is determined by the antenna configuration and tuning.

Possible sensitivity levels at the RX pin are listed below:

Table 156. Setting of the RF level detector

VRx typical [Vpp] CIU Power-Down bit set to logic	CIU_RFCfg setting	CIU_RFCfg setting with additional amplifier
1 0		see Remark
2 1.9	1111b	
1.35 1.3	1110b	
0.95 0.9	1101b	
0.6 0.57	1100b	
0.41 0.40	1011b	
0.28 0.27	1010b	
0.17 0.17	1001b	
0.12 0.12	1000b	1xxx1111b
0.085 -	0111b[1]	1xxx1110b
0.055 -	0110b[1]	1xxx1101b
0.040 -	0101b[1]	1xxx1100b
- -	0100b[1]	1xxx1011b[1]
- -	0011b[1]	1xxx1010b[1]
- -	0010b[1]	1xxx1001b[1]
- -	0001b[1]	1xxx1000b[1]
- -	0000b[1]	1xxx0111b[1]

[1] Due to noise, it is recommended not to use this setting to avoid misleading results.

To increase the sensitivity of the RF level detector an amplifier may be activated by setting the bit RFLevelAmp in register CIU_RFCfg to 1 (see Table 245).

Remark: With typical antenna, lower sensitivity levels without the additional amplifier set (below 1000b) can provoke misleading results because of intrinsic noise in the environment.

Remark: For the same reasons than above, it is recommended to use the RFLevelAmp only with upper RF level settings (above 1001b).

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Remark: During the CIU Power-down mode the additional amplifier of the RF level detector is automatically switched off to ensure that the power usage is minimal.

8.6.9 Antenna presence self test

The goal of the Antenna Presence Self Test is to facilitate at assembly phase the detection of the absence of the antenna and/or antenna matching components. Such a detection is done by mean of measuring the current consumption.

Consequently the functionality is guaranteed within a restricted temperature and supply voltage range:

- VBAT voltage is above 5 V
- Ambient temperature is between 0 and 40 ° C

8.6.9.1 Principle

The principle is explained with typical antenna tuning and matching components.

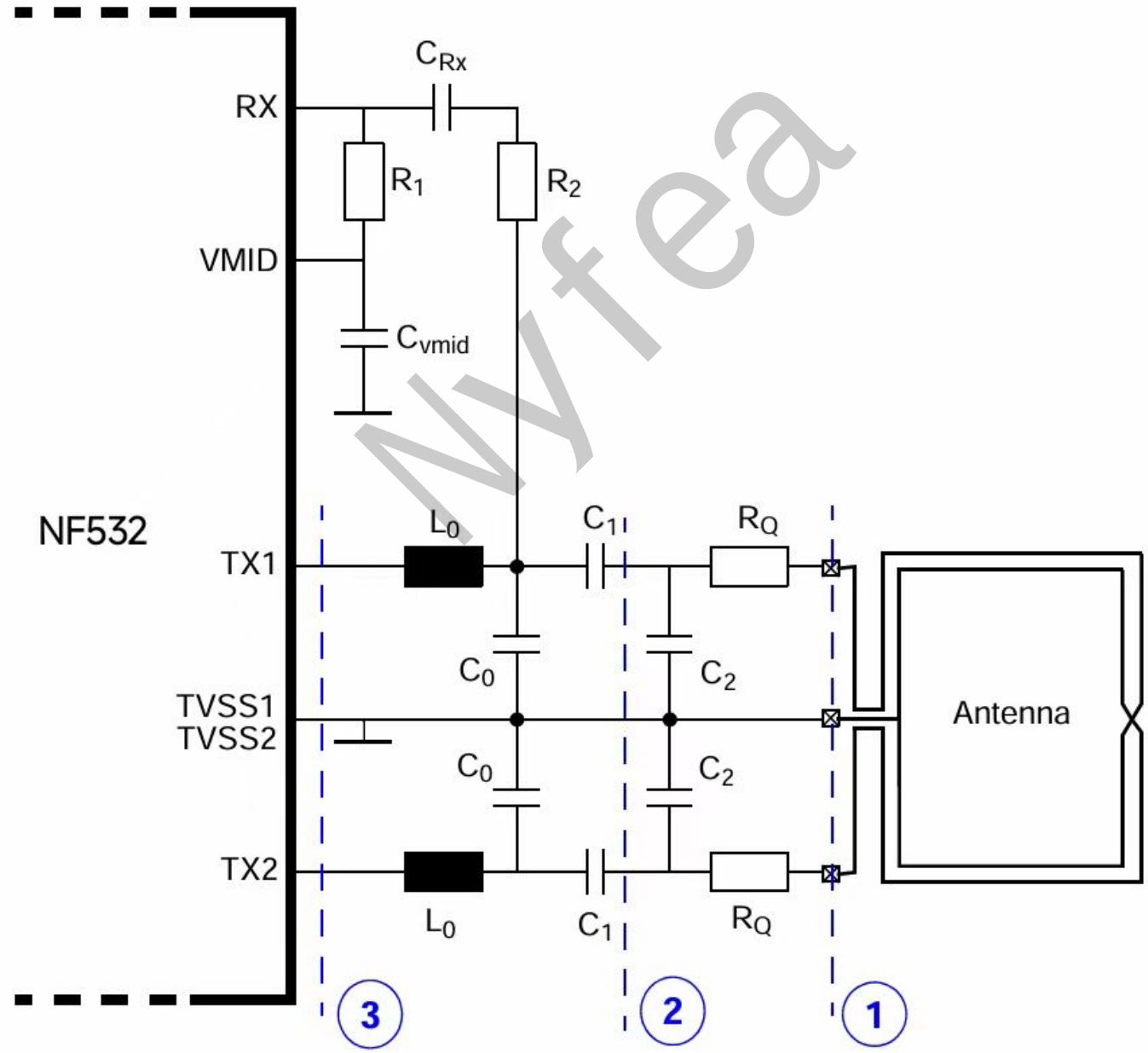


Fig 37. Disconnection localization for the antenna detection

The testing operation may be managed via a dedicated register Table 158 and needs the transmitter to be activated. When activated by asserting bit 0, the detector will monitor the current consumption through the internal low dropout voltage regulator. Any violation to the current limits is reported via bits 7 and 6 of the register.

Several levels of detection may be programmed through the register to offer a large panel of compatibility to various type of antennas. The high current threshold may be programmed from 40 mA to 150 mA with 15 mA steps (total current consumption of the IC). The low current threshold may be programmed from 5mA to 35 mA with 10 mA step (total current consumption of the IC).

There is no dedicated pin for the output of the detector. The result of the detection is to be read out from the antenna test register.

- Cases 1 and 2: If the antenna and/or the tuning network are not connected, the TVDD current exceeds the nominal one. The antenna detector detects this higher consumption and the andet_up bit in andet_control register is set to high
- Case 3: If the EMC filter is not correctly connected, the current within TVDD is below the nominal one. The antenna detector detects this lower consumption and the andet_bot bit in andet_control register is set to high.

For correct operation of this function, the transmitter must generate an RF field in the antenna.

8.6.9.2 Antenna presence detector register

Table 157. andet_control register (address 610Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	andet_bot	andet_up	andet_	ithl[1:0]	an	det_ithh[2	:0]	andet_en
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 158. Description of andet_control bits

Bit	Symbol	Description
7	andet_bot	A too low power consumption has been detected
6	andet_up	A too high power consumption has been detected
5 to 4	andet_ithl[1:0	Set the low current consumption threshold to be detected
		Define the overcurrent threshold
		00: do not use
		01: do not use
		10: 25 mA
		11: 35 mA
3 to 1	andet_ithh[2:0]	Set the high current consumption threshold to be detected 000: 45 mA
		001: 60 mA
		010: 75 mA
		011: 90 mA
		100: 105 mA
		101: 120 mA
		110: 130 mA
		111: 150 mA
0	andet_en	Enable the detection of the antenna presence detector functionality.

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8.6.10 Random generator

The random generator serves to produce various random number needed for the NFCIP-1 protocol, as well as for MIFARE security.

It may also be used for test purpose, by generating random data through the field.

Table 159. Data_rng register (address 6105h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				data_	rng			
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 160. Description of Data_rng bits

Bit	Symbol	Description
7 to 0	data_rng	Random number data register.

The Control_switch_rng register may also be used to control the behavior of the SVDD switch.

Table 161. Control_switch_rng register (address 6106h) bit allocation

Bit	7	6	5	4	3 2	1	0
Symbol	-	hide_svdd_	sic_switch_	sic_switch_	- cpu_need_	random_	-
		sig	overload	en	rng	dataready	
Reset	0	1	0	0	0 0	0	1
Access	R	R/W	R	R/W	R R/W	R/W	R

Table 162. Description of Control_switch_rng bits

Bit	Symbol	Description
7	-	Reserved.
6	hide_svdd_sig	**Configure the internal state of SIGIN and P34 in an idle state.** This bit may be used to avoid spikes on SIGIN and P34 when the SVDD switch becomes enabled or disabled. When this bit is cleared to 0, the internal state of SIGIN and P34 signals are driven by respectively the pads SIGIN and P34. When this bit is set to 1, the internal state of SIGIN is fixed to 0 and the internal state of P34 is fixed set to 1.
5	sic_switch_overload	**State of the current limitation of the SVDD switch.** When set to 0, it indicates that the current consumption into the SVDD switch does no exceed the limit.
		When this bit is set to 1, the current limitation of the SVDD switch is activated by the switch.
4	sic_switch_en	**Enable of the SVDD switch.** When this bit is cleared to 0, the SVDD switch is disabled and the SVDD output power is tied to the ground. When this bit is set to 1, the SVDD switch is enabled and the SVDD output deliver power to the secure IC and to the internal pads (SIGIN, SIGOUT and P34).
3	-	Reserved
2	cpu_need_rng	**Force the random number generator in running mode.** When set to 0, the random number generator is under control of the CIU. When this bit is set to 1, the random number generator is forced to run.
1	random_dataready	**Indicates availability of random number.** When this bit is set to 1, it indicates that a new random number is available.
		It is automatically cleared to 0 when the register data_rng is read.
0	-	Reserved.

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8.6.11 Data mode detector

The data mode detector is able to detect received signals in accordance with the ISO/IEC 14443A/ MIFARE, FeliCa or NFCIP-1 schemes and the standard baud rates for 106 kbit/s, 212 kbit/s and 424 kbit/s to prepare the internal receiver in a fast and convenient way for further data processing.

The data mode detector can only be activated by the AutoColl command (see Section 8.6.20.12 “AutoColl command”). The mode detector is reset, when no external RF field is detected by the RF level detector.

The data mode detector could be switched off during the Autocoll command by setting the bit ModeDetOff in the register Mode to 1 (see Table 207).

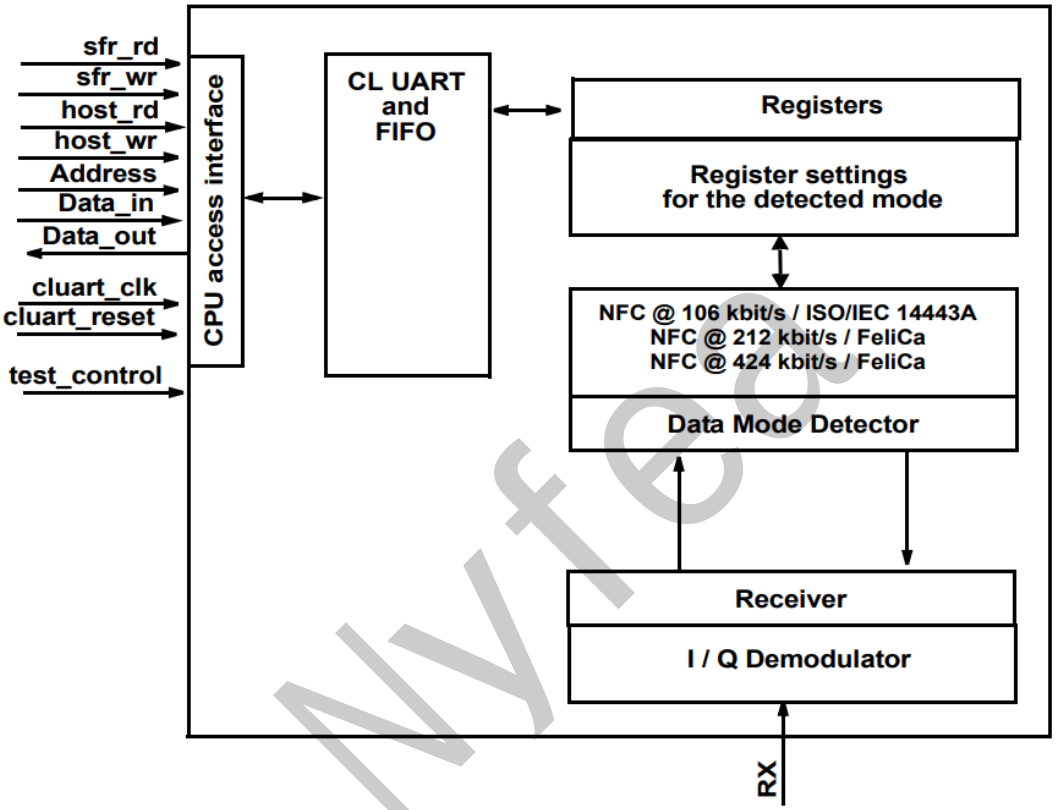


Fig 38. Data mode detector

8.6.12 Serial data switch

Two main blocks are implemented in the CIU. A digital block comprising state machines, coder and decoder logic and an analog block with the modulator and antenna drivers, receiver and amplifier. The Serial Data Switch is the interface between these two blocks.

The Serial Data Switch can route the interfacing signals to the pins SIGIN and SIGOUT.

SIGOUT and SIGIN are mainly used to enable the NFC-WI/S^2 C interface in the secure IC to emulate card functionality with the NF532. SIGIN is capable of processing a digital signal on data rates above 424 kbit/s. SIGOUT pin can also offer a digital signal that may be used with an additional external circuit to produce data rates at 106 kbit/s, 212 kbit/s, 424 kbit/s and above.

Load modulation is usually carry outed internally by the CIU, via TX1 and TX2. Nevertheless, it is supported to use LOADMOD to drive an external circuitry carry outing load modulation at the antenna (see optional circuitry of Figure 51).

The Serial Data Switch is controlled by the registers CIU_TxSel (see Table 217) and CIU_RxSel (see Table 219).

8.6.12.1 Serial data switch for driver and loadmod

The figure below shows the serial data switch for pins TX1 and TX2.

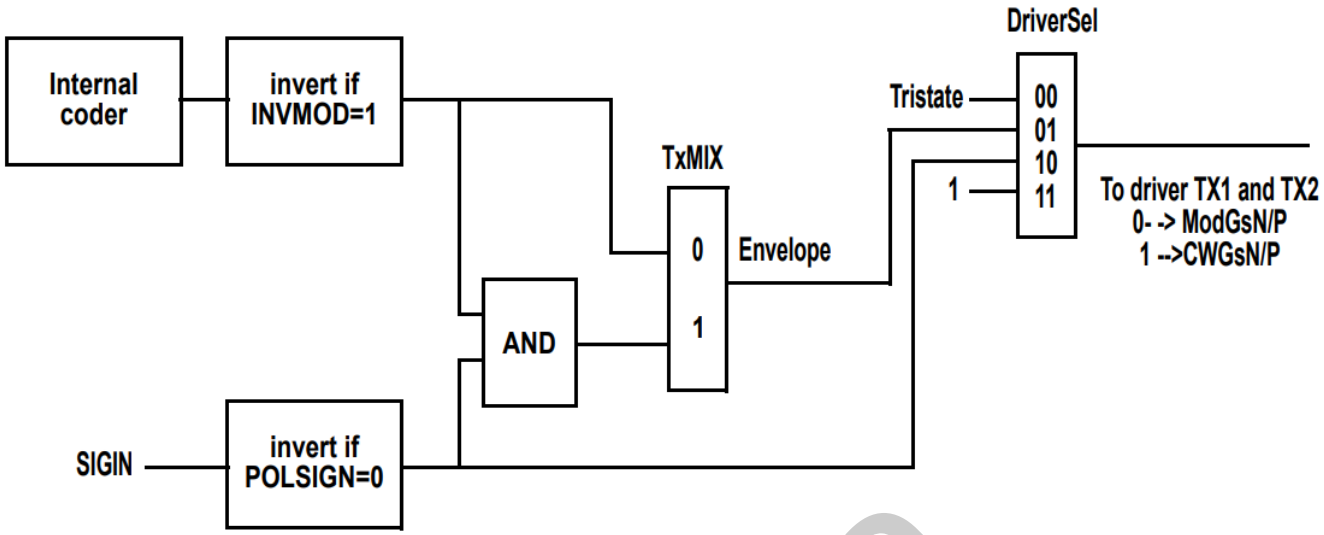


Fig 39. Serial data switch for TX1 and TX2

SIGIN is in general only used for secure IC communication. If TxMix is set to 1 (see Table 217), the driver pins are at the same time controlled by SIGIN and the internal coder.

The figure below shows the serial data switch for the LOADMOD pin.

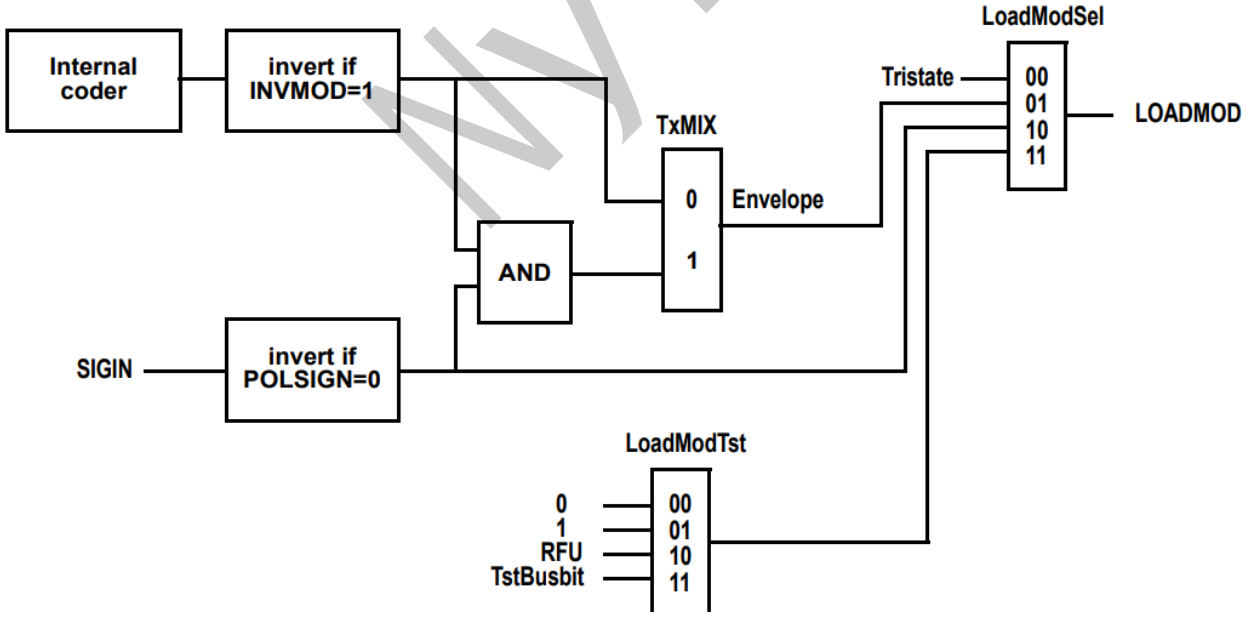


Fig 40. Serial data switch for LOADMOD pin

8.6.13 NFC-WI/S²C interface support

The NFC-WI/S²C interface allows a compatible secure IC to connect directly to NF532 and participate in contactless card operation. The interfacing signals may be routed to the pins SIGIN and SIGOUT. SIGIN can receive either a digital FeliCa or digital ISO/IEC 14443A signal sent by the secure IC. The SIGOUT pin can offer a digital signal and a clock to communicate to the secure IC. The secure IC may be any compatible smart-card or secure-element device that meets the interface requirements.

The NF532 produces the supply SVDD to the secure IC. The pins SIGIN and SIGOUT are referred to this supply, as well as pin P34 / SIC_CLK, which may be used as an extra pin for the connection with a secure IC.

The figure below outlines the supported communication flows via the NF532 to the secure core IC.

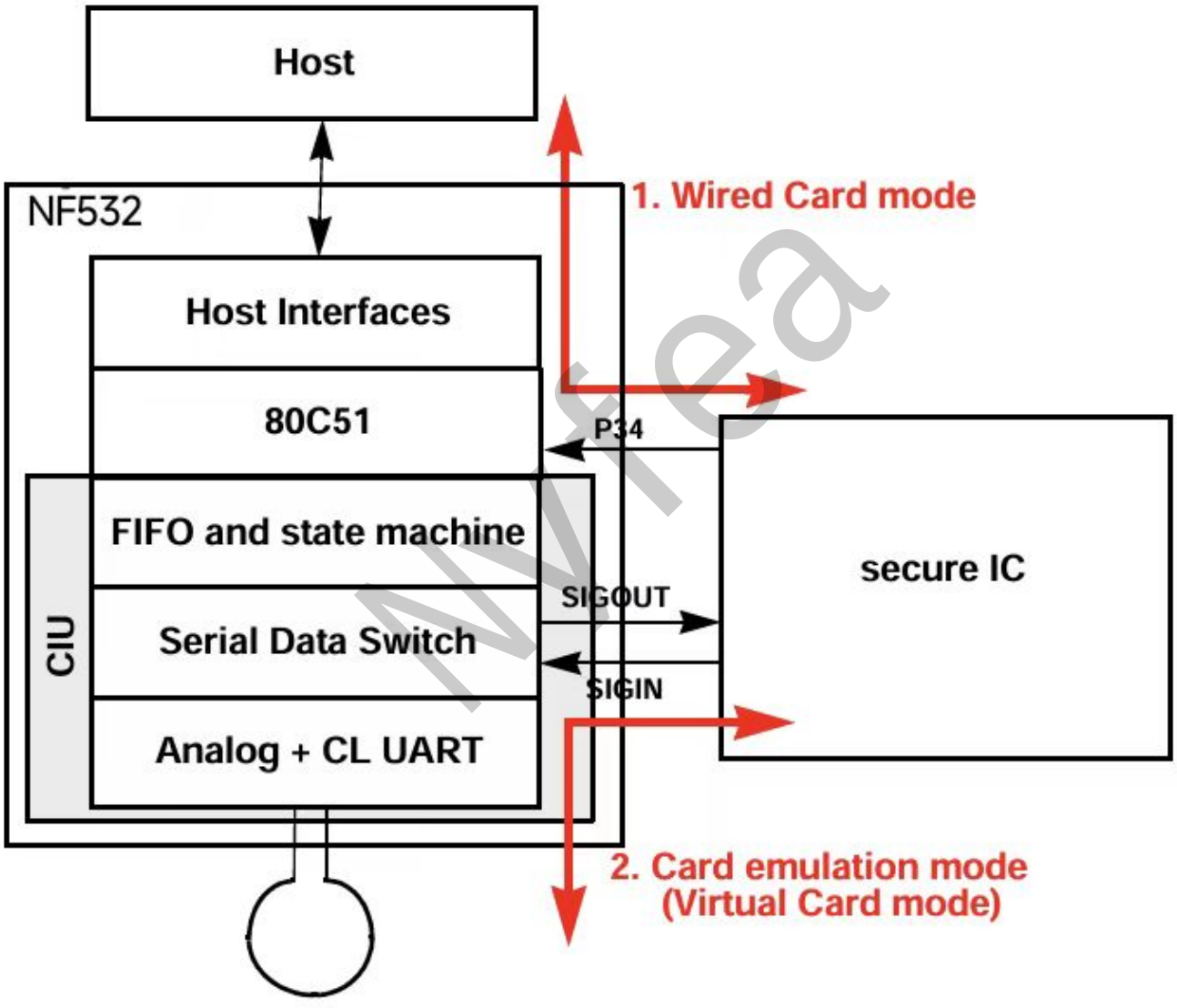


Fig 41. Communication flows supported by the NFC-WI interface

Configured in the Wired Card mode the host controller can directly communicate to the secure IC via SIGIN/SIGOUT. In this mode the NF532 produces the RF clock and carries out the communication on the SIGOUT line. To enable the Wired Card mode the clock has to be derived by the internal oscillator of the NF532 (see bits sic_clock_sel in Table 265.)

Configured in Card emulation mode the secure IC can act as contactless smart card IC via the NF532. In this mode, the SIGOUT timing signal is derived from the RF field generated by the external Reader/Writer. To enable the Virtual Card mode the clock derived by the external RF field has to be used.

The configuration of the NFC-WI/S^2 C interface differs for the FeliCa and MIFARE scheme as outlined in the next chapters.

8.6.13.1 Signal shape for FeliCa NFC-WI/S^2C interface support

The FeliCa secure IC is connected with the NF532 via the pins SIGOUT and SIGIN.

The signal at SIGOUT holds the information of the 13.56 MHz clock and the digitized demodulated signal. The clock and the demodulated signal are combined by through the logical function exclusive OR; XOR.

To ensure that this signal is free of spikes, the demodulated signal is digitally filtered first. The time delay for the digital filtering is in the range of one bit length. The demodulated signal changes only at a positive edge of the clock.

The register CIU_TxSel (see Table 217) controls the setting at SIGOUT

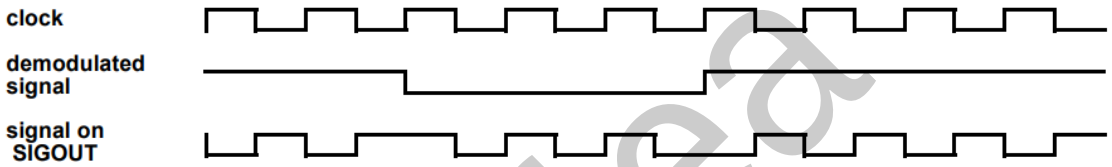


Fig 42. Signal shape for SIGOUT in FeliCa secure IC mode

Remark: The NF532 differs from the ECMA 373 specification, by the fact that when in FeliCa card emulation mode, the NF532 does send preamble bytes at 212kbps on SIGOUT as soon as the NF532 detects RF field.

Remark: In FeliCa card emulation mode, when the NF532 mode detector is activated, the data sent on SIGOUT are clocked at the incoming data rate only after the SYNC bytes are accepted. If per default the FeliCa card emulation mode is expected at 212kpbs, the 424kbps may need specific implementation at application level: the NF532 will sent beginning of first received frame (preamble+SYNC bytes) at 212kbps.

Remark: To properly work in FeliCa wired card mode, the SIGIN signal produced by the FeliCa secure element must be synchronous with the received SIGOUT bit clock, and the bit RCVOFF in the register 6331h (or SFR register D1h) must be set to logic level 1. The phase relationship of the SIGIN and SIGOUT bit clocks must respect a modulo[4] 13.56MHz clock cycles.

The response from the FeliCa secure IC is transferred from SIGIN directly to the antenna driver. The modulation is done in accordance with the register setting of the antenna drivers.

The 13.56MHz clock may be switched to P34 / SIC_CLK (see sic_clk_p34_en bit in Table 177).

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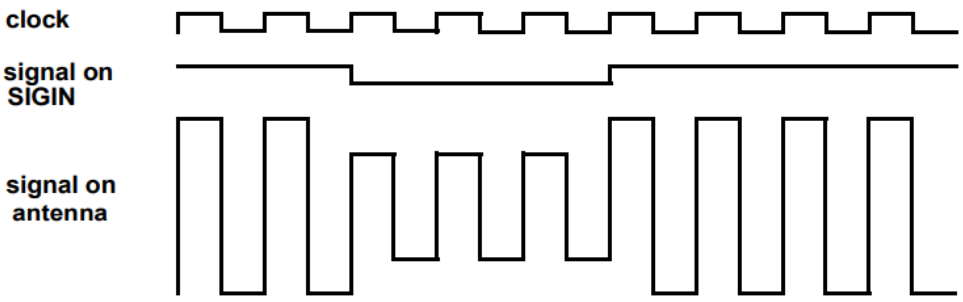


Fig 43. Signal shape for SIGIN in FeliCa secure IC mode

Remark: The signal on antenna is shown in principle only. This signal is sinusoidal. The clock for SIGIN is the same as the clock for SIGOUT.

8.6.13.2 Signal shape for ISO/IEC14443A and MIFARE NFC-WI/S²C support

The secure IC, e.g. the SmartMX is connected with the NF532 via the pins SIGOUT, SIGIN and P34 / SIC_CLK.

The signal at SIGOUT is a digital 13.56 MHz Miller coded signal between PVSS and SVDD. It is either derived from the external 13.56 MHz carrier signal when in Virtual Card Mode or internally produced when in Wired Card mode.

The register CIU_TxSel controls the setting at SIGOUT.

Note: The clock settings for the Wired Card mode and the Virtual Card mode differ. Refer to the description of the bit SicClockSel in register CIU_TestSel1.

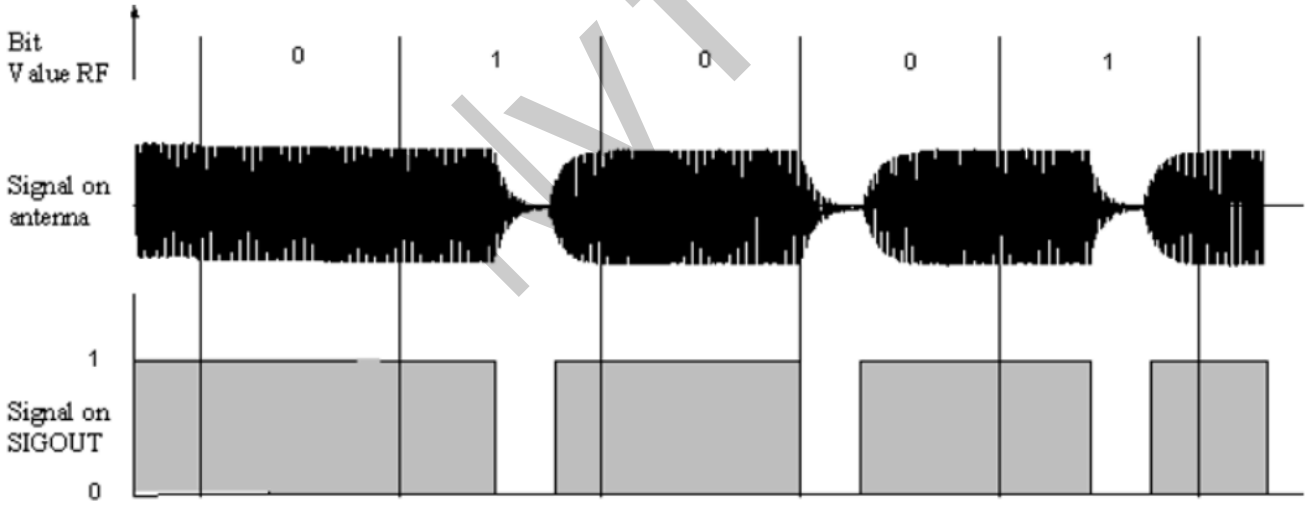


Fig 44. Signal shape for SIGOUT in NFC-WI mode

The signal at SIGIN is a digital Manchester coded signal compliant with ISO/IEC 14443A with a subcarrier frequency of 847.5 kHz produced by the secure IC.

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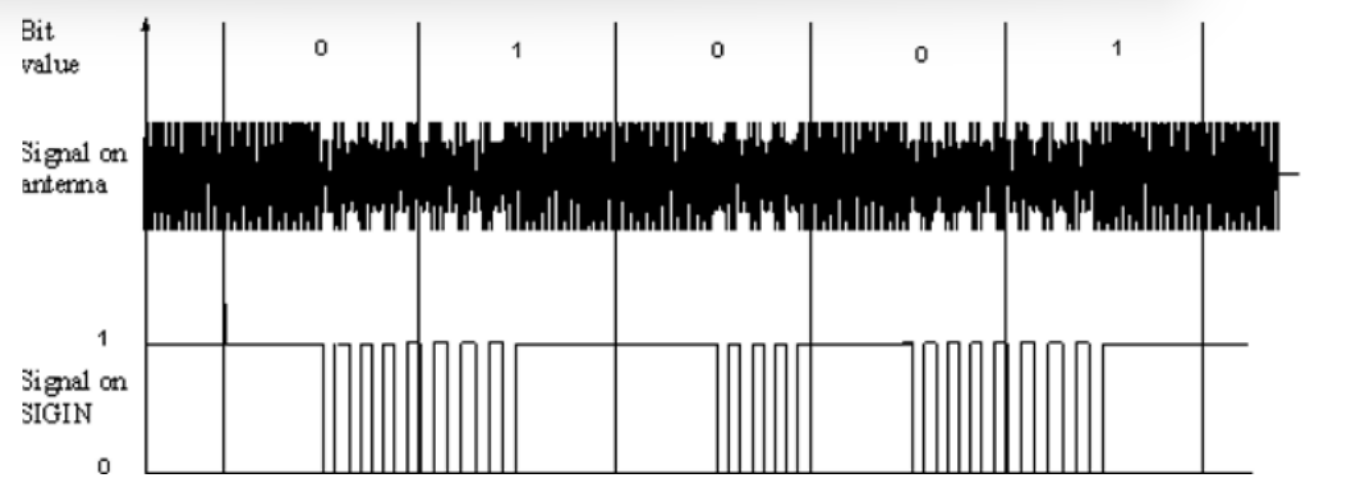


Fig 45. Signal shape for SIGIN in NFC-WI mode

8.6.13.3 NFC-WI/S²C initiator mode

The NF532 includes 2 counters of 127 and 31, with digital filtering, to enable activation from the secure IC (ACT_REQ_Si), or the command to go from data to command mode (ESC_REQ).

Table 163. NFC_WI_control register (address 610Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	nfc_wi_status	-	nfc_wi_en_	nfc_wi_en_
							act_req_im	clk
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 164. Description of NFC_WI_control bits

Bit	Symbol	Description
7 to 4	-	Reserved.
3	nfc_wi_status	Indicates a NFC-WI counter has reached its limit. Set to 1, when the counter has reached its limit. It may also be used as an interrupt for the 80C51 if the IE0_6 bit is set to 1 (see Table 10).
2	-	Reserved.
1	nfc_wi_en_act_req_im	**Selection of the NFC-WI counter.** This bit serves to select the 31 or 127 counter. When this bit is cleared to 0, the 31 counter is selected. When this bit is set to 1, the 127 counter is selected.
0	nfc_wi_en_clk	Enable the NFC-WI counters on SIGIN. When this bit is set to 1, the counters can run and count the clock cycles within 2 and 12 MHz.

8.6.14 Hardware support for FeliCa and NFC polling

8.6.14.1 Polling sequence functionality for initiator

1. Timer: The CIU has a timer, which may be programmed to produce an interrupt at the end of each timeslot, or if needed at the end of the last timeslot only.
2. The receiver may be configured to receive frames continuously. The receiver is ready to receive immediately after the last frame has been transmitted. This mode is activated by setting to 1 the bit RxMultiple in the register CIU_RxMode. It must be cleared to 0 by firmware.

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3. The CIU adds one byte at the end of every received frame, before it is transferred into the FIFO buffer. This byte shows whether the received frame is correct (see register Err). The first byte of each frame holds the length byte of the frame.
4. The length of one frame is 18 or 20 bytes (+1 byte error Info). The size of the FIFO is 64 bytes. This allows up to three frames to be held in the FIFO at the same time. If greater than 3 frames are expected, the 80C51 has to read out data from the FIFO, before the FIFO becomes full. In the case that the FIFO overflows, data is lost. (See error flag BufferOvfl).

8.6.14.2 Polling sequence functionality for target

1. The 80C51 has to configure the CIU with the correct polling response parameters for the Polling command.
2. To activate the automatic polling in target mode, the AutoColl Command has to be activated.
3. The CIU receives the polling command send out by an initiator and answers with the polling response. The timeslot is chosen automatically (The timeslot itself is randomly produced, but in the range 0 to TSN, which is defined by the polling command). The CIU compares the system code, held in byte 17 and 18 of the Config Command with the system code received with the polling command by an initiator. If the system code is equal, the CIU answers in accordance with the configured polling response. The system code FF(hex) acts as a wildcard for the system code bytes (i.e. a target of a system code 1234(hex) answers to the polling command with one of the next system codes 1234(hex), 12FF(hex), FF34 (hex) or FFFF(hex)). If the system code does not match no answer is sent back by the NF532. If a valid command, which is not a Polling command, is accepted by the CIU, no answer is sent back and the command AutoColl is stopped. The received frame is held in the FIFO.

8.6.14.3 Additional hardware support for FeliCa and NFC

Additionally to the polling sequence support for the FeliCa mode, the NF532 supports the check of the LEN-byte.

The received LEN-byte is checked by the registers CIU_FelNFC1 and CIU_FelNFC2:

DataLenMin in register CIU_FelNFC1 specifies the minimum length of the accepted frame length. This register is 6 bits long. Each value represents a length of 4.

DataLenMax in register CIU_FelNFC2 specifies the maximum length of the accepted frame. This register is 6 bits long. Each value represents a length of 4. If cleared to 0 this limit is switched off. If the length is not in the supposed area, the packed is not transferred to the FIFO and receiving is kept active.

Example 1:

- DataLenMin = 4
  - The length shall be greater or equal 16.
- DataLenMax = 5
  - The length shall be smaller than 20. Valid area: 16, 17, 18, 19

Example 2:

- DataLenMin = 9
  - The length shall be greater or equal 36.

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- DataLenMax = 0
    - The length shall be smaller than 256. Valid area: 36 to 255

8.6.15 CRC co-processor

The CRC preset value of the CRC co-processor may be configured to 0000h, 6363h, A671h or FFFFh depending on the bits CRCPreset in the register Mode.This is only valid when by means of CalcCRC command (see Section 8.6.20.7 “CalcCRC command”)

During a communication, the preset value of the CRC coprocessor is set in accordance with the bits CIU_RxMode and CIU_TxMode.

The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$.

The CRC co-processor is configurable to handle the various MSB and LSB requirements for the various protocols.The bit MSBFirst in the register CIU_Mode shows that the data is written with MSB first

The registers CRCResult-Hi and CRCResult-Lo show the result of the CRC calculation.

8.6.16 FIFO buffer

An 64*8 bits FIFO buffer is implemented in the CIU. It buffers the input and output data stream between the 80C51 and the internal state machine of the CIU. Thus, it is supported to handle data streams with lengths of up to 64 bytes without taking timing constraints into account.

8.6.16.1 Accessing the FIFO buffer

The FIFO-buffer input and output data bus is connected with the register CIU_FIFOData. Writing to this register stores one byte in the FIFO-buffer and increments the internal FIFO-buffer write-pointer. Reading from this register shows the FIFO-buffer contents held at the FIFO-buffer read-pointer and decrements the FIFO-buffer read-pointer. The distance between the write- and read-pointer may be obtained by reading the register CIU_FIFOLevel.

When the 80C51 begins a command, the CIU may, while the command is in progress, access the FIFO-buffer in accordance with that command. Physically only one FIFO-buffer is implemented, which may be used in input- and output direction. Consequently the 80C51 has to take care, not to access the FIFO-buffer in an unintended way.

8.6.16.2 Controlling the FIFO buffer

Besides writing to and reading from the FIFO-buffer, the FIFO-buffer pointers might be reset by setting the bit FlushBuffer in the register CIU_FIFOLevel. Consequently, the FIFOLevel[6:0] bits are cleared to 0, the bit BufferOvfl in the register CIU_Error is cleared to 0, the actually held bytes are not accessible anymore and the FIFO-buffer may be filled with another 64 bytes again.

8.6.16.3 Status information about the FIFO buffer

The 80C51may obtain the next data about the FIFO-buffers status:

- Number of bytes already held in the FIFO-buffer: FIFOLevel[6:0] in register CIU_FIFOLevel
- Warning, that the FIFO-buffer is quite full: HiAlert in register CIU_Status1
- Warning, that the FIFO-buffer is quite empty: LoAlert in register CIU_Status1
- Indication, that bytes were written to the FIFO-buffer although it was already full: BufferOvfl in register CIU_Error.

BufferOvfl may be cleared to 0 only by setting to 1 bit FlushBuffer in the register CIU_FIFOLevel.

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The CIU can produce an interrupt signal

- If LoAlertIEn in register CIU_CommIEn is set to 1, it will set to 1 CIU_IRQ_0 in the register CIU_Status1, when LoAlert in the same register changes to 1.
- If HiAlertIEN in register CIU_CommIEn is set to 1, it will set to 1 CIU_IRQ_0 in the register CIU_Status1, when HiAlert in the same register changes to 1.

The flag HiAlert is set to 1 if only WaterLevel[5:0] bits (as set in register CIU_WaterLevel) or less may be held in the FIFO-buffer. It is produced by the next equation:

HiAlert = (64 - FIFOLength) ≤ WaterLevel

The flag LoAlert is set to 1 if WaterLevel[5:0] bits (as set in register CIU_WaterLevel) or less are actually held in the FIFO-buffer. It is produced by the next equation:

LoAlert = FIFOLength ≤ WaterLevel

8.6.17 CIU_timer

A timer unit is implemented in the CIU: CIU_timer. The 80C51 use CIU_timer to manage timing relevant tasks for contactless communication. CIU_timer may be used in one of the next configurations:

- Timeout-Counter
- Watch-Dog Counter
- Stop Watch
- Programmable One-Shot
- Periodical Trigger

CIU_timer may be used to measure the time interval between two events or to show that a specific event occurred after a specific time. CIU_timer may be triggered by events which is explained in the next, but it does not itself influence any internal event (e.g. A timeout during data reception does not influence the reception process automatically). Furthermore, multiple timer related bits are set and these bits may be used to produce an interrupt.

CIU_timer has a input clock of 6.78 MHz (derived from the 27.12 MHz quartz). CIU_timer is made up of 2 stages: 1 prescaler and 1 counter.

The prescaler is a 12 bits counter. The reload value for the prescaler may be defined between 0 and 4095 in register CIU_TMode and CIU_TPrescaler. This decimal value is called TPrescaler.

The reload value TReloadVal for the counter is defined with 16 bits in a range from 0 to 65535 in the registers CIU_TReloadVal_Lo and CIU_TReloadVal_Hi.

The current value of CIU_timer is shown by the registers CIU_TCounterVal_lo and CIU_TCounterVal_hi.

If the counter reaches 0 an interrupt is produced automatically shown by setting the TimerIRq flag in the register CommonIRq. If enabled, it will set to 1 CIU_IRQ_1 in the register CIU_Status1. TimerIRq flag may be set to 1 or to 0 by the 80C51. Depending on the configuration, CIU_timer will stop at 0 or restart with the setting of the registers CIU_TReloadVal_Lo and CIU_TReloadVal_Hi.

Status of CIU_timer is shown by the bit TRunning in the register CIU_Status1.

CIU_timer may be manually started by TStartNow in register Control or manually stopped by TStopNow in register Control.

Furthermore CIU_timer may be activated automatically by setting the bit TAuto in the register CIU_TMode to fulfill dedicated protocol requirements automatically.

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The time delay of a timer stage is the reload value +1.

Maximum time:

TPrescaler = 4095, TReloadVal = 65535 => 4096*65536/6.78 MHz = 39.59 s

Example:

To show 100 ms it is needed to count 678 clock cycles. This means the setting for TPrescaler has to be set to TPrescaler = 677.The timer has now an input clock of 100 us. The timer can count up to 65535 timeslots of 100 ms.

8.6.18 Interrupt request system

The CIU shows certain events by setting interrupt bits in the register CIU_Status1 and, additionally it will set to 1 CIU_IRQ_1 or CIU_IRQ_0. If this interrupt is enabled (see Table 12) the 80C51 is interrupted. This enables the implementation of efficient interrupt-driven firmware.

8.6.18.1 Interrupt sources

The table below shows the integrated interrupt flags, the associated source and the condition for its activation.

The interrupt flag TimerIRq in the register CIU_CommIrq reports an interrupt set by the timer unit. The setting is done when the timer decrements from 1 down to 0.

The TxIRq bit in the register CIU_CommIrq shows that the transmitter has finished. If the state changes from sending data to transmitting the end of frame pattern, the transmitter unit sets automatically the interrupt bit to 1.

The CRC coprocessor sets the flag CRCIRq in the register CIU_DivIrq after having processed all data from the FIFO buffer. This is shown by the flag CRCReady set to 1.

The RxIRq flag in the register CIU_CommIrq reports an interrupt when the end of the incoming data is detected.

The flag IdleIRq in the register CIU_CommIrq is set to 1 if a command finishes and the contents of the CIU_Command register changes to idle.

The flag HiAlertIRq in the register CIU_CommIrq is set to 1 if the HiAlert bit is set to 1, that means the Contactless FIFO buffer has reached the level shown by the bits WaterLevel[5:0].

The flag LoAlertIRq in the register CIU_CommIrq is set to 1 if the LoAlert bit is set to 1, that means the Contactless FIFO buffer has reached the level shown by the bits WaterLevel[5:0].

The flag RFOnIRq in the register CIU_DivIrq is set to 1, when the RF level detector detects an external RF field.

The flag RFOffIRq in the register CIU_DivIrq is set to 1, when a present external RF field is switched off.

The flag ErrIRq in the register CIU_CommIrq shows an error detected by the CIU during sending or receiving. This is shown by any bit set to 1 in register CIU_Error.

The flag ModeIRq in the register CIU_DivIrq shows that the data mode detector has detected the current mode.

These flags are summarized with 2 interrupt bits within the register CIU_Status1:

- the high priority interrupt sources are summarized with CIU_IRQ_0.
- the low priority interrupt sources are summarized with CIU_IRQ_1.

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See the register Table 190.

Table 165. High priority interrupt sources (CIU_IRQ_0)

Interrupt Flag	Interrupt source	Set automatically, WHEN
TxIRq	Transmitter	a transmitted data stream ends
RxIRq	Receiver	a received data stream ends
HiAlertIRq	FIFO-buffer	the FIFO-buffer is getting full
LoAlertIRq	FIFO-buffer	the FIFO-buffer is getting empty

Table 166. Low priority interrupt sources (CIU_IRQ_1)

Interrupt Flag	Interrupt source	Set automatically, WHEN
TimerIRq	Timer Unit	the timer counts from 1 to 0
CRCIRq	CRC-Coprocessor	all data from the FIFO buffer have been processed
IdleIRq	CIU_Command Register	a command execution finishes
RFOnIRq	RF Level Detector	an external RF field is detected
RFOffIRq	RF Level Detector	a present external RF field is switched off
ErrIRq	CIU	an error is detected
ModeIRq	data mode detector	the mode has been detected

8.6.19 CIU Power Reduction Modes

8.6.19.1 Hard-Power-Down

A Hard-Power-Down is enabled when RSTPD_N is low. None of the CIU blocks are running, even the RF level detector.

8.6.19.2 CIU Power-down

The CIU Power-down mode is entered immediately by setting the Power-down bit in the register CIU_Command. All CIU blocks are switched off, except the 27.12 MHz oscillator and the RF level detector.

All registers and the FIFO will keep the content during CIU Power-down.

If the bit AutoWakeUp in the register CIU_TxAuto is set and an external RF field is detected, the CIU Power-down mode is left automatically.

After setting bit Power-down to 0 in the register CIU_Command, it needs 1024 clocks cycle until the CIU Power-down mode is left shown by the Power-down bit itself. Setting it to 0 does not immediately set it to 0. It is automatically cleared to 0 by the CIU when the CIU Power-down mode is left.

When in CIU Power-down mode and DriverSel[1:0] is no set to 00b (see Table 217), to ensure a minimum impedance at the transmitter outputs, the CWGsNOn[3], CWGsNOff[3], ModGsNOn[3], ModGsNOff[3], CWGsP[5], ModGsP[5] bits are set to 1, but it is not readable in the registers.

8.6.19.3 Transmitter Power-down

The Transmitter Power-down mode switches off the internal antenna drivers to turn off the RF field by setting the bits Tx1RFEn and Tx2RFEn in the register CIU_TxControl to 0. The receiver is still switched on, meaning the CIU may be accessed by a second NFC device as a NFCIP-1 target.

Note: In case the bit InitialRFOn has been set to 1, when the drivers were already switched on, it is needed either to set InitialRFOn to 0, prior to setting the bits Tx1RFEn and Tx2RFEn in the register CIU_TxControl to 0, or to set also the bits Tx1RFAutoEn and Tx2RFAutoEn in the register CIU_TxAuto to 0.

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8.6.20 CIU command set

8.6.20.1 General description

The CIU behavior is determined by an internal state machine capable to carry out a certain set of commands. Writing the according command code to the CIU_Command register begins the commands.

Arguments and/or data necessary to process a command are mainly exchanged via the FIFO buffer.

8.6.20.2 General behavior

- Each command, that needs a data stream (or data byte stream) as input will immediately process the data it finds in the FIFO buffer. An exception to this rule is the Transceive command. Using this command the transmission is started with the StartSend bit in CIU_BitFraming register.
- Each command that needs a certain number of arguments will start processing only when it has received the correct number of arguments via the FIFO buffer.
- The FIFO buffer is not cleared automatically at command start. Consequently, it is also possible to write the command arguments and/or the data bytes into the FIFO buffer and start the command afterwards.
- Each command may be interrupted by the 80C51 by writing a new command code into the CIU_Command register e.g.: the Idle command.

8.6.20.3 Commands overview

Table 167. Command overview

Command	Command code	Action
Idle	0000	No action; cancels current command execution.
Config	0001	Configures the CIU for FeliCa, MIFARE and NFCIP-1 communication.
Generate RandomID	0010	Generates 10-byte random ID number
CalcCRC	0011	Activates the CRC co-processor or perform self-test.
Transmit	0100	Transmits data from the FIFO buffer.
NoCmdChange	0111	No command change. This command may be used to modify different bits in the CIU_Command register without touching the command. e.g. Power-down bit.
Receive	1000	Activates the receiver circuitry.
SelfTest	1001	Activates the self-test. Not described in this chapter.
Transceive	1100	If bit Initiator in the register CIU_Control is set to 1: Transmits data from FIFO buffer to the antenna and activates automatically the receiver after transmission is finished. If bit Initiator in the register CIU_Control is cleared to 0: Receives data from antenna and activates automatically the transmitter after reception.
AutoColl	1101	Handles FeliCa polling (Card operating mode only) and MIFARE anticollision (Card operating mode only)
MFAuthent	1110	Performs the MIFARE Classic 1K or MIFARE Classic 4K authentication in MIFARE Reader/Writer mode only.
Soft Reset	1111	Resets the CIU.

8.6.20.4 Idle command

The CIU is in idle mode. This command is also used to terminate the actual command.

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8.6.20.5 Config command

To configure the automatic MIFARE Anticollision, FeliCa Polling and NFCID3, the data used for these transactions have to be held internally. All the next data have to be written to the FIFO in this order:

- SENS_RES (2 bytes): in order byte0, byte1
- NFCID1 (3 Bytes): in order byte0, byte1, byte 2; the first NFCID1 byte if fixed to 08h and the check byte is calculated automatically
- SEL_RES (1 byte)
- Polling response (2 bytes (shall be 01h, FEh)+ 6 bytes NFCID2 + 8 bytes Pad + 2 bytes system code)
- NFCID3 (1 byte)

In total 25 bytes which are transferred into an internal buffer with the Config command.

The complete NFCID3 is 10 bytes long and consist of the 3 NFCID1 bytes, the 6 NFCID2 bytes and the NFCID3 byte listed above.

To read out this configuration (after it has been loaded), the command Config with an empty FIFO buffer has to be started. For this case the 25 bytes are transferred from the internal buffer to the FIFO.

The CIU has to be configured after each power up, prior to through the automatic Anticollision/ Polling function (AutoColl command). During a Hard-Power-Down (RSTPD_N cleared to 0) this configuration stays unchanged.

This command terminates automatically when finished and the active command is Idle.

8.6.20.6 Generate RandomID command

This command produces a 10-byte random number held in the internal 25 bytes buffer and overwrites the 10 NFCID3 bytes. This random number might be used for fast generation of all necessary ID bytes for the automatic Anticollision / Polling function.

Note: To configure the CIU, Config command has to be used first.

This command terminates automatically when finished and the active command is Idle

8.6.20.7 CalcCRC command

The contents of the FIFO is transferred to the CRC co-processor and a CRC calculation is started. The result is held in the CRCResult register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO gets empty during the data stream. The next byte written to the FIFO is added to the calculation.

The preset value of the CRC is defined by the CRCPreset bits of the register CIU_Mode, and the chosen value is loaded to the CRC co-processor when the command is started.

This command has to be terminated by firmware by writing any command to the CIU_Command register e.g. the Idle command.

If SelfTest in register CIU_AutoTest is set to 1, the CRC co-processor is in Self Test mode and carries out a digital self-test. The result of the self-test is written in the FIFO.

8.6.20.8 Transmit command

The FIFO contents are sent immediately after starting the command. Before transmitting FIFO content, all relevant register settings have to be set to send data in the selected mode.

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This command terminates automatically when the FIFO gets empty and the active command is Idle. It may be terminated by any other command written to the CIU_Command register.

8.6.20.9 NoCmdChange command

This command does not influence any ongoing command in the CIU_Command register. It may be used to manipulate any bit except the command bits in the CIU_Command register, e.g. the bits RcvOff or Power-down.

8.6.20.10 Receive command

The CIU activates the receiver path and waits for any data stream to be received. The correct settings for the expected mode have to be set prior to starting this command.

This command terminates automatically when the reception finishes and the active command is Idle.

In case of data rates at 212 kbps or 424 kbps with NFC or FeliCa framing, the reception finishes when the number of bytes shown by the LEN byte (received) are accepted. If less bytes than shown by LEN are accepted from the RF, the CIU will sample noise to add the missing bytes. If more bytes than shown by LEN are accepted from the RF, the last bytes is ignored. When LEN is 0, the frame has no effect, and the NF532 waits for a new frame.

In case of data rate at 106 kbps in NFC communication mode, the reception finishes when the CIU detects an end of frame, except if the CIU detects more bytes than shown by the received LEN byte. In that case, after receiving LEN bytes, a new reception rebegins and the CIU timer begins (if Tauto in register CIU_TMode Table 252 is set to 1). The end of reception is then seen if a new valid frame is accepted or the firmware has to end the reception phase on time-out.

In all other cases, the end of the reception is detected by the end of frame.

In case no frame is accepted and Tauto in register CIU_TMode Table 252 is set to 1, then TimerIRQ in register CommIRQ is set to 1. The firmware has to end the reception phase.

Note: If the bit RxMultiple in the register CIU_RxMode is set to 1, the Receive command does not terminate automatically. It has to be terminated by setting any other command in the CIU_Command register.

8.6.20.11 Transceive command

This circular command repeats transmitting data from the FIFO and receiving data from the RF field continuously. If the bit Initiator in the register CIU_Control is set to 1, it shows that the first action is transmitting and after having finished transmission the receiver is activated to receive data. If the bit Initiator in the CIU_Control register is cleared to 0, the first action is receiving and after having received a data stream, the transmitter is activated to send data. In the second configuration the NF532 first acts as a receiver and if a data stream is accepted it switches to the Transmit mode.

The end of the reception phase is detected in the same way than for the receive command and also when the RF field is cut.

The transceive command always take into account the presence or absence of the RF field. No transmission or reception may be done when no RF field.

Table 168. Transceive command scenario

Communication step	Initiator =1	Initiator=0
1	Send	Receive
2	Receive	Send
3	Send	Receive
4	Receive	Send

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Each transmission process has to be started with setting bit StartSend in the register CIU_BitFraming. This command has to be cleared by firmware by writing any command to the CIU_Command register e.g. the command idle.

Note: If the bit RxMultiple in register CIU_RxMode is set, this command will never leave the receiving state, because the receiving is not cancelled automatically.

8.6.20.12 AutoColl command

This command automatically handles the MIFARE activation and the FeliCa polling in the Card Operation mode. The bit Initiator in the CIU_Control register must be cleared to 0 for correct operation. During this command, Mode Detector is active if not deactivated by setting the bit ModeDetOff in the CIU_Mode register. After Mode Detector detects a mode, the mode dependent registers are set in accordance with the incoming data. In case of no external RF field this command resets the internal state machine and returns to the initial state but it is not terminated.

When the Autocoll command terminates the Transceive command gets active.

During Autocoll command:

- The CIU interrupt bits, except RfOnIRq, RfOffIRq and SIGINActIRq (see Table 187), are not supported. Only the last received frame will serve the CIU interrupts.
- During ISO/IEC 14443A activation, TxCRCEn and RxCRCEn bits are defined by the AutoColl command. The changes cannot be observed at the CIU_TxMode and CIU_RxMode registers. When the Transceive command is active, the setting of the bits is relevant.
- During Felica activation (polling), TxCRCEn and RxCRCEn bits are always relevant and are not overruled by the Autocoll command. Their value must be set to 1 according the FeliCa protocol.

Note: Pay attention, that the FIFO will also receive the two CRC check bytes of the last command, even if they are already checked and correct, and if the state machine (Anticollision and Select routine) has not been executed, and 106 kbit is detected.

This command may be cleared by firmware by writing any other command to the CIU_Command register, e.g. the Idle command. Writing the same content again to the CIU_Command register resets the state machine.

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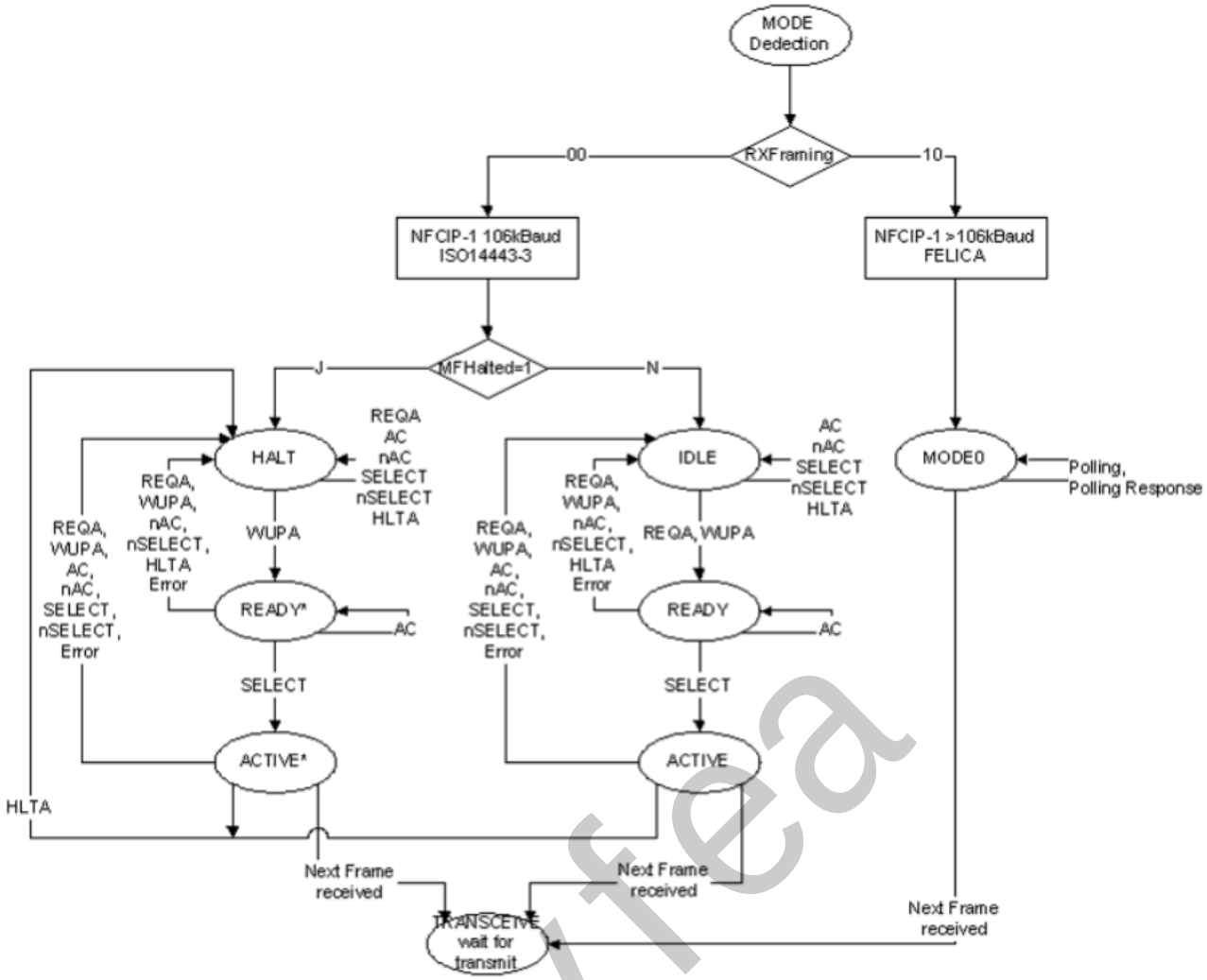


Fig 46. AutoColl command

- NFCIP-1 106 kbps passive communication mode:

The MIFARE anticollision is finished and the command changes automatically to Transceive. The FIFO holds the ATR_REQ frame including the start byte F0h. The bit TargetActivated in the register CIU_Status2 is set to 1

- NFCIP-1 212 and 424 kbps passive communication mode:

The FeliCa polling command is finished and the command has automatically changed to Transceive. The FIFO holds the ATR_REQ frame. The bit TargetActivated in the register CIU_Status2 is set to 1.

- NFCIP-1 106, 212 and 424 kbps active communication mode:

This command is changing automatically to Transceive. The FIFO holds the ATR_REQ frame. The bit TargetActivated in the register CIU_Status2 is cleared to 0. For 106 kbps only, the first byte in the FIFO reports the start byte F0h and the CRC is added into the FIFO.

- ISO/IEC 14443A/MIFARE (Card Operating mode):

The MIFARE anticollision is finished and the command has automatically changed to Transceive. The FIFO holds the first command after the Select. The bit TargetActivated in the register CIU_Status2 is set to 1.

- FeliCa (Card Operating mode):

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The FeliCa polling command is finished and the command has automatically changed to Transceive. The FIFO holds the command after the Polling in the FeliCa protocol. The bit TargetActivated in the register CIU_Status2 is set to 1.

8.6.20.13 MFAuthent command

This command handles the MIFARE authentication in Reader/Writer mode to enable a secure communication to any MIFARE Classic 1K and MIFARE Classic 4K emulation card. Write the following data to the FIFO before activating the command:

- Authentication command code (60h for key A, 61h for key B)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes shall be written to the FIFO.

Note: When the MFAuthent command is active, any FIFO access is blocked. Anyhow if there is an access to the FIFO, the bit WrErr in the register CIU_Error is set to 1.

This command terminates automatically when the MIFARE Classic 1K or MIFARE Classic 4K emulation card is authenticated. The bit MFCrypto1On in the register CIU_Status2 is set to 1.

This command does not terminate automatically when the card does not answer, consequently CIU timer should be initialized to automatic mode. For this case, beside the bit IdleIRq, the bit TimerIRq may be used as termination criteria. During authentication processing, the bits RxIRq and TxIRq of CIU_CommIrq register are blocked.

The Crypto1On bit is only valid after termination of the MFAuthent command (either after processing the authentication or after writing the Idle command in the register CIU_Command).

In case there is an error during the MIFARE authentication, the ProtocolErr bit in the CIU_Error register is set to 1 and the Crypto1On bit in CIU_Status2 register is cleared to 0.

8.6.20.14 SoftReset command

This command carries out a reset of the CIU. The configuration data of the internal buffer stays unchanged. All registers are set to the reset values.

When SoftReset is finished, the active command switches to Idle.

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8.6.21 CIU tests signals

8.6.21.1 CIU self-test

The CIU has the capability to carry out a self-test. To start the self-test the next procedure has to be carry outed:

1. Perform a SoftReset.
2. Clear the internal buffer by writing 25 bytes of 00h and carry out the Config command.
3. Enable the self-test by writing the setting 09h to the register CIU_AutoTest.
4. Write 00h to the FIFO.
5. Start the self-test with the CalcCRC command.
6. The self-test is carry outed.
7. When the self-test is finished, the FIFO is holds the next bytes:

- Correct answer for VersionReg equal to 80h: 0x00, 0xaa, 0xe3, 0x29, 0x0c, 0x10, 0x29, 0x6b 0x76, 0x8d, 0xaf, 0x4b, 0xa2, 0xda, 0x76, 0x99 0xc7, 0x5e, 0x24, 0x69, 0xd2, 0xba, 0xfa, 0xbc 0x3e, 0xda, 0x96, 0xb5, 0xf5, 0x94, 0xb0, 0x3a 0x4e, 0xc3, 0x9d, 0x94, 0x76, 0x4c, 0xea, 0x5e 0x38, 0x10, 0x8f, 0x2d, 0x21, 0x4b, 0x52, 0xbf 0xfb, 0xf4, 0x19, 0x94, 0x82, 0x5a, 0x72, 0x9d 0xba, 0x0d, 0x1f, 0x17, 0x56, 0x22, 0xb9, 0x08

8.6.21.2 CIU test bus

The test bus is implemented for production test purposes. The following configuration may be used to improve the design of a system through the NF532. The test bus allows to route internal signals to output pins.

The Observe_testbus register serves to enable this functionality.

Table 169. Observe_testbus register (address 6104h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	observe_ciu
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W

Table 170. Description of Observe_testbus bits

Bit	Symbol	Description
7 to 1	-	Reserved.
0	observe_ciu	Configure the pads P3x (P30 to P35), RSTOUT_Nand P70_IRQ to observe internal CIU data bus.
		When this bit is set to 1, the pads are configured in output mode and show the internal data bus D0 to D6 of the CIU. P70_IRQ is the 13.56 MHz
		digital clock of CIU (generated from field or crystal).

The test bus signals are chosen by accessing TestBusSel in register CIU_TestSel2.

Table 171. TstBusBitSel set to 07h

Test bus bit	Test signal	Comments
D6	sdata	shows the actual received data value.
D5	scoll	shows if in the actual bit a collision has been detected (106 kbit/s only)
D4	svalid	shows if sdata and scoll are valid

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Test bus bit	Test signal	Comments
D3	sover	shows that the receiver has detected a stop bit (ISO/IEC 14443A/MIFARE mode only)
D2	RCV_reset	shows if the receiver is reset
D1	RFon filtered	shows the value of the internal RF level detector
D0	Envelope	shows the output of the internal coder

Table 172. TstBusBitSel set to 0Dh

Test bus bit	Test signal	Comments
D6	clkstable	shows if the oscillator delivers a stable signal
D5	clk27/8	shows the output signal of the oscillator divided by 8
D4	clk27rf/8	shows the clk27rf signal divided by 8
D3	clk13/4	shows the clk13rf divided by 4
D2	clk27	shows the output signal of the oscillator
D1	clk27rf	shows the RF clock multiplied by 2
D0	clk13rf	shows the RF clock of 13.56 MHz

8.6.21.3 Test signals at pin AUX

Each signal may be switched to pin AUX1 or AUX2 by setting SelAux1 or SelAux2 in the register CIU_AnalogTest. See Table 279

8.6.21.4 PRBS

Enables the Pseudo Random Bit Stream of 9-bit or 15-bit length sequence, PRBS9 or PRBS15, in accordance with ITU-T0150. To start the transmission of the defined datastream, Transmit command has to be activated. The preamble/Sync byte/start bit/parity bit are produced automatically depending on the selected mode.

Note: All relevant registers to send data have to be configured prior to entering PRBS mode according ITU-T0150.

8.6.22 CIU memory map

The registers of the CIU are either map into the SFR or into the XRAM memory space.

Table 173. Contactless Interface Unit SFR memory map

ADDR	Byte size	Register name	Description
D1h	1	CIU_Command	Starts and stops the command execution
D2h	1	CIU_CommlEn	Control bits to enable and disable the passing of interrupt requests
D3h	1	CIU_DivlEn	Control bits to enable and disable the passing of interrupt requests
D4h	1	CIU_CommIrq	Contains common Interrupt Request flags
D5h	1	CIU_DivIrq	Contains diverse Interrupt Request flags
D6h	1	CIU_Error	Error flags showing the error status of the last command executed
DFh	1	CIU_Status1	Contains status flags of the CRC, Interrupt Request System and FIFO buffer
E9h	1	CIU_Status2	Contain status flags of the Receiver, Transmitter and Data Mode Detector
EAh	1	CIU_FIFOData	in- and output of 64 bytes FIFO buffer
EBh	1	CIU_FIFOLevel	Indicates the number of bytes stored in the FIFO
ECh	1	CIU_WaterLevel	Specifies the thresholds for FIFO under- and overflow warning
EDh	1	CIU_Control	Contains miscellaneous Control bits

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ADDR	Byte size	Register name	Description
EEh	1	CIU_BitFraming	Adjustments for bit oriented frames
EFh	1	CIU_Coll	Bit position of the first bit collision detected on the RF-interface

Table 174. Contactless Interface Unit extension memory map

ADDR	Byte size	Register name	Description
6301h	1	CIU_Mode	Defines general modes for transmitting and receiving
6302h	1	CIU_TxMode	Specifies the transmission data rate and framing during transmission
6303h	1	CIU_RxMode	Specifies the transmission data rate and framing during receiving
6304h	1	CIU_TxControl	Controls the logical behavior of the antenna driver pins TX1 and TX2
6305h	1	CIU_TxAuto	Controls the settings of the antenna driver
6306h	1	CIU_TxSel	Selects the internal sources for the antenna driver
6307h	1	CIU_RxSel	Selects internal receiver settings
6308h	1	CIU_RxThreshold	Selects thresholds for the bit decoder
6309h	1	CIU_Demod	Defines demodulator settings
630Ah	1	CIU_FelNFC1	Specifies the length of the valid range for the received frame
630Bh	1	CIU_FelNFC2	Specifies the length of the valid range for the received frame
630Ch	1	CIU_MifNFC	Controls the communication in ISO/IEC 14443/MIFARE and NFC target mode at 106 kbit/s
630Dh	1	CIU_ManualRCV	Allows manual fine tuning of the internal receiver
630Eh	1	CIU_TypeB	Configure the ISO/IEC 14443 type B
630Fh	1	-	Reserved
6310h	1	-	Reserved
6311h	1	CIU_CRCResultMSB	Shows the actual MSB values of the CRC calculation
6312h	1	CIU_CRCResultLSB	Shows the actual LSB values of the CRC calculation
6313h	1	CIU_GsNOff	Selects the conductance of the antenna driver pins TX1 and TX2 for load modulation when own RF field is switched OFF
6314h	1	CIU_ModWidth	Controls the setting of the width of the Miller pause
6315h	1	CIU_TxBitPhase	Bit synchronization at 106 kbit/s
6316h	1	CIU_RFCfg	Configures the receiver gain and RF level
6317h	1	CIU_GsNOn	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation, when own RF field is switched ON
6318h	1	CIU_CWGsP	Selects the conductance of the antenna driver pins TX1 and TX2 when not in modulation phase
6319h	1	CIU_ModGsP	Selects the conductance of the antenna driver pins TX1 and TX2 when in modulation phase
631Ah	1	CIU_TMode	Defines settings for the internal timer
631Bh	1	CIU_TPrescaler	
631Ch	1	CIU_TReloadVal_hi	Summarizes the 16-bit long timer reload value (Higher 8 bits)
631Dh	1	CIU_TReloadVal_lo	Summarizes the 16-bit long timer reload value (Lower 8 bits)
631Eh	1	CIU_TCounterVal_hi	Summarizes the 16-bit long timer actual value (Higher 8 bits)
631Fh	1	CIU_TCounterVal_lo	Summarizes the 16-bit long timer actual value (Lower 8 bits)
6320h	1	-	Reserved
6321h	1	CIU_TestSel1	General test signals configuration
6322h	1	CIU_TestSel2	General test signals configuration and PRBS control
6323h	1	CIU_TestPinEn	Enables test signals output on pins.
6324h	1	CIU_TestPinValue	Specifies the values for the 8-bit parallel bus when it is used as I/O bus

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ADDR	Byte size	Register name	Description
6325h	1	CIU_TestBus	Shows the status of the internal test bus
6326h	1	CIU_AutoTest	Controls the digital self-test
6327h	1	CIU_Version	Shows the CIU version
6328h	1	CIU_AnalogTest	Controls the pins AUX1 and AUX2
6329h	1	CIU_TestDAC1	Specifies the test value for the TestDAC1
632Ah	1	CIU_TestDAC2	Specifies the test value for the TestDAC2
632Bh	1	CIU_TestADC	Show the actual value of ADC I and Q
632Ch	1	-	Reserved for test use
632Dh	1	-	Reserved for test use
632Eh	1	-	Reserved for test use
632Fh	1	CIU_RFlevelDet	Power down of the RF level detector
6330h	1	CIU_SIC_CLK_en	Enables the use of secure IC clock on P34 / SIC_CLK.

8.6.23 CIU register description

8.6.23.1 CIU register bit behavior

Depending of the functionality of a register, the access condition to the bits can vary. The table below summarizes the access conditions:

Table 175. Behavior of register bits

Abbreviation	Behavior	Description
R/W	Read and Write	These bits may be written and read by the 80C51. Since they are used only for control means, there content is not influenced by internal state machines, e.g. CIU_CommIEn may be written and read by the CPU. It will also be read by internal state machines, but never changed by them.
DY	DYnamic	These bits may be written and read by the 80C51. Nevertheless, they may also be written automatically by CIU internal state machines, e.g. the commands in the CIU_Command register change their values automatically after their execution.
R	Read only	These registers hold flags, which value is determined by CIU internal states only, e.g. the CRCReady register can not be written from external but shows CIU internal states.
W	Write only	These registers are used for control means only. They may be written by the 80C51 but can not be read. Reading these registers returns always 0.
Reserved		These registers are unimplemented or reserved for internal test purposes.

8.6.23.2 CIU_SIC_CLK_en register (6330h)

Enables the use of P34 / SIC_CLK as secure IC clock.

Table 176. CIU_SIC_CLK_en register (address 6330h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	sic_clk_p34_en	-	-	-	Errorbusbitenable	Error	busbitse	1[2:0]
Reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R/W	R/W	R/W	R/W

Table 177. Description of CIU_SIC_CLK_en bits

Bit	Symbol	Description
7	sic_clk_p34_en	Set to 1, this bit configures P34 / SIC_CLK to be used as secure IC clock: SIC_CLK.
		Set to 0, P34 / SIC_CLK is in normal mode: P34.
6 to 4	-	Reserved

Bit	Symbol	Description
3	Errorbusbitenable	Set to 1, enable the error source selected by Errorbusbitsel on AUX pads in accordance with SelAux1 and SelAux2 bits (code 1010b).
2 to 0	Errorbusbitsel[2:0]	Define the error source on ErrorBusBit:

Value	Description
000	selects ProtocollErr on test bus
001	selects ParityErr on test bus
010	selects CRCErr on test bus
011	selects CollErr on test bus
100	selects BufferOvfl on test bus
101	selects RFErr on test bus
110	selects TempErr on test bus
111	selects WrErr on test bus

8.6.23.3 CIU_Command register (D1h or 6331h)

Starts and halts the command execution.

Table 178. CIU_Command register (address D1h or 6331h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	RcvOff	Power-down		Com	mand	
Reset	0	0	1	0	0	0	0	0
Access	R	R	R/W	DY	DY	DY	DY	DY

Table 179. Description of CIU_Command bits

Bit	Symbol	Description
7 to 6	-	Reserved
5	RcvOff	Set to 1, the analog part of the receiver is switched off.
4	Power-down	Set to 1, the CIU Power-down mode is entered. This means, internal current consuming blocks of the contactless analog module are switched off, except for the RF level detector. Set to 0, the NF532 starts the wake up procedure. During this procedure this bit still shows a 1. A 0 indicates that the NF532 is ready for operations; see Section 8.6.19.2 “ CIU Power-down ”.
		Note:The Power-down bit can not be set, when the SoftReset command has been activated.
3 to 0	Command	Activates a command according the Command Code. Reading this register shows, which command is actually executed. See Section 8.6.20 “ CIU command set ”

8.6.23.4 CIU_CommIEn register (D2h or 6332h)

Control bits to enable and disable the passing of interrupt requests.

Table 180. CIU_CommIEn register (address D2h or 6332h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	TxIEn	RXIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 181. Description of CIU_CommIEn bits

Bit	Symbol	Description
7	-	Reserved.
6	TxIEn	Setting this bit to 1 enables the transmitter interrupt request (indicated by bit TxIRq) to be propagated to CIU_IRQ_1.
5	RxIEn	Setting this bit to 1 enables the receiver interrupt request (indicated by bit RxIRq) to be propagated to CIU_IRQ_1.
4	IdleIEn	Setting this bit to 1 enables the idle interrupt request (indicated by bit IdleIRq) to be propagated to CIU_IRQ_0.
3	HiAlertIEn	Setting this bit to 1 enables the high alert interrupt request (indicated by bit HiAlertIRq) to be propagated to CIU_IRQ_1.
2	LoAlertIEn	Setting this bit to 1 enables the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to CIU_IRQ_1.
1	ErrIEn	Setting this bit to 1 enables the error interrupt request (indicated by bit ErrIRq) to be propagated to CIU_IRQ_0.
0	TimerIEn	Setting this bit to 1 enables the timer interrupt request (indicated by bit TimerIRq) to be propagated to CIU_IRQ_0.

8.6.23.5 CIU_DivIEn register (D3h or 6333h)

Controls bits to enable and disable the passing of interrupt requests.

Table 182. CIU_DivIEn register (address D3h or 6333h) bit allocation

Bit	7	6	5 4	3	2	1	0
Symbol	-	-	- SiginAct IEn	ModeIEn	CRCIEn	RfOnIEn	RfOffIEn
Reset	0	0	0 0	0	0	0	0
Access	R	R	R R/W	R/W	R/W	R/W	R/W

Table 183. Description of CIU_DivIEn bits

Bit	Symbol	Description
7 to 5	-	Reserved.
4	SiginAct IEn	Enables the SIGIN active interrupt request to be propagated to CIU_IRQ_0.
3	ModeIEn	Setting this bit to 1 enables the mode interrupt request (indicated by bit ModeIRq) to be propagated to CIU_IRQ_0.
2	CRCIEn	Setting this bit to 1 enables the CRC interrupt request (indicated by bit CRCIRq) to be propagated to CIU_IRQ_0.
1	RfOnIEn	Setting this bit to 1 enables the RF field on interrupt request (indicated by bit RfOnIRq) to be propagated to CIU_IRQ_0.
0	RfOffIEn	Setting this bit to 1 enables the RF field off interrupt request (indicated by bit RfOffIRq) to be propagated to CIU_IRQ_0.

8.6.23.6 CIU_CommIrq register (D4h or 6334h)

Contains common CIU interrupt request flags.

Table 184. CIU_CommIrq register (address D4h or 6334h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIrq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Reset	0	0	0	1	0	1	0	0
Access	W	DY	DY	DY	DY	DY	DY	DY

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Table 185. Description of CIU_CommIRQ bits

Bit	Symbol	Description
7	Set1	When written as 0, bits written as 1 in the write command are cleared in the register. When written as 1, bits written as 1 in the write command are set in the register.
6	TxIRq	Set to 1 immediately after the final bit of transmitted data has been sent.
5	RxIRq	Set to 1 when the receiver detects the end of a valid data stream. If RxNoErr in CIU_RxMode is 1, RxIRq is asserted only when data bytes are available in the FIFO.
4	IdleIrq	Set to 1 when a command terminates by itself, for example when CIU_Command changes from a command to Idle. An unknown command also causes the command register to return to Idle and sets IdleIrq. Starting Idle directly from the 80C51 does not set IdleIrq.
3	HiAlertIRq	Set to 1 when HiAlert in CIU_Status1 becomes 1. Unlike HiAlert, this flag latches the event and is cleared through Set1.
2	LoAlertIRq	Set to 1 when LoAlert in CIU_Status1 becomes 1. Unlike LoAlert, this flag latches the event and is cleared through Set1.
1	ErrIRq	Set to 1 when any error flag in CIU_Error is set.
0	TimerIRq	Set to 1 when the timer decrements TimerValue to zero.

Remark: Firmware shall clear all bits in CIU_CommIrq to 0 as required by the interrupt-handling sequence.

8.6.23.7 CIU_DivIrq register (D5h or 6335h)

Contains miscellaneous interrupt request flags. These bits are latched.

Table 186. CIU_DivIrq register (address D5h or 6335h) bit allocation

Bit	7	6	5 4	3	2	1	0
Symbol	Set2	-	- SiginActIrq	ModeIRq	CRCIRq	RfOnIRq	RfOffIRq
Reset	0	0	0 X	0	0	X	X
Access	W	R	R DY	DY	DY	DY	DY

Table 187. Description of CIU_DivIrq bits

Bit	Symbol	Description
7	Set2	When set to logic level 0 during write operation, the bit set to 1 in the write command are written to 0 in the register. When set to logic level 1 during write operation, the bit set to 1 in the write command are written to 1 in the register.
6 to 5	-	Reserved.
4	SiginActIrq	Set to 1, when SIGIN is active. See Section 8.6.13 “ NFC-WI/S 2 C interface support ”.This interrupt is set to 1 when either a rising or falling edge is detected on SIGIN~~.~~[1]
3	ModeIRq	Asserted to 1 when the mode has been detected by the Data Mode Detector. **Note**:The Data Mode Detector can only be activated by the AutoColl command and is terminated automatically having the detected the communication mode. **Note**:The Data Mode Detector is automatically restarted after each RF reset.
2	CRCIRq	Asserted to 1 when the CRC command is active and all data are processed.
1	RfOnIRq	Asserted to 1 when an external RF field is detected~~.~~[1] [2]

Bit	Symbol	Description
0	RfOffIRq	Asserted to 1 when an present external RF field is switched off.[1] [2]

- [1] At power-up, after reset modes (including Hard Power Down), the logical value of this bit is undefined.
- [2] After Power-Down bit of Table 181 goes from 1 to 0, after pd_rfleveldet bit of Table 286 goes from 1 to 0, the logical value of this bit is undefined.

8.6.23.8 CIU_Error register (D6h or 6336h)

Error flags showing the error status of the last command executed.

Table 188. CIU_Error register (address D6h or 6336h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	RFErr	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocollErr
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 189. Description of CIU_Error bits

Bit	Symbol	Description
7	WrErr	Set to 1 when the 80C51 writes to the FIFO during AutoColl or MFAuthent, or during the interval between the last transmitted RF bit and the last received RF bit.
6	TempErr	Set to 1 when the internal temperature sensor detects overheating; the antenna drivers are then switched off automatically.[1]
5	RFErr	Set to 1 in Active Communication mode if the counterpart does not switch on its RF field within the NFCIP-1 timing requirement. RFErr is only used in Active Communication mode; RxFraming or TxFraming must be 01h to enable this function.
4	BufferOvfl	Set to 1 if the 80C51 or internal state machine attempts to write to the FIFO while the FIFO is already full.
3	CollErr	Set to 1 when a bit collision is detected. It is cleared automatically at receiver start-up. This flag is valid only for bitwise anticollision at 106 kbit/s and remains 0 for 212/424 kbit/s communication.
2	CRCErr	Set to 1 when RxCRCEn is enabled and CRC verification fails. It is cleared automatically at receiver start-up.
1	ParityErr	Set to 1 when parity checking fails. It is cleared automatically at receiver start-up and is valid for ISO/IEC 14443A/MIFARE or NFCIP-1 at 106 kbit/s.
0	ProtocollErr	Set to 1 when a protocol error is detected, including: • Incorrect SOF at 106 kbit/s in Active or Passive Communication mode. • Byte-length violation during FeliCa or Active Communication above 106 kbit/s when DetectSync is enabled. • AutoColl with Initiator set to 1 in CIU_Control. • Incorrect received byte count during MFAuthent. • Miller decoder detecting two pauses shorter than the ISO/IEC 14443A minimum.

[1] Command execution clears all error flags except TempErr; firmware cannot set these flags.

8.6.23.9 CIU_Status1 register (DFh or 6337h)

Contains status flags of the CRC, Interrupt Request System and FIFO buffer.

Table 190. CIU_Status1 register (address DFh or 6337h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CIU_IRQ_1	CRCOk	CRCReady	CIU_IRQ_0	TRunning	RFOn	HiAlert	LoAlert
Reset	0	0	1	0	0	X	0	1
Access	R	R	R	R	R	R	R	R

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Table 191. Description of CIU_Status1 bits

Bit	Symbol	Description
7	CIU_IRQ_1	Shows whether any CIU_IRQ_1 source requests service, subject to CIU_CommIEn and CIU_DivIEn. IE1_2 must also be set to 1 for the CPU interrupt.
6	CRCOk	Set to 1 when the CRC result is zero. During ordinary transmission/reception, CRCOk is undefined; use CRCErr instead. During CRC coprocessor operation, it goes to 0 while calculating and returns to 1 when the calculation finishes correctly.
5	CRCReady	Set to 1 when the CRC calculation has completed. Valid for CRC-coprocessor calculation through CalcCRC.
4	CIU_IRQ_0	Shows whether any CIU_IRQ_0 source requests service, subject to CIU_CommIEn and CIU_DivIEn. IE1_3 must also be set to 1 for the CPU interrupt.
3	TRunning	Set to 1 while CIU_timer is running and will decrement CIU_TCounterVal_lo on the next timer clock. In gated mode, TRunning reflects timer enable by register settings and is not affected by the gate signal itself.
2	RFOn	Set to 1 when an external RF field is detected. This bit does not latch the RF field state.
1	HiAlert	Set to 1 when the FIFO occupancy satisfies 64 − FIFOLength ≤ WaterLevel. Example: FIFOLength = 60, WaterLevel = 4 → HiAlert = 1; FIFOLength = 59, WaterLevel = 4 → HiAlert = 0.
0	LoAlert	Set to 1 when the FIFO occupancy satisfies FIFOLength ≤ WaterLevel. Example: FIFOLength = 4, WaterLevel = 4 → LoAlert = 1; FIFOLength = 5, WaterLevel = 4 → LoAlert = 0.

8.6.23.10 CIU_Status2 register (E9h or 6338h)

Contain status flags of the receiver, transmitter and Data Mode Detector.

Table 192. CIU_Status2 register (address E9h or 6338h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TempSensClear	-	RFFreqOK	TgActivated	MFCrypto1On	Mod	emStat	e[2:0]
Reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	DY	DY	R	R	R

Table 193. Description of CIU_Status2 bits

Bit	Symbol	Descri	ption
7	TempSensClear	Set to l below t	ogic 1, this bit clears the temperature error, if the temperature is he alarm limit of 125° C.
6	-	Reserv	ed
5	RFFreqOK	Indicat 13.56 Set to l RX pin **Note**: freque 19 MH	es if the frequency detected at the RX pin is in the range of MHz. ogic 1, if the frequency at the RX pin is in the range 12 MHz < frequency < 15 MHz. The contents of RFFreqOK is not defined if the external RF ncy is in the range of 9 to 12 MHz or in the range of 15 to z.
4	TgActivated	Set to l Polling **Note**: Comm **Note**: field.	ogic 1 if the Select command is received correctly or if the command was answered. This bit can only be set during the AutoColl command in Passive unication mode or Card operating modes. Hardware clears this bit automatically by switching off the RF
3	MFCrypto1On	Set to l data co This bit MFAut MIFAR This bit	ogic 1, MIFARE Crypto1 unit is switched on and therefore all mmunication with the card is encrypted. can only be set to 1 by a successful execution of the hent command. This is only valid in Reader/Writer mode for E Classic 1K or MIFARE Classic 4K emulation cards. shall be cleared to 0 by firmware.
2 to 0	ModemState[2:0]	Modem machin **Value** 000	State shows the logic state of the transmitter and receiver state es. **Description** Idle
		001	Wait for StartSend in CIU_BitFraming register

Bit	Symbol	Descri	ption
		010 011 100	TxWait: Wait until RF field is present, if TxWaitRF is set to 1. The minimum time for TxWait is defined by the TxWait register. Transmitting RxWait: Wait until RF field is present, if the bit RxWaitRF is set to 1. The minimum time for RxWait is defined by the RxWait register
		101 110	Wait for data Receiving

8.6.23.11 CIU_FIFOData register (EAh or 6339h)

In- and output of 64 byte FIFO buffer.

Table 194. CIU_FIFOData register (address EAh or 6339h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				FIFOD	ata[7:0]			
Reset	X	X	X	X	X	X	X	X
Access	DY	DY	DY	DY	DY	DY	DY	DY

Table 195. Description of CIU_FIFOData bits

Bit	Symbol	Description
7 to 0	FIFOData[7:0]	Data input and output port for the internal 64 bytes FIFO buffer. The FIFO
		buffer acts as parallel in/parallel out converter for all data stream in- and outputs

8.6.23.12 CIU_FIFOLevel register (EBh or 633Ah)

Indicates the number of bytes held in the FIFO.

Table 196. CIU_FIFOLevel register (address EBh or 633Ah) bit allocation

Bit	7	6	5	4 3	2	1	0
Symbol	FlushBuffer			FIFOLevel[6:0]			
Reset	0	0	0	0 0	0	0	0
Access	W	R	R	R R	R	R	R

Table 197. Description of CIU_FIFOLevel bits

Bit	Symbol	Description
7	FlushBuffer	Set to 1, this bit clears the internal FIFO-buffer’s read- and write-pointer and the bit BufferOvfl in the CIU_Error register immediately.
		Reading this bit will always return 0.
6 to 0	FIFOLevel[6:0]	Indicates the number of bytes stored in the FIFO buffer. Writing to the CIU_FIFOData Register increments, reading decrements FIFOLevel.

8.6.23.13 CIU_WaterLevel register (ECh or 633Bh)

Specifies the thresholds for FIFO under- and overflow warning.

Table 198. CIU_WaterLevel register (address ECh or 633Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-			WaterLe	vel[6:0]		
Reset	0	0	0	0	1	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

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Table 199. Description of CIU_WaterLevel bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5 to 0	WaterLevel[5:0]	This register defines a threshold to indicate a FIFO buffer over- or underflow to the 80C51:
		The HiAlert bit in CIU_Status1 register is set to 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined WaterLevel[5:0] bits.
		The LoAlert bit in CIU_Status1 register is set to 1, if equal or less than WaterLevel[5:0] bits are in the FIFO.
		Remark:For the calculation of the HiAlert and LoAlert see Table 191 .

8.6.23.14 CIU_Control register (EDh or 633Ch)

Contains miscellaneous control bits.

Table 200. CIU_Control register (address EDh or 633Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	WrNFCIP-1IDtoFIFO	Initiator	-	RxL	astBits	[2:0]
Reset	0	0	0	0	0	0	0	0
Access	W	W	DY	R/W	R	R	R	R

Table 201. Description of CIU_Control bits

Bit	Symbol	Description
7	TStopNow	Set to 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to 1, the timer starts immediately. Reading this bit will always return 0.
5	WrNFCIP-1IDtoFIFO	Set to 1, the internal stored NFCID3 (10 bytes) is copied into the FIFO. Afterwards the bit is cleared to 0 automatically
4	Initiator	Set to 1, the NF532 acts as Initiator or Reader/Writer, otherwise it acts as Target. or a Card.
3	-	Reserved.
2 to 0	RxLastBits[2:0]	Shows the number of valid bits in the last received byte. If set to 000b, the whole byte is valid.

8.6.23.15 CIU_BitFraming register (EEh or 633Dh)

Adjustments for bit oriented frames.

Table 202. CIU_BitFraming register (address EEh or 633Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend		RxAlign[2:0]		-	Tx	LastBits[2	:0]
Reset	0	0	0	0	0	0	0	0
Access	W	R/W	R/W	R/W	R	R/W	R/W	R/W

Table 203. Description of CIU_BitFraming bits

Bit	Symbol	Description
7	StartSend	Set to 1, the transmission of data starts. This bit is only valid in combination with the Transceive command.

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Bit	Symbol	Description
6 to 4	RxAlign[2:0]	Used for reception of bit oriented frames: RxAlign[2:0] specifies the bit position for the first received bit to be stored in the FIFO. Further received bits are stored in the following bit positions. Example: RxAlign[2:0] = 0: The LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1. RxAlign[2:0] = 1: The LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2 RxAlign[2:0] = 7: The LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at bit position 0. These bits shall only be used for bitwise anticollision at 106 kbit/s in Passive Communication or Reader/Writer mode. In all other modes it shall be cleared to 0.
3	-	Reserved.
2 to 0	TxLastBits[2:0]	Used for transmission of bit oriented frames: TxLastBits defines the number of bits of the last byte that shall be transmitted. A 000b indicates that all bits of the last byte shall be transmitted.

8.6.23.16 CIU_Coll register (EFh or 633Eh)

Specifies the first bit collision detected on the RF interface.

Table 204. CIU_Coll register (address EFh or 633Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ValuesAfterColl	-	CollPosNotValid			CollPos		
Reset	1	0	1	X	X	X	X	X
Access	R/W	R	R	R	R	R	R	R

Table 205. Description of CIU_Coll bits

Bit	Symbol	Description
7	ValuesAfterColl	If this bit is 0, all receiving bits is cleared after a collision. This bit shall only be used during bitwise anticollision at 106 kbit/s, otherwise it shall be set to 1.
6	-	Reserved
5	CollPosNotValid	Set to 1, if no Collision is detected or the Position of the collision is out of range of the CollPos[4:0] bits. This bit shall only be interpreted in Passive Communication mode at 106 kbit/s or ISO/IEC 14443A/MIFARE Reader/Writer mode.
4 to 0	CollPos	These bits show the bit position of the first detected collision in a received frame, only data bits are interpreted. Example: 00h indicates a bit collision in the 32ndbit. 01h indicates a bit collision in the 1stbit 08h indicates a bit collision in the 8thbit This bit shall only be interpreted in Passive Communication mode at 106 kbit/s or ISO/IEC 14443A/MIFARE Reader/Writer mode if CollPosNotValid is cleared to 0.

8.6.23.17 CIU_Mode register (6301h)

Defines general modes for transmitting and receiving.

Table 206. CIU_Mode register (address 6301h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	DetectSync	TXWaitRF	RxWaitRF	PolSigin	ModeDet	CRC	Preset
						Off	[	1:0]
Reset	0	0	1	1	1	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 207. Description of CIU_Mode bits

Bit	Symbol	Description
7	MSBFirst	Set to 1, the CRC co-processor calculates the CRC with MSB first. The bit order in the registers CRCResultMSB and the CIU_CRCResultLSB is reversed.
		Note:During RF communication this bit is ignored.
6	DetectSync	If set to 1, the CIU waits for the F0h byte before the receiver is activated and F0h byte is added as a Sync-byte for transmission. This bit is only valid for 106 kbit/s during NFCIP-1 data exchange protocol.
		In all other modes it shall be cleared to 0.
5	TXWaitRF	Set to 1 the transmitter in Reader/Writer or Initiator mode for NFCIP-1 can only be started, if an own RF field is generated (i.e. Tx1RFEn and/or Tx2RFen is set to 1).
4	RxWaitRF	Set to 1, the counter for RxWait starts only, if an external RF field is detected in Target mode for NFCIP-1 or in Card Operating mode
3	PolSigin	PolSigin specifies the polarity of the SIGIN pin. Set to 1, the polarity of SIGIN pin is active high. Set to 0 the polarity of SIGIN pin is active low. **Note**:The internal envelope signal is coded active low. **Note**:Changing this bit will generate a SiginActIrq event.
2	ModeDetOff	Set to 1, the internal Data Mode Detector is switched off. **Note**:The Data Mode Detector is only active during the AutoColl command.
1 to 0	CRCPreset[1:0]	Specifies the preset value for the CRC co-processor for the CalCRC command.
		Note: During any communication, the preset values is selected automatically in accordance with the mode definition in the CIU_RxMode and CIU_TxMode registers.
		Value **Description**
		00 00 00
		01 63 63
		10 A6 71 11 FF FF

8.6.23.18 CIU_TxMode register (6302h)

Specifies the transmission data rate and framing during transmission.

Table 208. CIU_TxMode register (address 6302h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	Tx	Speed[2	:0]	InvMod	TxMix	TxFra	ming[1:0]
Reset	0	0	0	0	0	0	0	0
Access	R/W	DY	DY	DY	R/W	R/W	DY	DY

Table 209. Description of CIU_TxMode bits

Bit	Symbol	Description	
7	TxCRCEn	Set to 1 transmission	, this bit enables the CRC generation during data.
		Note:This b	it shall only cleared to 0 at 106 kbit/s.
6 to 4	TxSpeed[2:0]	Defines bit r	ate while data transmission.
		Value	**Description**
		000	106 kbit/s
		001	212 kbit/s

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Bit	Symbol	Description	
		010	424 kbit/s
		011	848 kbit/s
		100	1696 kbit/s
		101	3392 kbit/s
		110 - 111	Reserved
		Note:The bi to the bit cod the ISO/IEC	t coding for transfer speeds above 424 kbit/s is equivalent ing of the Active Communication mode of the 424 kbit/s of 18092 / ECMA340.
3	InvMod	Set to 1	, the modulation for transmitting data is inverted.
2	TxMix	Set to 1 Section 8.6.	, the signal at SIGIN is mixed with the internal coder. See 12 “ Serial data switch ”.
1 to 0	TxFraming[1:0]	Specifies the f	raming used for data transmission.
		Value	**Description**
		00	ISO/IEC 14443A/MIFARE and Passive Communication mode 106 kbit/s
		01	Active Communication mode
		10	FeliCa and Passive Communication mode at 212 kbit/s and 424 kbit/s
		11	ISO/IEC 14443B

8.6.23.19 CIU_RxMode register (6303h)

Specifies the reception data rate and framing during receiving.

Table 210. CIU_RxMode register (address 6303h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RXCRCEn	R	xSpeed[2	:0]	RxNoErr	RxMultiple	RxFra	ming[1:0]
Reset	0	0	0	0	0	0	0	0
Access	R/W	DY	DY	DY	R/W	R/W	DY	DY

Table 211. Description of CIU_RxMode bits

Bit Symbol Description 7 RxCRCEn Set to 1, this bit enables the CRC calculation during reception. The CRC bytes is not written within the CIU FIFO. **Note**: This bit shall only cleared to 0 at 106 kbit/s. 6 to 4 RxSpeed[2:0] Specifies the bit rate while data receiving. The analog part of the CIU handles only data rates up to 424 kbit/s internally, the digital part of the CIU handles the higher data rates as well.

6 to 4 RxSpeed[2:0] Specifies the bit rate while data receiving.

Value Description 000 106 kbit/s 001 212 kbit/s 010 424 kbit/s 011 848 kbit/s 100 1696 kbit/s 101 3392 kbit/s 110 - 111 Reserved Note: The bit coding for data rates above 424 kbit/s is equivalent to the bit coding of the active communication mode of the 424 kbit/s of the of the ISO/IEC18092 / ECMA340.

3 RxNoErr If set to 1, a not valid incoming data stream (less than 4 bits received) is ignored. The receiver will stay active. 2 RxMultiple Set to 0, the receiver is deactivated after receiving a data frame. Set to 1, it is supported to receive greater than one data frame. This bit is only valid for 212 and 424 kbit/s to handle the Polling command. Having set this bit, the receive and transceive commands will not end automatically. For this case the multiple receiving can only be deactivated by writing the Idle command to the CIU_Command register or clearing this bit by the 80C51. If set to 1, at the end of a incoming data stream an error byte is added to the FIFO. The error byte is a copy of the CIU_Error register.

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1 to 0 RxFraming[1:0] Specifies the expected framing for data reception.

Value	Description
00	ISO/IEC 14443A/MIFARE and Passive Communication mode 106 kbit/s
01	Active communication mode
10	FeliCa and Passive Communication mode at 212 kbit/s and 424 kbit/s
11	ISO/IEC 14443B

8.6.23.20 CIU_TxControl register (6304h)

Controls the logical behavior of the antenna driver pins TX1 and TX2. See alsoTable 154 and Table 155.

Table 212. CIU_TxControl register (address 6304h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2	InvTx1	InvTx2	InvTx1	Tx2	CheckRF	Tx2	Tx1
	RFon	RFon	RFoff	RFoff	CW		RFEn	RFEn
Reset	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W

Table 213. Description of CIU_TxControl bits

Bit	Symbol	Description
7	InvTx2RFon	With this bit = 1 and Tx2RFEn = 1, the TX2 output signal is inverted.
6	InvTx1RFon	With this bit = 1 and Tx1RFEn = 1, the TX1 output signal is inverted.
5	InvTx2RFoff	With this bit = 1 and Tx2RFEn = 0, the TX2 output signal is inverted.
4	InvTx1RFoff	With this bit = 1 and Tx1RFEn = 0, the TX1 output signal is inverted.
3	Tx2CW	Set to 1 to output a continuous unmodulated 13.56 MHz carrier on TX2. Set to 0 to allow modulation of the 13.56 MHz carrier.
2	CheckRF	When set to 1, Tx2RFEn and Tx1RFEn cannot be set while an external RF field is detected. Used together with Tx2RFAutoEn and Tx1RFAutoEn in CIU_TxAuto.
1	Tx2RFEn	Set to 1 to output the 13.56 MHz carrier on TX2, modulated by transmission data.
0	Tx1RFEn	Set to 1 to output the 13.56 MHz carrier on TX1, modulated by transmission data.

8.6.23.21 CIU_TxAuto register (6305h)

Controls the setting of the antenna driver.

Table 214. CIU_TxAuto register (address 6305h) bit allocation

Bit	7	6	5	4 3	2	1	0
Symbol	Auto	Force	AutoWakeUp	- CAOn	InitialRFOn	Tx2	Tx1
	RFOFF	100ASK				RFAutoEn	RFAutoEn
Reset	0	0	0	0 0	0	0	0
Access	R/W	R/W	R/W	R R/W	W	R/W	R/W

Table 215. Description of CIU_TxAuto bits

Bit	Symbol	Description
7	AutoRFOff	Set to 1 to switch off the locally generated RF field after the final data bit is transmitted, as defined by NFCIP-1.
6	Force100ASK	Set to 1 to force 100% ASK modulation independent of CIU_ModGsP.
5	AutoWakeUp	Set to 1 to allow the RF level detector to wake NF532 from CIU Power-down mode.

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Bit	Symbol	Description
4	-	Reserved.
3	CAOn	Set to 1 to activate collision avoidance and select the internal parameter n in accordance with ISO/IEC 18092 / ECMA-340 NFCIP-1.
2	InitialRFOn	Set to 1 to execute initial RF collision avoidance. InitialRFOn is cleared automatically when RF is switched on. The driver(s) to be enabled must be selected through Tx2RFAutoEn and/or Tx1RFAutoEn. If the RF field is already on when InitialRFOn is set, the bit is not cleared.
1	Tx2RFAutoEn	Set to 1 to switch RF on at TX2 after an external RF field disappears, in accordance with TADT. With InitialRFOn also set, TX2 is enabled if no external field is detected during TIDT. TADT and TIDT follow ISO/IEC 18092 / ECMA-340 NFCIP-1.
0	Tx1RFAutoEn	Set to 1 to switch RF on at TX1 after an external RF field disappears, in accordance with TADT. With InitialRFOn also set, TX1 is enabled if no external field is detected during TIDT. TADT and TIDT follow ISO/IEC 18092 / ECMA-340 NFCIP-1.

8.6.23.22 CIU_TxSel register (6306h)

Selects the sources for the analogue transmitter part

Table 216. CIU_TxSel register (address 6306h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LoadMo	dSel[1:0]	Driver	Sel[1:0]		SigOut	Sel[3:0]	
Reset	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 217. Description of CIU_TxSel bits

Bit	Symbol	Descript	ion
7 to 6	LoadMod - Sel[1:0]	Selects th	e signal to be output on LOADMOD
		Value	**Description**
		00	Tristate
		01	Modulation signal (envelope) from the internal coder
		10	Modulation signal (envelope) from SIGIN
		11	Test signal defined by LoadModtest in register CIU_TestSel1
5 to 4	Dri - verSel[1:0]	Selects th	e signals to be output on Tx1 and Tx2.
		Value	**Description**
		00	Tristate
		01	Modulation signal (envelope) from the internal coder
		10	Modulation signal (envelope) from SIGIN
		11	HIGH
		Note:Th InvTx1RF	e HIGH level depends on the setting of ON/InvTx1RFOff and InvTx2RFON/InvTx2RFOff.
3 to 0	SigOut - Sel[3:0]	Select th	e signal to be output on SIGOUT
		0000	Tristate
		0001	Low
		0010	High
		0011	Test bus signal as defined by TestBusBitSel in CIU_TestSel1.
		0100	Modulation signal (envelope) from the internal coder
		0101	Serial data stream to be transmitted

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Bit	Symbol	Descript	ion	
		0110	Output signal of the receiver circuit (card modulation signal regenerated and delayed). This signal is used as data output signal for secure IC interface connection using 3 lines.	
			Note:To have a valid signal the CIU has to be set to the receiving mode by either the Transceive or Re - ceive command. The RxMultiple bit may be used to keep the CIU in receiving mode. **Note**:Do not use this setting in ISO/IEC 14443A/ MIFARE mode. Data collisions will not be transmitted on SIGOUT when using Manchester coding.	
		0111	Serial data stream received.	
			Note:Do not use this setting in ISO/IEC 14443A/ MIFARE mode. Miller coding parameters as the bitlength can vary	
		1000-1011	FeliCa 1000	secure IC modulation RX*
			1001	TX
			1010 1011	Demodulator comparator output Reserved
			Note: receiv comm CIU in	* To have a valid signal the CIU has to be set to the ing mode by either the Transceive or Re - ceive ands. The bit RxMultiple may be used to keep the receiving mode
		1000-1011	MIFA	RE secure IC modulation
			1100	RX* with RF carrier
			1101	TX with RF carrier
			1110	RX with RF carrier unfiltered
			1111	RX envelope unfiltered
			Note: receiv comm CIU in	* To have a valid signal the CIU has to be set to the ing mode by either the Transceive or Re - ceive ands. The bit RxMultiple may be used to keep the receiving mode

8.6.23.23 CIU_RxSel register (6307h)

Selects internal receiver settings.

Table 218. CIU_RxSel register (address 6307h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UartS	el[1:0]			RxWa	it[5:0]		
Reset	1	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 219. Description of CIU_RxSel bits

Bit	Symbol	Description	
7 to 6	UartSel[1:0]	Selects the input **Value**	of the digital part (CL UART) of the CIU **Description**
		00	Constant Low
		01	Envelope signal at SIGIN
		10	Modulation signal from the internal analog part
		11	Modulation signal from SIGIN pin. Only valid for transfer speeds above 424 kbit/s
5 to 0	RxWait[5:0]	After data transm bit-clocks. Durin This parameter i (e.g. Transceive, the mode of the Communication transmitted data immediately afte	ission, the activation of the receiver is delayed for RxWait g this 'frame guard time' any signal at pin Rx is ignored. s ignored by the Receive command. All other commands Autocoll, MFAuthent) use this parameter. Depending on CIU, the counter starts differently. In Passive mode the counters starts with the last modulation of the stream. In Active Communication mode the counter starts r the external RF field is switched on.

8.6.23.24 CIU_RxThreshold register (6308h)

Selects thresholds for the bit decoder.

Table 220. CIU_RxThreshold register (address 6308h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol		MinLe	vel[3:0]		-		Collevel[2:0]	
Reset	1	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Table 221. Description of CIU_RxThreshold bits

Bit	Symbol	Description
7 to 4	MinLevel[3:0]	Specifies the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is not evaluated.
3	-	Reserved
2 to 0	Collevel[2:0]	Specifies the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

8.6.23.25 CIU_Demod register (6309h)

Defines demodulator settings.

Table 222. CIU_Demod register (address 6309h) bit allocation

Bit	7	6	5	4 3	2	1	0
Symbol	AddIQ	[1:0]	FixIQ	- TauRc	v[1:0]	TauSy	nc[1:0]
Reset	0	1	0	0 1	1	0	1
Access	R/W	R/W	R/W	R R/W	R/W	R/W	R/W

Table 223. Description of CIU_Demod bits

Bit	Symbol	Description
7 to 6	AddIQ[1:0]	Specifies the use of I and Q channel during reception. **Note**:FixIQ must be cleared to 0 to enable the following settings. ValueDescription 00Select the stronger channel 01Select the stronger and freeze the selected during communication 10Combines the I and Q channel 11RFU

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Bit	Symbol	Description
5	FixIQ	If set to 1 and AddIQ[0] is cleared to 0, the reception is fixed to I channel. If set to 1 and AddIQ[0] is set to 1, the reception is fixed to Q channel.
4	-	Reserved
3 to 2	TauRcv[1:0]	Changes time-constant of internal PLL during data receiving. **Note**:If set to 00h, the PLL is frozen during data receiving.
1 to 0	TauSync[1:0]	Changes time-constant of internal PLL during burst (out of data reception)

8.6.23.26 CIU_FelNFC1 register (630Ah)

Specifies the length of the FeliCa Sync bytes and the minimum length of the received frame.

Table 224. CIU_FelNFC1 register (address 630Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FelSync	Len[1:0]			DataLen	Min[5:0]		
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 225. Description of CIU_FelNFC1 bits

Bit	Symbol	Description
7 to 6	FelSyncLen[1:0]	Defines the Sync-byte length. Value: 00 → Sync bytes: B2 4D; 01 → 00 B2 4D; 10 → 00 00 B2 4D; 11 → 00 00 00 B2 4D
5 to 0	DataLenMin[5:0]	Defines the minimum accepted frame length: DataLenMin × 4 ≤ DataPacketLength. This parameter has no effect at 106 kbit/s when DetectSync in CIU_Mode is 0. Frames shorter than the configured DataLenMin are ignored.

8.6.23.27 CIU_FelNFC2 register (630Bh)

Specifies the maximum length of the received frame.

Table 226. CIU_FelNFC2 register (address 630Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WaitForSelected	ShortTimeSlot			DataLen	Max[5:0]		
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 227. Description of CIU_FelNFC2 bits

Bit	Symbol	Description
7	WaitForSelected	When set to 1, AutoColl ends automatically only after one of the following conditions: • A valid command is accepted after a valid ISO/IEC 14443A Select procedure. • A valid command is accepted after a valid FeliCa Polling procedure. **Note**: Active Communication is not supported while this bit is set. Enabling it can reduce 80C51 interaction during Passive Communication with another device in the same RF field.
6	ShortTimeSlot	Defines the time-slot length for Active Communication at 424 kbit/s. Set to 1 for a short time slot (half the 212 kbit/s slot); set to 0 for a long time slot (equal to the 212 kbit/s slot).
5 to 0	DataLenMax[5:0]	Defines the maximum accepted frame length: DataLenMax × 4 ≥ DataPacketLength. If the field is 0, the maximum data length is 256 bytes. This parameter has no effect at 106 kbit/s when DetectSync in CIU_Mode is 0. Frames longer than the configured DataLenMax are ignored.

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8.6.23.28 CIU_MifNFC register (630Ch)

Defines ISO/IEC 14443A/MIFARE/NFC specific settings in target or card operating state.

Table 228. CIU_MifNFC register (address 630Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Se	nsMiller[2	:0]	TauMil	ler[1:0]	MFHalted	TxW	ait[1:0]
Reset	0	1	1	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	DY	R/W	R/W

Table 229. Description of CIU_MifNFC bits

Bit	Symbol	Description
7 to 5	SensMiller[2:0]	This bit specifies the sensitivity of the Miller decoder.
4 to 3	TauMiller[1:0]	This bit specifies the time constant of the Miller decoder.
2	MFHalted	Set to 1, this bit indicates that the CIU is set to HALT mode in Card Operating mode at 106 kbit/s. This bit is either set by the 80C51 or by the internal state machine and indicates that only the code 52h is accepted as a Request command. This bit is automatically cleared to 0 by RF reset.
1 to 0	TxWait[1:0]	In combination with TxBitPhase[6:0] in CIU_TxBitPhase register, specifies the additional response time for the target at 106 kbit/s in Passive Communication mode and during the AutoColl command. See CIU_TxBitPhase register.

8.6.23.29 CIU_ManualRCV register (630Dh)

Allows manual fine tuning of the internal receiver.

IMPORTANT NOTE: For standard application it is not recommended to change this register settings.

Table 230. CIU_ManualRCV register (address 630Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	FastFilt MF_SO	Delay MF_SO	ParityDisable	LargeBWPLL	ManualHPCF	HPC	F[1:0]
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 231. Description of CIU_ManualRCV bits

Bit	Symbol	Description
7	-	Reserved
6	FastFiltMF_SO	If this bit is 1, the internal filter for the Miller-Delay circuit is set to Fast-Mode **Note**:This bit should only be set to 1, if the Miller pauses length expected are less than 400 ns. At 106 kbit/s, the Miller pauses duration is around 3µs.
5	DelayMF_SO	If this bit is 1, when SigoutSel=1100b (register 6306h), the Signal at SIGOUT-pin is delayed according the delay defined by TxBitPhase[6:0] (register 6315h) and TxWait bits (register 630Ch). **Note**:In ISO/IEC 14443A/MIFARE Card MIFARE Classic 1K or MIFARE Clasic 4K card emulation (Virtual Card) mode (DriverSel = 10b and SigoutSel=1110b), the Signal at SIGIN must then be 128 /fc faster compared to the ISO/IEC 14443A restrictions on the RF-Field for the Frame Delay Time. **Note**:This delay shall only be activated for setting bits SigOutSel to (1110b) or (1111b) in register CIU_TxSel. If this bit is 0, the SIGOUT-pin delay is not adjustable. **Note**:In ISO/IEC 14443A/MIFARE Card MIFARE Classic 1K or MIFARE Clasic 4K card emulation (Virtual Card) mode (DriverSel = 10b and SigoutSel=1110b), the ISO/IEC 14443A restrictions on the RF-Field for the Frame Delay Time should be adjusted on the secure IC side
4	ParityDisable	If this bit is 1, the generation of the Parity bit for transmission and the parity check for receiving is switched off. The received parity bit is handled like a data bit.

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Bit	Symbol	Description
3	LargeBWPLL	Set to 1, the bandwidth of the internal PLL for clock recovery is extended. **Note**:As the bandwidth is extended, the PLL filtering effect is weaker and the performance of the communication may be affected.
2	ManualHPCF	Set to 0, the HPCF[1:0] bits are ignored and the HPCF[1:0] settings are adapted automatically to the receiving mode.
1 to 0	HPCF[1:0]	Selects the High Pass Corner Frequency (HPCF) of the filter in the internal receiver chain
		Value **Description**
		00 For signals with frequency spectrum down to 106 kHz
		01 For signals with frequency spectrum down to 212 kHz
		10 For signals with frequency spectrum down to 424 kHz
		11 For signals with frequency spectrum down to 848 kHz

8.6.23.30 CIU_TypeB register (630Eh)

Selects the specific settings for the ISO/IEC 14443B

Table 232. CIU_TypeB register (address 630Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Rx	Rx	-	EOFSOF	NoTx	NoTx	TxEG	T[1:0]
	SOFReq	EOFReq		Width	SOF	EOF		
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Table 233. Description of CIU_TypeB bits

Bit	Symbol	Description
7	RxSOFReq	If this bit is 1, the SOF is required. A datastream starting without SOF is ignored. If this bit is 0, a datastream with and without SOF is accepted. The SOF will be removed and not written into the FIFO.
6	RxEOFReq	If this bit is 1, the EOF is required. A datastream ending without EOF will generate a protocol error: ProtocollErr in the CIU_Error register is set to 1. If this bit is 0, a datastream with and without EOF is accepted. The EOF will be removed and not written into the FIFO.
5	-	Reserved.
4	EOFSOFWidth	If this bit is 1, the SOF and EOF will have the maximum length defined in the ISO/IEC 14443B. If this bit is 0, the SOF and EOF will have the minimum length defined in the ISO/IEC 14443B.
3	NoTxSOF	If this bit is 1, the generation of the SOF is suppressed.
2	NoTxEOF	If this bit is 1, the generation of the EOF is suppressed.
1 to 0	TxEGT[1:0]	These bits define the length of the EGT, as defined in the ISO/IEC 14443B
		Value **Description**
		00 0 bit
		01 1 bit
		10 2 bits

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Bit	Symbol	Description
		11 3 bits

8.6.23.31 CIU_CRCResultMSB register (6311h)

Shows the actual MSB values of the CRC calculation.

Note: The CRC is split into two 8-bit registers. See also the CIU_CRCResultLSB register.

Note: Setting the bit MSBFirst in CIU_Mode register reverses the bit order, the byte order is not changed

Table 234. CIU_CRCResultMSB register (address 6311h) bit allocation

Bit	7	6	5	4 3	2	1	0
Symbol				CRCResultMSB[7:0]			
Reset	1	1	1	1 1	1	1	1
Access	R	R	R	R R	R	R	R

Table 235. Description of CIU_CRCResultMSB bits

Bit	Symbol	Description
7 to 0	CRCResultMSB[7:0]	This register shows the actual value of the most significant byte of
		the CRC calculation. It is valid only if CRCReady bit in CIU_Status1 register is set to 1.

8.6.23.32 CIU_CRCResultLSB register (6312h)

Shows the actual LSB values of the CRC calculation.

Note: The CRC is split into two 8-bit registers. See also the CIU_CRCResultMSB register.

Note: Setting the bit MSBFirst in CIU_Mode register reverses the bit order, the byte order is not changed

Table 236. CIU_CRCResultLSB register (address 6312h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				CRCResu	ltLSB[7:0]			
Reset	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R

Table 237. Description of CIU_CRCResultLSB bits

Bit	Symbol	Description
7 to 0	CRCResultLSB[7:0]	This register shows the actual value of the most significant byte of
		the CRC register. It is valid only if CRCReady bit in CIU_Status1 register is set to 1.

8.6.23.33 CIU_GsNOff register (6313h)

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when there is no RF produced by the NF532.

Table 238. CIU_GsNOff register (address 6313h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol		CWGsN	Off[3:0]			ModGs	NOff[3:0]	
Reset	1	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 239. Description of CIU_GsNOff bits

Bit	Symbol	Description
7 to 4	CWGsNOff[3:0]	The contents of this register specify the conductance of the output N-driver during the time of no modulation and when there is no RF generated by the NF532 (neither Tx1RFEn nor Tx2RFEn is set to 1). **Note**:The conductance value is binary weighted. **Note**:During CIU Power-down mode, if DriverSel[1:0] is not equal to 01b, CWGsNOff[3] is set to 1. This is not readable in the register. **Note**:The contents of the register is only used if no RF is generated by the driver, otherwise the value CWGsNOn in the CIU_GsNOn register is used.
3 to 0	ModGsNOff[3:0]	The contents of this register specify the conductance of the output N-driver for the time of modulation and when there is no RF generated by the NF532 (neither Tx1RFEn nor Tx2RFEn is set to 1). This may be used to regulate the modulation index when doing load modulation. **Note**:The conductance value is binary weighted. **Note**:During CIU Power-down, if DriverSel[1:0] is not equal to 01b, ModGsNOff[3] is set to 1. This is not readable in the register. **Note**:The contents of the register is only used if no RF is generated by the driver, otherwise the value ModGsNOn in the CIU_GsNOn register is used.

8.6.23.34 CIU_ModWidth register (6314h)

Controls the setting of the modulation width.

Table 240. CIU_ModWidth register (address 6314h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				ModWi	dth[7:0]			
Reset	0	0	1	0	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 241. Description of CIU_ModWidth bits

Bit	Symbol	Description
7 to 0	ModWidth[7:0]	These bits define the width of the Miller modulation as initiator in Active and Passive Communication mode as multiples of the carrier frequency (ModWidth+1 / fc). The maximum value is half the bit period.
		Acting as a target in Passive Communication mode at 106 kbit/s or in Card Operating mode for ISO/IEC 14443A/MIFARE these bits are used to change the duty cycle of the subcarrier frequency.
		Number of cycles with low value: NCLV = (Modwidth modulo 8)+1
		Number of cycles with high value: NCHV = 16 - NCLV

8.6.23.35 CIU_TxBitPhase register (6315h)

Adjust the bit phase at 106 kbit/s during transmission.

Table 242. CIU_TxBitPhase register (address 6315h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RcvClkChange			Tx	BitPhase[6	:0]		
Reset	1	0	0	0	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 243. Description of CIU_TxBitPhase bits

Bit	Symbol	Description
7	RcvClkChange	When set to 1, the demodulator clock is derived from the external RF field.
6 to 0	TxBitPhase[6:0]	Together with TxWait[1:0] in CIU_MifNFC (630Ch), defines an additional delay for bit synchroniza - tion in Passive Communication at 106 kbit/s and in ISO/IEC 14443A/MIFARE Reader/Writer mode. TxBitPhase represents the delay in carrier-clock cycles. **Recommended ranges**: TxWait = 01b with TxBitPhase = 1Bh to 7Fh (20 to 120 added clock cycles), or TxWait = 10b with TxBitPhase = 00h to 0Fh (121 to 136 added clock cycles). **Notes**: The required delay depends on the antenna circuit. When DriverSel = 01b, this delay is added before data transmission in all communication modes. When SigOutSel = 1110b and DelayMF_SO = 1b, the same delay is added to SIGOUT.

8.6.23.36 CIU_RFCfg register (6316h)

Configures the receiver gain and RF level detector sensitivity.

Table 244. CIU_RFCfg register (address 6316h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFLevelAmp		RxGain[2:0]			RFLe	vel[3:0]	
Reset	0	1	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 245. Description of CIU_RFCfg bits

Bit	Symbol	Descrip tion	
7	RFLevelAmp	Set to logi Section 8.	c 1, this bit activates the RF level detector' s amplifier, see 6.8 " RF level detector " .
6 to 4	RxGain[2:0]	This regis	ter specifies the receivers signal voltage gain factor:
		Value	Description
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	RFLevel[3:0]	Defines th 8.6.8 " RF	e sensitivity of the RF level detector, for description see Section level detector " .

8.6.23.37 CIU_GsNOn register (6317h)

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when generating RF.

Table 246. CIU_GsNOn register (address 6317h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol		CWGsN	On[3:0]			ModGsN	On[3:0]	
Reset	1	0	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 247. Description of CIU_GsNOn bits

Bit	Symbol	Description
7 to 4	CWGsNOn[3:0]	Defines the output N-driver conductance during non-modulated periods while NF532 generates the RF field. It can be used to control output power, current consumption and operating distance. The conductance code is binary weighted. During CIU Power-down, if DriverSel[1:0] ≠ 01b, CWGsNOn[3] is forced to 1 (not readable). This setting is used only while RF is generated by TX1/TX2; otherwise CWGsNOff in CIU_GsNOff applies.
3 to 0	ModGsNOn[3:0]	Defines the output N-driver conductance during modulation while NF532 generates the RF field. It can be used to adjust modulation index. The conductance code is binary weighted. During CIU Power-down, if DriverSel[1:0] ≠ 01b, ModGsNOn[3] is forced to 1 (not readable). This setting is used only while RF is generated by TX1/TX2; otherwise ModGsNOff in CIU_GsNOff applies.

8.6.23.38CIU_CWGsP register (6318h)

Specifies the conductance of the P-driver.

Table 248. CIU_CWGsP register (address 6318h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-			CWGs	P[5:0]		
Reset	0	0	1	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 249. Description of CIU_CWGsP bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5 to 0	CWGsP[5:0]	The contents of this register specify the conductance of the output P-driver, during times of no modulation. This may be used to regulate the output power and subsequently current consumption and operating distance.

Note: The conductance value is binary weighted.

Note: During CIU Power-down mode, if DriverSel[1:0] is not equal to 01b, CWGsP[5] is set to 1. This is not readable in the register.

8.6.23.39 CIU_ModGsP register (6319h)

Specifies the driver P-output conductance for the time of modulation.

Table 250. CIU_ModGsP register (address 6319h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-			ModGs	P[5:0]		
Reset	0	0	1	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 251. Description of CIU_ModGsP bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5 to 0	ModGsP[5:0]	The contents of this register specify the conductance of the output P-driver for
		the time of modulation.

This may be used to regulate the modulation index.

Note: The conductance value is binary weighted.

Note: During CIU Power-down mode, if DriverSel[1:0] is not equal to 01b, ModGsP[5] is set to 1. This is not readable in the register. **Note**: If Force100ASK in CIU_TxAuto register is set to 1, the ModGsP[5:0] setting has no effect.

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8.6.23.40 CIU_TMode register (631Ah)

Defines settings for the internal timer.

Table 252. CIU_TMode register (address 631Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TAuto	TGat	ed[1:0]	TAutoRestart		TPrescal	er_Hi[3:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 253. Description of CIU_TMode bits

Bit	Symbol	Description
7	TAuto	Set to 1, the timer starts automatically at the end of the transmission in all communication modes at all speed, or when InitialRFOn (in CIU_TxAuto) is set to 1 and the external RF field is switched on. The timer stops immediately after receiving the first data bit if RxMultiple in the CIU_RxMode register is cleared to 0. If RxMultiple is set to 1, the timer never stops. In this case the timer may be stopped by setting the bit TStopNow in register CIU_Control to 1. Set to 0 indicates, that the timer is not influenced by the protocol.
6 to 5	TGated[1:0]	The internal timer is running in gated mode. **Note**:In the gated mode, the bit TRunning is 1 when the timer is enabled by the register bits. This bit does not influence the gating signal **Value** **Description**
		00 No gated mode
		01 Gated by SIGIN
		10 Gated by AUX1
		11 Reserved
4	TAutoRestart	Set to 1 the timer automatically restart its count-down from TReloadValue defined within when reaches zero. Set to 0 the timer decrements to zero and the bit TimerIRq is set to 1.
3 to 0	TPrescaler_Hi[3:0]	Defines higher 4 bits for the TPrescaler. The following formula serves to calculate fTimer:
		fTimer 6,78MHz TPreScaler ÷ =
		For detailed description seeSection 8.6.17 “ CIU_timer ” . **Note**:TPreScaler is defined with TPreScaler_Hi[3:0] in this register and TPreScaler_LO[7:0] in CIU_TPrescaler.

8.6.23.41 CIU_TPrescaler register (631Bh)

Define the LSB of the Timer-Prescaler.

Table 254. CIU_TPrescaler register (address 631Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				TPrescaler	_LO[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 255. Description of CIU_TPrescaler bits

Bit	Symbol	Description
7 to 0	TPres - caler_LO[7:0]	Defines lower 8 bits for TPrescaler. The following formula serves to calculate fTimer: fTimer = 6,78MHz ÷ TPreScaler. For detailed description see Section 8.6.17 “CIU_timer”.

Note: The TPreScaler time is defined with TPreScaler_Hi[3:0] in CIU_TMode and TPreScaler_LO[7:0] in this register.

8.6.23.42 CIU_TReload_hi register (631Ch)

Specifies the MSB of the 16-bit long timer reload value.

Table 256. CIU_TReloadVal_hi register (address 631Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				TReloadV	al_Hi[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 257. Description of CIU_TReloadVal_hi bits

Bit	Symbol	Description
7 to 0	TReloadV - al_Hi[7:0]	Specifies the higher 8 bits for the TReloadValue. With a start event the timer loads with the TReload - Value. Changing this register affects the timer only with the next start event. **Note**: The reload value is defined with TReloadVal_Hi[7:0] in this register and TReloadVal_Lo[7:0] in CIU_TReloadVal_lo.

8.6.23.43 CIU_TReloadVal_lo register (631Dh)

Specifies the LSB of the 16 bit long timer reload value.

Table 258. CIU_TReload_lo register (address 631Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				TReloadV	al_Lo[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 259. Description of CIU_TReload_lo bits

Bit	Symbol	Description
7 to 0	TReloadVal_Lo[7:0]	Specifies the lower 8 bits for the TReloadValue.

With a start event the timer writes with the TReloadValue. Changing this register affects the timer only with the next start event. **Note**: The reload value is defined with TReloadVal_Lo[7:0] in this register and TReloadVal_Hi[7:0] in CIU_TReload_Hi.

8.6.23.44 CIU_TCounterVal_hi register (631Eh)

Specifies the MSB byte of the current value of the timer.

Table 260. CIU_TCounterVal_hi register (address 631Eh) bit allocation

Bit	7	6	5	4 3	2	1	0
Symbol				TCounterVal_Hi[7:0]			
Reset	x	x	x	x x	x	x	x
Access	R	R	R	R R	R	R	R

Table 261. Description of CIU_TCounterVal_hi bits

Bit	Symbol	Description
7 to 0	TCounterVal_Hi[7:0]	MSB of the current value of the timer (Higher 8 bits).

8.6.23.45 Register CIU_TCounterVal_lo (631Fh)

Specifies the LSB byte of the current value of the timer.

Table 262. CIU_TCounterVal_lo register (address 631Fh) bit allocation

Bit	7	6	5 4 3	2	1	0
Symbol			TCounterVal_LO[7:0]			
Reset	x	x	x x x	x	x	x
Access	R	R	R R R	R	R	R

Table 263. Description of CIU_TCounterVal_lo bits

Bit	Symbol	Description
7 to 0	TCounterVal_LO[7:0]	LSB of the current value of the timer (Lower 8 bits).

8.6.23.46 CIU_TestSel1 register (6321h)

General test signal configuration.

Table 264. CIU_TestSel1 register (address 6321h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LoadMo	dTst[1:0]	SICclk	sel[1:0]	SICClkD1	TstB	usBitSe	l[2:0]
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 265. Description of CIU_TestSel1 bits

Bit	Symbol	Description	
7 to 6	LoadModTst[1:0]	Defines the **Note**:The b 1 to en	test signal for the LOADMOD pin its LoadModSel in register CIU_TxSel has to be set to able LoadModTst:
		Value	**Description**
		00	Low
		01	High
		10	RFU
		11	TstBusBit as defined by the TestBusBitSel bit of this register
5 to 4	SICclksel[1:0]	Defines the	source for the 13.56 MHz secure IC clock
		Value	**Description**
		00	GND - secure IC clock is switched off
		01	Clock derivated by the internal oscillator
		10	Internal CIU clock
		11	Clock derivated from the RF Field
3	SICClkD1	Set to logic observe_ciu	1, the secure IC clock is delivered to P31 / UART_TX if the bit is set to 1.
2 to 0	TstBusBitSel(2:0]	Select the T	stBusBit from the test bus.

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8.6.23.47 CIU_TestSel2 register (6322h)

General test signal configuration and PRBS control.

Table 266. CIU_TestSel2 register (address 6322h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15		Tst	BusSel[4	:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 267. Description of CIU_TestSel2 bits

Bit	Symbol	Description
7	TstBusFlip	If set to 1, the internal test bus(D6-D0) is mapped to the external test bus pins by the following order: D4,D3, D2,D6,D5, D0, D1. See Section 8.6.21.2 “ CIU test bus ”.
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-T0150. **Note**:All relevant register to transmit data have to be configured before entering PRBS9 mode. **Note**:The data transmission of the defined sequence is started by the Transmit command.
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-T0150. **Note**:All relevant register to transmit data have to be configured before entering PRBS15 mode.
		Note:The data transmission of the defined sequence is started by the Transmit command.
4 to 0	TstBusSel[4:0]	Selects the test bus source. SeeSection 8.6.21.2 “ CIU test bus ”.

8.6.23.48 CIU_TestPinEn register (6323h)

Enable the output drivers for the test pins.

Table 268. CIU_TestPinEn register (address 6323h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol				TestPin	En[7:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 269. Description of CIU_TestPinEn bits

Bit	Symbol	Description
7 to 0	TestPinEn[7:0]	Each of the bit enables the output driver for an internal test pin: P70_IRQ (MSB), RSTOUT_N, P35, P34 / SIC_CLK, P33_INT1, P32_INT0, P31 /
		UART_TX, P30 / UART_RX (LSB). DataEn[7] enables P70_IRQ, DataEn[0] enables P30 / UART_RX.
		Note:The data transmission of the defined sequence is started by the Transmit command.

8.6.23.49 CIU_TestPinValue register (6324h)

Specifies the settings for the 7 bit test bus signals to be I/O on P70_IRQ, RSTOUT_N, P35, P34 / SIC_CLK, P33_INT1, P32_INT0, P31 / UART_TX and P30 / UART_RX pins.

Table 270. CIU_TestPinValue register (address 6324h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	useio			Tes	tPinValue[	6:0]		
Reset	0	0	0	0	0	0	0	0

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Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 271. Description of CIU_TestPinValue bits

Bit	Symbol	Description
7	useio	Set to 1, this bit enables the I/O functionality for the internal test
		bus on the pins P70_IRQ (MSB), RSTOUT, P35, P34 / SIC_CLK, P33_INT1, P32_INT0, P31 / UART_TX, P30 / UART_RX (LSB)
		Note:Before using P34 / SIC_CLK as a test output, the SVDD switch should be closed. See register address 6106h.
6 to 0	TestPinValue[6:0]	UseIO set to 1, Read or write the value of the test bus.
		UseIO cleared to 0, Read 000_0000. No write.

8.6.23.50 CIU_TestBus register (6325h)

Shows the state of the internal test bus.

Table 272. CIU_TestBus register (address 6325h) bit allocation

Bit	7	6	5	4 3	2	1	0
Symbol				TestBus[7:0]			
Reset	x	x	x	x x	x	x	x
Access	R	R	R	R R	R	R	R

Table 273. Description of CIU_TestBus bits

Bit	Symbol	Description
7 to 0	TestBus[7:0]	Shows the status of the internal test bus. The test bus is selected by the register CIU_TestSel2.
		See Section 8.6.21.2 “ CIU test bus ” .

8.6.23.51 CIU_AutoTest register (6326h)

Controls the digital self-test.

Table 274. CIU_AutoTest register (address 6326h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	AmpRcv	-	-		SelfTe	st[3:0]	
Reset	0	1	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

Table 275. Description of CIU_AutoTest bits

Bit	Symbol	Description
7	-	Reserved.
6	AmpRcv	Set to 1 the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit/s. **Note**:Due to non linearity the effects of MinLevel and CollLevel in CIU_RxThreshold register are as well non linear.
5 to 4	-	Reserved
3 to 0	SelfTest[3:0]	Enables the digital Self Test. The self-test may be started by the Selftest command in the CIU_Command register. The self-test is enabled by 1001. **Note**:For default operation the self-test has to be disabled (0000).

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8.6.23.52 CIU_Version register (6327h)

Shows the version of the CIU.

Table 276. CIU_Version register (address 6327h) bit allocation

Bit	7	6 5	4	3	2	1	0
Symbol		Product[3:0]			Versi	on[3:0]	
Reset	1	0 0	0	0	0	0	0
Access	R	R R	R	R	R	R	R

Table 277. Description of CIU_Version bits

Bit	Symbol	Description
7 to 4	Product	Product 1000 (NF532)
3 to 0	Version	Version 0000

8.6.23.53 CIU_AnalogTest register (6328h)

Controls the pins AUX1 and AUX2.

Table 278. CIU_AnalogTest register (address 6328h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol		AnalogSe	lAux1[3:0]			AnalogSel	Aux2[3:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 279. Description of CIU_AnalogTest bits

Bit	Symbol	Descr	iption
7 to 4	AnalogSelAux1[3:0]	Contr Sectio	ols the AUX1 pin. Note: All test signals are described in n 8.6.21.3 “ Test signals at pin AUX ”.
		0000	Tristate
		0001	DAC output: register CIU_TestDAC1[1]
		0010	DAC output: test signal corr1[1]
		0011	DAC output: test signal corr2[1]
		0100	DAC output: test signal MinLevel[1]
		0101	DAC output: ADC_I[1]
		0110	DAC output: ADC_Q[1]
		0111	DAC output: ADC_I combined with ADC_Q[1]
		1000	Test signal for production test
		1001	secure IC clock
		1010	ErrorBusBit as described inTable 177
		1011	Low
		1100	TxActive At 106 kbit/s: High during Start bit, Data bits, Parity and CRC At 212 kbit/s and 424 kbit/s: High during Preamble, Sync, Data bits and CRC
		1101	RxActive
		1110	At 106 kbit/s: High during Data bits, Parity and CRC At 212 kbit/s and 424 kbit/s: High during Data bits and CRC Subcarrier detected

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Bit	Symbol	Descr	iption
			At 106 kbit/s: not applicable At 212 kbit/s and 424 kbit/s: High during last part of preamble, Sync, Data bits and CRC.
		1111	Test bus bit as defined by the TstBusBitSel inTable 265
3 to 0	AnalogSelAux2[3:0]	Contr Sectio	ols the AUX2 pin. Note: All test signals are described in n 8.6.21.3 “ Test signals at pin AUX ”.
		0000	Tristate
		0001	DAC output: register CIU_TestDAC2[2]
		0010	DAC output: test signal corr1[2]
		0011	DAC output: test signal corr2[2]
		0100	DAC output: test signal MinLevel[2]
		0101	DAC output: ADC_I[2]
		0110	DAC output: ADC_Q[2]
		0111	DAC output: ADC_I combined with ADC_Q[2]
		1000	Test signal for production test
		1001	secure IC clock
		1010	ErrorBusBit as described inTable 177
		1011	Low
		1100	TxActive At 106 kbit/s: High during Start bit, Data bits, Parity and CRC At 212 kbit/s and 424 kbit/s: High during Preamble, Sync, Data bits and CRC
		1101	RxActive
			At 106 kbit/s: High during Data bits, Parity and CRC At 212 kbit/s and 424 kbit/s: High during Data bits and CRC
		1110	Subcarrier detected
			At 106 kbit/s: not applicable At 212 kbit/s and 424 kbit/s: High during last part of preamble, Sync, Data bits and CRC.
		1111	Test bus bit as defined by the TstBusBitSel inTable 264

- [1] Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.
- [2] Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.

8.6.23.54 CIU_TestDAC1 register (6329h)

Specifies the test value for TestDAC1.

Table 280. CIU_TestDAC1 register (address 6329h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-			TestDA	C1[5:0]		
Reset	0	0	X	X	X	X	X	X
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 281. Description of CIU_TestDAC1 bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5 to 0	TestDAC1[5:0]	Specifies the test value for TestDAC1. The output of the DAC1 may be switched to AUX1 by setting AnalogSelAux1 to 0001 in the CIU_AnalogTest register.

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8.6.23.55 CIU_TestDAC2 register (632Ah)

Specifies the test value for TestDAC2.

Table 282. CIU_TestDAC2 register (address 632Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-			TestDA	C2[6:0]		
Reset	0	0	X	X	X	X	X	X
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 283. Description of CIU_TestDAC2 bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5 to 0	TestDAC2[6:0]	Specifies the test value for TestDAC2. The output of the DAC2 can be
		switched to AUX2 by setting AnalogSelAux2 to 0001 in the
		CIU_AnalogTest register.

8.6.23.56 CIU_TestADC register (632Bh)

Shows the actual value of ADC I and Q channel.

Table 284. CIU_TestADC register (address 632Bh) bit allocation

Bit	7	6	5	4	3 2	1	0
Symbol		ADC_I[3:0]			ADC_Q[3:0]		
Reset	X	X	X	X	X X	X	X
Access	R	R	R	R	R R	R	R

Table 285. Description of CIU_TestADC bits

Bit	Symbol	Description
7 to 4	ADC_I[3:0]	Shows the actual value of ADC I channel.
3 to 0	ADC_Q[3:0]	Shows the actual value of ADC Q channel.

8.6.23.57 CIU_RFlevelDet register (632Fh)

Power down of the RF level detector.

Table 286. CIU_RFlevelDet register (address 632Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	pd_rflvldet	-	-	-	-
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 287. Description of CIU_RFlevelDet bits

Bit	Symbol	Description
7 to 5	-	Reserved. These bits must be cleared to 0.
4	pd_rfleveldet	Power down of the RF level detector.
		When this bit is set to 1, the RF level detector is in power down mode.
3 to 0	-	Reserved. These bits must be cleared to 0.

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8.7 Registers map

8.7.1 Standard registers

Table 288. Standard registers mapping

Register address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1
6000h to 6102h	Reserved							
6103h	Config IO_I1	int1_pol	Reserved	pad_I1	Reserved	pad_I0	enselif	Selif[1
6104h	Observe_testbus	Reserved						
6105h	Data_rng	data_rng						
6106h	Control_switch_rng	Reserved	hide_svdd_sig	sic_switch_overload	sic_switch_en	Reserved	cpu_need_rng	random_
6107h	GPIRQ	gpirq_level_P71	gpirq_level_P50	gpirq_level_P35	gpirq_level_P34	gpirq_enable_P71	gpirq_enable_P50	gpirq_e
6108h	Reserved							
6109h	LDO	Reserved		overcurrent_status	sel_overcurrent[1:0]		enoffset	soft_hi
610Ah	i²c_wu_control	Reserved					i²c_wu_en_wr	i²c_wu_e
610Bh	Reserved							
610Ch	Andet_control	andet_bot	andet_up	andet_ithl[1:0]		andet_ithh[2:0]		
610Dh	Reserved							
610Eh	NFC_WI_control	Reserved				nfc_wi_status	Reserved	nfc_wi_
610Fh to 61FFh	Reserved							
6200h	PCR CFR	Reserved						cpu_fre
6201h	PCR CER	Reserved				hsu_enable	Reserved	
6202h	PCR ILR	Reserved	por_pulse_latched	Reserved	enable_pdselif	Reserved	gpirq_level	int1_le
6203h	PCR Control	Reserved						clear_w
6204h	PCR Status	i²c_wu	gpirq_wu	SPI_wu	HSU_wu	CIU_wu	Reserved	int1_wu
6205h	PCR Wakeupen	i²c_wu_en	GPIRQ_wu_en	SPI_on_en	HSU_on_en	CIU_wu_en	Reserved	int1_en
6206h to 6300h	Reserved							
6301h	CIU_Mode	MSBFirst	DetectSync	TXWaitRF	RxWaitRF	PolSigin	ModeDetOff	CRCPres
6302h	CIU_TxMode	TxCRCEn	TxSpeed[2:0]			InvMod	TxMix	TxFrami
6303h	CIU_RxMode	RXCRCEn	RxSpeed[2:0]			RxNoErr	RxMultiple	RxFrami
6304h	CIU_TxControl	InvTx2RFon	InvTx1RFon	InvTx2RFoff	InvTx1RFoff	Tx2CW	CheckRF	Tx2RFEn
6305h	CIU_TxAuto	AutoRFOFF	Force100ASK	AutoWakeUp	Reserved	CAOn	InitialRFOn	Tx2RFAu
6306h	CIU_TxSel	LoadModSel[1:0]		DriverSel[1:0]		SigOutSel[3:0]		
6307h	CIU_RxSel	UartSel[1:0]		RxWait[5:0]				
6308h	CIU_RxThreshold	MinLevel[3:0]				Reserved	Collevel[2:0]	
6309h	CIU_Demod	AddIQ[1:0]		FixIQ	Reserved	TauRcv[1:0]		TauSync
630Ah	CIU_FelNFC1	FelSyncLen[1:0]		DataLenMin[5:0]				
630Bh	CIU_FelNFC2	WaitForSelected	ShortTimeSlot	DataLenMax[5:0]				
630Ch	CIU_MifNFC	SensMiller[2:0]			TauMiller[1:0]		MFHalted	TxWait[
630Dh	CIU_ManualRCV	Reserved	FastFiltMF_SO	DelayMF_SO	ParityDisable	LargeBWPLL	ManualHPCF	HPCF[1:
630Eh	CIU_TypeB	RxSOFReq	RxEOFReq	Reserved	EOFSOFWidth	NoTxSOF	NoTxEOF	TxEGT[1

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Register address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1
630Fh to 6310h	Reserved							
6311h	CIU_CRCResultMSB	CRCResultMSB[7:0]						
6312h	CIU_CRCResultLSB	CRCResultLSB[7:0]						
6313h	CIU_GsNOff	CWGsNOff[3:0]				ModGsNOff[3:0]		
6314h	CIU_ModWidth	ModWidth[7:0]						
6315h	CIU_TxBitPhase	RcvClkChange	TxBitPhase[6:0]					
6316h	CIU_RFCfg	RFLevelAmp	RxGain[2:0]			RFLevel[3:0]		
6317h	CIU_GsNOn	CWGsNOn[3:0]				ModGsNOn[3:0]		
6318h	CIU_CWGsP	Reserved		CWGsP[5:0]				
6319h	CIU_ModGsP	Reserved		ModGsP[5:0]				
631Ah	CIU_TMode	TAuto	TGated[1:0]		TAutoRestart	TPrescaler_Hi[3:0]		
631Bh	CIU_TPrescaler	TPrescaler_LO[7:0]						
631Ch	CIU_TReloadVal_Hi	TReloadVal_Hi[7:0]						
631Dh	CIU_TReloadVal_Lo	TReloadVal_Lo[7:0]						
631Eh	CIU_TCounterVal_hi	TCounterVal_Hi[7:0]						
631Fh	CIU_TCounterVal_lo	TCounterVal_LO[7:0]						
6320h	Reserved							
6321h	CIU_TestSel1	LoadModTst[1:0]		SICclksel[1:0]		SICClkD1	TstBusBitSel[2:0]	
6322h	CIU_TestSel2	TstBusFlip	PRBS9	PRBS15	TstBusSel[4:0]			
6323h	CIU_TestPinEn	TestPinEn[7:0]						
6324h	CIU_TestPinValue	useio	TestPinValue[6:0]					
6325h	CIU_TestBus	TestBus[7:0]						
6326h	CIU_AutoTest	Reserved	AmpRcv	Reserved		SelfTest[3:0]		
6327h	CIU_Version	Product				Version		
6328h	CIU_AnalogTest	AnalogSelAux1[3:0]				AnalogSelAux2[3:0]		
6329h	CIU_TestDAC1	Reserved		TestDAC1[5:0]				
632Ah	CIU_TestDAC2	Reserved		TestDAC2[5:0]				
632Bh	CIU_TestADC	ADC_I[3:0]				ADC_Q[3:0]		
632Ch to 632Eh	Reserved							
632Fh	CIU_RFlevelDet	Reserved			pd_rfleveldet	Reserved		
6330h	SIC_CLK	sic_clk_p34_en	Reserved			Errorbusbitenable	Errorbusbitsel[2:0]	
6331h	CIU_Command	Reserved		RcvOff	Power-down	Command		
6332h	CIU_CommIEn	Reserved	TxIEn	RXIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn
6333h	CIU_DivIEn	Reserved			SiginAct IEn	ModeIEn	CRCIEn	RfOnIEn
6334h	CIU_CommIrq	Set1	TxIRq	RxIRq	IdleIrq	HiAlertIRq	LoAlertIRq	ErrIRq
6335h	CIU_DivIrq	Set2	Reserved		SiginActIrq	ModeIRq	CRCIRq	RfOnIRq

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Register address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1
6336h	CIU_Error	WrErr	TempErr	RFErr	BufferOvfl	CollErr	CRCErr	ParityE
6337h	CIU_Status1	CIU_IRQ_1	CRCOk	CRCReady	CIU_IRQ_0	TRunning	RFOn	HiAlert
6338h	CIU_Status2	TempSensClear	Reserved	RFFreqOK	TgActivated	MFCrypto1On	ModemState[2:0]	
6339h	CIU_FIFOData	FIFOData[7:0]						
633Ah	CIU_FIFOLevel	FlushBuffer	FIFOLevel[6:0]					
633Bh	CIU_WaterLevel	Reserved		WaterLevel[5:0]				
633Ch	CIU_Control	TStopNow	TStartNow	WrNFCIP-1IDtoFIFO	Initiator	Reserved	RxLastBits[2:0]	
633Dh	CIU_BitFraming	StartSend	RxAlign[2:0]			Reserved	TxLastBits[2:0]	
633Eh	CIU_Coll	ValuesAfterColl	Reserved	CollPosNotValid		CollPos		
633Fh to FFFFh	Reserved							

8.7.2 SFR registers

Table 289. SFR registers mapping

Register address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
80h	Reserved								
81h[1]	SP Stack Pointer	SP[7:0]							
82h[1]	DPL Data Pointer Low	DPL[7:0]							
83h[1]	DPH Data Pointer High	DPH[7:0]							
84h to 86h	Reserved								
87h	PCON	SMOD	Reserved					CPU_PD	Reserved
88h	T01CON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	T01MOD	GATE1	C/T1	M11	M10	GATE0	C/T0	M01	M00
8Ah	T0L	T0L.7	T0L.6	T0L.5	T0L.4	T0L.3	T0L.2	T0L.1	T0L.0
8Bh	T1L	T1L.7	T1L.6	T1L.5	T1L.4	T1L.3	T1L.2	T1L.1	T1L.0
8Ch	T0H	T0H.7	T0H.6	T0H.5	T0H.4	T0H.3	T0H.2	T0H.1	T0H.0
8Dh	T1H	T1H.7	T1H.6	T1H.5	T1H.4	T1H.3	T1H.2	T1H.1	T1H.0
8Eh to 97h	Reserved								
98h	SOCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	SOBUF	SOBUF[7:0]							
9Ah	RWL	RWaterlevel[7:0]							
9Bh	TWL	TWaterlevel[7:0]							
9Ch	FIFOFS	Transmit-Freespace[7:0]							
9Dh	FIFOFF	ReceiveFull-ness[7:0]							
9Eh	SFF	FIFO_EN	Reserved	TWLL	TFF	TFE	RWLH	RFF	RFE
9Fh	FIT	Reset	Reserved	WCOL_IRQ	TWLL_IRQ	TFF_IRQ	RWLH_IRQ	ROVR_IRQ	RFF_IRQ
A0h	Reserved								
A1h	FITEN	TFLUSH	RFLUSH	EN_W-COL_IRQ	EN_T-WLL_IRQ	EN_TFF_IRQ	EN_RWLH_IRQ	EN_ROVR_IRQ	EN_RFF_IRQ

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Register address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A2h	FDATA	FDATA[7:0]							
A3h	FSIZE	ReceiveSize[7:0]							
A4h to A7h	Reserved								
A8h	IE0	IE0_7	IE0_6	IE0_5	IE0_4	IE0_3	IE0_2	IE0_1	IE0_0
A9h	SPIcontrol	Reserved		Enable	Reserved	CPHA	CPOL	IE1	IE0
AAh	SPIstatus	Reserved				TR_FE	RCV_OVR	Reserved	READY
ABh	HSU_STA	set_bit	Reserved		disable_preamb	irq_rx_over_en	irq_rx_fer_en	irq_rx_over	irq_rx_fer
ACh	HSU_CTR	hsu_wu_en	start_frame	tx_stopbit[1:0]		rx_stopbit	tx_en	rx_en	soft_reset_n
ADh	HSU_PRE	hsu_prescaler[7:0]							
AEh	HSU_CNT	hsu_counter[7:0]							
AFh	Reserved								
B0h	P3	Reserved		P3[5]	P3[4]	P3[3]	P3[2]	P3[1]	P3[0]
B1h to B7h	Reserved								
B8h	IP0	IP0_7	IP0_6	IP0_5	IP0_4	IP0_3	IP0_2	IP0_1	IP0_0
B9h to C7h	Reserved								
C8h	T2CON	TF2	Reserved	RCLK0	TCLK0	Reserved	TR2	C/T2	CP/RL2
C9h	T2MOD	Reserved					T2RD		DCEN
CAh	RCAP2L	R2L.7	R2L.6	R2L.5	R2L.4	R2L.3	R2L.2	R2L.1	R2L.0
CBh	RCAP2H	R2H.7	R2H.6	R2H.5	R2H.4	R2H.3	R2H.2	R2H.1	R2H.0
CCh	T2L	T2L.7	T2L.6	T2L.5	T2L.4	T2L.3	T2L.2	T2L.1	T2L.0
CDh	T2H	T2H.7	T2H.6	T2H.5	T2H.4	T2H.3	T2H.2	T2H.1	T2H.0
CEh to CFh	Reserved								
D0h[1]	PSW Program Status Word	PSW[7:0]							
D1h	CIU_Command	Reserved		RcvOff	Power-down	Command			
D2h	CIU_CommIEn	Reserved	TxIEn	RXIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
D3h	CIU_DivIEn	Reserved			SiginActIEn	ModeIEn	CRCIEn	RfOnIEn	RfOffIEn
D4h	CIU_CommIrq	Set1	TxIRq	RxIRq	IdleIrq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
D5h	CIU_DivIrq	Set2	Reserved		SiginActIrq	ModeIRq	CRCIRq	RfOnIRq	RfOffIRq
D6h	CIU_Error	WrErr	TempErr	RFErr	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocollErr
D7h	Reserved								
D8h	I^2CCON	CR[2]	ENS1	STA	STO	SI	AA	CR[1:0]	
D9h	I^2CSTA	ST[7:0]							
DAh	I^2CDAT	I^2CDAT[7:0]							
DBh	I^2CADR	SA[6:0]							GC
DCh to DEh	Reserved								
DFh	CIU_Status1	CIU_IRQ_1	CRCOk	CRCReady	CIU_IRQ_0	TRunning	RFOn	HiAlert	LoAlert
E0h[1]	ACC Accumulator	ACC[7:0]							

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Register address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E1h to E7h	Reserved								
E8h	IE1	IE1_7	Reserved	IE1_5	IE1_4	IE1_3	IE1_2	Reserved	IE1_0
E9h	CIU_Status2	TempSensClear	Reserved	RFFreqOK	TgActivated	MFCrypto1On	Modem State[2:0]		
EAh	CIU_FIFOData	FIFOData[7:0]							
EBh	CIU_FIFOLevel	FlushBuffer	FIFOLevel[6:0]						
ECh	CIU_WaterLevel	WaterLevel[5:0]							
EDh	CIU_Control	TStopNow	TStartNow	WrNF CIP-1ID to FIFO	Initiator	Reserved	RxLast Bits[2:0]		
EEh	CIU_BitFraming	StartSend	RxAlign[2:0]			Reserved	TxLast Bits[2:0]		
EFh	CIU_Coll	ValuesAfterColl	Reserved	CollPos NotValid		CollPos			
F0h[1]	B register	B[7:0]							
F1h to F3h	Reserved								
F4h	P7CFGA						P7CFGA[2]	P7CFGA[1]	P7CFGA[0]
F5h	P7CFGB						P7CFGB[2]	P7CFGB[1]	P7CFGB[0]
F6h	Reserved								
F7h	P7						P7[2]	P7[1]	P7[0]
F8h	IP1	IP1_7	Reserved	IP1_5	IP1_4	IP1_3	IP1_2	Reserved	IP1_0
F9h	Reserved								
FAh[1]	XRAMP						XRAMP[4:0]		
FBh	Reserved								
FCh	P3CFGA			P3CFGA[5]	P3CFGA[4]	P3CFGA[3]	P3CFGA[2]	P3CFGA[1]	P3CFGA[0]
FDh	P3CFGB			P3CFGB[5]	P3CFGB[4]	P3CFGB[3]	P3CFGB[2]	P3CFGB[1]	P3CFGB[0]
FEh to FFh	Reserved								

[1] This register is not specified in this document as it is a standard 80C51 register.

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9 Limiting values

Table 290. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
PVDD	Supply Voltage			-0.5	4	V
VBAT	Power Supply Voltage			-0.5	6.0	V
Ptot	Total power dissipation				500	mW
ITVDD	Maximum current in TVDD		[1]		150	mA
ISVDD	Maximum current in SVDD switch				30	mA
VESD	Electrostatic discharge voltage					
VESDH	ESD Susceptibility (Human Body model)	1500Ω, 100pF; EIA/JESD22-A114-D			±2.0	kV
VESDM	ESD Susceptibility (Machine model)	0.75 mH, 200 pF; EIA/JESD22-A115-A			200	V
VESDC	ESD Susceptibility (Charge Device model)	Field induced model; EIA/JESC22-C101-C			±1.0	kV
Tstg	Storage temperature			-55	150	° C
Tj	Junction temperature			-40	125	° C

[1] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

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10 Recommended operating conditions

Table 291. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Tamb	Ambient Temperature			-30	+25	+85	° C
VBAT	Power Supply Voltage	VSS= 0 V	[1] [2]	2.7		5.5	V
PVDD	Supply Voltage for host interface	VSS= 0 V	[3]	1.6	1.8 to 3.3	3.6	V

- [1] VSS represents DVSS, TVSS1, TVSS2, AVSS.
- [2] Supply voltage of VBAT below 3.3 V reduces the carry outance (e.g. the achievable operating distance).
- [3] The device can supply PVDD=0V and to use the NF532 with reduced functionality (see Section 8.4 “Power management”)

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11 Thermal characteristics

Table 292. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rthj-a	thermal resistance	in free air		37	41.1	K/W
	from junction to ambient	with exposed pad soldered on a				
		4 layer Jedec PCB-0.5				

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12 Characteristics

Unless otherwise specified, the limits are given for the full operating conditions. The typical value is given for 25° C, VBAT = 3.4 V and PVDD = 3 V.

Timings are only given from characterization results.

12.1 Power management characteristics

Table 293. Power management characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Battery power supply range	VSS= 0 V	2.7		5.5	V
VDVDD	LDO output	VBAT > 3.4 V IDVDD= 150 mA	2.7	3	3.4	V
LDOOFF	LDO offset	VBAT = 3.4 V IDVDD=150 mA Offset enabled	300	400	700	mV
Vth1	Reset threshold on DVDDfalling		2.04	2.32	2.6	V
Vhys1	Vth1 hysteresis		40		90	mV
Cdec	DVDD decoupling capacitor	Low ESR, like X7R or X5R ceramic capacitor [1]	10			µF
PSR	Power supply rejection on DVDD	LDO offset enabled. F <10 kHz. Cdec = 10µF		-46		dB
FcPSR	PSR -3dB cut-off frequency	Standard LDO mode. Cdec = 10µF		10		kHz
SVDD	SVDDoutput voltage	VBAT > 3.4 V ISVDD= 30 mA	2.7		3.3	VV

[1] Decreasing the decoupling capacitance can decrease the power supply bursts rejection.

[2] The capacitance should be placed closed to the pins, and may be splitted (see Figure 51)

12.2 Overcurrent detection

The following values are guaranteed by design. Only functional testing is done in production for case Sel_overcurrent1 = Sel_overcurrent0 =1.

Table 294. Overcurrent detection characteristics

Symbol	Parameter	Conditions Min	Typ	Max	Unit
IOvercurrent	IDVDDthreshold for overcurrent detection	Sel_overcurrent1=0 Sel_overcurrent0=0	300		mA
		Sel_overcurrent1=0	210		mA
		Sel_overcurrent0=1			
		Sel_overcurrent1=1	180		mA
		Sel_overcurrent0=0			
		Sel_overcurrent1=1	150		mA
		Sel_overcurrent0=1			

12.3 Current consumption characteristics

Table 295. Current consumption characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IHPD	Hard-Power-Down current	VBAT = 3.4 V PVDD = 3 V	[5]			2	µA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ISPD	Soft-Power-Down current	VBAT = 3.6 V PVDD = 3 V RF level detector ON	[5] [7]		25	45	µA
ISPD	Soft-Power-Down current	VBAT = 3.6 V PVDD = 3 V RF level detector OFF	[5] [7]		18	40	µA
IAVDD	Analog supply current	VBAT = 3.4 V PVDD = 3 V			3	10	mA
IPVDD	Pad supply current		[2]		0.5	45	mA
ISVDD	Secure IC supply current	Switch closed	[3]		3	30	mA
ITVDD	Transmitter supply current	Continuous wave, VBAT = 3.4 V	[1]		60	100	mA
IVBAT	Total supply current	Continuous wave, VBAT = 3.4 V	[4] [6]			150	mA

- [1] Typical value with a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz.
- [2] IPVDD is determined by the overall load at the pins. The maximum is given assuming 4mA output current for the I/O or output pads.
- [3] ISVDD is determined by the overall load on SVDD pad.
- [4] During operation with recommended antenna tuning circuitry the overall current is below 100 mA.
- [5] ISPD and IHPD denote the total current drawn from all supply domains for the characterized device configuration.
- [6] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)
- [7] These values are valid when applied the Soft-Power-Down sequence specified in Section 8.5.4 , and with TESTEN pin connected with DVSS.

12.4 Antenna presence self test thresholds

The following values are guaranteed by design. Testing is done in production for cases andet_ith1[1:0]=10b and for andet_ithh[2:0]=011b.

The operating range is:

- VBAT voltage above 5V
- Ambient temperature between 0 and 40° C

Table 296. Antenna presence detection lower levels characteristics

Symbol	Parameter	Conditions	Min Typ	Max	Unit
IAndetH	IDVDDlower current threshold for	andet_ith1[1:0] = 10b	20	37	mA
	antenna presence detection	andet_ith1[1:0] = 11b	27	49	mA

Table 297. Antenna Presence Detection Upper Levels characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IAndetH	IDVDDupper current threshold for	andet_ithh[2:0] = 000b	31		56	mA
	antenna presence detection	andet_ithh[2:0] = 001b	42		74	mA
		andet_ithh[2:0] = 010b	52		92	mA
		andet_ithh[2:0] = 011b	63		110	mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		andet_ithh[2:0] = 100b	73		128	mA
		andet_ithh[2:0] = 101b	84		146	mA
		andet_ithh[2:0] = 110b	94		164	mA
		andet_ithh[2:0] = 111b	105		182	mA

12.5 Typical 27.12 MHz Crystal requirements

Table 298. Crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fXTAL	XTAL frequency		27.107	27.12	27.133	MHz
ESR	Equivalent series resistance			50		Ω
CLOAD	Load capacitance			10		pF
PXTAL	Drive level		100			µW

12.6 Pin characteristics for 27.12 MHz XTAL Oscillator (OSCIN, OSCOUT)

Table 299. Pin characteristics for 27.12 MHz XTAL Oscillator (OSCIN, OSCOUT)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CinOSCIN	OSCIN Input Capacitance	AVDD= 2.8 V, VDC = 0.65 V, VAC = 0.9 Vpp			2		pF
VOHOSCOUT	High level output voltage				1.1		V
VOLOSCOUT	Low level output voltage				0.2		V
CinOSCOUT	OSCOUT Input Capacitance				2		pF
fOSCIN	Clock Frequency	with appropriate quartz and capacitances values	[1]		27.12		MHz
DFEC	Duty Cycle of Clock Frequency	with appropriate quartz and capacitances values	[1]	45	50	55	%
tjitter	Jitter of Clock Edges	with appropriate quartz and capacitances values	[1]			10	ps RMS

- [1] See the Figure 51 as an example of appropriate connected components. The layout should ensure minimum distance between the pins and the components

12.7 RSTPD_N input pin characteristics

Table 300. RSTPD_N input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level input voltage	PVDD > 1.6 V	0.9×PVDD		3.6	V
VIH	High level input voltage	PVDD < 0.4 V (seeSection 8.4)	0.65×VBAT		3.6	V
VIL	Low level input voltage	PVDD > 1.6 V	0		0.4	V
VIL	Low level input voltage	PVDD < 0.4 V (seeSection 8.4)	0		0.4	V
IIH	High level input current	VI= PVDD	-1		1	µA
IIL	Low level input current	VI= 0 V	-1		1	µA
Cin	Input capacitance			2.5		pF

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12.8 Input pin characteristics for I0 and I1

Table 301. Input pin characteristics for I0, I1 and TESTEN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level input voltage		[1] 0.7×DVDD		DVDD	V
VIL	Low level input voltage		[2] 0		0.3×DVDD	V
IIH	High level input current I0 and I1	VI = DVDD	-1		1	µA
IIL	Low level input current	VI= 0 V	-1		1	µA
Cin	Input capacitance			2.5		pF

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is DVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.

12.9 RSTOUT_N output pin characteristics

Table 302. RSTOUT_N output pin characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VOH	High level output voltage	PVDD= 3 V, IOH= -4 mA		0.7×PVDD		PVDD	V
		PVDD= 1.8 V, IOH= -2 mA	[2]	0.7×PVDD		PVDD	V
VOL	Low level output voltage	PVDD= 3 V, IOL= 4 mA		0		0.3×PVDD	V
		PVDD= 1.8 V, IOL= 2 mA	[2]	0		0.3×PVDD	V
Cout	Load capacitance					30	pF
trise,fall	Rise and fall times	PVDD= 3 V, VOH= 0.8×PVDD, VOL= 0.2×PVDD, Cout= 30 pF	[1]		13.5		ns
		PVDD= 1.8 V, VOH= 0.7×PVDD, VOL= 0.3×PVDD, Cout= 30 pF			10.8		ns

- [1] IOH and IOL give the output drive capability from which the rise and fall times may be calculated as a function of the load capacitance.
- [2] Data at PVDD= 1.8V are only given from characterization results.

12.10 Input/output characteristics for pin P70_IRQ

Table 303. Input/output pin characteristics for pin P70_IRQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level input voltage		[1]	0.7×PVDD		PVDD	V
VIL	Low level input voltage		[2]	0		0.3×PVDD	V
VOH	Push-pull mode high level output voltage	PVDD= 3 V, IOH= -4 mA		0.7×PVDD		PVDD	V
		PVDD= 1.8 V, IOH= -2 mA	[3]	0.7×PVDD		PVDD	V
VOL	Push-pull mode low level output voltage	PVDD= 3 V, IOL= 4 mA		0		0.3×PVDD	V
		PVDD= 1.8 V, IOL= 2 mA	[3]	0		0.3×PVDD	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IIH	Input mode high level input current	VI = DVDD		-1		1	μA
IIL	Input mode low level input current	VI = 0 V		-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V		-1		1	μA
Cin	Input capacitance				2.5		pF
Cout	Load capacitance					30	pF
trise,fall	Rise and fall times	PVDD= 3 V, VOH= 0.8×PVDD, VOL= 0.2×PVDD, Cout= 30 pF			13.5		ns
		PVDD= 1.8 V, VOH= 0.7×PVDD, VOL= 0.3×PVDD, Cout= 30 pF			10.8		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is PVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V
- [3] Data at PVDD= 1.8V are only given from characterization results.

12.11 Input/output pin characteristics for P30 / UART_RX, P31 / UART_TX, P32_INT0, P33_INT1

Table 304. Input/output pin characteristics for P30 / UART_RX, P31 / UART_TX, P32_INT0, P33_INT1

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level input voltage		[1]	0.7×PVDD		PVDD	V
VIL	Low level input voltage		[2]	0		0.3×PVDD	V
VOH	Push-pull mode high level output voltage	PVDD= 3 V, IOH= -4 mA		PVDD- 0.4		PVDD	V
		PVDD= 1.8 V, IOH= -2 mA	[3]	PVDD- 0.4		PVDD	V
VOL	Push-pull mode low level output voltage	PVDD= 3 V, IOL= 4 mA		0		0.4	V
		PVDD= 1.8 V, IOL= 2 mA	[3]	0		0.4	V
IIH	Input mode high level input current	VI = PVDD		-1		1	μA
IIL	Input mode low level input current	VI = 0 V		-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V		-1		1	μA
Cin	Input capacitance				2.5		pF
Cout	Load capacitance					30	pF
trise,fall	Rise and fall times	PVDD= 3 V, VOH= 0.8×PVDD, VOL= 0.2×PVDD, Cout= 30 pF			13.5		ns
		PVDD= 1.8 V, VOH= 0.7 PVDD, VOL= 0.3×PVDD, Cout= 30 pF			10.8		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is PVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V
- [3] Data at PVDD= 1.8V are only given from characterization results.

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12.12 Input/output pin characteristics for P34 / SIC_CLK

Table 305. Input/output pin characteristics for P34 / SIC_CLK

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level input voltage		[1] 0.7×SVDD		SVDD	V
VIL	Low level input voltage		[2] 0		0.3×SVDD	V
VOH	Push-pull mode high level output voltage	VBAT = 3.4 V, IOH= -4 mA	SVDD- 0.4		SVDD	V
VOL	Push_pull mode low level output voltage	VBAT = 3.4 V, IOL= 4 mA	0		0.4	V
IIH	Input mode high level input current	VI= SVDD	-1		1	μA
IIL	Input mode low level input current	VI= 0 V	-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V	-1		1	μA
Cin	Input Capacitance			2.5		pF
Cout	Load Capacitance				30	pF
trise,fall	Rise and fall times	VBAT= 3.4 V, VOH= 0.8×SVDD, VOL= 0.2×SVDD, Cou t= 30 pF		13.5		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is SVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.

12.13 Input/output pin characteristics for P35

Table 306. Input/output pin characteristics for P35

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level Input voltage		[1] 0.7×DVDD		DVDD	V
VIL	Low level Input voltage		[2] 0		0.3×DVDD	V
VOH	High level output voltage	VBAT = 3.4 V, IOH= -4 mA	DVDD- 0.4		DVDD	V
VOL	Low level output voltage	VBAT = 3.4 V, IOL= 4 mA	0		0.4	V
IIH	High level input current	VI = DVDD	-1		1	μA
IIL	Low level input current	VI = 0 V	-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V	-1		1	μA
Cin	Input Capacitance			2.5		pF
Cout	Load Capacitance				30	pF
trise,fall	Rise and fall times	VBAT= 3.4 V, VOH= DVDD- 0.4, VOL= 0.4, Cou t= 30 pF		16.5		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is DVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.

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12.14 Input pin characteristics for NSS / P50_SCL / HSU_RX

Table 307. Input pin characteristics for NSS / HSU_RX for HSU / SPI interfaces

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level Input voltage	PVDD> 1.6V	[1] [3] 0.7×PVDD		PVDD	V
VIL	Low level Input voltage	PVDD> 1.6V	[2] 0		0.3×PVDD	V
IIH	High level input current	VI = DVDD	-1		1	μA
IIL	Low level input current	VI = 0 V	-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V	-1		1	μA
Cin	Input Capacitance			2.5		pF
TSP	Width of suppressed spikes			20		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is PVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.
- [3] When PVDD is not present, it is not possible to define a high level on NSS. When by means of SPI host interface, a wake-up condition can not be avoided if PVDD is absent.

Table 308. Input/open drain output pin characteristics for P50_SCL for I²C interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7×PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3×PVDD	V
VOL	Low level output voltage	PVDD= 3 V, IOL= 4 mA		0		0.3	V
		PVDD= 1.8 V, IOL= 2 mA	[3]	0		0.3	V
IIH	High level input current	VI = DVDD		-1		1	μA
IIL	Low level input current	VI = 0 V		-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V		-1		1	μA
Cin	Input Capacitance				2.5		pF
Cout	Load Capacitance					30	pF
TSP	Width of suppressed spikes	Out of SPD mode			20		ns
TSP	Width of suppressed spikes	In SPD mode			120		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is PVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.
- [3] Data at PVDD= 1.8V are only given from characterization results.

12.15 Input/output pin characteristics for MOSI / SDA / HSU_TX

Table 309. Input/output pin characteristics for MOSI / HSU_TX for HSU and SPI Interfaces

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level Input voltage		[1] 0.7×PVDD		PVDD	V
VIL	Low level Input voltage		[2] 0		0.3×PVDD	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH	HSU_TX high level output voltage	PVDD= 3 V, IOH= -4 mA	PVDD- 0.4		PVDD	V
		PVDD=1.8 V, IOH= -2 mA	[3] PVDD- 0.4		PVDD	V
VOL	HSU_TX low level output voltage	PVDD= 3 V, IOL= 3 mA	0		0.3	V
IIH	MOSI high level input current	VI = DVDD	-1		1	μA
IIL	MOSI low level input current	VI = 0 V	-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V	-1		1	μA
Cin	Input Capacitance			2.5		pF
Cout	Load Capacitance				30	pF
TSP	Width of suppressed spikes			20		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is PVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.
- [3] Data at PVDD= 1.8V are only given from characterization results.

Table 310. Input/open drain output pin characteristics for SDA for I²C interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level Input voltage		[1] 0.7×PVDD		PVDD	V
VIL	Low level Input voltage		[2] 0		0.3×PVDD	V
VOL	Low level output voltage	PVDD= 3 V, IOL= -4 mA	0		0.3	V
		PVDD=1.8 V, IOL= -2 mA	[3] 0		0.3	V
IIH	High level input current	VI = DVDD	-1		1	μA
IIL	Low level input current	VI = 0 V	-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V	-1		1	μA
Cin	Input Capacitance			2.5		pF
Cout	Load Capacitance				30	pF
TSP	Width of suppressed	Out of SPD mode		20		ns
	spikes	In SPD mode		150		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is PVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.
- [3] Data at PVDD= 1.8V are only given from characterization results.

12.16 Input/output pin characteristics for MISO / P71 and SCK / P72

Table 311. Input/output pin characteristics for MISO / P71 and SCK / P72

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7×PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3×PVDD	V
VOH	Push_pull / MISO mode high level output voltage	PVDD= 3 V, IOH= -4 mA		PVDD- 0.4		PVDD	V
		PVDD=1.8 V, IOH= -2 mA	[3]	PVDD- 0.4		PVDD	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VOL	Push_pull / MISO mode low level output voltage	PVDD= 3 V, IOL= -4 mA		0		0.4	V
		PVDD=1.8 V, IOL= -2 mA	[3]	0		0.4	V
IIH	Input mode high level input current	VI = DVDD		-1		1	μA
IIL	Input mode low level input current	VI = 0 V		-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V		-1		1	μA
Cin	Input Capacitance				2.5		pF
Cout	Load Capacitance					30	pF
TSP	Width of suppressed spikes	Only valid for SCK			15		ns

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is PVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.
- [3] Data at PVDD= 1.8 V are only given from characterization results.

12.17 Input pin characteristics for SIGIN

Table 312. Input/output pin characteristics for SIGIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level Input voltage		[1] 0.7×SVDD		SVDD	V
VIL	Low level Input voltage		[2] 0		0.3×SVDD	V
IIH	High level input current	VI= SVDD	-1		1	μA
IIL	Low level input current	VI= 0 V	-1		1	μA
ILeak	Input leakage current	RSTPD_N = 0.4 V	-1		1	μA
Cin	Input Capacitance			2.5		pF

- [1] To minimize power usage when in Soft-Power-Down mode, the limit is SVDD - 0.4 V.
- [2] To minimize power usage when in Soft-Power-Down mode, the limit is 0.4 V.

12.18 Output pin characteristics for SIGOUT

Table 313. Output pin characteristics for SIGOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH	High level output voltage	DVDD- 0.1 < SVDD< DVDD IOH= -4 mA	SVDD- 0.4		SVDD	V
VOL	Low level output voltage	DVDD- 0.1 < SVDD< DVDD IOL= +4 mA	0		0.4	V
ILeak	Input leakage current	RSTPD_N = 0.4 V	-1		1	μA
Cin	Input Capacitance			2.5		pF
Cout	Load Capacitance				30	pF
trise,fall	Rise and fall times	VBAT = 3.4 V, VOH= 0.8×SVDD, VOL= 0.2×SVDD, Cout= 30 pF		9		ns

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12.19 Output pin characteristics for LOADMOD

Table 314. Output pin characteristics for LOADMOD

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH	High level output voltage	VBAT = 3.4 V, IOH= -4 mA	DVDD -0.4		DVDD	V
VOL	Low level output voltage	VBAT = 3.4 V, IOL= 4 mA	0		0.4	V
Cout	Load Capacitance				10	pF
trise,fall	Rise and fall times	VBAT = 3.4 V, VOH= 0.8×DVDD, VOL×= 0.2×DVDD, Cout= 10 pF		4.5		ns

12.20 Input pin characteristics for RX

Table 315. Input pin characteristics for RX

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VINRX	Dynamic Input voltage Range	VBAT = 3.4 V		-1		AVDD+1	V
Cinrx	RX Input Capacitance				10		pF
Rinrx	RX Input Series resistance	VBAT = 3.4 V, Receiver active, VRX = 1 Vpp, 1.5 V DC offset			350		Ω
VRX,MinIV,Mill	Minimum Dynamic Input voltage, Miller coded	VBAT = 3.4 V, 106 kbit/s			150	500	mVpp
VRX,MinIV,Man	Minimum Dynamic Input voltage, Manchester Coded	VBAT = 3.4 V, 212 and 424 kbit/s			100	200	mVpp
VRX,MaxIV,Mill	Maximum Dynamic Input voltage, Miller coded	VBAT = 3.4 V, 106 kbit/s		AVDD+1			Vpp
VRX,MaxIV,Man	Maximum Dynamic Input voltage, Manchester Coded	VBAT = 3.4 V, 212 and 424 kbit/s		AVDD+1			Vpp
VmRX,Mill	Minimum Modulation index, Miller coded	VBAT = 3.4 V, 106 kbit/s VRX = 1.5 Vpp, SensMiller = 3			33		%
VRXMod,Man	Minimum modulation voltage	VBAT = 3.4 V, RxGain = 6 and 7	[1]			6	mV
VRXMod,Man	Minimum modulation voltage	VBAT = 3.4 V, RxGain = 4 and 5	[1]			18	mV
VRXMod,Man	Minimum modulation voltage	VBAT = 3.4 V, RxGain = 0 to 3	[1]			120	mV

[1] The minimum modulation voltage is valid for all modulation schemes except Miller coded signals.

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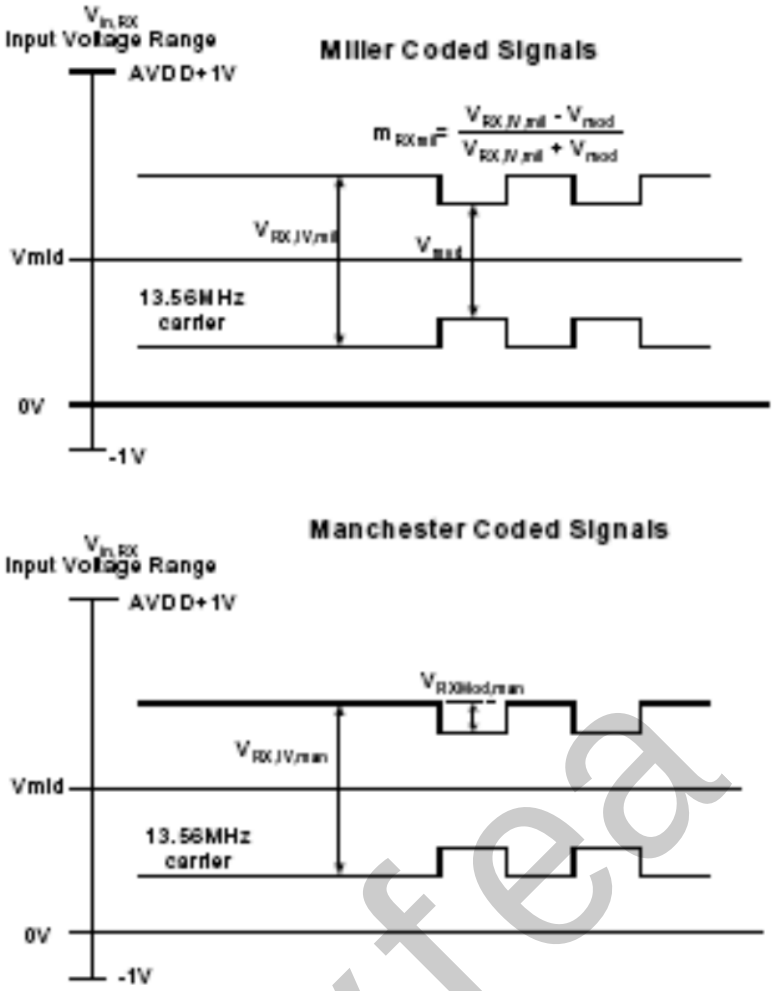


Fig 47. RX Voltage definitions

12.21 Output pin characteristics for AUX1/AUX2

Table 316. Output pin characteristics for AUX1/AUX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH	High level output voltage	VBAT = 3.4 V, IOH= -4 mA	DVDD- 0.4		DVDD	V
VOL	Low level output voltage	VBAT = 3.4 V, IOL= 4 mA	DVSS		DVSS+0.4	V
ILeak	Input leakage current	RSTPD_N = 0 V	-1		1	μA
Cin	Input Capacitance			2.5		pF
Cout	Load Capacitance				15	pF

12.22 Output pin characteristics for TX1/TX2

Table 317. Output pin characteristics for TX1/TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH, C32, 3 V	High level output voltage	VBAT = 3.4 V, ITX1/2= 32 mA, CWGsP[5:0] = 3Fh	TVDD- 150			mV
VOH, C80, 3 V	High level output voltage	VBAT =3.4 V, ITX1/2= 80 mA, CWGsP[5:0] = 3Fh	TVDD- 400			mV
VOL, C32, 3 V	Low level output voltage	VBAT = 3.4 V, ITX1/2 = 32 mA, CWGsN[3:0] = Fh			150	mV

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOL, C80, 3 V	Low level output voltage	VBAT = 3.4 V, ITX1/2= 80 mA, CWGsN[3:0] = Fh			400	mV

12.23 Timing for Reset and Hard-Power-Down

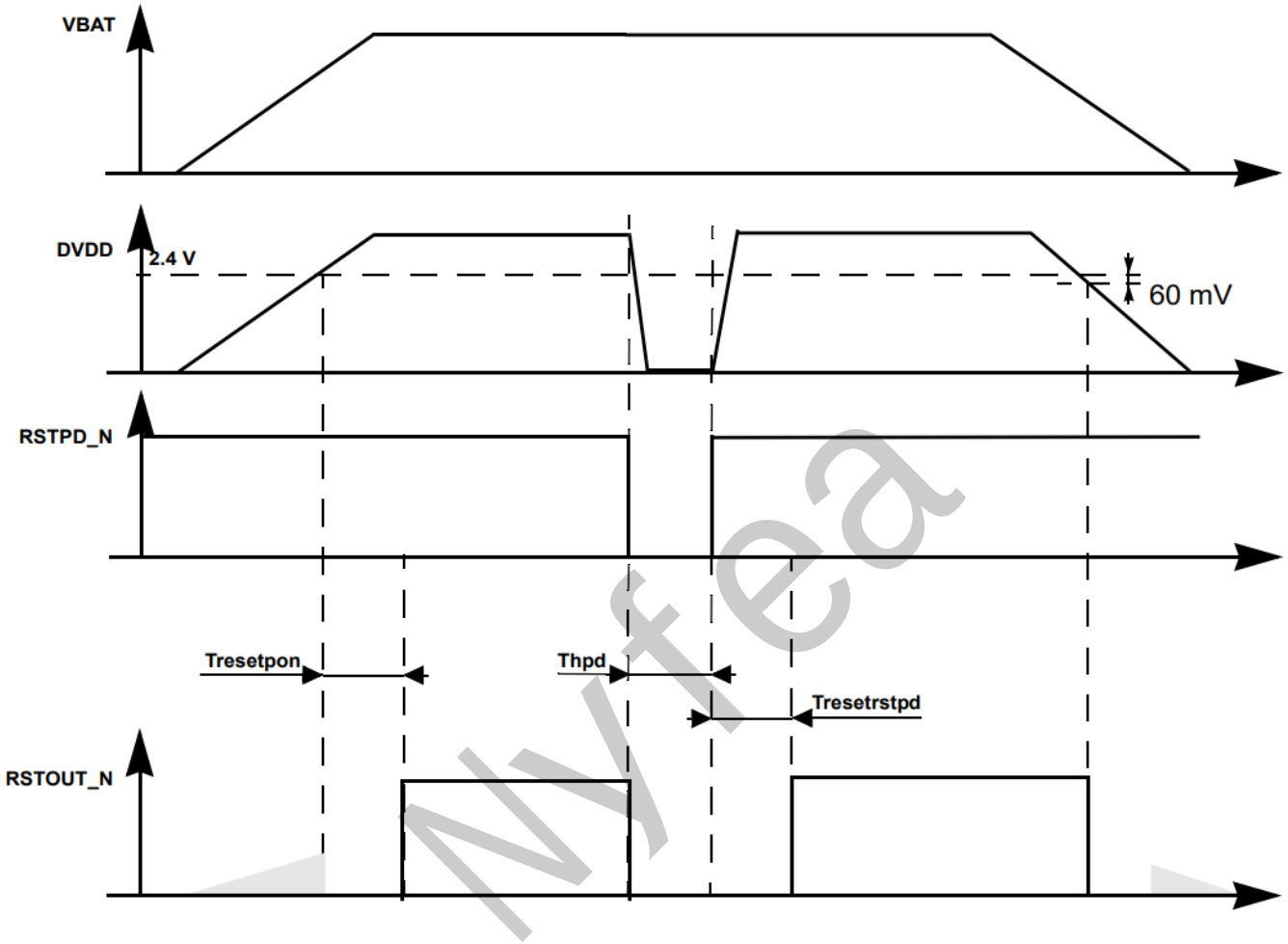


Fig 48. Timings for reset overview

Table 318. Reset duration time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tresetpon	Reset time at power on		[1] 0.1	0.4	2	ms
THPD	Hard Power-Down time	User dependent	20			ns
TresetRSTPD_N	Reset time when RSTPD_N is released		[1] 0.1	0.4	2	ms

[1] 27.12 MHz quartz begins in less than 800 µs. As an example, quartz like TAS-3225A, TAS-7 or KSS2F with appropriate layout.

12.24 Timing for the SPI compatible interface

Table 319. SPI timing specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tSCKL	SCK low pulse width		50			ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tSCKH	SCK high pulse width		50			ns
tSHDX	SCK high to data changes		25			ns
tDXSH	data changes to SCK high		25			ns
tSLDX	SCK low to data changes				25	ns
tSLNH	SCK low to NSS high		0			ns

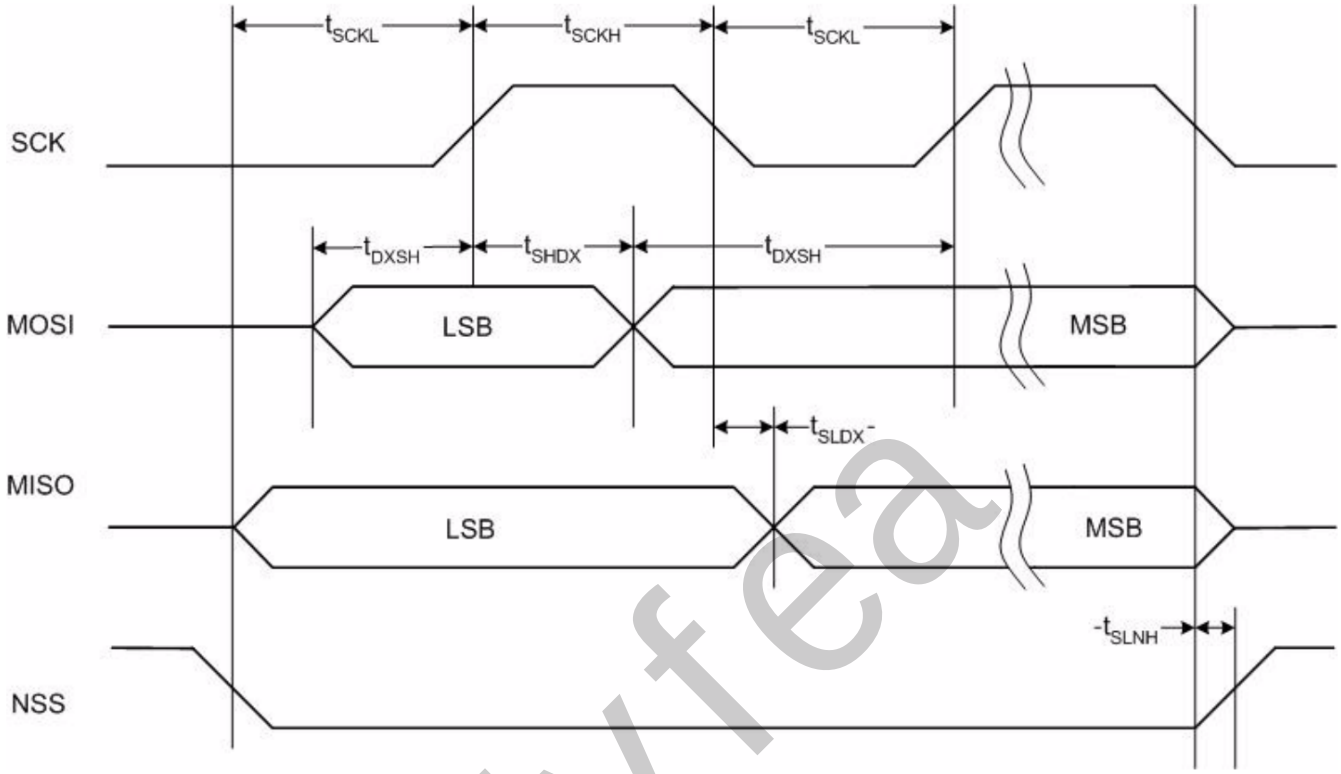


Fig 49. SPI timing diagram

12.25 Timing for the I²C interface

Table 320. I²C timing specification

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
fSCL	SCL clock frequency			0		400	kHz
tHD; STA	Hold time (repeated) START condition.	After this period, the first clock pulse is generated		600			ns
tSU; STA	Set-up time for a repeated START condition			600			ns
tSU; STO	Set-up time for STOP condition			600			ns
tLOW	LOW period of the P50_SCL clock			1300			ns
tHIGH	HIGH period of the P50_SCL clock			600			ns
tHD; DAT	Data hold time			0		900	ns
tSU; DAT	Data set-up time			100			ns
tr	Rise time P50_SCL and SDA		[1]	20		1000	ns
tf	Fall time P50_SCL and SDA		[1]	20		300	ns
tBUF	Bus free time between a STOP and START condition			1.3			ms

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
tStrWuSpd	Stretching time on P50_SCL when woken-up on its own address		[2]			1	ms
tHDSDA	Internal hold time for SDA			330		590	ns
tHDSDA	Internal hold time for SDA in SPD mode		[3]		270		ns

- [1] The NF532 has a slope control in accordance with the I^2 C specification for the Fast mode. The slope control is always present and not dependant of the I^2 C speed.
- [2] 27.12 MHz quartz begins in less than 800 µs. As an example, quartz like TAS-3225A, TAS-7 or KSS2F with appropriate layout.
- [3] The NF532 has an internal hold time of around 270ns for the SDA signal to bridge the undefined region of the falling edge of P50_SCL.

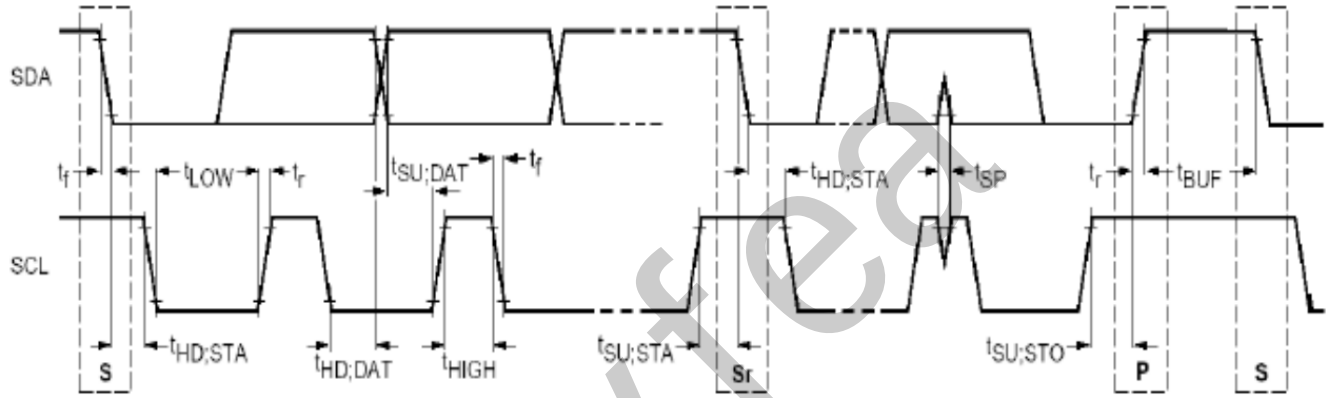


Fig 50. I^2C timing diagram

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13 Application information

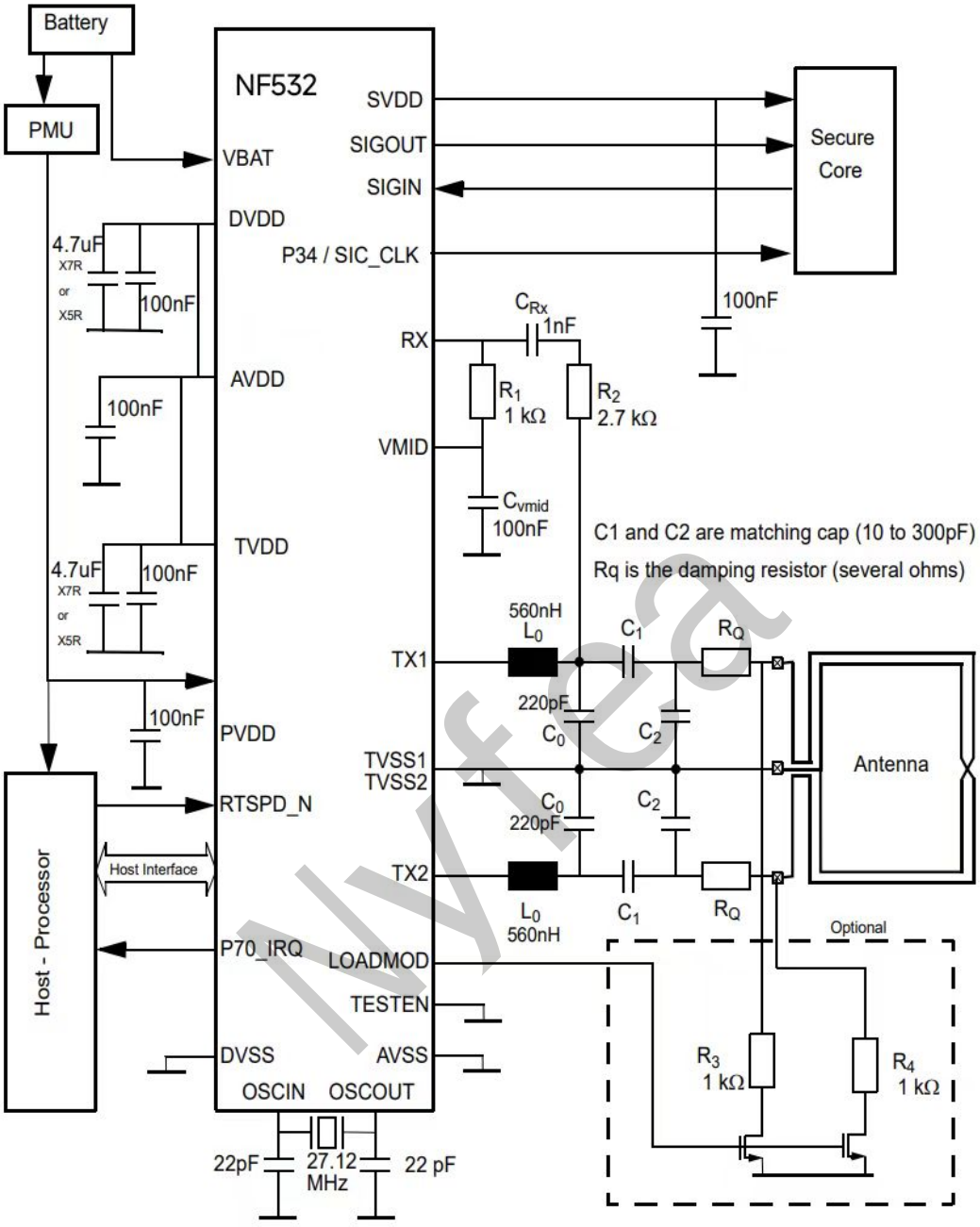
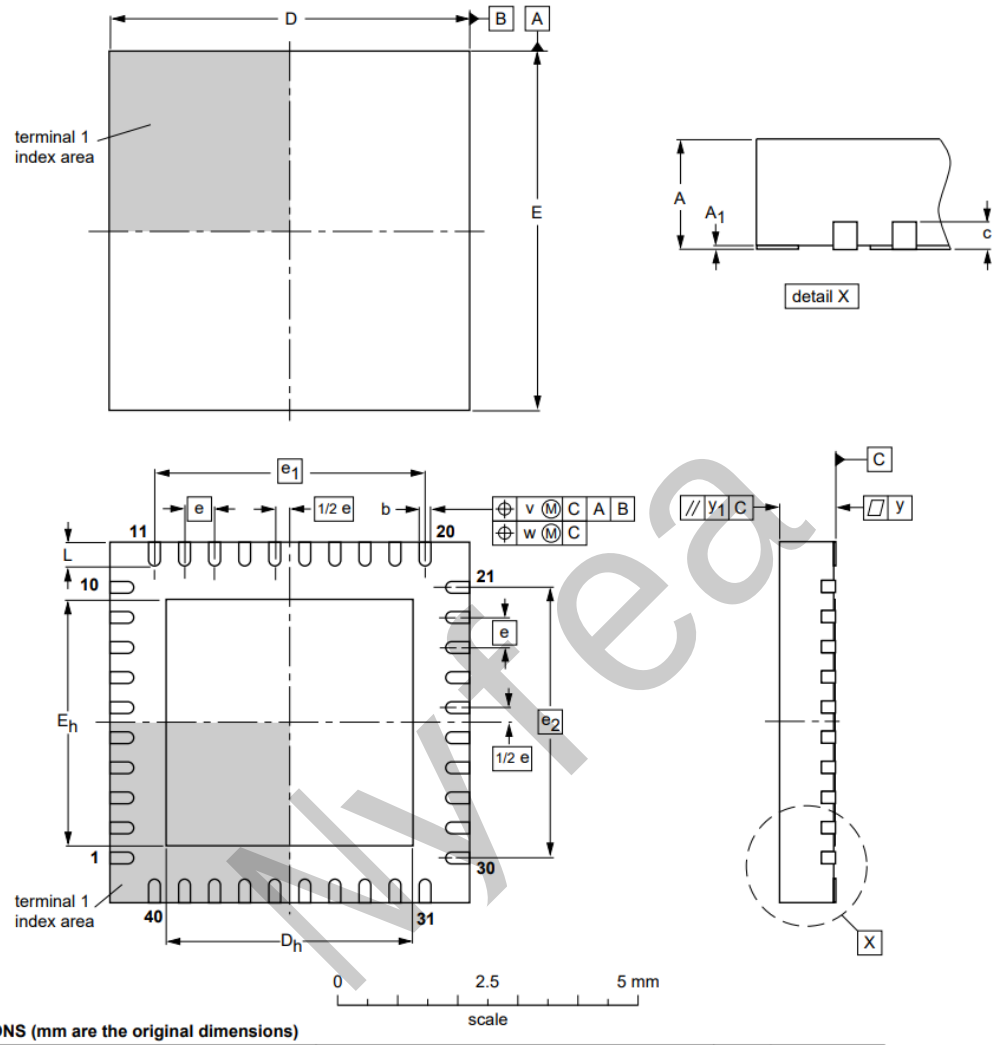


Fig 51. Application diagram of NF532

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14 Package outline

The mechanical target shown in this engineering draft is a 40-terminal HVQFN footprint with a nominal 6 mm × 6 mm body and 0.85 mm maximum body height. The final NF532 package designation, production drawing, and qualification status shall be confirmed prior to product release.



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	---	MO-220	---			~~01-08-08~~ 02-10-22

Fig 52. Package outline HVQFN40 (SOT618-1)

The final NF532 moisture-sensitivity classification shall be stated in the released package specification.

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15 Abbreviations

Table 321. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
BPSK	Bit Phase Shift Keying
CIU	Contactless Interface Unit
CRC	Cyclic Redundancy Check
ECMA	European Computer Manufacturers Association organization
GPIO	General-purpose Input Output
GPIRQ	General-purpose Interrupt ReQuest
HPD	Hard Power Down (seeSection 8.5.3)
HSU	High Speed UART
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
LDO	Low Drop-Out regulator
Load modulation Index	The load modulation index is defined as the card’ s voltage ratio (Vmax - Vmin) / (Vmax + Vmin) measured at the card’ s coil.
MIF	Multi InterFace block
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin) / (Vmax + Vmin).
MSL	Moisture Sensitivity Level
NFCIP	NFC Interface and Protocol
NFC-WI	NFC Wired Interface to connect NFC front end to a SIC
PCD	Proximity Coupling Device. Definition for a Card Reader/ Writer in accordance with the ISO/IEC 14443 Specification
PCR	Power Clock Reset controller
PICC	Proximity Cards. Definition for a contactless Smart Card in accordance with the ISO/IEC 14443 specification
SIC	Secure Integrated Circuit (may be a Smart Card IC, a Secure Access Module (SAM),...)
SPI	Serial Parallel Interface
SPD	Soft Power Down mode (see Section 8.5.4)
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self-generated RF field (no RF field generated by initiator during target answer).
UART	Universal Asynchronous Receive Transmit

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16 Revision history

Table 322. Revision history

Document ID	Release date	Status	Change summary
NF532 functional specification v1.0 draft	2026-09-16	Engineering draft	Initial NF532 compatibility-oriented rewrite based on the verified technical baseline. Compatibility-critical constants and numbering are retained; explanatory wording is independently rewritten.

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