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PRODUCT SPECIFICATION

Customer : _____

Product Name : RTD-to-Digital Converter

Part NO : FRTD31865

Issue Date : _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- Chip operating temperature range:
  -55° C~+150° C
- Handles 100ohm to 1kohm(at0° C) Platinum RTDs(PT100 to PT1000)
- Internal ADC resolution:15bits
- ADC Full-scale error:±1LSB
- 50/60Hz noise rejection:80dB
- Single measurement conversion Time:
  50Hznotch:20.0ms
  60Hznotch:16.7ms
- Compatible with Mode 1/3 SPI interface
- Supports 2-wire,3-wire,and 4-wire RTD connection
- Supply voltage range:2.7V~3.9V
- Supports RTD fault detection
- Package Information:

Part Number	Package	BodySize(mm²)
FRTD31865Q	QFN20	5.00 ×5.00
FRTD31865S	SSP20L	7.20 ×5.30

2 Applications

IndustrialEquipment

MedicalEquipment

Instrumentation

3 Description

The FRTD31865 is a precision resistance-to-digital converter specifically designed for PT100 and PT1000 RTD temperature sensors. It generates a stable external reference voltage through its dedicated BIAS pin, which is applied to a series-connected reference resistor (RREF) and the RTD element. The internal ADC operates by measuring the voltage ratio between the RTD and RREF, enabling high-accuracy temperature readings.

To enhance measurement integrity in electrically noisy environments,the device incorporates programmable noise fitering that attenuates interference from 50Hz or 60Hz power-ine frequencies.This feature effectively reduces the impact of ambient electromagnetic disturbances on the conversion result.

The FRTD31865 accommodates a variety of system configurations by supporting 2-wire,3-wire,and 4-wire RTD connection to pologies, offering flexibility for different sensing schemes and lead-compensation requirements.Integrated diagnostic capabilities allow the converter to detect common RTD wiring faults,including open-circuit conditions, short-circuit failures,and unintentional connections to the supply rail or ground.

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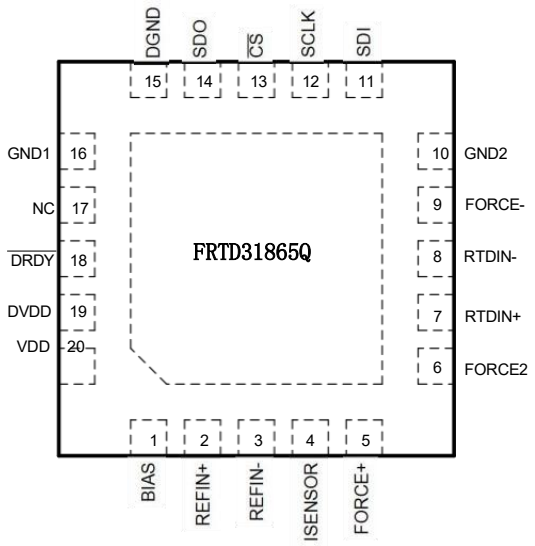
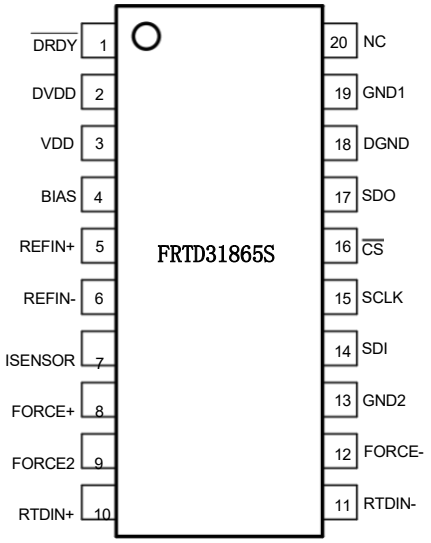
4 Pin Configuration and Functions

QFN-20 Top View



SSOP20L Top View



Pin Function

PIN Name	PIN No.		Description
	FRTD31865Q	FRTD31865S	
BIAS	1	4	Bias voltage output (V_{BIAS}).
REFIN+	2	5	Positive reference voltage input. Connect to BIAS. Connect the R_{REF} between REFIN+ and REFIN- .
REFIN-	3	6	Negative reference voltage input. Connect the R_{REF} between REFIN+ and REFIN- .
ISENSOR	4	7	Low-Side of R_{REF} . Connect to REFIN- .
FORCE+	5	8	High-Side RTD drive, Connect to FORCE2 in 3-wire connection .
FORCE2	6	9	Positive input used in 3-Wire only. When in 3-wire connection, connect to FORCE+ . When in 2-wire or 4-wire connection , connect to ground.
RTDIN+	7	10	Positive RTD input.
RTDIN-	8	11	Negative RTD input.
FORCE-	9	12	Low-Side RTD return.
GND2	10	13	Analog ground. Connect to GND1.
SDI	11	14	Serial-Data input in SPI interface.
SCLK	12	15	Serial-Clock input in SPI interface.
CS	13	16	Active-Low chip select Set CS low to enable the SPI interface
SDO	14	17	Serial-Data output in SPI interface .
DGND	15	18	Digital ground.
GND1	16	19	Analog ground. Connect to GND2 .
NC	17	20	Do Not Connect.
DRDY	18	1	Low active Data-Ready pin. Push-pull output.
DVDD	19	2	Digital supply with 2.7V to 3.9V , bypass to DGND with a 0.1μF
VDD	20	3	Analog supply with 2.7V to 3.9V , by pass to GND1 with a 0.1μF

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5 Specifications

5.1 Absolute Maximum Ratings

	MIN	MAX	Unit
VDD / DVDD	-0.3	6	V
Analog input/output pins	-0.3	VDD + 0.3	V
Digital input/output pins	-0.3	6	V
Operating temperature	-55	150	℃
Junction temperature		150	℃
Storage temperature	-60	160	℃

Unless explicitly stated otherwise,the electrical and performance parameters listed in the table above are valid under standard ambient temperature conditions.Operating the device beyond the specified stress limits may result in irreversible damage to the internal circuitry.

5.2 Electrostatic Protection

		Value	Unit
Electrostatic Discharge Voltage	Human-body mode (HBM), per ANSI/ ESDA/ JEDEC JS-001- 2017	±8000	V
	Charged-device model (CDM), per ANSI/ ESDA/JEDEC JS-002-2022	±1400	V
	Machine model (MM), per JESD22-A115 C (2010)	±300	V
Latch-up effect	Latch-up (LU), per JESD 78F (2022)	±200	mA

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	Unit
Supply Voltage VDD / DVDD	2.7	3.3	3.9	V
Operating Temperature T_A	-55		150	℃
FORCE+ / FORCE2 / FORCE- / RTDIN+ / RTDIN-	0		V_{BIAS}	V
R_{REF}	350		10k	ohm
Cable resistance of RTD (per lead)	0		50	ohm

Unless otherwise noted the specifications in the above table apply within the atmospheric temperature range .

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5.4 Electrical Characteristics

All electrical characteristics listed below are guaranteed over the operating ambient temperature range of TA = -40℃ to +125℃ and with a supply voltage VDD between 3.0 V and 3.6 V , unless otherwise noted. Typical values are specified at TA = 27℃ and VDD = 3.3 V.

Parameters	Test Conditions	MIN	TYP	MAX	Unit
Chip Operating Temperature Range		-55		150	℃
Internal ADC Resolution			15		bit
Input Leakage Current	RTDIN+ / RTDIN-			20	nA
Bias Voltage	V_{BIAS}	1.95	2.00	2.05	V
Bias Voltage Output Current	I_{OUT}	0.2		5.75	mA
Bias Voltage Load Regulation	I_{OUT} ≤5.75 mA		30		mV/mA
Bias Voltage Start-up Time	(Note 1)			10.5	ms
ADC Full-Scale Error			±1		LSB
ADC Offset Error				± 3	LSB
50/60Hz Noise Rejection			80		dB
Common-Mode Rejection			90		dB
Conversion Time (Note 2)	Continuous conversion (60 Hz notch)		16.7	18	ms
	Single conversion (60 Hz notch)		52	56	
	Continuous conversion (50 Hz notch)		20	21.5	
	Single conversion (50 Hz notch)		62.5	67.5	
Auto Fault Detection Cycle Time	From CS high to cycle complete		550	600	μs
Power-Supply Rejection			±1		LSB/V
Quiescent Current	Active conversion		2	2.3	mA
	Shutdown mode		1	1.2	
Power-on and Power-off Reset Threshold	Power-on reset		2.28		V
	Power-off reset		2. 16		
Input Capacitance	Logic inputs		6		pF
Input Leakage Current	Logic inputs			±1	μA
Output High Voltage	Logic outputs, I_{OUT} = -1 .6 mA	DVDD -0.4			V
Output Low Voltage	Logic outputs, I_{OUT} = 1.6 mA			0.4	V

Note 1 : The maximum startup time of V_{BIAS} is determined by the RC delay formed by the 10kohm Reference Resistor and the 0.1μF by pass capacitor connected across the RTD.

Note 2: In continuous conversion mode, for 60Hz noise rejection , the initial conversion time is 52ms, and each subsequent conversion time is 16.7 ms; for 50 Hz noise rejection, the initial conversion time is 62.5ms, and each subsequent conversion time is 20ms .

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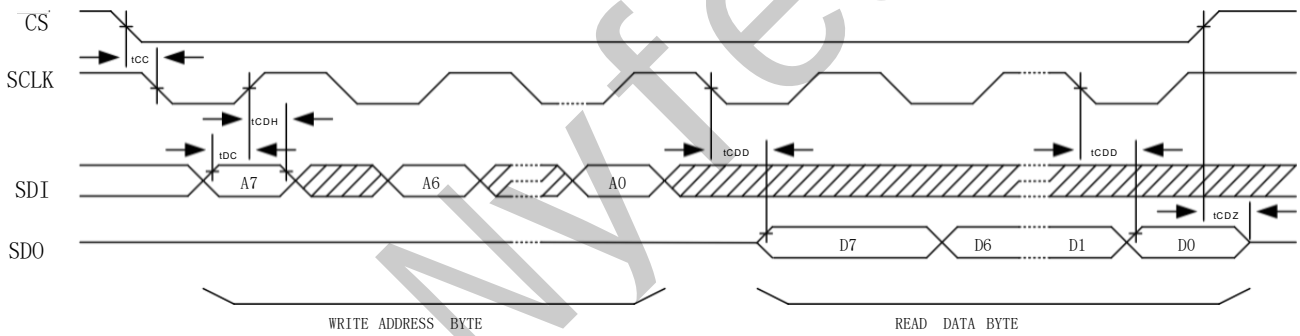
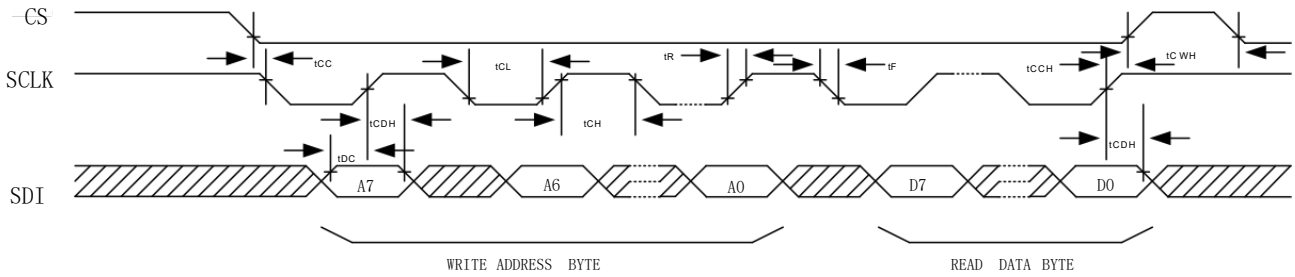
5.5 SPI Timing Requirements

Unless otherwise specified, the following data are the characteristics of the chip at TA = -40 ℃ ~ 125℃ and VDD = 3.0V ~ 3.6V.

Symbol	Description	MIN	TYP	MAX	Unit
t_{DC}	Data to SCLK Setup	35			ns
t_{CDH}	SCLK to Data Hold	35			ns
t_{CDD}	SCLK to Data Valid			80	ns
t_{CDL}	SCLK Low Time	100			ns
t_{CDH}	SCLK High Time	100			ns
f_{CLK}	SCLK Frequency	DC		5	MHz
t_R , t_F	SCLK Rise and Fall			200	ns
t_{CC}	CS to SCLK Setup	400			ns
t_{CCH}	SCLK to CS Hold	100			ns
t_{CWH}	CS Inactive Time	400			ns
t_{CDZ}	CS to Output High-Z			40	ns
t_{DRDYH}	Address 01 h or 02h Decoded to DRDY High		50		ns



NOTE:SCLK CAN BE EITHER POLARITY ,TIMING SHOWN FOR CPOL = 1



NOTE:SCLK CAN BE EITHER POLARITY ,TIMING SHOWN FOR CPOL = 1

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6 Detailed Description

6.1 Device Functional Modes

6.1.1 Overview of Temperature Measurement Based on RTD

RTD temperature sensing relies on the predictable resistance variation of a thermistor element in response to temperature changes. Among the various types available, platinum-based RTDs (PT-RTDs) are the most widely adopted, capable of performing measurements at temperatures up to 800 ℃ and above. They are recognized for their high accuracy, excellent measurement repeatability, and favorable linearity characteristics.

Among platinum RTD sensors, PT100 and PT1000 are the two predominant types, featuring nominal resistances of 100 Ω and 1000 Ω, respectively, at the ice-point temperature of 0 ℃. For a PT100 element, the average temperature coefficient of resistance (α) over the 0° C to 100 ° C interval is influenced by the purity level and impurity composition of the platinum material employed. Two internationally recognized standards define this coefficient: IEC 751 specifies a value of 0.00385, while the SAMA standard adopts 0.00392. Therefore, the resistance of a PT100 is approximately linearly related to temperature, which can be specifically expressed by the Callendar- Van Dusen equation:

$$R(T)=R_0*(1+aT+bT^2+c(T-100)T^3)$$

In the above formula, T represents the temperature in degrees Celsius, R(T) is the resistance of the platinum at that temperature, and R_0 is the resistance of the platinum at 0 ℃; taking the IEC751 standard as an example, a = 3.90830 × 10_³, b = -5.77500 × 10_⁷, c = -4.18301 × 10_¹² (-200° C ≤ T ≤ 0° C) / 0 (0° C ≤ T ≤ 850° C).

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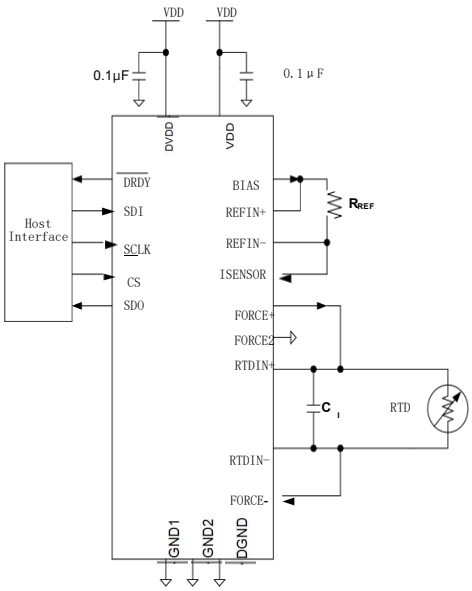

Figure1 FRTD31865 2-wire Connection Circuit

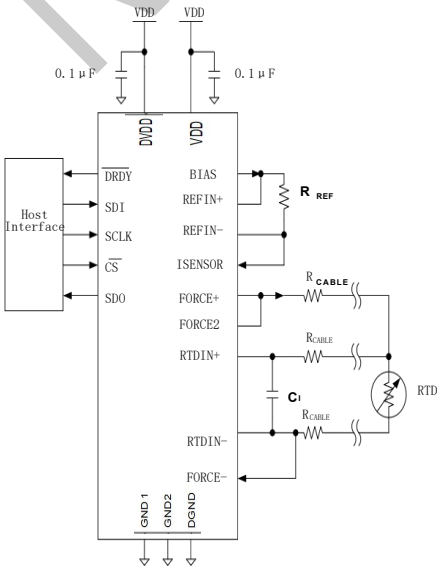

Figure2 FRTD31865 3-wire Connection Circuits

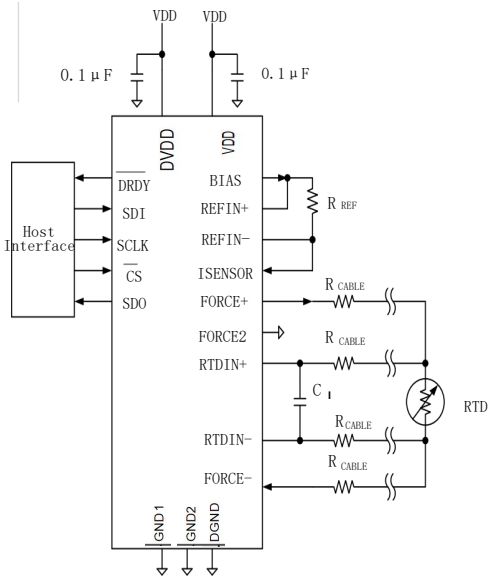

Figure3 FRTD31865 4-Wire Connection Circuits

The FRTD31865 offers a highly accurate and efficient approach to platinum RTD measurement. As illustrated in Figure 1, a reference resistor (RREF) is placed in series with the RTD element and driven by the BIAS pin output. This configuration ensures that an identical current flows through both resistive components. The recommended RREF value is four times the RTD's nominal resistance at 0 ℃—specifically, 400 Ω for PT100 sensors and 4k Ω for PT1000 sensors. The voltage developed across RREF is utilized as the ADC's internal reference input, while the voltage across the RTD is taken as the differential signal to be measured. The resulting digital output from the ADC directly corresponds to the resistance ratio of the RTD to the reference resistor:

$$R_{RTD} = (ADC_Code * R_{REF}) / 2^{15}$$

To accommodate diverse application requirements, the FRTD31865 offers flexible support for 2-wire, 3-wire, and 4-wire RTD connection topologies. For installations where the RTD sensor is positioned in close proximity to the device, the 2-wire configuration (depicted in Figure 2) may be employed. However, users should be aware that lead-wire resistances introduce measurement offsets-for instance, a line resistance of just 0.4Ω can translate into a temperature reading error of approximately 1 ℃. When higher accuracy over long cable runs is required, the 4-wire hookup (shown in Figure 1) is recommended, as it effectively eliminates lead-wire-induced errors; in this configuration, each individual wire should be kept below 50Ω of resistance. For a balanced trade-off between accuracy and cabling complexity, the 3-wire connection (illustrated in Figure 3) can be adopted. In this setup, the FORCE2 pin must be tied to FORCE+, and the 3-wire mode is activated by setting bit D4 (the 3-Wire bit) of the Configuration register to 1. Once enabled, the internal ADC adjusts its quantization scheme accordingly; provided that the three leads are well matched in resistance, the resulting wire-resistance effects are effectively canceled out.

When using an RTD to measure temperatures in the range of -100 ℃ to 100 ℃, the final temperature measurement value can be calculated according to the following formula:

$$Temperature\ (℃) = (ADC\ code / 32) - 256$$

The temperature measurement error of the above formula is -1.75℃ at -100℃, 0 ℃ at 0℃, and -1.4℃ at 100 ℃ (in the above results, it is assumed that the RTD used complies with the IEC 751 standard, and the value of R_{REF} is four times the resistance of the platinum RTD at 0 ℃). For higher accuracy conversion can be performed using the Callendar-Van Dusen equation or by referring to the data in Table 1.

The FRTD31865 is not limited to PT100 or PT1000 sensors alone; it remains fully functional with other RTD types as well. When using a non-standard RTD, the only requirement is that the reference resistor RREF be selected with a resistance value equal to or greater than the maximum expected RTD resistance across the target temperature range. Under this condition, the ADC output continues to represent the ratiometric value of the RTD resistance relative to RREF. The table below shows the relationship between the actual temperature, RTD resistance, ADC output code, and measured temperature value when using PT100 with R_{REF} = 400ohms:

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Table 1 Temperature Measurement Reference Table Using PT100 and 400ohm R_{REF}

Temperature(℃)	RTD Resistance(ohm)	RTD Data Reg (01h - 02h) (hex)	ADC Code (dec)	ADC Code/32 - 256(℃)
-200	18.52	0BDAh	1517	-208.59
-175	29.22	12B4h	2394	-181.19
-150	39.72	196Ch	3254	-154.31
-125	50.06	200Ah	4101	-127.84
-100	60.26	2690h	4936	-101.75
-75	70.33	2D04h	5762	-75.94
-50	80.31	3366h	6579	-50.41
-40	84.27	35EEh	6903	-40.28
-30	88.22	3876h	7227	-30.16
-20	92. 16	3AFCh	7550	-20.06
-10	96.09	3D7Eh	7871	-10.03
0	100.00	4000h	8192	0.00
10	103.90	4280h	8512	10.00
20	107.79	44FCh	8830	19.94
30	111.67	4778h	9148	29.88
40	115.54	49F2h	9465	39.78
50	119.40	4C6Ah	9781	49.66
60	123.24	4EE0h	10096	59.50
70	127.08	5154h	10410	69.31
80	130.90	53C6h	10723	79.09
90	134.71	5636h	11035	88.84
100	138.51	58A4h	11346	98.56
110	142.29	5B12h	11657	108.28
120	146.07	5D7Ch	11966	117.94
130	149.83	5FE4h	12274	127.56
140	153.58	624Ch	12582	137.19
150	157.33	64B0h	12888	146.75
160	161.05	6714h	13194	156.31
170	164.77	6974h	13498	165.81
180	168.48	6BD4h	13802	175.31
190	172.17	6E30h	14104	184.75
200	175.86	708Ch	14406	194.19
225	185.01	7668h	15156	217.63
250	194.10	7C3Ah	15901	240.91
275	203. 11	81FEh	16639	263.97
300	212.05	87B6h	17371	286.84
325	220.92	8D64h	18098	309.56

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(Continued)

Temperature(℃)	RTD Resistance(ohm)	RTD Data Reg (01h - 02h) (hex)	ADC Code (dec)	ADC Code/32 - 256(℃)
350	229.72	9304h	18818	332.06
375	238.44	989Ah	19533	354.41
400	247.09	9E24h	20242	376.56
425	255.67	A3A2h	20945	398.53
450	264.18	A914h	21642	420.31
475	272.61	AE7Ah	22333	441.91
500	280.98	B3D4h	23018	463.31
525	289.27	B922h	23697	484.53
550	297.49	BE64h	24370	505.56

6.1.2 Continuous Conversion Mode

Upon power-up, the FRTD31865 defaults to a shutdown state, characterized by low power consumption. In this mode, the BIAS pin is inactive (no VBIAS output), and the internal ADC remains idle without performing any conversions. To transition the device into continuous conversion mode, two bits in the Configuration register must be set to logic 1: the VBIAS bit (D7) and the Conversion Mode bit (D6). Once enabled, the device begins repetitive conversions governed by the settings of the 3-Wire bit (D4) and the 50/60Hz Filter Select bit (D0). The nominal conversion cycle time is 16.7 ms when D0 = 0 (60 Hz rejection) and 20 ms when D0 = 1 (50 Hz rejection). However, the very first conversion following the mode change requires a longer settling period—approximately 52 ms for the 60 Hz notch setting and 62.5 ms for the 50 Hz notch setting.

6.1.3 One-Shot Mode

In addition to continuous operation, the FRTD31865 also supports a single-conversion mode, referred to as One-Shot mode. When the device is in shutdown mode (i.e., the Conversion Mode bit, D6 of the Config register, is set to 0), a single conversion can be triggered by writing 1 to the 1-Shot bit (D5). The start-up behavior depends on the status of the VBIAS bit (D7):

If VBIAS (D7) is already 1: Writing 1 to the 1-Shot bit (D5) immediately initiates the conversion.

If VBIAS (D7) is 0: The user must first set D7 to 1, then allow a settling delay of at least 10.5 ms for the external RC network (associated with the RTD) to stabilize, before finally writing 1 to D5 to launch the conversion.

Once the single conversion completes, the 1-Shot bit(D5) is automatically cleared to 0 by the hardware.

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6.1.4 50/60Hz Noise Rejection

The 50/60 Hz Filter Select bit (D0) in the FRTD3 1865 ' s Configuration register allows the user to adjust the first notch frequency of the internal SINC3 filter. By selecting the appropriate notch frequency, the device effectively attenuates interference from 50Hz or 60Hz power-line noise, along with their relevant harmonics, thereby enhancing measurement precision and output stability. A critical operational note: do not modify the D0 bit while the device is operating in continuous conversion mode .

6.1.5 RTD Fault Detection

The FRTD31865 incorporates comprehensive diagnostic capabilities to identify a range of potential RTD failures . Fault detection is supported through two distinct operational modes:1) automatic real- time monitoring , and 2) manual triggered verification . When a fault condition is detected, the corresponding status flags within the Fault Status register are asserted to logic 1. Additionally, any fault occurrence—regardless of its type—will set bit D0 of the RTD LSB register to 1, providing a global fault indicator for quick system checks.

Real-time automatic detection includes the following checks:

1) Upon power-up , the FRTD31865 actively monitors the voltage levels at the FORCE+ ,FORCE2 , FORCE – , RTDIN+ , and RTDIN – pins for any overvoltage or undervoltage conditions—specifically , whether these pins are driven above VDD or below GND. When such an out- of- range condition is detected , the device responds by setting bit D2 of the Fault Status register to 1 and immediately halting all ongoing ADC conversions;

2) After the ADC completes each conversion , it determines whether the measured RTD resistance exceeds the value in the High Fault Threshold register or is below the value in the Low Fault Threshold register. If either condition occurs, bits D7/ D6 of the Fault Status register will be in the 1 ; fault this check does not affect ADC conversions .

In manual detection mode , the FRTD31865 allows users to perform diagnostics by selectively disconnecting the internal switch that ties the FORCE - pin to ground. This mode offers two timing options: automatic delay mode and manual delay mode .The manual delay mode becomes mandatory when the settling time of the RC network across The RTD exceeds 100μs.During the detection process , three voltage comparisons are executed to identify the root cause of any fault ,and the diagnosis results are subsequently stored in the Fault Status register for user access:

1) Determine whether the voltage at the REFIN- pin is higher than 0.85 * V_{BIAS} ; if it is, set bit D5 of the Fault Status register to 1 ;

2) Disconnect the switch that internally grounds the FORCE- pin , and determine whether the voltage at the REFIN- pin is lower than 0.85 * V_{BIAS} ; if it is, set bit D4 of the Fault Status register to 1 ;

3) Keep the switch that internally grounds the FORCE-pin disconnected , and determine whether the voltage at the RTDIN-pin is lower than 0.85 * V_{BIAS} ; if it is, set bit D3 of the Fault Status register to 1.

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The three-step detection sequence is performed in both the automatic delay mode and the manual delay mode . The key distinction between the two lies in step 2: after the internal ground switch for the FORCE - pin is opened , the procedure either proceeds automatically (in automatic delay mode) or awaits a host-issued command to continue (in manual delay mode) .

This behavior is governed by bits D3 and D2 of the Configuration register, as outlined in Table 2. Upon completion of the manually triggered detection sequence , the FORCE - grounding switch is re-engaged , and bits D3 and D2 are automatically cleared to 0.

Before initiating a manual fault detection sequence , certain configuration prerequisites must be satisfied: bit D7 of the Configuration register must be set to 1, while bits D6 and D5 must be cleared to 0. This ensures that the chip performs the detection while in shutdown mode with VBIAS stable. If bit D5 is set to 1 during the configuration of bits D3 and D2 , the entire setting will be disregarded and no detection will occur. Additionally , note that writing 100X110 Xb directly to the Config register—without first writing 100X100Xb—will cause the FRTD31865 to start detection in automatic delay mode rather than manual mode .

Table 2 FRTD31865 Fault-Detection Cycle Control Bits

D3	D2	Config Register Write	Write Action	Read Meaning
0	0	XXXX00XXb	/	Fault detection finished
0	1	100X010Xb	Fault detection with automatic delay	Automatic fault detection still running
1	0	100X100Xb	Run fault detection with manual delay (cycle 1)	Manual cycle 1 still running; waiting for user to write 1 1
1	1	100X110Xb	Finish fault detection with manual delay (cycle 2)	Manual cycle 2 still running

The complete RTD fault detection flow is illustrated in Figure 4. Table 3 summarizes the relationship between various fault types—organized by RTD connection topology (2-wire , 3 -wire, or 4-wire) and the corresponding bit patterns reported in the Fault Status register .

To clear the fault status flags , the user may write 1 to the Fault Status Clear bit (D1) in the Configuration register, provided that bits D5 , D3 , and D2 are all set to 0. This operation resets bits D7 through D2 of the Fault Status register and bit D0 of the RTD LSB register to 0. However, it is important to note that if the underlying fault condition persists , bit D2 of the Fault Status register and bit D0 of the RTD LSB register may be re-asserted to 1 immediately after the clearing operation .

After completing the clearing of the aforementioned flags , the Fault Status Clear bit will automatically reset to 0

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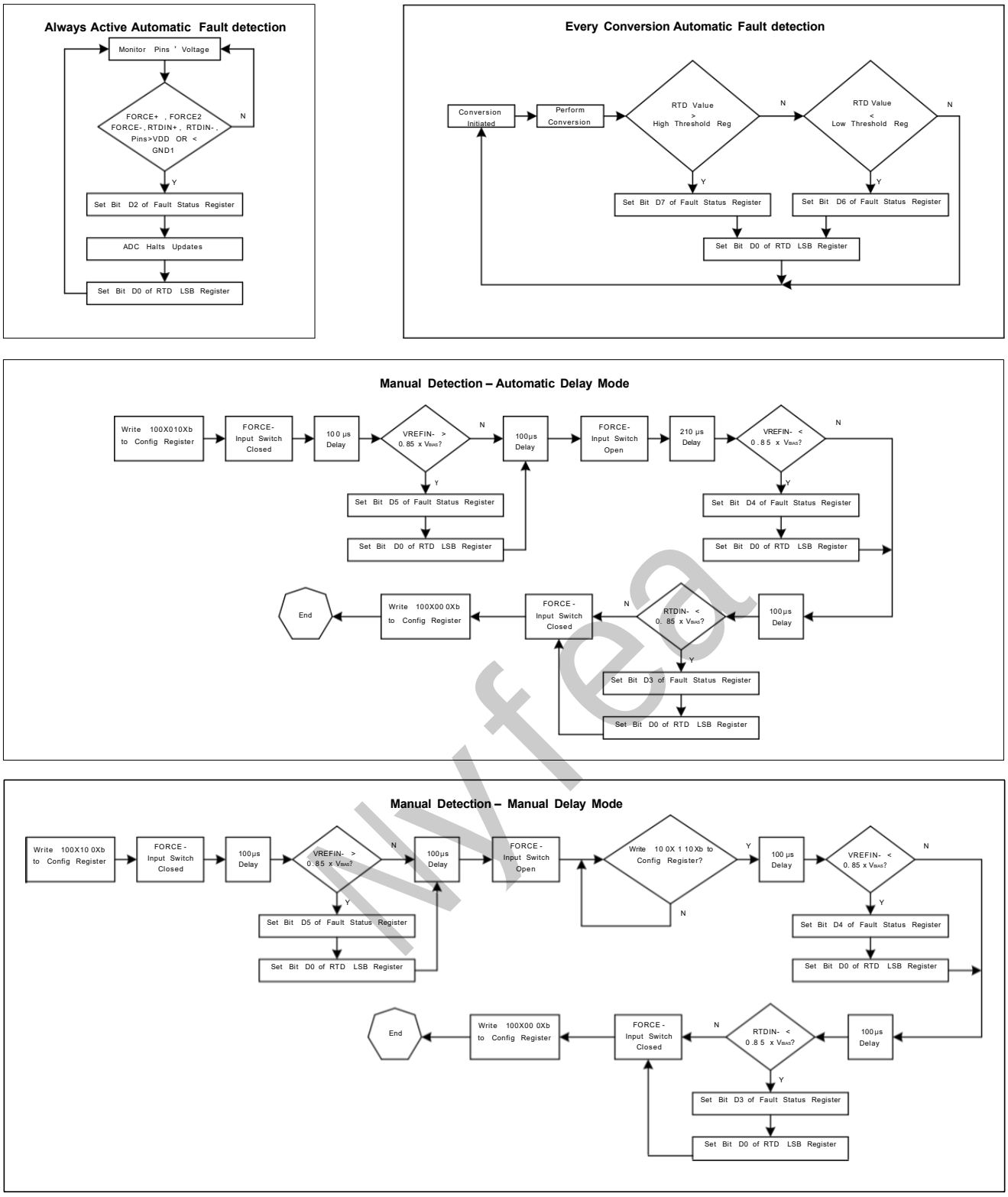

Figure 4 FRTD31865 Fault Detection

Table 3 Summary of Faults in Different RTD Connection

Fault Status Reg	Possible Cause	Condition Detected	RTD Reg
2-Wire Connection			
D7	RTD Open	RTD Register > High Fault Threshold Register	FFFFh
D6	RTD Short	RTD Register < Low Fault Threshold Register	≈0000h
	RTDIN+ Short to GND		
D5	RTD Open	VREFIN- > 0.85 * V_{BIAS}	FFFFh
	RTDIN+ Short to VDD		Indeterminate
	RTDIN- Short to VDD		Indeterminate
D4	RTDIN- Short to GND	VREFIN- < 0.85 * V_{BIAS} (FORCE- Open)	Valid
D3	RTDIN- Short to GND	VRTDIN- < 0.85 * V_{BIAS} (FORCE- Open)	Valid
	RTDIN+ Short to GND		≈0000h
D2	>VDD / <GND1		Indeterminate
3-Wire Connection			
D7	RTD Open	RTD Register > High Fault Threshold Register	FFFFh
	RTDIN+ Short to VDD and Open with RTD		
	FORCE+ Short to VDD and Connect with RTD		
D6	RTDIN+ Short to RTDIN-	RTD Register < Low Fault Threshold Register	≈0000h
	RTDIN+ Short to GND and Open with RTD		
	FORCE+ Short to GND		
D5	RTD Open	VREFIN- > 0.85 * V_{BIAS}	FFFFh
	FORCE+ Short to VDD and Connect with RTD		
	FORCE+ Open		Indeterminate
	FORCE+ Short to VDD and Open with RTD		
	RTDIN- Short to VDD		
D4	RTDIN- Short to GND	VREFIN- < 0.85 * V_{BIAS} (FORCE- Open)	Valid
D3	FORCE+ Short to GND	VRTDIN- < 0.85 * V_{BIAS} (FORCE- Open)	≈0000h
	RTDIN+ Short to GND and Connect with RTD		
	RTDIN- Short to GND		Valid
D2	>VDD / <GND1		Indeterminate

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(Continued)

Fault Status Reg	Possible Cause	Condition Detected	RTD Reg
		4-Wire Connection	
D7	RTD Open	RTD Register > High Fault Threshold Register	FFFFh
	RTDIN+ Short to VDD and Open with RTD		
	FORCE+ Short to VDD and Connect with RTD		
D6	RTDIN+ Short to RTDIN-	RTD Register < Low Fault Threshold Register	≈0000h
	RTDIN+ Short to GND and Open with RTD		
	RTDIN- Short to VDD and Open with RTD		
	FORCE+ Short to GND		
D5	RTD Open	VREFIN- > 0.85 * V_{BIAS}	FFFFh
	FORCE+ Short to VDD and Connect with RTD		
	FORCE+ Open		Indeterminate
	FORCE- Open		
	FORCE+ Short to VDD and Open with RTD		
	FORCE- Short to VDD and Open with RTD		
	FORCE- Short to VDD and Connect with RTD		
	FORCE- Short to GND and Open with RTD		
D4	FORCE- Short to GND and Connect with RTD	VREFIN- < 0.85 * V_{BIAS} (FORCE- Open)	Indeterminate
	RTDIN- Short to GND and Connect with RTD		Valid
D3	FORCE+ Short to GND	VRTDIN- < 0.85 * V_{BIAS} (FORCE- Open)	≈0000h
	RTDIN+ Short to GND and Connect with RTD		
	RTDIN- Short to GND and Connect with RTD		Valid
	FORCE- Short to GND		
D2	>VDD / <GND1		Indeterminate

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6.1.6 DRDY Pin

The DRDY pin of the FRTD31865 will be pulled low after each update of the conversion results in the RTD register, indicating that the latest conversion results are available for reading. Once the read operation of the RTD register is completed, the DRDY pin will be pulled high again.

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6.2 Serial Interface

6.2.1 Bus Overview

FRTD31865 supports the Mode 1/3 SPI interface, that is, the SPI bus polarity CPOL = 0/ 1 and SPI bus phase CPHA = 1 . The FRTD31865 implements SPI communication using four pins: Serial Data Input (SDI) , Serial Data Output (SDO) , Serial Clock (SCLK) , and Chip Select (CS).

The CS pin is active low, indicating the start and end of data transmission. The SCLK is generate by the host only when the CS pin is low.

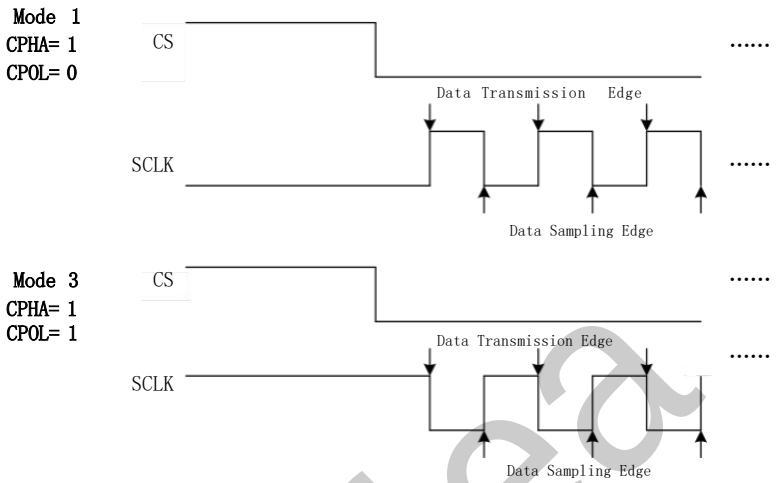

Figure 5 CPOL in Mode 1/3 SPI Interface

The SCLK timing relationship with CPOL under Mode 1 and Mode 3 operation is illustrated in Figure 5. In Mode 1 (CPOL = 0 , CPHA = 1) , SCLK idles low; data is driven on the SDI/ SDO lines at the rising edge of SCLK and sampled at the falling edge. In Mode 3 (CPOL = 1 , CPHA = 1) , SCLK idles high; data is driven at the falling edge and sampled at the rising edge. During SPI transactions between the FRTD31865 and the host, the device captures incoming data on SDI at the sampling edge, while outgoing data is presented on SDO at the transmission edge. All register addresses and data are 8-bit words, transmitted with the most significant bit (MSB) first. This protocol is summarized in Table 4.

Table 4 Mode 1/3 SPI Interface Action

Mode	CSN	SCLK	SDI	SDO
Bus Idle	High		Input Disabled	High impedance
Write	Low	CPOL = 0 , SCLK Falling	Data Bit Latch	High impedance
		CPOL = 1, SCLK Rising		
Read	Low	CPOL = 0 , SCLK Rising	X	Next data bit shift
		CPOL = 1 , SCLK Falling		

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6.2.2 Read and Write Operations

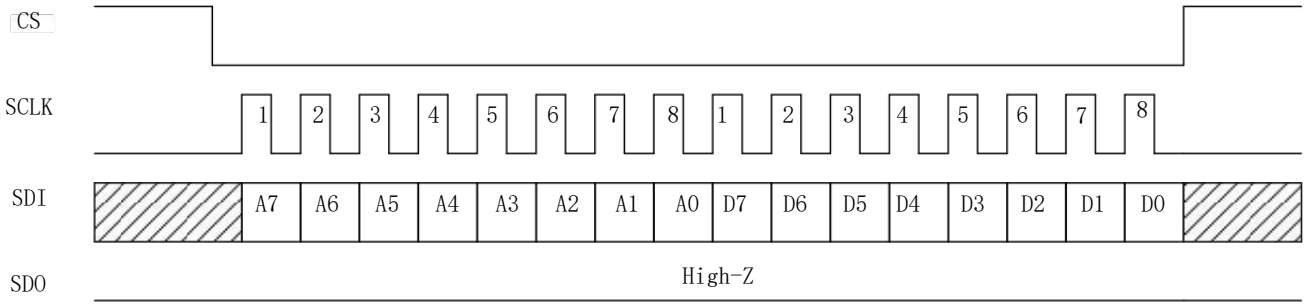

Figure 6 Single Byte Write Operation

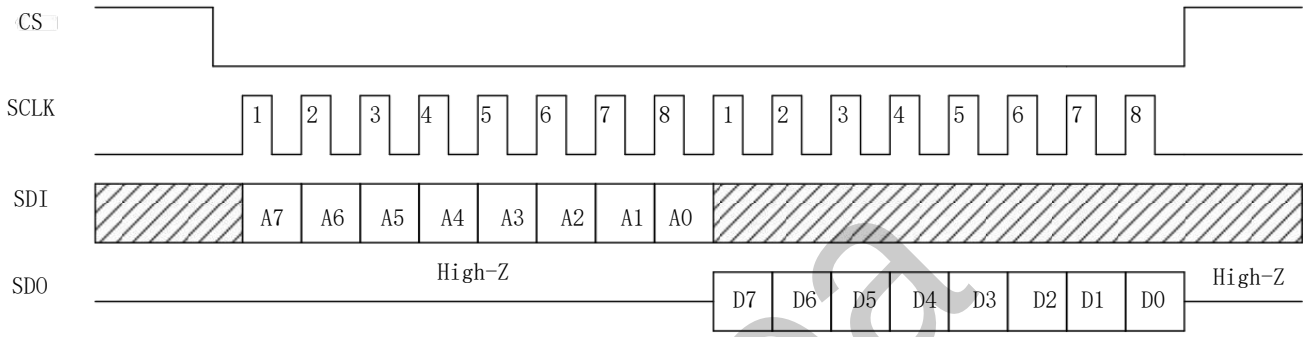

Figure 7 Single Byte Read Operation

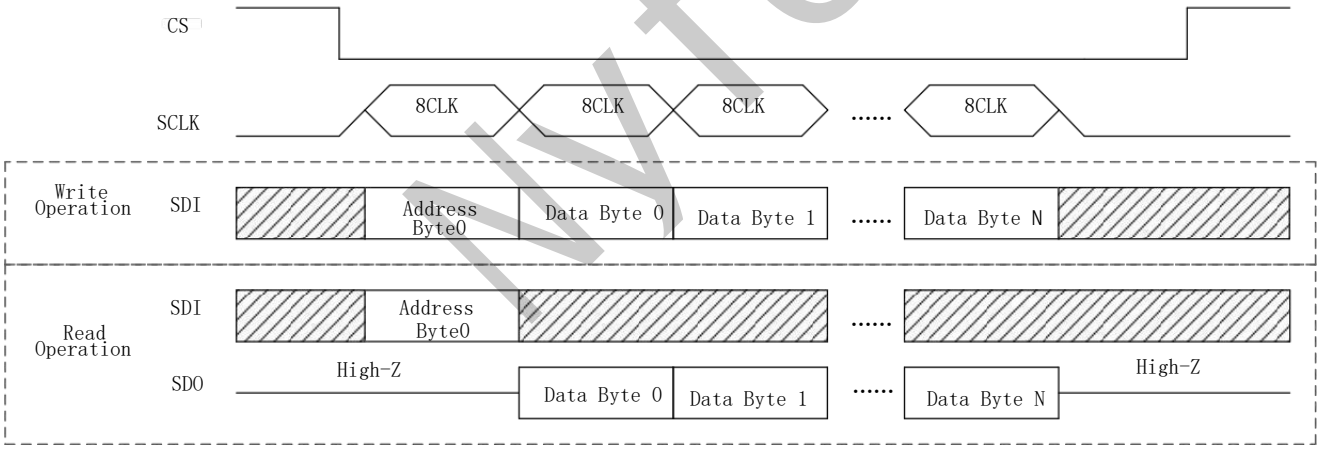

Figure 8 Multiple Bytes Write and Read Operation

During SPI communication between the FRTD31865 and the host computer, both the address and data bytes are shifted into the serial data input line (SDI) in MSB-first order to perform write operations , and shifted out from the serial data output line (SDO) to complete read operations .During communication , after CS pulling low, the address byte must be sent first , with the most significant bit of the address byte indicating whether the subsequent data will be written or read , followed by one or more data bytes. If the most significant bit of the address byte is 1,it indicates that the following bytes are write data; if the most significant bit is 0, it indicates that the following bytes are read data

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FRTD31865 supports single-byte or multi-byte read and write operations. For single-byte read/write operations, after CS pulling low, the bus begins transmitting the address byte and 1 byte of data, and then CS pulling high ends this communication(see Figure 6 and Figure 7). After transmitting 1 byte of data, the host can keep pulling CS low and send SCLK, allowing the chip to continue multi-byte read/write operations. The address byte corresponding to the subsequent data bytes will automatically increment (see Figure 8). When the address byte increments to 7 Fh / FFh, it will automatically wrap around to 00h / 80h. Data read from registers not defined in Table 5 will return FFh; writing to read-only registers will not change their values.

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6.3 Register Description

Table 5 provides the read and write addresses as well as the power-on initial values of the internal registers of the FRTD31865. All registers within the FRTD31865 have a bit width of 8 bits.

Table 5 FRTD31865 Internal Registers

Register Name	Read Address	Write Address	POR Value	Type
Configuration	00h	80h	00h	R / W
RTD MSB	01h	/	00h	R
RTD LSB	02h	/	00h	R
High Fault Threshold MSB	03h	83h	FFh	R / W
High Fault Threshold LSB	04h	84h	FFh	R / W
Low Fault Threshold MSB	05h	85h	00h	R / W
Low Fault Threshold LSB	06h	86h	00h	R / W
Fault Status	07h	/	00h	R

6.3.1 Configuration Register

Table 6 Configuration Register Description

Bit	Bit Name	Description	POR Value
D7	V_{BIAS}	0 =V_{BIAS} Disabled; 1= V_{BIAS} Enabled;	0
D6	Conversion Mode	0 = Shutdown Mode; 1=Continuous Conversion Mode;	0
D5	1-Shot	1= One-Shot Mode when D7= 1 / D6=0 ; This bit can automatically reset to 0;	0
D4	3-Wire	0 = 2/ 4 Wire Connection; 1 =3 Wire Connection;	0
D3:D2	Fault Detection Control	See Details in Table 2;	00
D1	Fault Status Clear	1 = The D7: D2 bits in the Fault Status register and the D0 bit in the RTD LSB register are reset to 0 ; This bits can automatically reset to 0;	0
D0	50/ 60 Hz Filter Select	0 = 60 Hz Noise Rejection; 1 = 50 Hz Noise Rejection;	0

For detailed usage of each bit in the table, please refer toSection 6.1.

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6.3.2 RTD Register / Fault Threshold Register

Table 7 RTD Register / Fault Threshold Register Description

	RTD MSB Register (01h)								RTD LSB Register (02h)							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Bit	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	Fault
	High Fault Threshold MSB Register (04h)								High Fault Threshold LSB Register (04h)							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Bit	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	/
	Low Fault Threshold MSB Register (05h)								Low Fault Threshold LSB Register (06h)							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Bit	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	/

The RTD Register, High Fault Threshold Register, and Low Fault Threshold Register all employ an identical data representation format. Upon power-up, the High Fault Threshold Register defaults to FFFFh, whereas the Low Fault Threshold Register initializes to 0000h.

6.3.3 Fault Status Register

Table 8 Fault Status Register Description

Bit	Bit Name	Description of Bit = 1	POR Value
D7	RTD High Threshold	RTD measurement value > High Fault Threshold Register;	0
D6	RTD Low Threshold	RTD measurement value < Low Fault Threshold Register;	0
D5	REFIN- > 0.85 * V_{BIAS}	See details in Section 6.1.5;	0
D4	REFIN- < 0.85 * V_{BIAS} (FORCE- Open)		0
D3	RTDIN- < 0.85 * V_{BIAS} (FORCE- Open)		0
D2	Overvoltage/ Undervoltage Fault	FORCE+ / FORCE2 / FORCE- / RTDIN+ / RTDIN- Pin Voltage > VDD / < GND1;	0
D1:D0	/	/	00

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7 Specific Applications

NOTE

Customers are responsible for determining suitability of components for their purposes based on their own usage needs and application scenarios. Customers should test and verify their design implementation to confirm system functionality and avoid losses.

For optimal measurement stability, it is advisable to place a 0.1μF decoupling capacitor across both the VDD and DVDD supply pins of the FRTD31865.

The overall measurement accuracy of the device is largely determined by the precision and temperature coefficient of the external reference resistor RREF. Accordingly, when targeting high-accuracy applications, careful selection of an RREF with adequate tolerance and low drift is essential.

To further mitigate noise interference, a filter capacitor (CI) may be connected in parallel with the RTD element. Recommended CI values are 100 nF for PT100 sensors and 10nF for PT1000 sensors. For non- standard RTD types, the CI value should be chosen with consideration of the RC network's settling time to avoid measurement errors.

For 3-wire and 4-wire configurations, each individual lead should be kept under 50Ω of resistance and the leads should be well matched in resistance to achieve the best possible accuracy.

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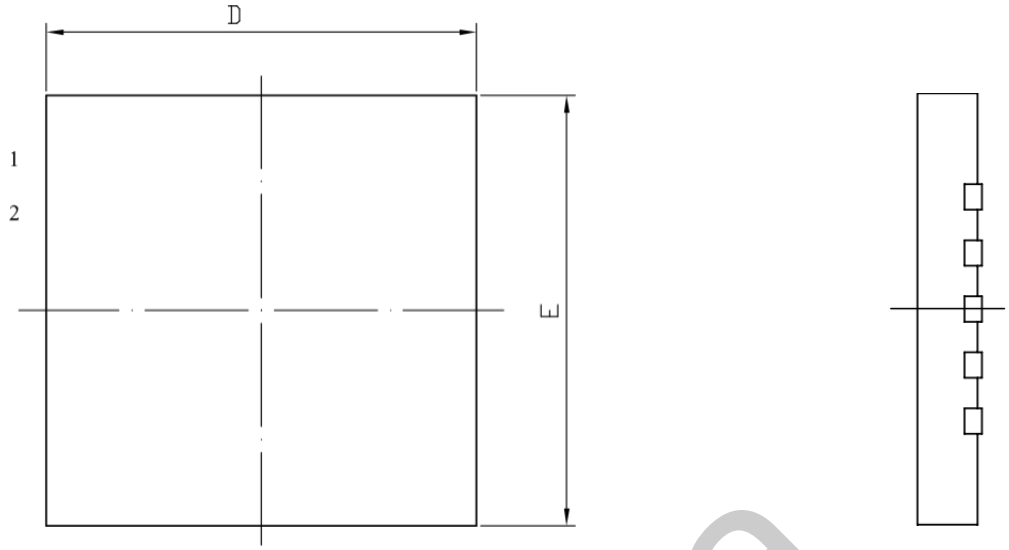
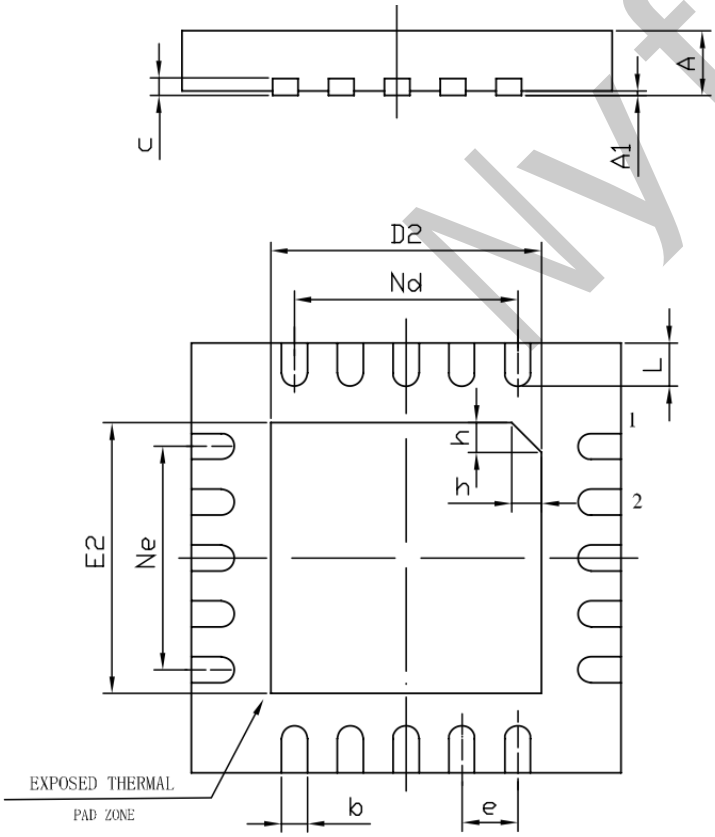
8 Package Information

8.1 QFN20 Package



TOP VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
e	0.65BSC		
Ne	2.60BSC		
Nd	2.60BSC		
E	4.90	5.00	5.10
E2	3.05	3.15	3.25
L	0.45	0.55	0.65
h	0.30	0.35	0.40
L/F Carrier Dimensions	138X138		

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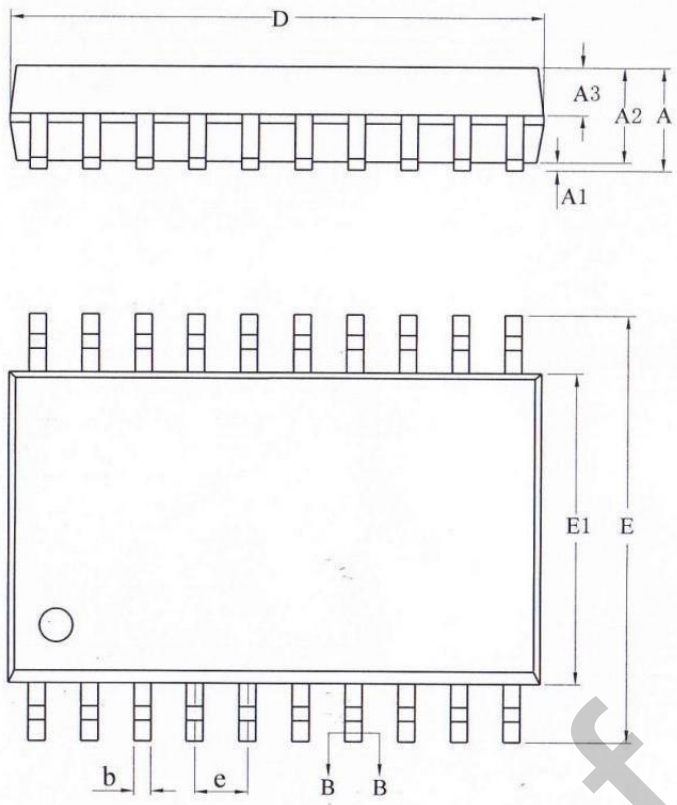
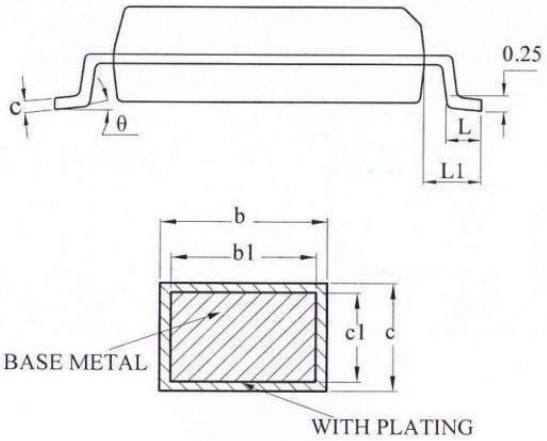
8.2 SSOP20L Package





SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.85
A1	0.05	—	0.25
A2	1.40	1.50	1.60
A3	0.62	0.67	0.72
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	7.10	7.20	7.30
E	7.60	7.80	8.00
E1	5.20	5.30	5.40
e	0.65BSC		
L	0.75	—	1.05
L1	1.25REF		
θ	0	—	8°

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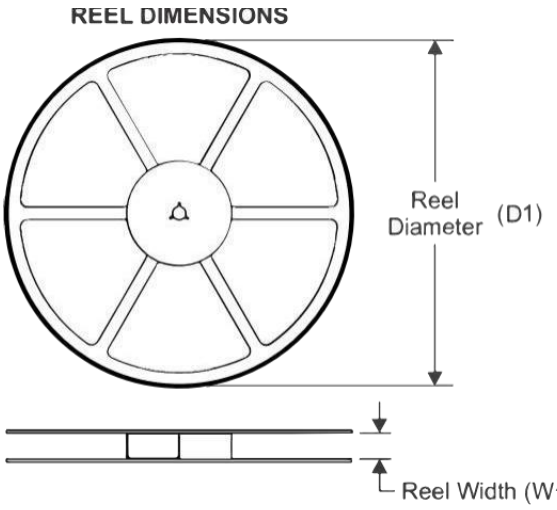
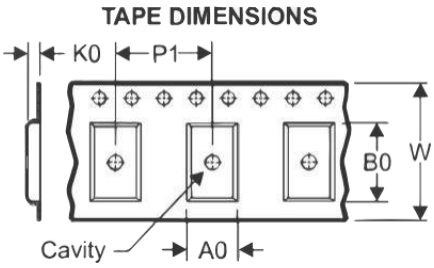
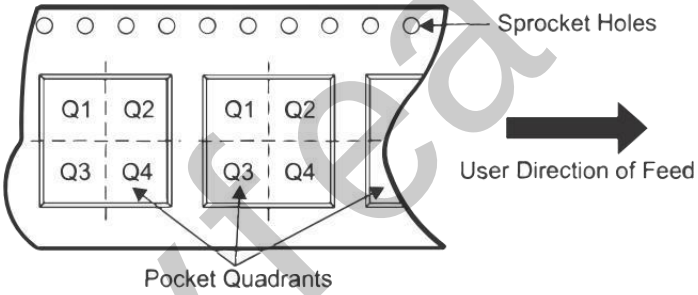
8.3 Reel and Tape Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANTASSIGNMENTS F ●r PIN 1 ORIENTATION IN TAPE



Package Type	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	329	12.4	5.30	5.30	1.10	8.00	12.00	Q1
SSOP20L	330	16.4	8.40	7.75	2.50	12.00	16.00	Q1

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9 Ordering Information

Order Number	Chip Model	Package	SPQ	Note
FRTD31865Q-T&R	FRTD31865Q	QFN-20	4000	Tape & Reel
FRTD31865S-T&R	FRTD31865S	SSOP20L	2000	Tape & Reel

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