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Nyfea product specification

PRODUCT SPECIFICATION

Customer : _____

Product Name : Contactless Reader/Writer IC

Part NO : NF663E

Issue Date: _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Introduction

This document describes the functionality and electrical specifications of the NF663E contactless reader/writer IC.

2 General description

The NF663E is a highly integrated transceiver IC for contactless communication at 13.56 MHz. The NF663E supports the following operating modes:

- Read/write mode supporting ISO/IEC 14443A and MIFARE.
- Read/write mode supporting ISO/IEC 14443B.
- Read/write mode supporting JIS X 6319-4, comparable with the FeliCa scheme.
- Passive initiator mode according to ISO/IEC 18092.
- Read/write mode supporting ISO/IEC 15693.
- Read/write mode supporting ICODE EPC UID and EPC OTP.
- Read/write mode supporting ISO/IEC 18000-3 mode 3 and EPC Class-1 HF.

In this document, the term FeliCa refers to JIS X 6319-4.

The integrated driver stage provides a direct matching interface to a reader/writer antenna. It enables contactless data exchange with ISO/IEC 14443A and MIFARE-series cards and transponders without requiring external active components in the RF path. The on-chip baseband processing unit manages framing and error-detection functions, including parity verification and CRC calculation, as required by ISO/IEC 14443A.

The NF663E supports MIFARE Classic 1K, MIFARE Classic 4K, MIFARE Ultralight, MIFARE Ultralight C, MIFARE Plus, and MIFARE DESFire products. Bidirectional transfer rates of up to 848 kbit/s are supported.

For ISO/IEC 14443B reader/writer operation, the device handles layer 2 and layer 3 functions, except for anticollision. Anticollision and higher-layer procedures are implemented in the host-controller firmware.

The device incorporates a dedicated receiver front-end for FeliCa-coded signal demodulation and decoding. The on-chip logic manages FeliCa frame formatting and CRC-based error detection, with bidirectional transfer rates of up to 424 kbit/s.

The NF663E supports passive initiator mode in accordance with ISO/IEC 18092. It also supports vicinity-range applications based on ISO/IEC 15693, EPC UID, and ISO/IEC 18000-3 mode 3 / EPC Class-1 HF.

The following host interfaces are supported:

- Serial Peripheral Interface (SPI).
- Serial UART, similar to RS232, with voltage levels dependent on the pin supply voltage.
- I^2C-bus interface, including I^2C and I^2CL implementations.

The NF663E provides a dedicated auxiliary I^2C interface for connection to a secure access module (SAM). The SAM can be used for secure key storage and as a cryptographic coprocessor.

3 Features and benefits

- High-RF-output-power frontend IC supporting transfer rates up to 848 kbit/s.
- Supports ISO/IEC 14443A, MIFARE, ISO/IEC 14443B, and FeliCa.
- P2P passive initiator mode in accordance with ISO/IEC 18092.
- Supports ISO/IEC 15693, ICODE EPC UID, and ISO/IEC 18000-3 mode 3 / EPC Class-1 HF.
- Supports MIFARE Classic encryption in read/write mode.
- Low-Power Card Detection (LPCD).
- RF-level compliance with the EMV contactless protocol specification can be achieved.
- Antenna connection requiring a minimum number of external components.

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- Supported host interfaces:
  - SPI up to 10 Mbit/s.
  - I^2C-bus up to 400 kBd in Fast mode and up to 1000 kBd in Fast-mode Plus.
  - Serial UART up to 1228.8 kBd, with voltage levels dependent on the pin supply voltage.
- Separate I^2C-bus interface for connection to a secure access module (SAM).
- 512-byte FIFO buffer for high transaction performance.
- Flexible power-saving modes, including hard power-down, standby, and low-power card detection.
- Integrated PLL derives the system clock from a 27.12 MHz RF crystal.
- 3.0 V to 5.5 V power supply.
- Up to eight freely programmable input/output pins.
- Typical read/write operating distance up to 12 cm with an ISO/IEC 14443A / MIFARE card, depending on antenna size and tuning.

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	3.0	5.0	5.5	V
$V_{DD}(PV_{DD})$	PVDD supply voltage	[1]	3.0	5.0	V_{DD}	V
$V_{DD}(TV_{DD})$	TVDD supply voltage	—	3.0	5.0	5.5	V
I_{pd}	Power-down current	PDOWN pin pulled HIGH [2]	—	8	40	nA
I_{DD}	Supply current	—	—	17	20	mA
$I_{DD}(TV_{DD})$	TVDD supply current	[3], [4]	—	180	350	mA
T_{amb}	Ambient temperature	—	−25	+25	+85	° C
T_{stg}	Storage temperature	No supply voltage applied	−40	+25	+100	° C

[1] $V_{DD}(PV_{DD})$ must always be equal to or lower than V_{DD}.
[2] I_{pd} is the sum of all supply currents.
[3] $I_{DD}(TV_{DD})$ depends on $V_{DD}(TV_{DD})$ and on the external circuitry connected to TX1 and TX2.
[4] Typical value assumes a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz.

5 Ordering information

Table 2. Ordering information

Type number	Package name	Description	Version
NF663E	HVQFN32	Plastic thermal-enhanced very thin quad flat package; no leads; 32 terminals plus one central ground connection; body 5 × 5 × 0.85 mm; MSL2.	SOT617-1

6 Block diagram

The analog front-end performs modulation and demodulation of the antenna signals used by the contactless interface. Protocol-dependent behavior is controlled by the contactless UART under host configuration. The FIFO buffer provides fast data exchange between the host and the contactless UART, while the register bank stores analog and digital configuration settings.

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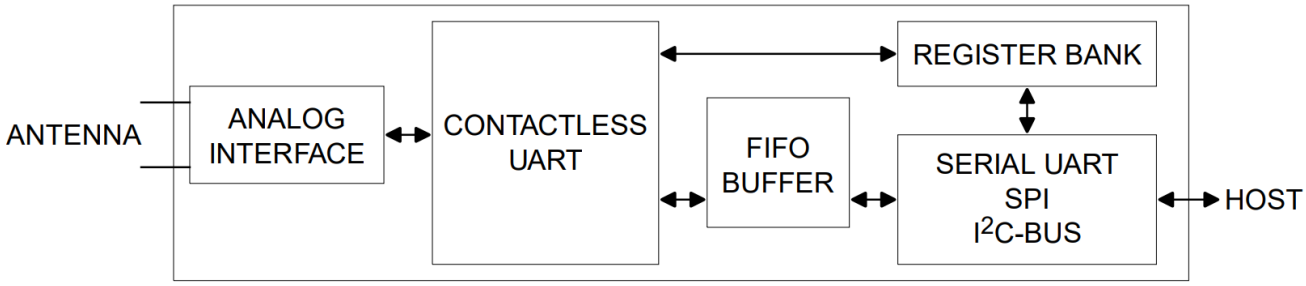


Figure 1. Simplified block diagram of the NF663E

7 Pinning information

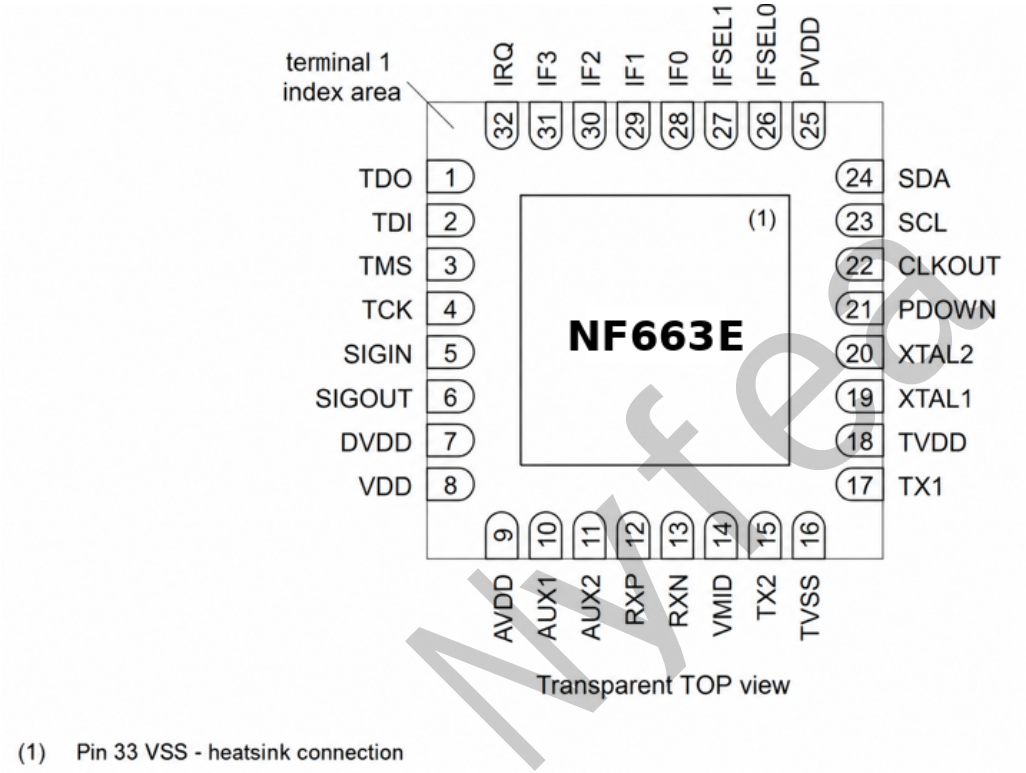


Figure 2. Pinning configuration HVQFN32 (SOT617-1)

7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type	Description
1	TDO	O	Test data output for the boundary-scan interface.
2	TDI	I	Test data input for the boundary-scan interface.
3	TMS	I	Test mode select for the boundary-scan interface.
4	TCK	I	Test clock for the boundary-scan interface.
5	SIGIN	I	Contactless communication interface output.
6	SIGOUT	O	Contactless communication interface input.
7	DV_{DD}	PWR	Digital power-supply buffer connection [1].
8	V_{DD}	PWR	Main power supply.
9	AV_{DD}	PWR	Analog power-supply buffer connection [1].
10	AUX1	O	Auxiliary output used for analog test signals.

Pin	Symbol	Type	Description
11	AUX2	O	Auxiliary output used for analog test signals.
12	RXP	I	Positive receiver input for the received RF signal.
13	RXN	I	Negative receiver input for the received RF signal.
14	VMID	PWR	Internal receiver reference-voltage buffer connection [1].
15	TX2	O	Transmitter output 2; delivers the modulated 13.56 MHz carrier.
16	TV_{SS}	PWR	Transmitter ground for the TX1 and TX2 output stage.
17	TX1	O	Transmitter output 1; delivers the modulated 13.56 MHz carrier.
18	TV_{DD}	PWR	Transmitter supply voltage.
19	XTAL1	I	Crystal oscillator input. Also accepts an externally generated 27.12 MHz clock.
20	XTAL2	O	Crystal oscillator output.
21	PDOWN	I	Power-down input.
22	CLKOUT	O	Clock output.
23	SCL	O	Serial clock line.
24	SDA	I/O	Serial data line.
25	PV_{DD}	PWR	Pad power supply.
26	IFSEL0	I	Host-interface selection input 0.
27	IFSEL1	I	Host-interface selection input 1.
28	IF0	I/O	Multifunction host-interface pin; assignable to UART, SPI, I^2C, or I^2CL.
29	IF1	I/O	Multifunction host-interface pin; assignable to SPI, I^2C, or I^2CL.
30	IF2	I/O	Multifunction host-interface pin; assignable to UART, SPI, I^2C, or I^2CL.
31	IF3	I/O	Multifunction host-interface pin; assignable to UART, SPI, I^2C, or I^2CL.
32	IRQ	O	Interrupt-request output.
33	V_{SS}	PWR	Ground and exposed heat-sink connection.

[1] This pin is intended only for connection of a buffer capacitor. Applying an external supply voltage may damage the device.

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8 Functional description

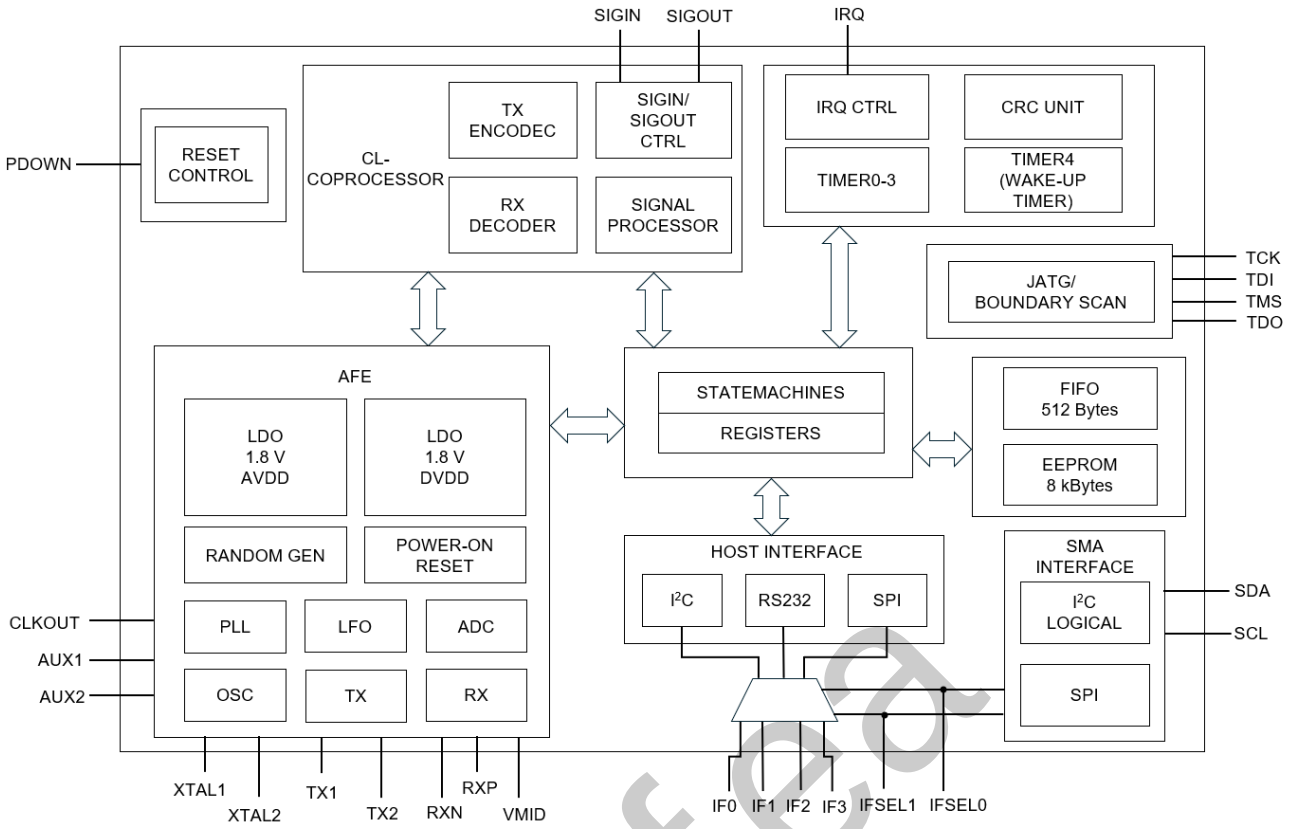


Figure 3. Detailed functional block diagram of the NF663E

8.1 Interrupt controller

The interrupt controller controls the activation and deactivation of interrupt requests. Each interrupt source can be enabled or disabled by firmware. Firmware can also set new interrupt events or clear pending events.

Two 8-bit interrupt-status registers and two corresponding 8-bit enable registers are provided. Bit 7 of each status register controls the setting or clearing of bits 0 to 6 in the same register.

Pending interrupt events are indicated through the global interrupt status and, when enabled, through the IRQ pin. The IRQ pin can be connected to an external interrupt input of the host controller.

Table 4. Interrupt sources

Interrupt bit	Interrupt source	Set automatically when
Timer0Irq	Timer unit	Timer0 counter underflows.
Timer1Irq	Timer unit	Timer1 counter underflows.
Timer2Irq	Timer unit	Timer2 counter underflows.
Timer3Irq	Timer unit	Timer3 counter underflows.
TxIrq	Transmitter	A transmitted data stream ends.
RxIrq	Receiver	A received data stream ends.
IdleIrq	Command register	A command execution finishes.
HiAlertIrq	FIFO pointer	The FIFO fill level reaches the upper threshold configured by WaterLevel.
LoAlertIrq	FIFO pointer	The FIFO fill level reaches the lower threshold configured by WaterLevel.

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Interrupt bit	Interrupt source	Set automatically when
ErrIrq	Contactless UART	A communication error is detected.
LPCDIrq	LPCD	A card is detected in low-power card-detection mode.
RxSOFIrq	Receiver	A start-of-frame delimiter or subcarrier is detected.
GlobalIrq	All enabled sources	Any enabled interrupt source becomes pending.

8.2 Timer module

The NF663E contains five timer channels. Timer0 to Timer3 use a selectable clock source configured through their control registers. Available clock sources include the 13.56 MHz system clock, a 212 kHz clock derived from the 27.12 MHz crystal, or an underflow event from another timer channel. Each timer contains a 16-bit down-counter with a programmable reload value from 0000h to FFFFh.

Timer4 is dedicated to wake-up functions and uses the internal Low-Frequency Oscillator (LFO) as its clock source.

The TControl register provides start/stop control and running-status information. Each timer has independent reload, counter-value, and operating-control registers. The timer unit supports timeout counting, watchdog operation, stopwatch measurement, programmable one-shot operation, and periodic triggering.

Each timer decrements on every active timer-clock edge. When the counter reaches 0000h, the associated interrupt is generated on the next clock edge if enabled. Depending on the selected mode, the timer either stops at zero or reloads automatically and continues counting.

8.2.1 Timer modes

8.2.1.1 Time-out and watchdog counter

After the reload value is programmed and counting is started, the timer counts down until a configured stop condition occurs or the counter reaches zero. If the stop condition occurs first, the timer stops without generating an interrupt. If the counter reaches zero first, a timer interrupt is generated, indicating that the expected event did not occur within the programmed time.

8.2.1.2 Wake-up timer

Timer4 can wake the system from standby after a programmable interval. For Low-Power Card Detection, T4AutoWakeUp and T4AutoRestart can be enabled so that the device wakes periodically, checks for a card, and returns automatically to standby when no card is detected.

8.2.1.3 Stopwatch

The timer can measure the interval between configurable start and stop events. After the reload value is programmed, counting begins at the selected start event and stops at the selected stop event. The elapsed time is calculated as:

$$\Delta T = (T_{reload} - T_{counter}) \times T_{timer} \quad (1)$$

If the timer underflows, the measured interval calculated with Equation (1) is invalid. The underflow condition can be identified from the corresponding interrupt flag.

8.2.1.4 Programmable one-shot timer

The host configures the timer and interrupt controller, starts the timer, and waits for the interrupt. A single interrupt is generated when the programmed interval expires.

8.2.1.5 Periodic trigger

When T(x)AutoRestart and the associated interrupt are enabled, the timer reloads automatically and generates an interrupt after each programmed timer period.

8.3 Contactless interface unit

The NF663E contactless interface supports the following read/write operating modes:

- ISO/IEC 14443A and MIFARE.
- ISO/IEC 14443B.

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- FeliCa.
- ISO/IEC 15693 and ICODE.
- ICODE EPC UID.
- ISO/IEC 18000-3 mode 3 / EPC Class-1 HF.

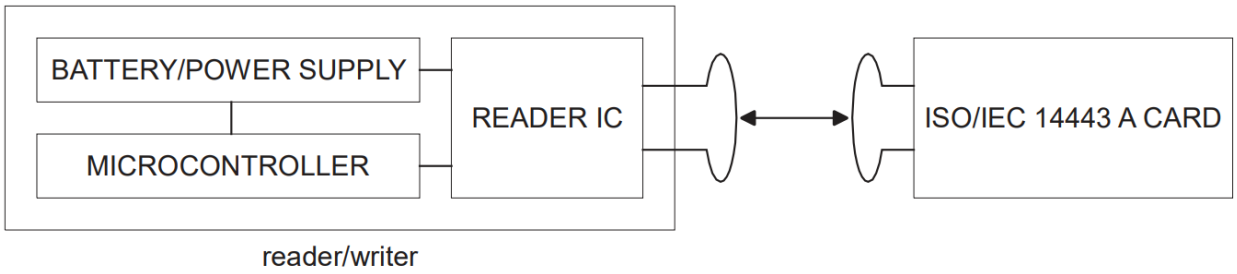
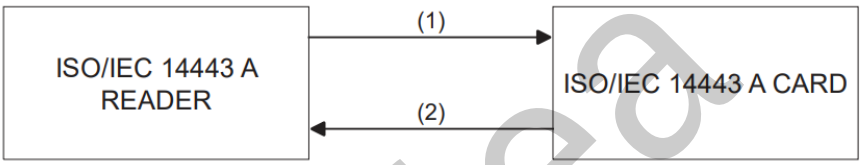


Figure 4. Typical NF663E contactless reader system

A typical application uses a host microcontroller to implement higher-layer protocol functions and a suitable power source for the NF663E and antenna driver.

8.3.1 ISO/IEC 14443A / MIFARE functionality



(1) Reader to Card 100 % ASK, Miller Coded, Transfer speed 106 kbit/s to 848 kbit/s

(2) Card to Reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Figure 5. ISO/IEC 14443A / MIFARE physical-layer communication

Table 5. Communication overview for ISO/IEC 14443A / MIFARE reader/writer

Direction	Signal parameter	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Reader to card	Modulation	100% ASK	100% ASK	100% ASK	100% ASK
	Bit encoding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
	Bit rate	$f_c/128$	$f_c/64$	$f_c/32$	$f_c/16$
Card to reader	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	$f_c/16$	$f_c/16$	$f_c/16$	$f_c/16$
	Bit encoding	Manchester	BPSK	BPSK	BPSK

The NF663E and its host controller together manage the complete ISO/IEC 14443A / MIFARE protocol. The on-chip CRC unit calculates CRC values according to ISO/IEC 14443A Part 3. Parity insertion is handled automatically and adapted to the selected transfer rate.

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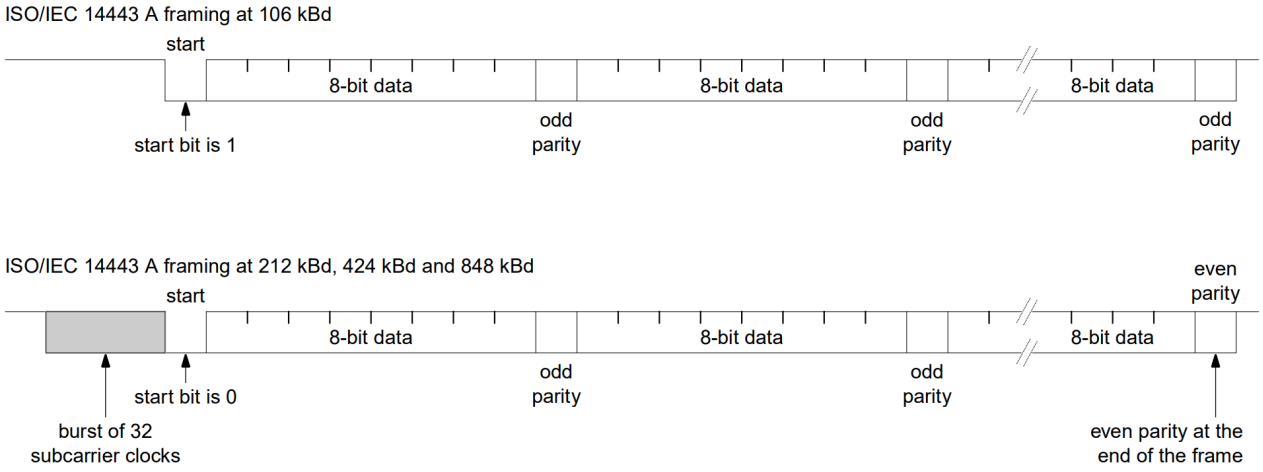
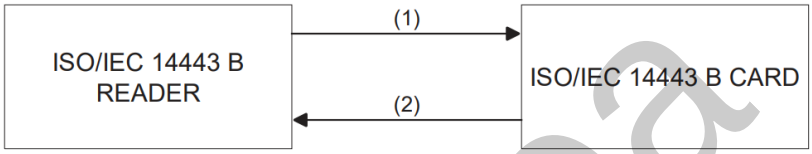


Figure 6. ISO/IEC 14443A / MIFARE framing and coding

8.3.2 ISO/IEC 14443B functionality



(1) Reader to Card NRZ, Miller coded, transfer speed 106 kbit/s to 848 kbit/s

(2) Card to reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Figure 7. ISO/IEC 14443B physical-layer communication

Table 6. Communication overview for ISO/IEC 14443B reader/writer

Direction	Signal parameter	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Reader to card	Modulation	10% ASK	10% ASK	10% ASK	10% ASK
	Bit encoding	NRZ	NRZ	NRZ	NRZ
	Bit rate	$f_c/128$	$f_c/64$	$f_c/32$	$f_c/16$
Card to reader	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	$f_c/16$	$f_c/16$	$f_c/16$	$f_c/16$
	Bit encoding	BPSK	BPSK	BPSK	BPSK

The NF663E and its host controller together manage the complete ISO/IEC 14443B protocol.

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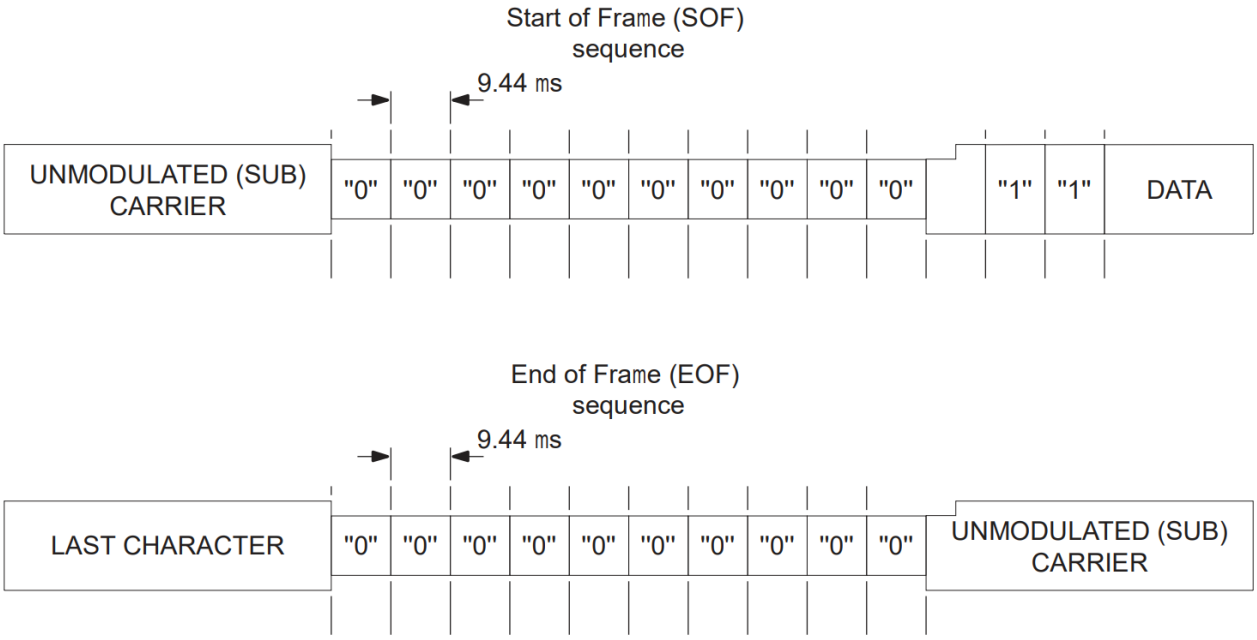


Figure 8. SOF and EOF according to ISO/IEC 14443B

8.3.3 FeliCa functionality

The FeliCa operating mode provides reader/writer-to-card communication according to the FeliCa protocol. The NF663E supports transfer rates of 212 kbit/s and 424 kbit/s.

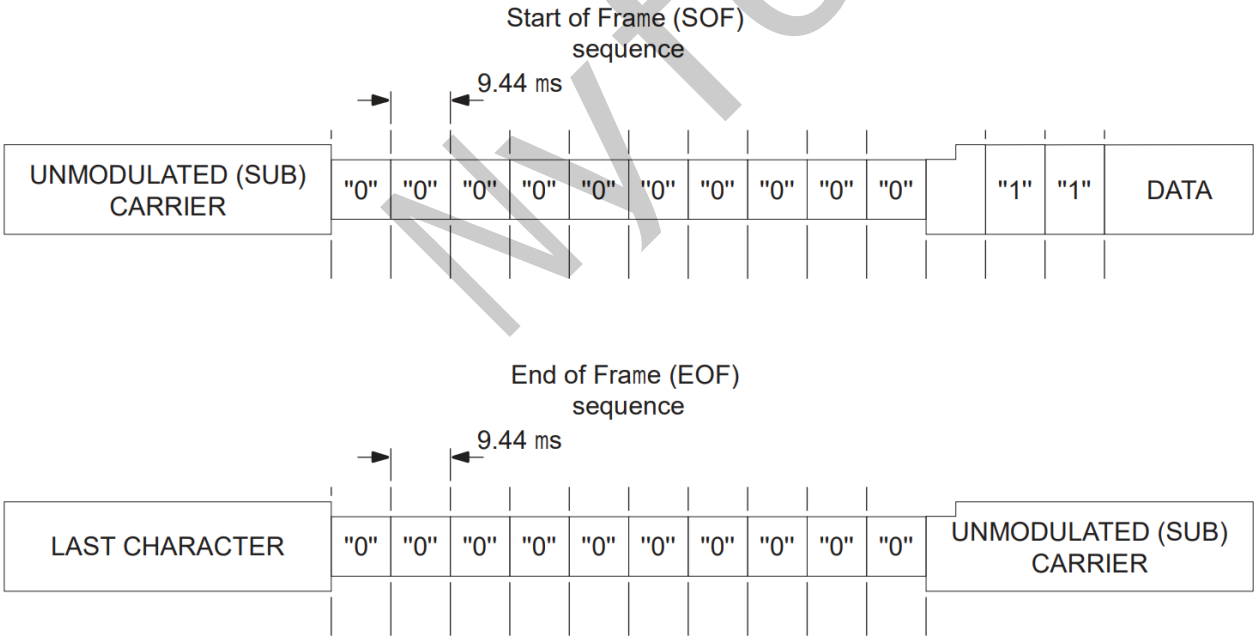


Figure 9. FeliCa read/write communication diagram

Table 7. Communication overview for FeliCa reader/writer

Direction	Signal parameter	212 kbit/s	424 kbit/s
Reader to card	Modulation	8% to 30% ASK	8% to 30% ASK
	Bit encoding	Manchester	Manchester
	Bit rate	$f_c/64$	$f_c/32$
Card to reader	Load modulation	$30/H^{1.2}$	$30/H^{1.2}$

Direction	Signal parameter	212 kbit/s	424 kbit/s
	Bit encoding	Manchester	Manchester

Note H is the RF field strength in A/m.

The NF663E must be connected to a dedicated host controller to support the complete FeliCa protocol.

8.3.3.1 FeliCa framing and coding

Table 8. FeliCa framing and coding

Preamble	Synchronization	Length	Data	CRC
00 00 00 00 00 00	B2 4D	LEN	n data bytes	CRC

A six-byte preamble of 00h values is followed by the two-byte synchronization pattern B2h and 4Dh. The length byte equals the number of payload bytes plus one for the length byte itself. The CRC is calculated using the FeliCa polynomial with most-significant-bit-first processing.

For transmission, the host writes only the length byte and payload data to the FIFO. The NF663E adds the preamble and synchronization pattern and calculates and appends the CRC automatically.

8.3.4 ISO/IEC 15693 functionality

Table 9. Communication overview for ISO/IEC 15693 reader/writer - reader to label

Communication direction	Signal type	Transfer speed	
		f_c / 8192	f_c / 512
Reader to label (send data from the NF663E to a card)	Reader-side modulation	10 % to 30 % ASK or 100 % ASK	10 % to 30 % ASK or 90 % to 100 % ASK
	Bit encoding	1/256	1/4
	Data rate	1.66 kbit/s	26.48 kbit/s

Table 10. Communication overview for ISO/IEC 15693 reader/writer - label to reader

Communication direction	Signal type	Transfer speed			
		6.62 (6.67) kbit/s	13.24 kbit/s[1]	26.48 (26.69) kbit/s	52.96 kbit/s
Label to reader (NF663E receives data from a card) f_c = 13.56 MHz	Card-side modulation	Not supported	Not supported	Single (dual) subcarrier load modulation ASK	Single subcarrier load modulation ASK
	Bit length (µs)	-	-	37.76 (37.46)	18.88
	Bit encoding	-	-	Manchester coding	Manchester coding
	Subcarrier frequency [MHz]	-	-	f_c / 32 (f_c / 28)	f_c / 32

[1] Fast inventory (page) read command only (ICODE proprietary command).

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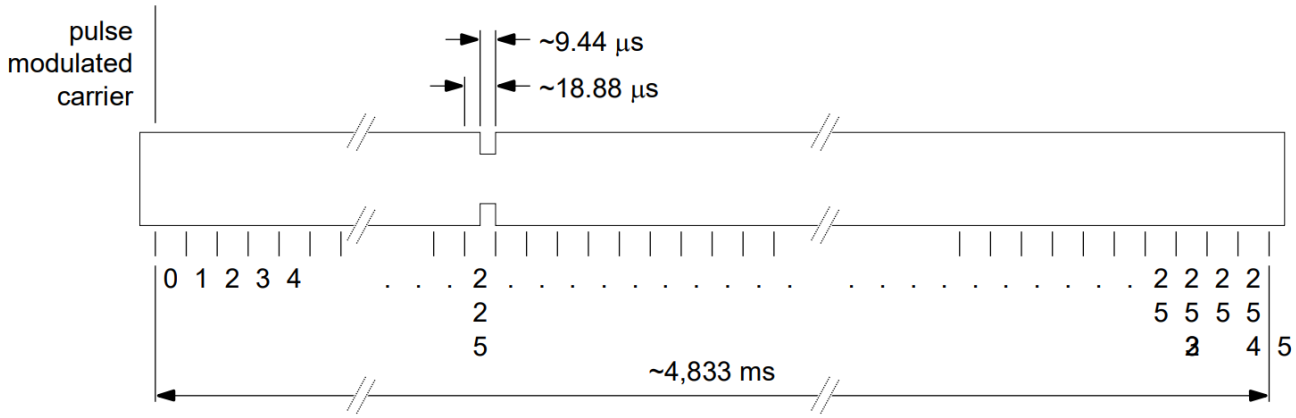


Figure 10. ISO/IEC 15693 standard mode reader-to-label data coding

8.3.5 EPC-UID/UID-OTP functionality

The physical parameters are described in Table 11.

Table 11. Communication overview for EPC/UID

Communication direction	Signal type	Transfer speed	
		26.48 kbit/s	52.96 kbit/s
Reader to card (send data from the NF663E to a card)	Reader-side modulation	10 % to 30 % ASK	
	Bit encoding	RTZ	
	Bit length	37.76 µs	
Card to reader (NF663E receives data from a card)	Card-side modulation		Single subcarrier load modulation
	Bit length		18.88 µs
	Bit encoding		Manchester coding

Data encoding and frame formatting are implemented in accordance with the EPCglobal Class-1 specification for the 13.56 MHz ISM band, covering RFID tag interface requirements as defined in the Candidate Recommendation, Revision 1.0.0.

8.3.6 ISO/IEC 18000-3 mode 3 / EPC Class-1 HF functionality

The ISO/IEC 18000-3 mode 3 / EPC Class-1 HF protocol is not described in this document. For a detailed explanation, refer to the ISO/IEC 18000-3 mode 3 / EPC Class-1 HF standard.

8.3.7 ISO/IEC 18092 mode

The NF663E supports passive-initiator operation at transfer rates of 106 kbit/s, 212 kbit/s, and 424 kbit/s, as specified in ISO/IEC 18092.

In this context, the following definitions apply:

Passive communication: the target responds to initiator commands through load-modulation backscatter. The initiator generates and maintains the RF carrier throughout the exchange.

Initiator: generates the 13.56 MHz RF carrier and initiates the communication sequence as defined by ISO/IEC 18092.

Target: replies to initiator commands through load-modulation backscatter in passive mode, or by generating and modulating its own RF carrier in active mode.

8.3.7.1 Passive communication mode

Passive-mode operation is characterized by the target responding to an initiator request via load modulation of the incident carrier, while the initiator powers the RF carrier.

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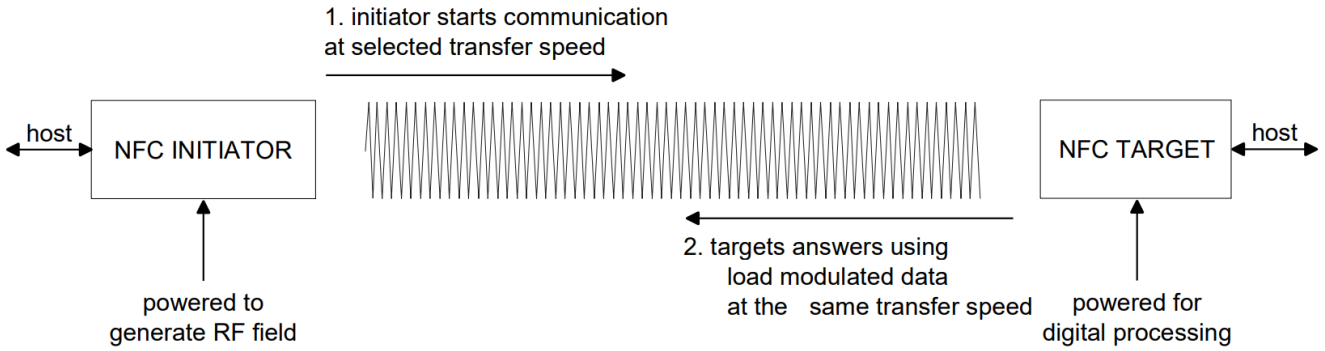


Figure 11. Passive communication mode

Table 12. Communication overview for passive communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s
Initiator → target	According to ISO/IEC 14443A: 100 % ASK, Modified Miller coded	According to FeliCa: 8 % to 30 % ASK, Manchester coded	
Target → initiator	According to ISO/IEC 14443A: subcarrier load modulation, Manchester coded	According to FeliCa: > 12 % ASK, Manchester coded	

The contactless UART of the NF663E and a dedicated host controller are required to handle the ISO/IEC 18092 passive initiator protocol.

8.3.7.2 ISO/IEC 18092 framing and coding

Framing and coding in passive communication mode are defined by ISO/IEC 18092.

Table 13. Framing and coding overview

Transfer speed	Framing and coding
106 kbit/s	According to the ISO/IEC 14443A / MIFARE scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

8.3.7.3 ISO/IEC 18092 protocol support

The ISO/IEC 18092 protocol is not described in this document. Refer to the ISO/IEC 18092 standard for protocol details.

8.3.8 EPC Class-1 HF and ICODE

8.3.8.1 Data encoding ICODE

The ICODE protocols mainly use three data-encoding methods:

- "1 out of 4" coding
- "1 out of 256" coding
- Return-to-Zero (RZ) coding

All three coding schemes are generated by the ICODE generator. Supported EPC Class-1 HF modes are:

- 2 pulses with a 424 kbit/s subcarrier
- 4 pulses with a 424 kbit/s subcarrier
- 2 pulses with an 848 kbit/s subcarrier

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- 4 pulses with an 848 kbit/s subcarrier

8.4 Host interfaces

8.4.1 Host interface configuration

The NF663E provides direct host connectivity through SPI, I^2C, I^2CL, and UART interfaces. After power-up or wake-up from power-down, the device evaluates IFSEL1 and IFSEL0 at the end of initialization and selects the active interface using the hard-wired pin-strapping scheme below.

Table 14. Connection scheme for detecting the different interface types

Pin	Pin symbol	UART	SPI	I^2C	I^2C-L
28	IF0	RX	MOSI	ADR1	ADR1
29	IF1	-	SCK	SCL	SCL
30	IF2	TX	MISO	ADR2	SDA
31	IF3	1	NSS	SDA	ADR2
26	IFSEL0	0	0	1	1
27	IFSEL1	0	1	0	1

8.4.2 SPI interface

8.4.2.1 General

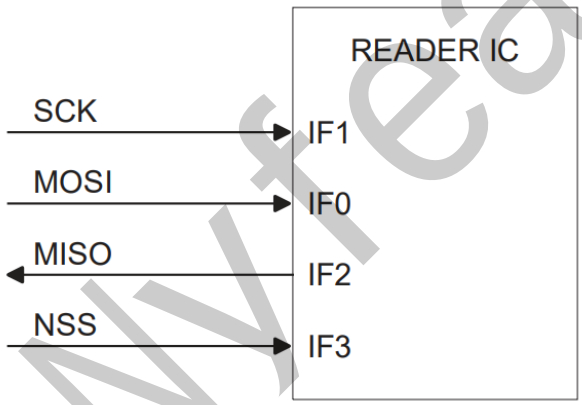


Figure 12. Connection to host with SPI

In SPI mode, the NF663E operates as a slave. The bus master supplies SCK. MOSI carries master-to-slave data and MISO carries slave-to-master data. The interface supports data rates up to 10 Mbit/s.

On MOSI and MISO, each byte is transmitted MSB first. MOSI is sampled on the rising SCK edge and changes on the falling edge. The NF663E drives MISO on the falling edge so that it can be sampled on the following rising edge. SCK is low during idle periods.

8.4.2.2 Read data

For an SPI read, the first byte defines the operation mode in the LSB and the register address in the remaining bits.

Table 15. Byte order for MOSI and MISO

	byte 0	byte 1	byte 2	byte 3 to n-1	byte n	byte n+1
MOSI	address 0	address 1	address 2	…	address n	00h
MISO	X	data 0	data 1	…	data n-1	data n

Remark: The Most Significant Bit (MSB) is sent first.

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8.4.2.3 Write data

For an SPI write, more than one byte can be transferred after a single address byte. The first byte defines the mode and register address.

Table 16. Byte order for MOSI and MISO

	byte 0	byte 1	byte 2	byte 3 to n-1	byte n	byte n+1
MOSI	address 0	data 0	data 1	···	data n-1	data n
MISO	X	X	X	···	X	X

Remark: The Most Significant Bit (MSB) is sent first.

8.4.2.4 Address byte

The least significant bit of the first byte selects the direction: 1 for read and 0 for write. Bits 7 to 1 contain the register address. During a multi-byte transfer, the register address increments automatically after each byte, except when the FIFO register is selected.

Table 17. Address byte structure

7	6	5	4	3	2	1	0
address 6	address 5	address 4	address 3	address 2	address 1	address 0	1 read 0 write
MSB							LSB

8.4.2.5 Timing specification SPI

Table 18. Timing conditions SPI

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	50	-	-	ns
t_{SCKH}	SCK HIGH time	50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	25	-	-	ns
$t_{su(D-SCKH)}$	Data input to SCK HIGH setup time	25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time	0	-	-	ns
t_{NSSH}	NSS HIGH time	50	-	-	ns

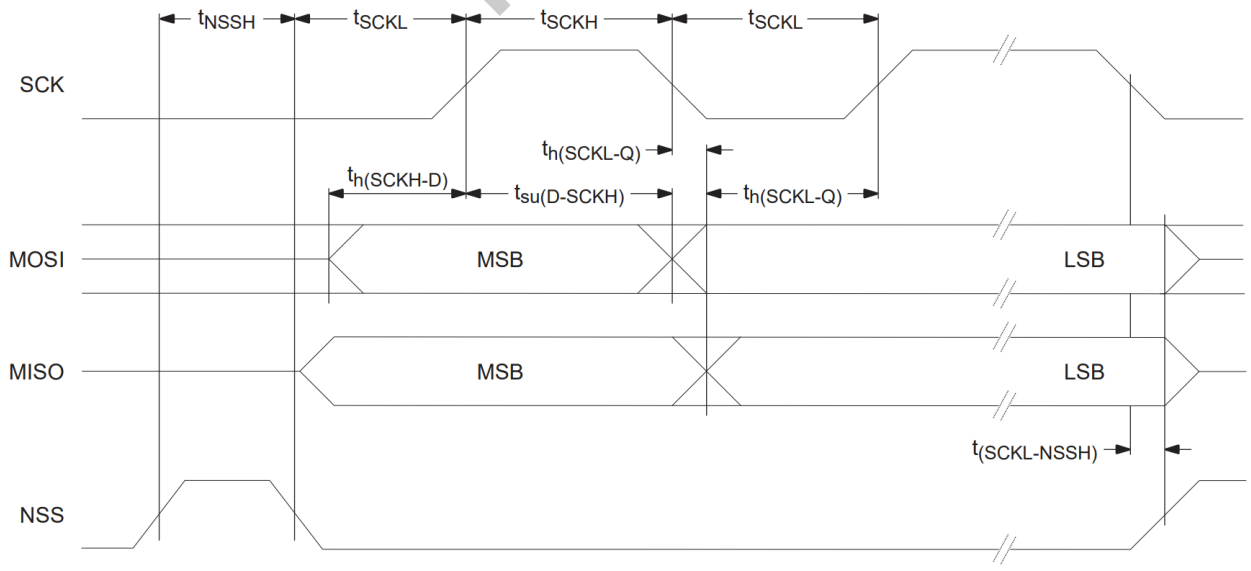


Figure 13. SPI timing diagram

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Remark: NSS must remain LOW while bytes in one data stream are transferred, and must return HIGH between separate data streams.

8.4.3 RS232 interface

8.4.3.1 Selection of the transfer speeds

The internal UART is compatible with an RS232-style serial interface. The SerialSpeed register selects the baud rate through fields BR_T0 and BR_T1. The default transfer speed is 115.2 kbit/s.

Table 19. Settings of BR_T0 and BR_T1

BR_T0	0	1	2	3	4	5	6	7
Factor BR_T0	1	1	2	4	8	16	32	64
Range BR_T1	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 20. Selectable transfer speeds

Transfer speed (kbit/s)	SerialSpeed register (hex.)	Transfer-speed error (%)
7.2	FA	-0.25
9.6	EB	0.32
14.4	DA	-0.25
19.2	CB	0.32
38.4	AB	0.32
57.6	9A	-0.25
115.2	7A	-0.25
128.0	74	-0.06
230.4	5A	-0.25
460.8	3A	-0.25
921.6	1C	1.45
1228.8	15	0.32

The selectable transfer speeds are calculated as follows:

$$BR\_T0 = 0: \text{transfer speed} = 27.12\ MHz\ /\ (BR\_T1 + 1)$$
$$BR\_T0 > 0: \text{transfer speed} = 27.12\ MHz\ /\ (BR\_T1 + 33)\ /\ 2^{(BR\_T0 - 1)}$$

Remark: Transfer speeds above 1228.8 kbit/s are not supported.

8.4.3.2 Framing

Table 21. UART framing

Bit	Length	Value
Start bit (Sa)	1 bit	0
Data bits	8 bit	Data
STOP bit (So)	1 bit	1

Remark: Data and address bytes are sent LSB first. No parity bit is used.

Read data: the first transmitted byte contains the operation and register address. IF3 must be asserted to enable the read operation.

Table 22. Byte order to read data

Mode	byte 0	byte 1
RX	address	-
TX	-	data 0

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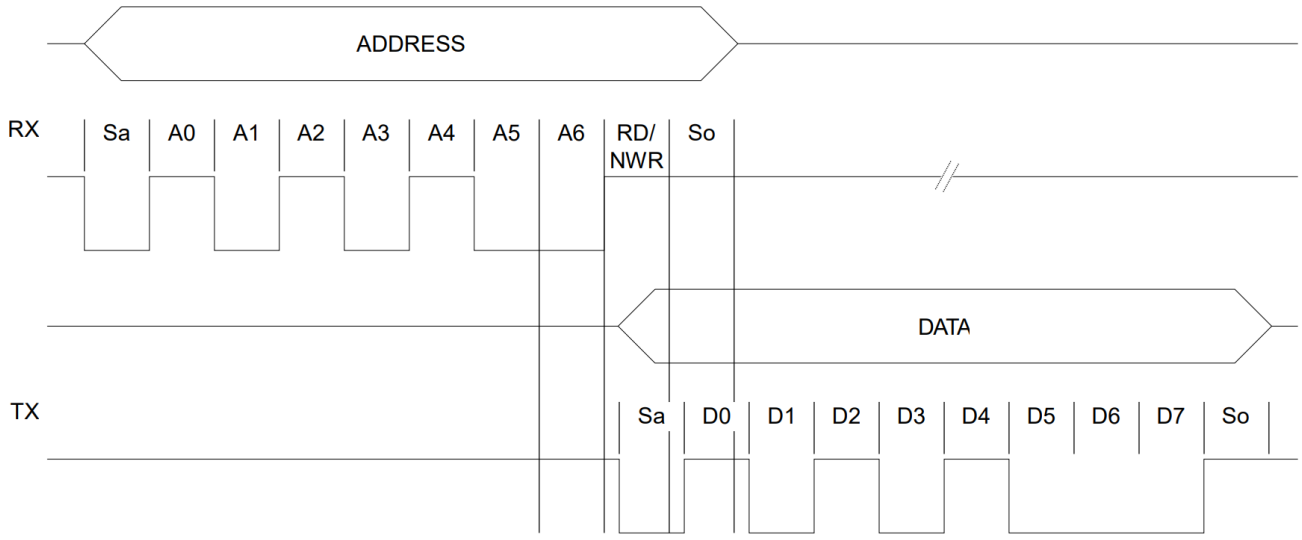


Figure 14. UART read timing diagram

Write data: the first transmitted byte defines the operation and register address.

Table 23. Byte order to write data

Mode	byte 0	byte 1
RX	address 0	data 0
TX	-	address 0

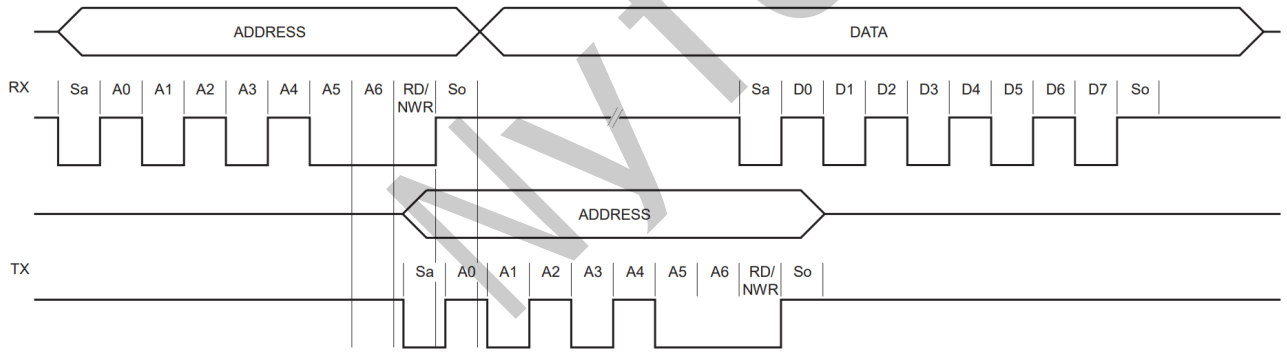


Figure 15. UART write timing diagram

Remark: Data can be sent before the address is received.

8.4.4 I²C-bus interface

8.4.4.1 General

The NF663E includes an I²C slave interface for low-pin-count host connectivity. It can operate as a slave receiver or slave transmitter and supports standard mode, fast mode, and fast-mode plus.

- The NF663E does not stretch the clock.
- The general call and software reset through the general call are not supported.
- The I²C device ID is not supported.
- The interface operates only as a slave; clock generation and bus arbitration are not implemented.
- High-speed mode is not supported.

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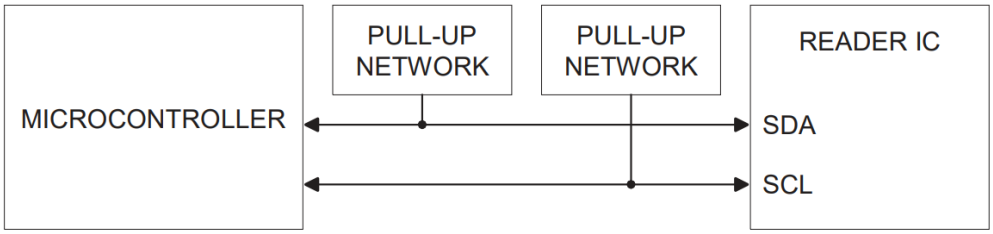


Figure 16. I²C-bus interface

SDA is bidirectional and is connected to a positive supply through a pull-up resistor. SDA and SCL are HIGH while no data is transmitted. Fast mode supports up to 400 kbit/s, and fast-mode plus supports up to 1 Mbit/s. When I²C is selected, spike suppression on SDA and SCL is enabled automatically.

8.4.4.2 I²C data validity

SDA must remain stable while SCL is HIGH. SDA may change only while SCL is LOW.

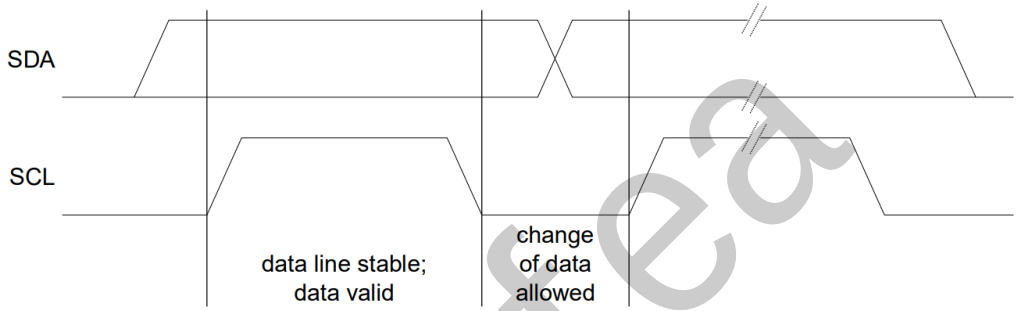


Figure 17. I²C-bus data validity

8.4.4.3 I²C START and STOP conditions

A START condition is a HIGH-to-LOW transition on SDA while SCL is HIGH. A STOP condition is a LOW-to-HIGH transition on SDA while SCL is HIGH. The master generates both conditions. A repeated START keeps the bus occupied and has the same functional role as START.

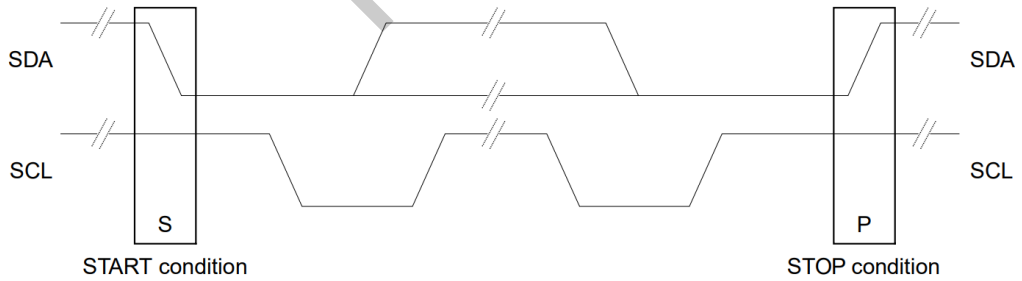


Figure 18. I²C-bus START and STOP conditions

8.4.4.4 I²C byte format

Every byte is followed by an acknowledge bit. Data is transferred MSB first. The number of bytes in one transfer is unrestricted, provided that the required read/write cycle format is observed.

8.4.4.5 I²C acknowledge

An acknowledge response is required after each transmitted byte. The master generates the acknowledge clock pulse. During this pulse, the transmitter releases SDA and the receiver drives SDA LOW for a valid acknowledge.

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A receiving master terminates a slave-transmitter transfer by withholding ACK on the final byte. The slave releases SDA, after which the master can generate STOP or repeated START.

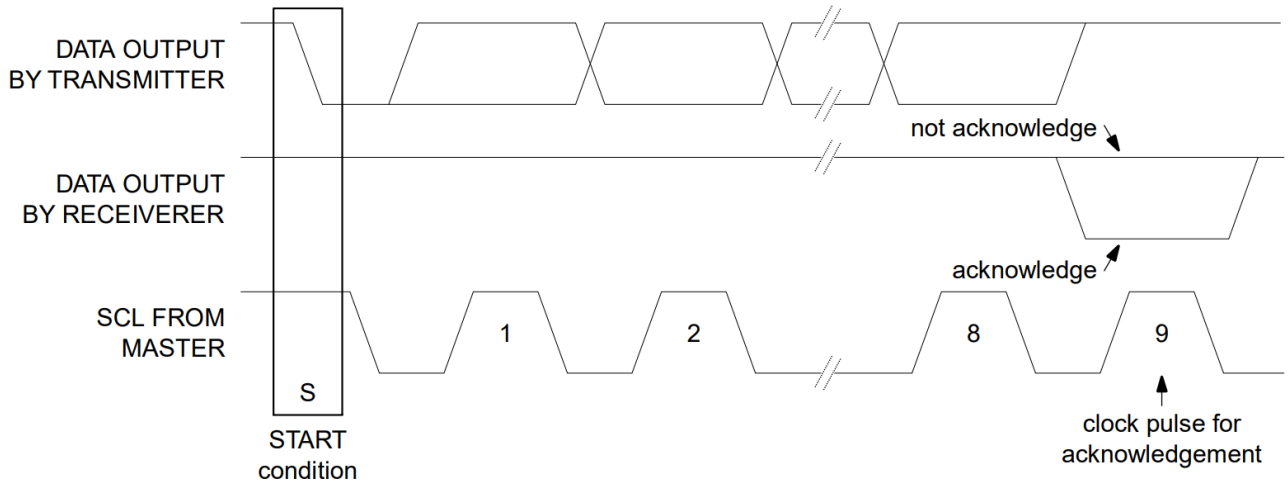


Figure 19. Acknowledge on the I²C-bus

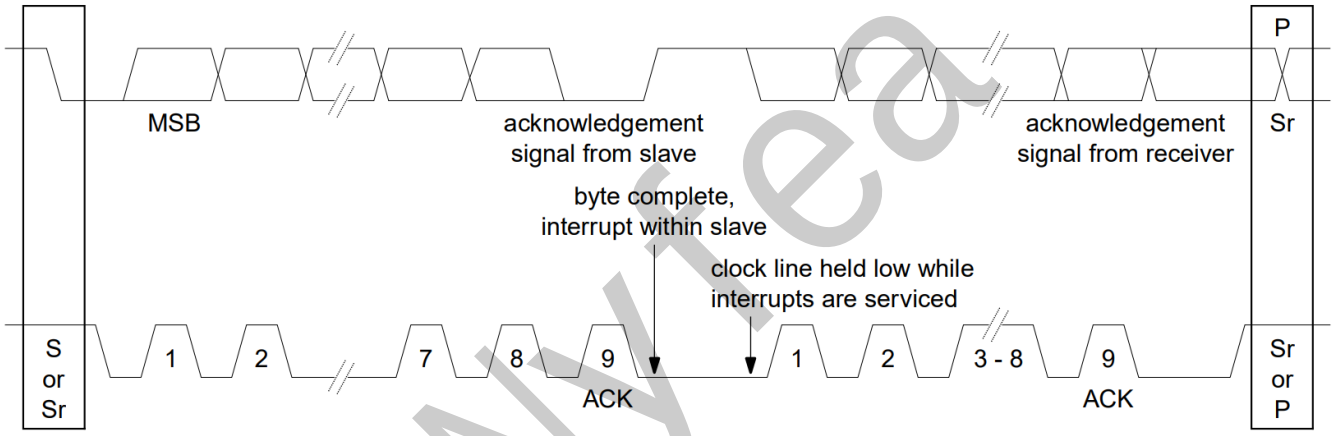


Figure 20. Data transfer on the I²C-bus

8.4.4.6 I²C 7-bit addressing

The first byte after START selects the slave. For all NF663E devices, the upper five address bits are fixed to 01010b. ADR_2 and ADR_1 are configurable through interface pins or the I²C-address EEPROM register. System design must avoid conflicts with reserved or already-used addresses.

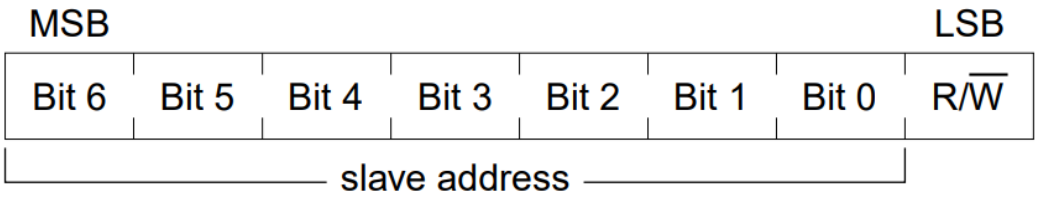


Figure 21. First byte following the START procedure

8.4.4.7 I²C-register write access

A write frame starts with the slave address, followed by the NF663E register address and one or more data bytes. For normal registers, the internal pointer increments automatically. When FIFO is selected, every data byte is written to the same FIFO address. The R/W bit is 0.

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8.4.4.8 I²C-register read access

A read begins with a write phase that selects the register address. The master then issues a read phase and the NF663E returns one or more data bytes. The address increments automatically, except for FIFO. The read-phase R/W bit is 1.

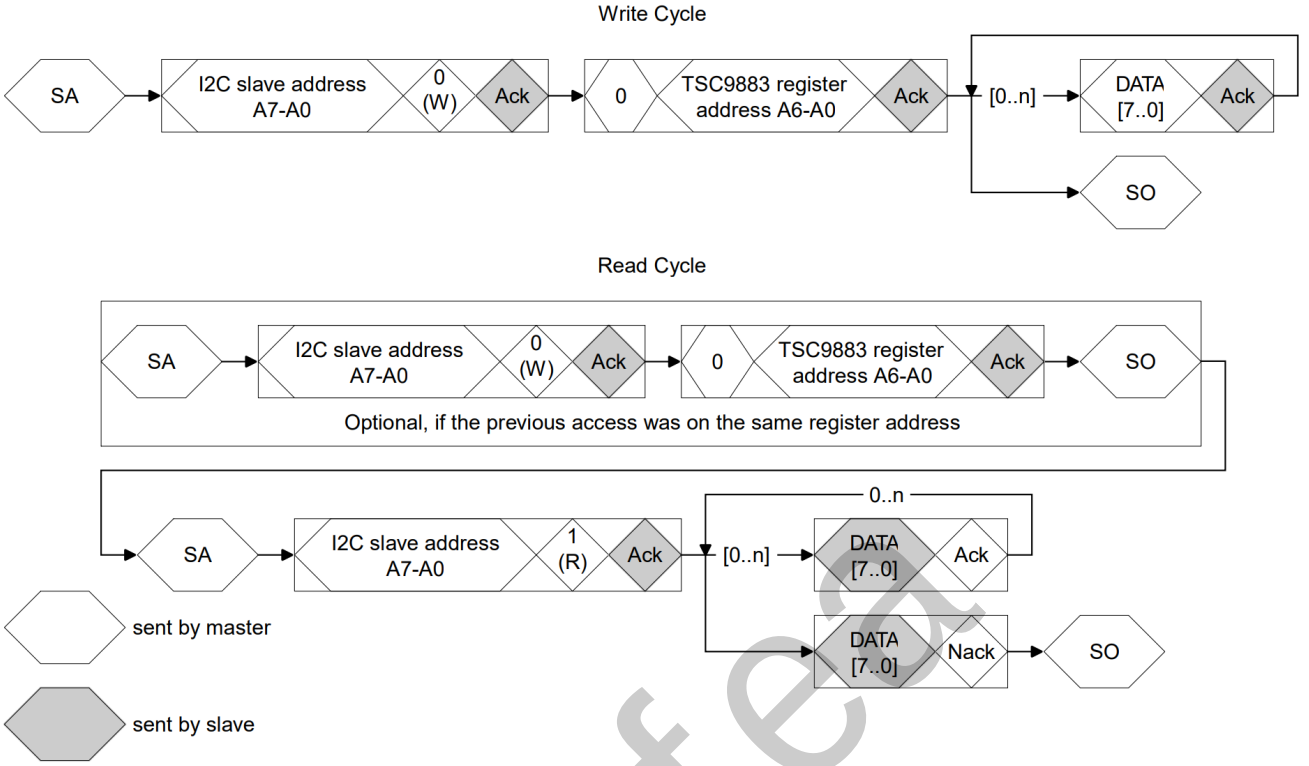


Figure 22. I²C register read and write access

8.4.4.9 I²CL-bus interface

The NF663E provides an I²C-like logical interface implemented with general-purpose I/O cells. Logical protocol behavior follows I²C fast mode, but the electrical timing does not comply with the standard. The maximum data rate is 5 MBaud. The fixed address prefix is 01010b and the last two bits are user configurable.

Table 24. Timing parameters I²CL

Parameter	Min	Max	Unit
f_{SCL}	0	5	MHz
$t_{HD;STA}$	80	-	ns
t_{LOW}	100	-	ns
t_{HIGH}	100	-	ns
$t_{SU;SDA}$	80	-	ns
$t_{HD;DAT}$	0	50	ns
$t_{SU;DAT}$	0	20	ns
$t_{SU;STO}$	80	-	ns
t_{BUF}	200	-	ns

No external SDA pull-up resistor is required. An integrated bus-keeper holds the line. The interface is intended for a short, point-to-point connection and does not support multi-drop operation.

- SCL is always controlled by the master because clock stretching is not supported.
- During idle, the master drives SDA HIGH.
- Between START and STOP, master or slave drives SDA only while SCL is LOW.

- When SCL is HIGH, neither device actively drives SDA; the bus keeper maintains the state.

8.4.5 SAM interface I²C

8.4.5.1 SAM functionality

The NF663E includes a dedicated I²C interface for convenient integration of a MIFARE Secure Access Module (SAM). The SAM can act as a cryptographic coprocessor between the microcontroller and the reader IC. Direct SAM-to-reader communication reduces protocol overhead and can improve transaction time.

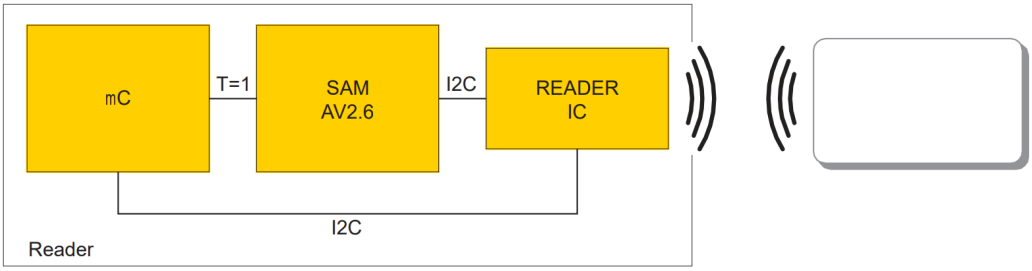


Figure 23. MIFARE SAM integration

8.4.5.2 SAM connection

A purpose-matched security module can be connected to the dedicated NF663E interface using I²C or I²CL. The host selects the SAM interface mode by command. I²CL is intended for a short connection between two ICs and supports a single device on the bus.

8.4.6 Boundary scan interface

The NF663E provides an IEEE 1149.1-compliant boundary-scan port for interconnection testing without physical probe access. Boundary cells associated with the I/O pads can override normal pin behavior during test.

Table 25. Boundary-scan commands

Value (decimal)	Command	Parameter in	Parameter out
0	bypass	-	-
1	preload	data (24)	-
1	sample	-	data (24)
2	ID code (default)	-	data (32)
3	USER code	-	data (32)
4	Clamp	-	-
5	HIGH Z	-	-
7	extest	data (24)	data (24)
8	interface on/off	interface (1)	-
9	register access read	address (7)	data (8)
10	register access write	address (7) - data (8)	-

IEEE 1149.1 defines the Test Access Port (TAP), TAP controller, instruction register, and data register.

8.4.6.1 Interface signals

The test port consists of TCK, TMS, and TDI inputs plus the TDO output. TCK and TMS are distributed to the boundary-scan controller, while TDI-to-TDO forms the serial scan path. Multiple boundary-scan devices can be controlled using the same four signals.

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8.4.6.2 Test Clock (TCK)

TCK clocks the boundary-scan logic independently of other device clocks. TCK may be stopped at either logic state without losing controller state or register contents. An internal pull-up prevents unintended clocking while the pin is undriven.

8.4.6.3 Test Mode Select (TMS)

TMS selects the next TAP-controller state and is sampled on the rising edge of TCK. TMS should therefore change on the falling edge. Holding TMS HIGH for five TCK cycles forces Test-Logic-Reset and loads the default IDCODE instruction. TMS has an internal pull-up.

8.4.6.4 Test Data Input (TDI)

TDI provides serial data to the instruction-register and data-register scan chains. TDI is sampled on the rising edge of TCK and should change on the falling edge. TDI has an internal pull-up.

8.4.6.5 Test Data Output (TDO)

TDO outputs serial data from the selected instruction or data register. It changes on the falling edge of TCK and is placed in a high-impedance state when no shift operation is active.

8.4.6.6 Data register

IEEE 1149.1 defines a bypass register and a boundary-scan register. The bypass register provides a short serial path through a device that is not under test. The boundary-scan register is the chain formed by the active boundary cells.

8.4.6.7 Boundary scan cell

A boundary-scan cell can control, drive, or observe a hardware pin independently of its normal function.

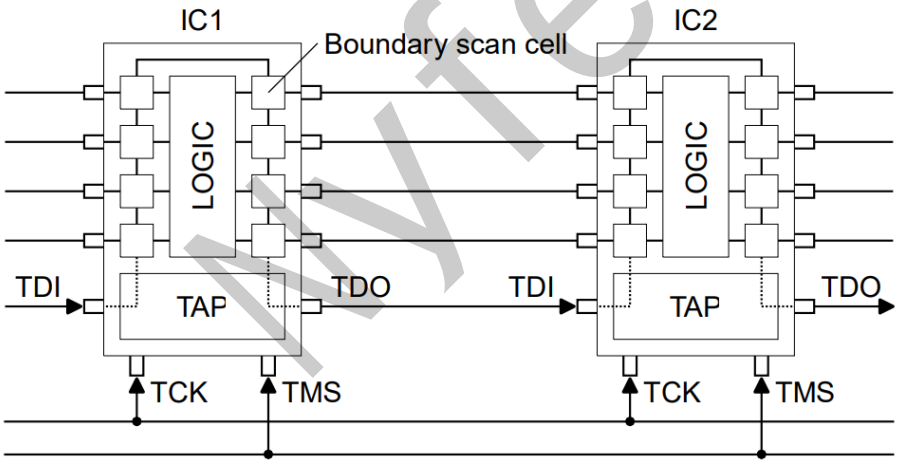


Figure 24. Boundary scan chain structure

8.4.6.8 Boundary scan path

Table 26. Boundary-scan path of the NF663E

Number (decimal)	Cell	Port	Function
23	BC_1	-	Control
22	BC_8	CLKOUT	Bidir
21	BC_1	-	Control
20	BC_8	SCL2	Bidir
19	BC_1	-	Control
18	BC_8	SDA2	Bidir
17	BC_1	-	Control

Number (decimal)	Cell	Port	Function
16	BC_8	IFSEL0	Bidir
15	BC_1	-	Control
14	BC_8	IFSEL1	Bidir
13	BC_1	-	Control
12	BC_8	IF0	Bidir
11	BC_1	-	Control
10	BC_8	IF1	Bidir
9	BC_1	-	Control
8	BC_8	IF2	Bidir
7	BC_1	IF2	Output2
6	BC_4	IF3	Bidir
5	BC_1	-	Control
4	BC_8	IRQ	Bidir
3	BC_1	-	Control
2	BC_8	SIGIN	Bidir
1	BC_1	-	Control
0	BC_8	SIGOUT	Bidir

Refer to the NF663E BSDL file.

8.4.6.9 Boundary Scan Description Language (BSDL)

The BSDL description identifies the test-bus signals, compliance pins, instruction register, data registers, and the structure and function of the boundary cells. NF663E uses BC_8 cells for most I/O lines, BC_4 for the I^2C pin, and BC_1 for pad-enable control.

The manufacturer's identification is 02Bh. The ID code contains:

- Version: 0001b
- Part number: 3C82h
- Manufacturer: 02Bh
- Mandatory least-significant bit: 1b

The user-code data contains the product ID and version stored in the first four EEPROM bytes.

8.4.6.10 Non-IEEE 1149.1 commands

Interface on/off: deactivates the host/SAM interface and enables boundary-scan read and write commands. The new state is applied at Update-DR.

Register access read: Capture-DR loads the current address into the data register. A new address is shifted in and applied at Update-DR.

8.5 Buffer

8.5.1 Overview

A 512-byte FIFO data buffer is integrated into the NF663E. It stores both incoming and outgoing data flowing between the host and the device's internal processing logic. This enables data blocks up to 512 bytes to be handled without imposing tight timing requirements on the host. The FIFO depth may also be configured to 255 bytes. In the reduced-size configuration, parameters such as FIFO length and fill-level threshold use one-byte fields; in the full 512-byte configuration, the corresponding fields use two bytes.

8.5.2 Accessing the FIFO buffer

When the host controller starts an operation, the NF663E may read from or write to the FIFO as required while the operation is in progress. A single physical FIFO serves as both input and output buffer. The host must therefore avoid accesses that could corrupt the FIFO contents.

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8.5.3 Controlling the FIFO buffer

In addition to normal read and write operations, the FIFO pointers can be cleared by setting the flush control bit in the FIFO configuration register. The fill-level indicator is then reset to zero, previously stored data is no longer accessible, and the buffer is ready for a new 512-byte block, or 255 bytes when reduced-size mode is selected.

8.5.4 Status information about the FIFO buffer

Current fill count

Number of bytes currently stored in the FIFO. It increments on writes and decrements on reads. The value is reported by the FIFOLength register, or through FIFOControl when 512-byte mode is used.

Fullness pre-warning (HiAlert)

Indicates that the FIFO is approaching full, according to the WaterLevel threshold.

Emptiness pre-warning (LoAlert)

Indicates that the FIFO is approaching empty, using the same WaterLevel threshold.

Overflow flag (FIFOOvl)

Indicates that data was written while the FIFO was already full. The condition is reported through ErrIrq in the IRQ0 register.

A single WaterLevel value defines both warning boundaries: HiAlert is measured from the top of the FIFO and LoAlert from the bottom. If LoAlertIRQEn or HiAlertIRQEn in IRQOEn is enabled, the interrupt output is asserted when the corresponding status bit changes to logic 1.

$$\text{HiAlert} = (\text{FIFOSize} - \text{FIFOLength}) \leqslant \text{WaterLevel} \quad (2)$$

$$\text{LoAlert} = \text{FIFOLength} \leqslant \text{WaterLevel} \quad (3)$$

8.6 Analog interface and contactless UART

8.6.1 General

The integrated contactless serial interface assists the host with frame formatting and integrity verification for supported protocols at data rates up to 848 kbit/s. External modulation and demodulation circuitry can be connected through SIGIN and SIGOUT. The protocol engine assembles bit-level and byte-level frames and performs parity and CRC-based error checking. Achievable field strength and operating range depend on antenna geometry, resonant tuning, output-driver supply voltage, and the card type.

8.6.2 TX transmitter

TX1 and TX2 provide the 13.56 MHz carrier, modulated by an envelope signal for energy and data transmission. With suitable passive matching and filtering components, the pins can directly drive the antenna. The output mode is configured by DrvMode, and the modulation index is set by TxAmp.

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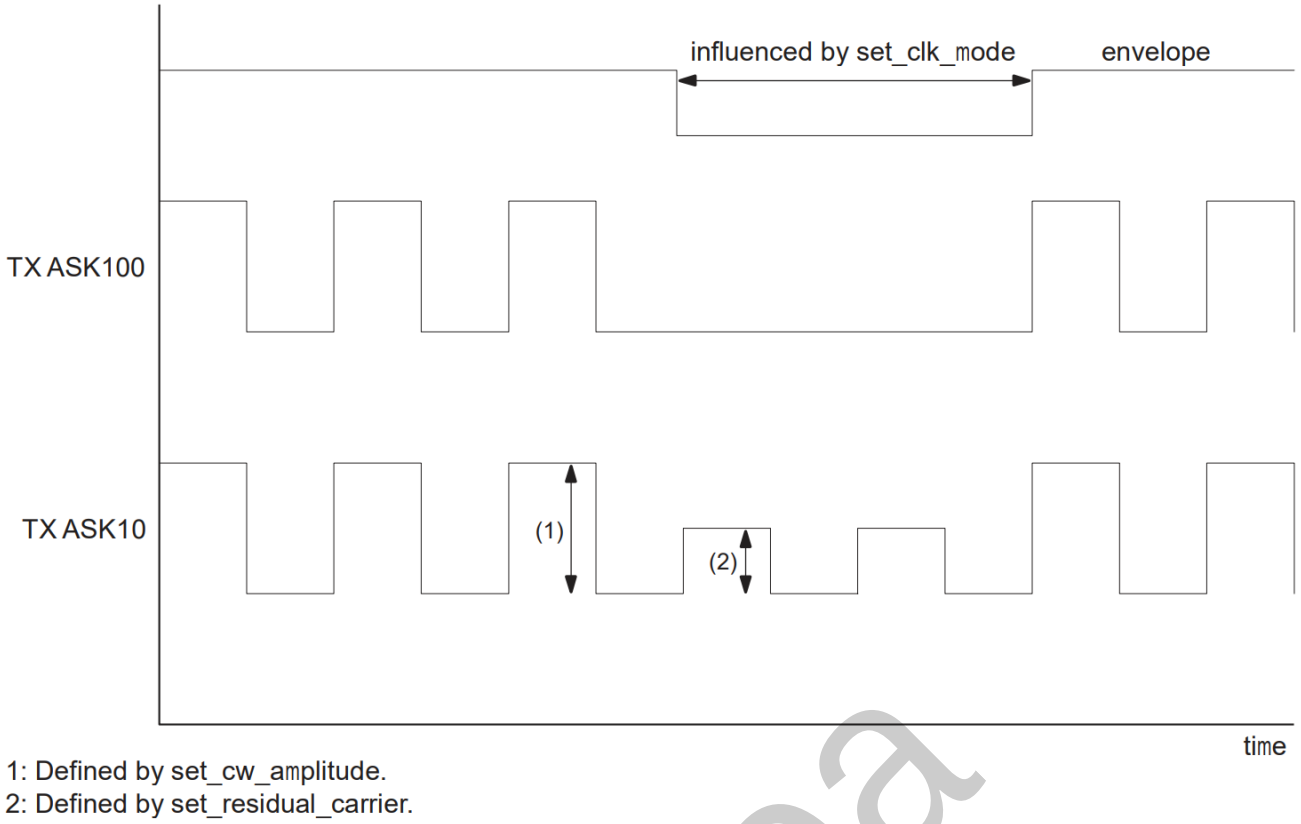


Figure 25. General dependences of modulation

Note: Changing the continuous-carrier amplitude also changes the residual-carrier amplitude, while the modulation index remains unchanged.

Table 27. Settings for TX1 and TX2

TxClkMode (binary)	TX1 and TX2 output	Remarks
000	High impedance	-
001	0	Output pulled to 0 in all cases
010	1	Output pulled to 1 in all cases
110	RF high-side push	Open-drain operation; only the high-side MOS is clocked. Clock polarity is defined by invtx; the low-side MOS is off.
101	RF low-side pull	Open-drain operation; only the low-side MOS is clocked. Clock polarity is defined by invtx; the high-side MOS is off.
111	13.56 MHz clock derived from the 27.12 MHz crystal divided by 2	Push/pull operation; clock polarity is defined by invtx. Used for 10 % modulation.

TXamp and the set_residual_carrier field define the modulation index.

Table 28. Setting residual carrier and modulation index by TXamp.set_residual_carrier

Set residual carrier (decimal)	Residual carrier [%]	Modulation index [%]
0	99	0.5
1	98	1.0
2	96	2.0
3	94	3.1
4	91	4.7

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Set residual carrier (decimal)	Residual carrier [%]	Modulation index [%]
5	89	5.8
6	87	7.0
7	86	7.5
8	85	8.1
9	84	8.7
10	83	9.3
11	82	9.9
12	81	10.5
13	80	11.1
14	79	11.7
15	78	12.4
16	77	13.0
17	76	13.6
18	75	14.3
19	74	14.9
20	72	16.3
21	70	17.6
22	68	19.0
23	65	21.2
24	60	25.0
25	55	29.0
26	50	33.3
27	45	37.9
28	40	42.9
29	35	48.1
30	30	53.8
31	25	60.0

Note: At $V_{DD(TVDD)}$ < 5 V and residual-carrier settings below 50 %, modulation-index accuracy may depend strongly on the antenna tuning impedance.

8.6.2.1 Overshoot protection

The NF663E includes an amplitude-transition control mechanism for 100 % ASK modulation. Two programmable intervals, phase1 and phase2, limit excessive amplitude excursions. During phase1 the output is driven at the full-power amplitude; during phase2 the output is driven at the residual-carrier level.

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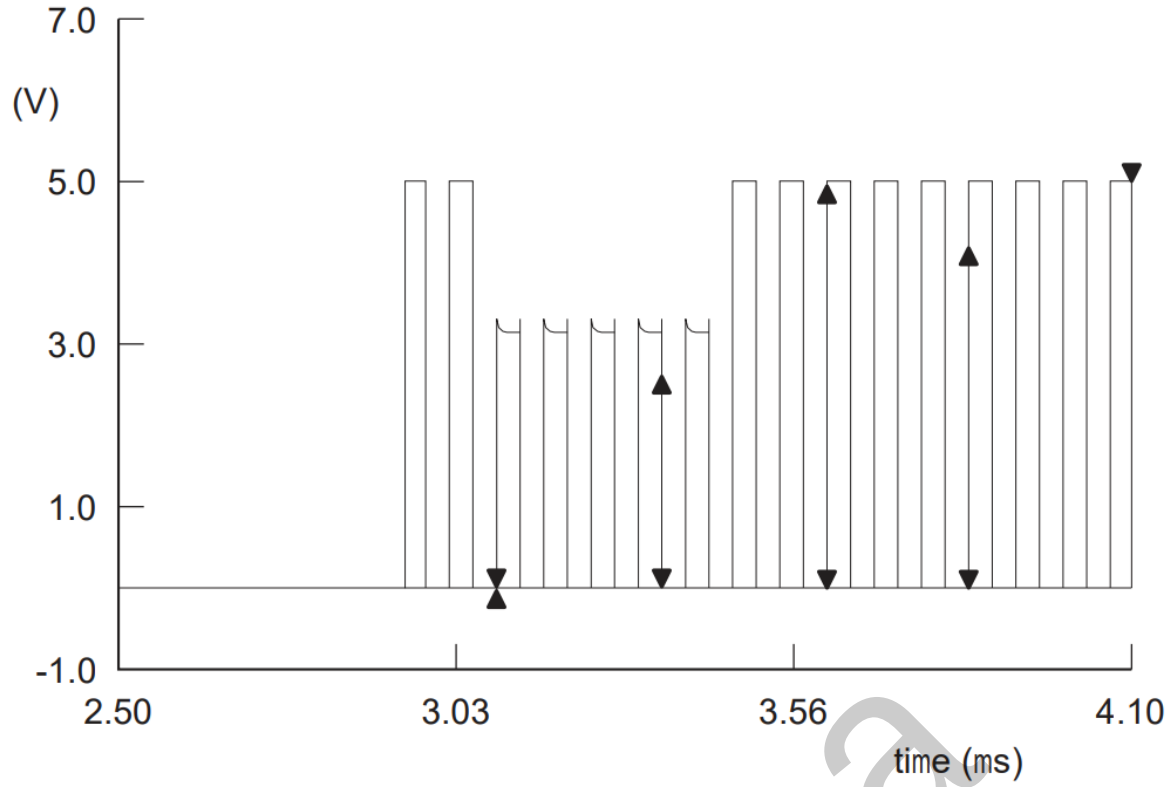


Figure 26. Overshoot protection example 1

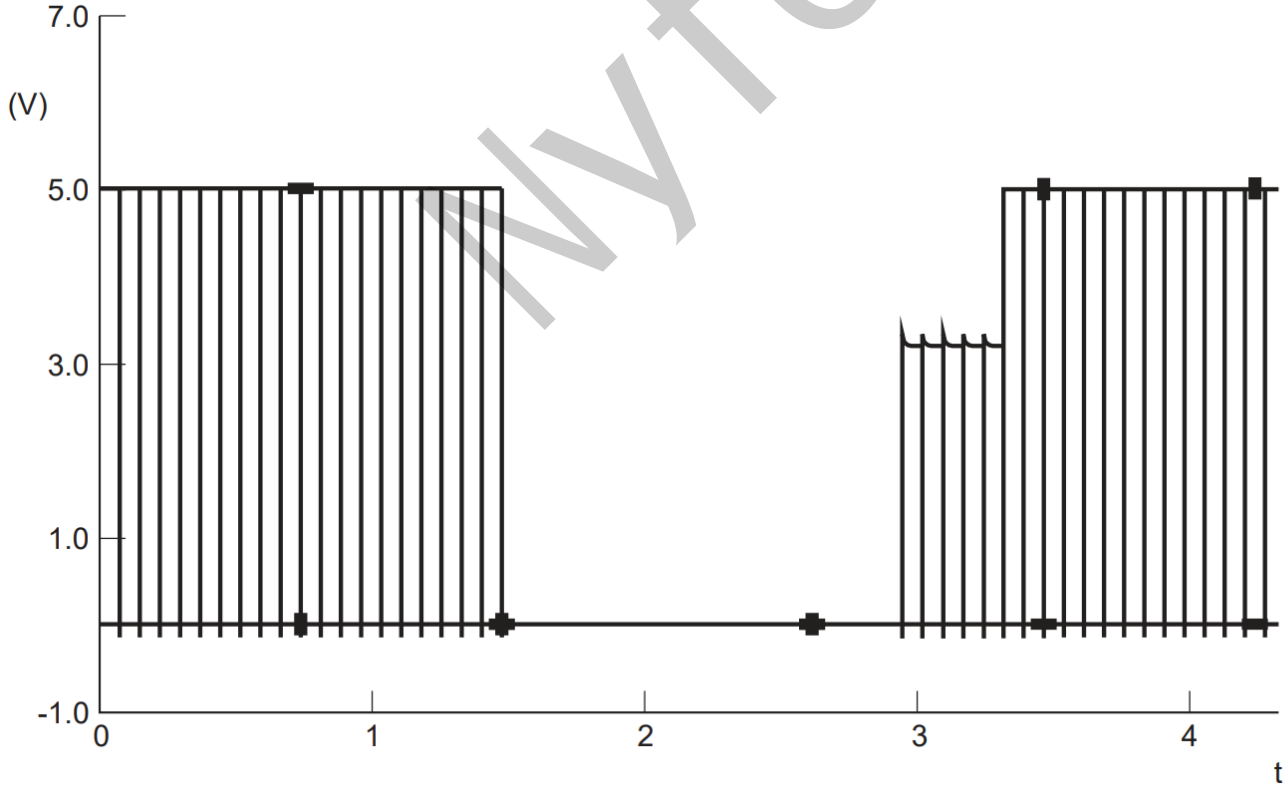


Figure 27. Overshoot protection example 2

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8.6.2.2 Bit generator

The default byte-oriented coding path uses the bit generator when TxFrameCon.DCodeType is 0000b. The bit generator can perform the following operations on each data byte:

1. Add a programmable start bit.
2. Add a programmable stop bit and up to six full EGT bits.
3. Add a programmable parity bit.
4. Skip TxFirstBits at the beginning of the first byte.
5. Skip TxLastBits at the end of the last byte.
6. Encrypt data bits using MIFARE encryption.

TxFirstBits and TxLastBits may be used together, but their ranges must not overlap for a single data byte.

$$((8 - \text{TxFirstBits}) + (8 - \text{TxLastBits})) < 8$$

Data is treated LSB first by default. For MSB-first coding, set TxMSBFirst in register CLCON1.

8.6.3 Receiver circuitry

8.6.3.1 General

The NF663E uses a quadrature receiver architecture with differential inputs RXP and RXN. The receive path can be adjusted for the supported 13.56 MHz protocols.

8.6.3.2 Block diagram

The receiver first performs quadrature demodulation of the 13.56 MHz carrier. The resulting I- and Q-channel baseband signals are amplified, filtered, digitized, and passed to the correlation processing block.

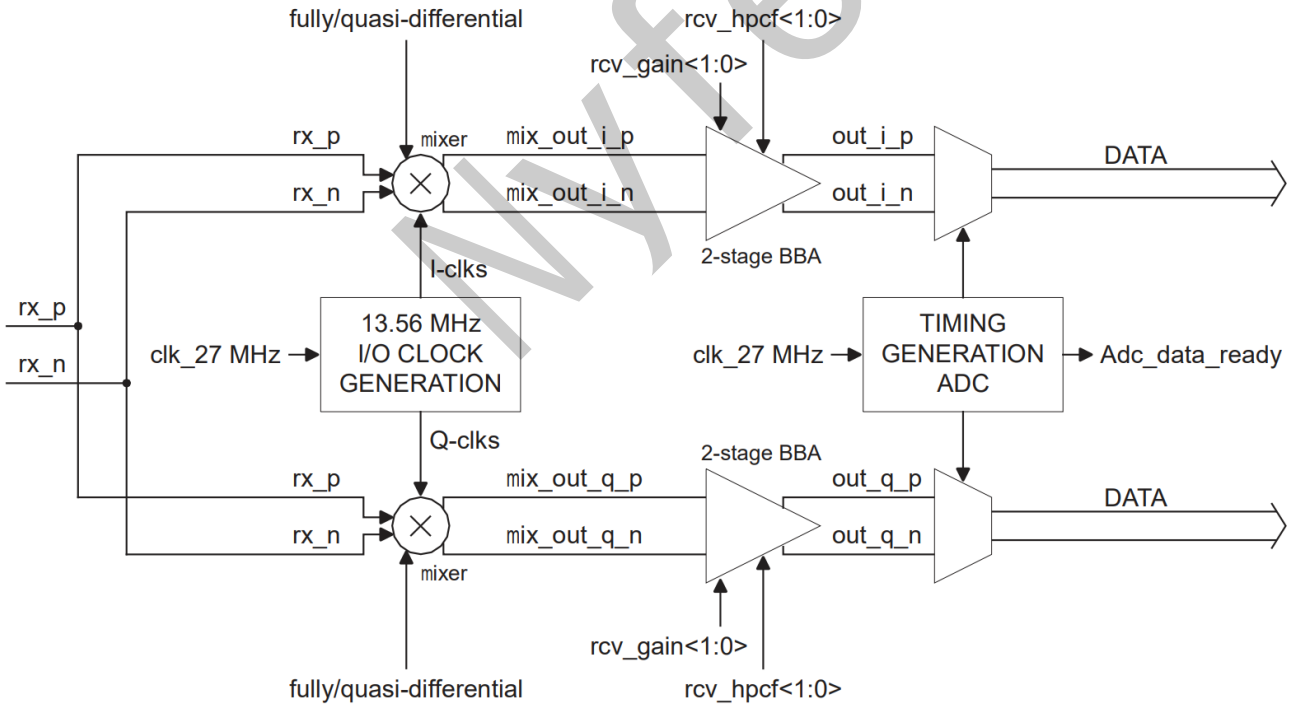


Figure 28. Block diagram of receiver circuitry

Table 29. Configuration for single or differential receiver

Mode	rcv_rx_single	Pins RXP and RXN
Fully differential	0	RXP and RXN provide a differential signal from separate antenna coupling branches.

Mode	rcv_rx_single	Pins RXP and RXN
Quasi-differential / single-ended	1	RXP and RXN are connected together and receive a single-ended signal through one coupling branch.

Fully differential operation provides the best sensitivity and maximum operating range. Quasi-differential operation can reduce the number of external matching components, with some loss of range. During LPCD, the DC values at the I- and Q-channel mixer outputs are evaluated. Direct mixer-to-ADC connection is selected with Rx_ADCmode in register Rcv (38h).

8.6.4 Active antenna concept

The active-antenna interface routes digital transmit and receive signals through SIGOUT and SIGIN. It can be used for monitoring during development and production test, or to connect an external active antenna assembly. A passive antenna connected to TX1/TX2/RX may also be used alongside an active antenna, with both RF paths controlled sequentially by the host.

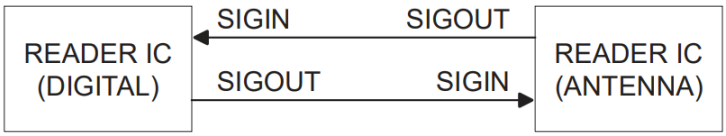


Figure 29. Block diagram of the active antenna concept

Table 30. Register configuration of NF663E active antenna concept (digital)

Register	Value (binary)	Description
SigOut.SigOutSel	0100	TxEnvelope
Rcv.SigInSel	10 11	Receive over SIGIN (ISO/IEC 14443A) Receive over SIGIN (Generic Code)
DrvCon.TxSel	00	Low (idle)

Table 31. Register configuration of NF663E active antenna concept (antenna)

Register	Value (binary)	Description
SigOut.SigOutSel	0110 0111	Generic Code (Manchester) Manchester with subcarrier (ISO/IEC 14443A)
Rcv.SigInSel	01	Internal
DrvCon.TxSel	10	External (SIGIN)
RxCtrl.RxMultiple	1	RxMultiple enabled

For an external active antenna, set SigOutSel to route the required encoded data stream to SIGOUT and select SIGIN as the receive source. The interface signals are then available at the SIGIN and SIGOUT pins.

8.6.5 Symbol generator

The symbol generator creates protocol-specific patterns, including ISO/IEC 14443 start- and end-of-frame symbols and ICODE EPC calibration patterns. Symbol0 and Symbol1 support sequences up to 16 bits and run-length extension up to 256 bits. Symbol2 and Symbol3 support up to 8 bits without run-length extension.

The bit pattern is written to the corresponding symbol register, and the least significant programmed bit is transmitted last. The configured length determines which bits are used. Symbols 0, 1, and 2 are available before the data field; Symbols 1, 2, and 3 are available after the data field. Configuration includes bit rate, subcarrier frequency, pulse type, pulse duration, and envelope parameters.

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8.7 Memory

8.7.1 Memory overview

The NF663E contains EEPROM, FIFO, and register memory. At power-up, selected EEPROM sections are copied into the register set to establish reset and protocol defaults. LoadProtocol transfers a selected protocol template from the protected protocol-storage area into active registers. Section 2 is available for application data or stored register configurations that can later be loaded with LoadReg. The FIFO acts as the input/output buffer and improves performance when the host interface has limited speed.

8.7.2 EEPROM memory organization

The embedded EEPROM has a capacity of 8 kB and is organized in 64-byte pages. Five sections are defined for production data, reset data, user storage, MIFARE keys, and protocol register sets.

Table 32. EEPROM memory organization

Section	Page	Byte addresses	Access rights	Memory content
0	0	00 to 31	r	Product information and configuration
0	0	32 to 63	r/w	Product configuration
1	1 to 2	64 to 191	r/w	Register reset
2	3 to 95	192 to 6143	r/w	Free
3	96 to 111	6144 to 7167	w	MIFARE key area
4	112 to 128	7168 to 8191	r	Register Set Protocol (RSP)

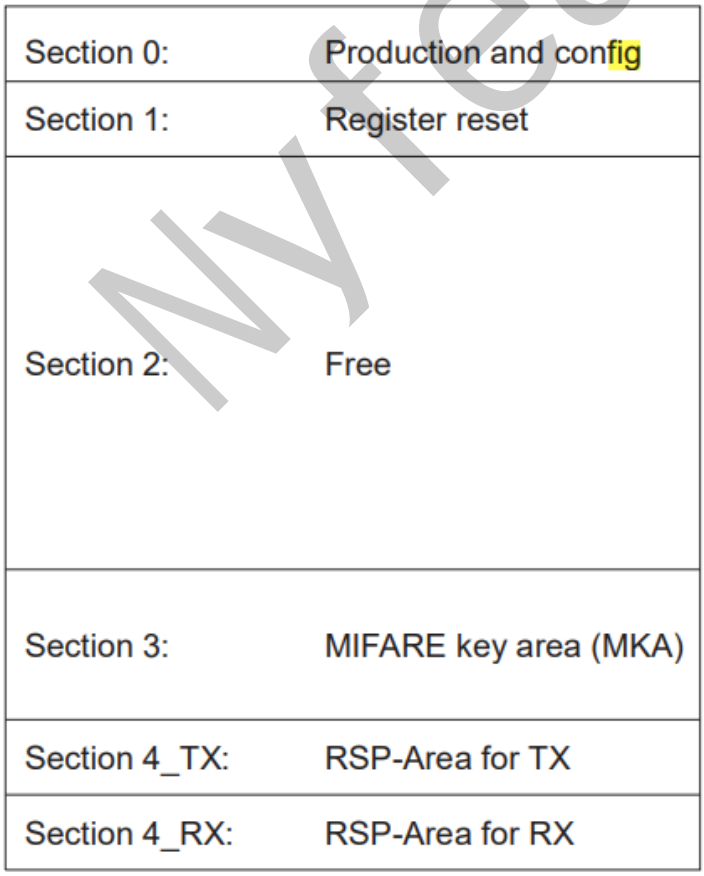


Figure 31. Sector arrangement of the EEPROM

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8.7.2.1 Product information and configuration - Page 0

The first EEPROM page contains production data and configuration information.

Table 33. Production area (Page 0)

Address (Hex.)	0	1	2	3	4	5	6	7
00	ProductID			Version	Unique identifier			
08	Unique identifier							Manufacturer data
10	Manufacturer data							
18	Manufacturer data							

ProductID: For NF663E identification, software evaluates address 01h. Addresses 00h and 02h are ignored.

Table 34. Product ID overview of NF663E family

Device	Product ID at address 01h
NF663E	01h
TSC9881	C0h
TSC9880	80h
TSC9882	20h

Version: Identifies the EEPROM initialization-data version programmed during production. The hardware revision is available in register 7Fh and is independent of EEPROM configuration.

Unique identifier: Device-specific unique identifier.

Manufacturer data: Production-programmed data not intended for application use; its contents must be treated as undefined.

Table 35. Configuration area (Page 0)

Address (Hex.)	0	1	2	3	4	5	6	7
20	I^2C_Address	Interface	I^2C SAM_Address	DefaultProtRx	DefaultProtTx	-	TxCRCPreset	
28	RxCRCPreset		-	-	-	-	-	-
30	-							
38	-							

I^2C address: The address can be selected from external pin strapping or from EEPROM. The fixed address prefix is 10101b and the two least significant bits are configurable.

Interface: The interface byte selects I^2C mode, boundary-scan state, and host-interface source.

Table 36. Interface byte

Bit	7	6	5	4	3	2	1	0
Symbol	I^2C_HSP	-	-	I^2C_Address	Boundary Scan	Host		
Access rights	r/w	RFU	RFU	r/w	r/w	r/w		

Table 37. Interface bits

Bit	Symbol	Description
7	I^2C_HSP	0: high-speed mode 1: high-speed-plus mode (default)
6, 5	RFU	Reserved
4	I^2C_Address	0: use address pins (default) 1: use EEPROM address
3	Boundary Scan	0: boundary-scan interface ON (default) 1: boundary-scan interface OFF

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Bit	Symbol	Description
2 to 0	Host	000b: RS232 001b: I²C 010b: SPI 011b: I²CL 1xxb: pin selection

I²C_SAM_Address: The SAM address is always defined by EEPROM content.

The Register Set Protocol area contains settings for 16 TX registers and 16 RX entries.

Table 38. TX and RX arrangements in the register-set protocol area

Section 4 TX	Tx0		Tx1		Tx2		Tx3	
Section 4 TX	Tx4		Tx5		Tx6		Tx7	
Section 4 RX	RX0	RX1	RX2	RX3	RX4	RX5	RX6	RX7
Section 4 RX	RX8	RX9	RX10	RX11	RX12	RX13	RX14	RX15

TxCRCPreset: Transmit data is automatically extended by the configured CRC preset.

8.7.3 EEPROM initialization content – LoadProtocol

During production, the EEPROM is initialized with values used to reset selected NF663E registers. Only read/write or dynamic fields are initialized from EEPROM. The addresses used for register initialization depend on the configured protocol and can be modified by the user.

Table 39. Register reset values (Hex.) – Page 0

Address	0 (8)	1 (9)	2 (A)	3 (B)	4 (C)	5 (D)	6 (E)	7 (F)
Function	Product ID			Version	Unique serial number			
00	XX	See Table 34	XX	XX	XX	XX	XX	XX
Function	Unique serial number							Factory trim value
08	XX	XX	XX	XX	XX	XX	XX	XX
Function	TrimLFO	Factory trim values						
10	XX	XX	XX	XX	XX	XX	XX	XX
Function	Factory trim values							
18	XX	XX	XX	XX	XX	XX	XX	XX
38	XX	XX	XX	XX	XX	XX	XX	XX

The reset values establish the initial operating state after power-up. They may be changed to modify the device defaults. Protocol-specific configurations are loaded through the LoadProtocol command.

Table 40. Register reset values (Hex.) – Pages 1 and 2

Address	0 (8)	1 (9)	2 (A)	3 (B)	4 (C)	5 (D)	6 (E)	7 (F)
	Command	HostCtrl	FIFOControl	WaterLevel	FIFOLength	FIFOData	IRQ0	IRQ1
40	40	00	80	05	00	00	00	00
	IRQ0En	IRQ1En	Error	Status	RxBitCtrl	RxColl	TControl	T0Control
48	10	00	00	00	00	00	00	00
	T0ReloadHi	T0ReloadLo	T0CounterValHi	T0CounterValLo	T1Control	T1ReloadHi	T1ReloadLo	T1CounterValHi
50	00	80	00	00	00	00	80	00
	T1CounterValLo	T2Control	T2ReloadHi	T2ReloadLo	T2CounterValHi	T2CounterValLo	T3Control	T3ReloadHi
58	00	00	00	80	00	00	00	00
	T3ReloadLo	T3CounterValHi	T3CounterValLo	T4Control	T4ReloadHi	T4ReloadLo	T4CounterValHi	T4CounterValLo
60	80	00	00	00	00	80	00	00
	DrvMode	TxAmp	DrvCon	TxI	TxCRCPreset	RxCRCPreset	TxDataNum	TxModWidth
68	86	15	11	06	18	18	08	27
	TxSym10BurstLen	TxWaitCtrl	TxWaitLo	FrameCon	RxSofD	RxCtrl	RxWait	RxThreshold
70	00	C0	12	CF	00	04	90	3F
	Rcv	RxAna	RFU	SerialSpeed	LFO_trimm	PLL_Ctrl	PLL_Div	LPCD_QMin
78	12	0A	00	7A	80	04	20	48

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Address	0 (8)	1 (9)	2 (A)	3 (B)	4 (C)	5 (D)	6 (E)	7 (F)
	LPCD_QMax	LPCD_IMin	LPCD_result_I	LPCD_result_Q	PadEn	PadOut	PadIn	SigOut
80	12	88	00	00	00	00	00	00
	TxBitMod	RFU	TxDataCon	TxDataMod	TxSymFreq	TxSym0H	TxSym0L	TxSym1H
88	20	XX	04	50	40	00	00	00

8.8 Clock generation

8.8.1 Crystal oscillator

The device clock is the master timing reference for the RF carrier, quadrature receiver mixer, and synchronous encode/decode logic. Frequency stability and low phase noise are therefore important. Best performance is obtained by operating the on-chip oscillator buffer with the recommended external components.

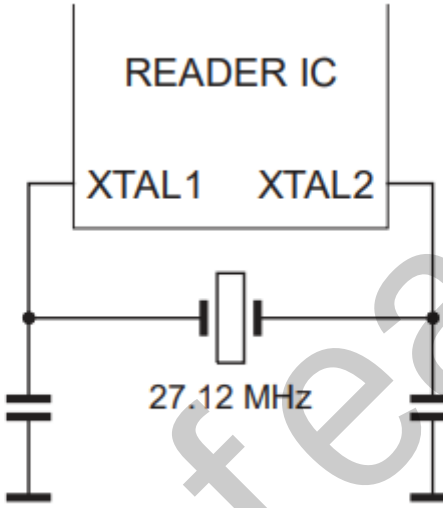


Figure 32. Quartz connection

Table 41. Crystal requirements recommendations

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	Crystal frequency	-	-	27.12	-	MHz
$\Delta f_{xtal}/f_{xtal}$	Relative crystal frequency variation	-	-250	-	+250	ppm
ESR	Equivalent series resistance	-	-	50	100	Ω
C_L	Load capacitance	-	-	10	-	pF
P_{xtal}	Crystal power dissipation	-	-	50	100	μW

8.8.2 Integer-N PLL clock line

The NF663E can provide a programmable 1 MHz to 24 MHz clock at CLKOUT for an external host controller. The synthesizer is referenced to the 27.12 MHz crystal. Feedback-divider values 23, 27, and 28 generate approximately 312 MHz, 366 MHz, and 380 MHz before the output divider. ClkOutEn enables the output.

$$f_{out} = 13.56\ MHz \times PLLDiv\_FB / PLLDiv\_Out$$

Table 42. Divider values for selected frequencies using the integer-N PLL

Frequency [MHz]	4	6	8	10	12	20	24	1.8432	3.6864
PLLDiv_FB	23	27	23	28	23	28	23	28	28
PLLDiv_Out	78	61	39	38	26	19	16	206	103

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Accuracy [%]	0.04	0.03	0.04	0.08	0.04	0.08	0.04	0.01	0.01

8.8.3 Low-Frequency Oscillator (LFO)

The LFO drives the wake-up counter used for periodic polling and LPCD. It is production-trimmed to approximately 16 kHz. For normal wake-up applications, the production trim value can be used directly. Optional digital trimming compares the LFO against the 13.56 MHz crystal reference when higher accuracy is required over temperature.

8.9 Power management

8.9.1 Supply concept

The NF663E uses independent V_{DD}, PVDD, and TVDD supplies. For a 3.3 V microcontroller, V_{DD} and PVDD are normally 3.3 V, while TVDD may range from 3.3 V to 5.0 V. Increasing TVDD increases available field strength. Place supply bypass capacitors close to the package: at least 100 nF on V_{DD} and PVDD, and 100 nF in parallel with 1.0 µF on TVDD. AVDD and DVDD are regulated outputs, not supply inputs, and each requires a 470 nF buffer capacitor.

8.9.2 Power reduction mode

8.9.2.1 Power-down

A HIGH level on PDOWN disables the internal 1.8 V regulators and oscillator. Digital input buffers are isolated and clamped, except for PDOWN, and output pins enter high impedance. Driving PDOWN LOW starts the internal start-up sequence.

8.9.2.2 Standby mode

Standby is entered by setting the power-down control bit in the Command register. Most internal blocks are disabled, but the LFO remains available. Digital inputs remain active, outputs keep their previous states, and register and FIFO contents are preserved. Clearing the bit starts the power-on sequence, which typically completes within 15 µs. A 55h wake-up pattern may also be sent through the serial interface.

8.9.2.3 Modem-off mode

Setting ModemOff in the Control register disables the RF transmitter and receiver. Clear ModemOff to return the modem to normal operation.

8.9.3 Low-Power Card Detection (LPCD)

LPCD alternates between a low-power sleep interval and a short sampling window. During the sampling window, I- and Q-channel values are stored and compared with programmable upper and lower thresholds. A value outside the configured range generates an LPCD interrupt.

After an LPCD command, the device can return to standby automatically. Enabling auto-wakeup and auto-restart on the wake-up timer is recommended. Card detection stops the timer and allows normal communication to begin.

8.9.4 Reset and start-up time

A constant HIGH level on PDOWN for at least 10 µs initiates the internal reset sequence.

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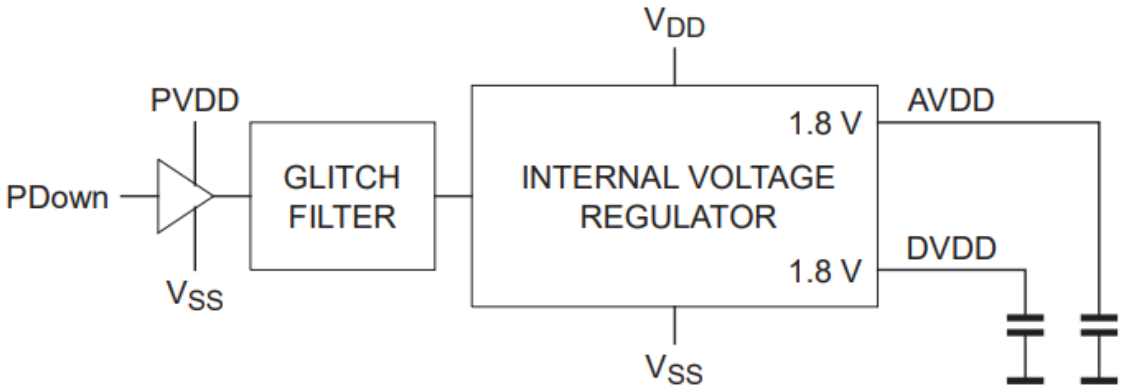


Figure 33. Internal PDOWN to voltage regulator logic

After reset is complete and the oscillator is stable, the device is ready for operation.

8.10 Command set

8.10.1 General

The command state machine is controlled by writing a command code to the Command register. Arguments and data are exchanged through the FIFO. A command starts only after all required arguments are present. The FIFO is not automatically cleared at command start, so arguments and data should normally be written before the command code. Any running command can be terminated by writing another command, such as Idle.

8.10.2 Command set overview

Table 43. Command set

Command	No.	Parameter (bytes)	Short description
Idle	00h	-	No action; cancels current command execution.
LPCD	01h	-	Performs low-power card detection.
LoadKey	02h	Six key bytes	Loads a 6-byte MIFARE key from FIFO into the key buffer.
MFAuthent	03h	60h or 61h; block address; four card serial-number bytes	Performs MIFARE Classic authentication in reader/writer mode.
AckReq	04h	-	Performs Query, ACK, and Req_Rn for ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF.
Receive	05h	-	Activates the receive circuit.
Transmit	06h	-	Transmits FIFO data.
Transceive	07h	-	Transmits FIFO data and automatically enables the receiver after transmission.
WriteE2	08h	Address low, address high, data	Writes one byte from FIFO to EEPROM within the MIFARE key area.
WriteE2Page	09h	Page address; data0 ... data63	Writes up to one 64-byte EEPROM page within the MIFARE key area.
ReadE2	0Ah	Address low, address high, length	Reads EEPROM data into FIFO within the MIFARE key area.
LoadReg	0Ch	EEPROM address low/high; register address; count	Copies EEPROM section-2 data into NF663E registers.
LoadProtocol	0Dh	Protocol number RX; protocol number TX	Loads protocol-specific register settings from EEPROM.
LoadKeyE2	0Eh	Key number	Copies an EEPROM key into the key buffer.
StoreKeyE2	0Fh	Key number; six key bytes	Stores a 6-byte MIFARE key in EEPROM.
ReadRNR	1Ch	-	Copies random-number-generator bytes into FIFO until full.
SoftReset	1Fh	-	Resets the NF663E.

8.10.3 Command functionality

8.10.3.1 Idle command

Command: 00h.

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Places the NF663E in idle mode and terminates the currently active command.

8.10.3.2 LPCD command

Command: 01h.

Performs low-power card detection and optional LFO auto-trimming. Sampled I- and Q-channel values are stored in the register map and compared with programmed limits. Exceeding a limit raises LPCD_Irq. Standby is entered after the command when configured.

8.10.3.3 Load key command

Command: 02h; **parameters**: six key bytes.

Loads a 6-byte MIFARE key from FIFO into the cryptographic key buffer. The command is aborted if fewer than six bytes are available.

8.10.3.4 MFAuthent command

Command: 03h; **parameters**: authentication code 60h or 61h, block address, and four card serial-number bytes.

Performs MIFARE Classic authentication in reader/writer mode. FIFO access is blocked while the command is active; an attempted access sets WrErr. Successful authentication sets Crypto1On. If the card does not respond, the command does not terminate automatically, so a timer-based timeout should be enabled.

The following six bytes must be written to FIFO before the command starts:

- Authentication command code (60h or 61h)
- Block address
- Card serial-number bytes 0 to 3

Remark: Receive and transmit status flags are masked during authentication. If authentication fails, ProtocolErr is set and Crypto1On is cleared.

8.10.3.5 AckReq command

Command: 04h.

Performs a Query, ACK, and Req_Rn sequence. The complete command must be written to FIFO. Responses and the error flag are returned through FIFO. The command terminates automatically when finished.

8.10.3.6 Receive command

Command: 05h.

Enables the receive channel and listens for incoming data according to the preconfigured protocol and antenna settings. All required registers must be configured before the command is started.

The Receive operation concludes automatically when the incoming data stream ends. Depending on the selected framing format and data rate, the end is detected by an end-of-frame marker or by the configured length field.

Remark: If RxMultiple in the RxMod register is set to logic 1, the Receive command does not terminate automatically. It must be terminated by starting another command.

8.10.3.7 Transmit command

> Command (06h);

Data transfer from the FIFO starts immediately after command execution. All transmitter-related registers must be configured before the command is issued. The operation ends automatically when the FIFO is empty, or can be aborted by writing another command to the Command register.

8.10.3.8 Transceive command

> Command (07h);

This command combines FIFO-to-air transmission and air-to-FIFO reception. The transmit phase is executed first; when transmission is complete, the device automatically enters receive mode and stores the incoming data in the FIFO.

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Remark: If RxMultiple is set to logic 1, the command remains in the receive state until another command is started.

8.10.3.9 WriteE2 command

> Command (08h); Parameter 1: address low byte; Parameter 2: address high byte; Parameter 3: data byte.

Writes one byte to the EEPROM. If the FIFO does not yet contain the required data, command execution waits until the data is available. The command is aborted if the parameter set is incomplete or if the address is outside the valid range.

8.10.3.10 WriteE2PAGE command

> Command (09h); Parameter 1: page address; Parameters 2 to 65: data0 to data63.

Writes up to 64 bytes, corresponding to one EEPROM page. The command is aborted if the FIFO contains insufficient parameters or if the page address is outside the valid range.

8.10.3.11 ReadE2 command

> Command (0Ah); Parameter 1: address low byte; Parameter 2: address high byte; Parameter 3: length.

Reads up to 256 bytes from EEPROM into the FIFO. If the read crosses address 1FFFh, access wraps to address 0000h. The command is aborted if parameters are missing or the starting address is invalid.

8.10.3.12 LoadReg command

> Command (0Ch); Parameters 1 and 2 define the source EEPROM address, Parameter 3 defines the first destination register address, and Parameter 4 defines the number of bytes to transfer.

The selected EEPROM bytes are copied to consecutive registers. Execution is aborted if the FIFO does not contain all parameters or if the source address is outside the valid memory range.

8.10.3.13 LoadProtocol command

> Command (0Dh); Parameter 1: RX protocol number; Parameter 2: TX protocol number.

Loads the selected Register Set Protocol entries from EEPROM and replaces the active receiver- and transmitter-related register settings. The command is aborted when the FIFO does not contain the required parameters.

Table 44. Predefined protocol overview RX [1]

Protocol number (decimal)	Protocol	Receiver speed [kbit/s]	Receiver coding
00	ISO/IEC 14443A	106	Manchester SubC
01	ISO/IEC 14443A	212	BPSK
02	ISO/IEC 14443A	424	BPSK
03	ISO/IEC 14443A	848	BPSK
04	ISO/IEC 14443B	106	BPSK
05	ISO/IEC 14443B	212	BPSK
06	ISO/IEC 14443B	424	BPSK
07	ISO/IEC 14443B	848	BPSK
08	FeliCa	212	Manchester
09	FeliCa	424	Manchester
10	ISO/IEC 15693	26	SSC
11	ISO/IEC 15693	52	SSC
12	ISO/IEC 15693	26	DSC
13	EPC/UID	26	SSC

Protocol number (decimal)	Protocol	Receiver speed [kbit/s]	Receiver coding
14	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	2/424
15	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	4/424
16	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	2/848
17	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	4/848
18	RFU	-	-

[1] For protocol details, refer to Section 8, Functional description.

Table 45. Predefined protocol overview TX [1]

Protocol number (decimal)	Protocol	Transmitter speed [kbit/s]	Transmitter coding
00	ISO/IEC 14443A	106	Miller
01	ISO/IEC 14443A	212	Miller
02	ISO/IEC 14443A	424	Miller
03	ISO/IEC 14443A	848	Miller
04	ISO/IEC 14443B	106	NRZ
05	ISO/IEC 14443B	212	NRZ
06	ISO/IEC 14443B	424	NRZ
07	ISO/IEC 14443B	848	NRZ
08	FeliCa	212	Manchester
09	FeliCa	424	Manchester
10	ISO/IEC 15693	26	1/4
11	ISO/IEC 15693	26	1/4
12	ISO/IEC 15693	1.66	1/256
13	EPC/UID	53	Unitary
14	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	Tari, ASK, PIE
15	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	Tari, ASK, PIE
16	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	Tari, ASK, PIE
17	ISO/IEC 18000-3 Mode 3 / EPC Class-1 HF	-	Tari, ASK, PIE
18	RFU	-	RFU

[1] For protocol details, refer to Section 8, Functional description.

8.10.3.14 LoadKeyE2 command

Command (0Eh); Parameter 1: key number.

Loads a six-byte MIFARE key from the EEPROM key area into the Crypto1 key buffer. The command is aborted if the key number lies outside the MIFARE key area or if the parameter is missing.

8.10.3.15 StoreKeyE2 command

Command (0Fh); Parameter 1: key number; Parameters 2 to 7: six key bytes.

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Stores one or more six-byte MIFARE keys in consecutive EEPROM key slots. Complete keys are processed until the FIFO no longer contains a full six-byte key. An incomplete final key remains in the FIFO. The command is aborted if the key number is outside the MIFARE key area.

8.10.3.16 GetRNR command

> Command (1Ch);

Copies random-number bytes from the internal random-number generator to the FIFO until the FIFO is full.

8.10.3.17 SoftReset command

> Command (1Fh);

Performs a software reset. The default register settings are read from EEPROM and copied into the register set.

9 NF663E registers

9.1 Register bit behavior

Register access behavior depends on the function of each register. Bits with the same behavior are grouped in common registers. The abbreviations used throughout the register description are defined below.

Table 46. Behavior of register bits and their designation

Abbreviation	Behavior	Description
r/w	Read and write	Can be written and read through the host interface. Internal state machines can read these bits but do not automatically change them.
dy	Dynamic	Can be written and read through the host interface and may also be changed automatically by internal state machines.
r	Read only	Contains values determined by internal states.
w	Write only	Reading these bits returns zero.
RFU	Reserved for future use	Must not be changed. When a write is unavoidable, write logic 0.

Table 47. NF663E registers overview

Address	Register name	Function
00h	Command	Starts and stops command execution
01h	HostCtrl	Host control register
02h	FIFOControl	FIFO control register
03h	WaterLevel	FIFO underflow and overflow warning threshold
04h	FIFOLength	Number of bytes in FIFO
05h	FIFOData	FIFO data input/output port
06h	IRQ0	Interrupt request register 0
07h	IRQ1	Interrupt request register 1
08h	IRQ0En	Interrupt enable register 0
09h	IRQ1En	Interrupt enable register 1
0Ah	Error	Error status of the last command
0Bh	Status	Communication status
0Ch	RxBitCtrl	Receiver bit-oriented anticollision control
0Dh	RxColl	Collision position register
0Eh	TControl	Timer 0 to Timer 3 control
0Fh	T0Control	Timer0 control
10h	T0ReloadHi	Timer0 reload value, high byte
11h	T0ReloadLo	Timer0 reload value, low byte
12h	T0CounterValHi	Timer0 counter, high byte
13h	T0CounterValLo	Timer0 counter, low byte
14h	T1Control	Timer1 control

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Address	Register name	Function
15h	T1ReloadHi	Timer1 reload value, high byte
16h	T1ReloadLo	Timer1 reload value, low byte
17h	T1CounterValHi	Timer1 counter, high byte
18h	T1CounterValLo	Timer1 counter, low byte
19h	T2Control	Timer2 control
1Ah	T2ReloadHi	Timer2 reload value, high byte
1Bh	T2ReloadLo	Timer2 reload value, low byte
1Ch	T2CounterValHi	Timer2 counter, high byte
1Dh	T2CounterValLo	Timer2 counter, low byte
1Eh	T3Control	Timer3 control
1Fh	T3ReloadHi	Timer3 reload value, high byte
20h	T3ReloadLo	Timer3 reload value, low byte
21h	T3CounterValHi	Timer3 counter, high byte
22h	T3CounterValLo	Timer3 counter, low byte
23h	T4Control	Timer4 control
24h	T4ReloadHi	Timer4 reload value, high byte
25h	T4ReloadLo	Timer4 reload value, low byte
26h	T4CounterValHi	Timer4 counter, high byte
27h	T4CounterValLo	Timer4 counter, low byte
28h	DrvMode	Driver mode register
29h	TxAmp	Transmitter amplifier register
2Ah	DrvCon	Driver configuration register
2Bh	TxI	Transmitter register
2Ch	TxCrcPreset	Transmitter CRC preset
2Dh	RxCrcPreset	Receiver CRC preset
2Eh	TxDataNum	Transmitter data-number register
2Fh	TxModWidth	Transmitter modulation-width register
30h	TxSym10BurstLen	Symbol 1 + Symbol 0 burst-length register
31h	TxWaitCtrl	Transmitter wait control
32h	TxWaitLo	Transmitter wait low
33h	FrameCon	Transmitter frame control
34h	RxSofD	Receiver start-of-frame detection
35h	RxCtrl	Receiver control
36h	RxWait	Receiver wait
37h	RxThreshold	Receiver threshold
38h	Rcv	Receiver configuration
39h	RxAna	Receiver analog configuration
3Ah	RFU	Reserved
3Bh	SerialSpeed	Serial interface speed
3Ch	LFO_Trimm	Low-frequency oscillator trim
3Dh	PLL_Ctrl	Integer-N PLL control
3Eh	PLL_DivOut	Integer-N PLL output divider
3Fh	LPCD_QMin	LPCD Q-channel minimum threshold
40h	LPCD_QMax	LPCD Q-channel maximum threshold
41h	LPCD_IMin	LPCD I-channel minimum threshold
42h	LPCD_I_Result	LPCD I-channel result
43h	LPCD_Q_Result	LPCD Q-channel result
44h	PadEn	Pin-enable register
45h	PadOut	Pin-output register
46h	PadIn	Pin-input register
47h	SigOut	SIGOUT pin control
48h	TxBitMod	Transmitter bit-mode register
49h	RFU	Reserved
4Ah	TxDataCon	Transmitter data configuration
4Bh	TxDataMod	Transmitter data modulation
4Ch	TxSymFreq	Transmitter symbol frequency
4Dh	TxSym0H	Symbol 0 high byte
4Eh	TxSym0L	Symbol 0 low byte
4Fh	TxSym1H	Symbol 1 high byte

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Address	Register name	Function
50h	TxSym1L	Symbol 1 low byte
51h	TxSym2	Symbol 2 register
52h	TxSym3	Symbol 3 register
53h	TxSym10Len	Symbol 1 + Symbol 0 length
54h	TxSym32Len	Symbol 3 + Symbol 2 length
55h	TxSym10BurstCtrl	Symbol 1 + Symbol 0 burst control
56h	TxSym10Mod	Symbol 1 + Symbol 0 modulation
57h	TxSym32Mod	Symbol 3 + Symbol 2 modulation
58h	RxBitMod	Receiver bit modulation
59h	RxEofSym	Receiver end-of-frame symbol
5Ah	RxSyncValH	Receiver synchronization value, high byte
5Bh	RxSyncValL	Receiver synchronization value, low byte
5Ch	RxSyncMod	Receiver synchronization mode
5Dh	RxMod	Receiver modulation
5Eh	RxCorr	Receiver correlation
5Fh	FabCal	Factory receiver calibration
7Fh	Version	Version and subversion register

9.2 Command configuration

9.2.1 Command

The Command register starts and stops command execution and controls standby and modem-off operation.

Table 48. Command register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	Standby	Modem Off	RFU	Command				
Access rights	dy	r/w	-	dy				

Table 49. Command bits

Bit	Symbol	Description
7	Standby	Set to logic 1 to enter standby mode.
6	ModemOff	Set to logic 1 to power down the receiver and transmitter circuits.
5	RFU	Reserved for future use.
4 to 0	Command	Selects the command executed by the NF663E.

9.3 SAM configuration register

9.3.1 HostCtrl

HostCtrl controls bus ownership and access rights between the host interface and the SAM interface.

Table 50. HostCtrl register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	RegEn	BusHost	BusSAM	RFU	SAMInterface		RFU	RFU
Access rights	dy	r/w	r/w	-	r/w		-	-

Table 51. HostCtrl bits

Bit	Symbol	Description
7	RegEn	When set, the next register write may change the protected bus-control bits. The next write clears RegEn automatically.
6	BusHost	Enables bus control for the host interface. BusHost and BusSAM must not be enabled together. RegEn must be set first.

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Bit	Symbol	Description
5	BusSAM	Enables bus control for the SAM interface. BusSAM and BusHost must not be enabled together. RegEn must be set first.
4	RFU	Reserved for future use.
3 to 2	SAMInterface	0h: interface off 1h: SPI active 2h: I2CL active 3h: I2C active
1 to 0	RFU	Reserved for future use.

9.4 FIFO configuration register

9.4.1 FIFOControl

FIFOControl defines FIFO size, warning status, flush control, and the most significant bits of the WaterLevel and FIFOLength values.

Table 52. FIFOControl register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOSize	HiAlert	LoAlert	FIFOFlush	RFU	WaterLevel	FIFOLength	
Access rights	r/w	r	r	w	-	r/w	r	

Table 53. FIFOControl bits

Bit	Symbol	Description
7	FIFOSize	1: FIFO size is 255 bytes. 0: FIFO size is 512 bytes. Change the size only after clearing the FIFO.
6	HiAlert	Set when the remaining FIFO capacity is less than or equal to WaterLevel: HiAlert = (FIFOSize − FIFOLength) ≤ WaterLevel.
5	LoAlert	Set when the number of stored bytes is less than or equal to WaterLevel: LoAlert = FIFOLength ≤ WaterLevel.
4	FIFOFlush	Writing logic 1 clears the FIFO. Reading this bit always returns 0.
3	RFU	Reserved for future use.
2	WaterLevel	Bit 8 of WaterLevel when 512-byte FIFO mode is selected. Bits 7 to 0 are in the WaterLevel register.
1 to 0	FIFOLength	Bits 9 and 8 of FIFOLength when 512-byte FIFO mode is selected. Bits 7 to 0 are in the FIFOLength register.

9.4.2 WaterLevel

Defines the warning threshold for FIFO underflow and overflow. In 512-byte mode, the value is extended by FIFOControl.WaterLevel.

Table 54. WaterLevel register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	WaterLevel							
Access rights	r/w							

Table 55. WaterLevel bits

Bit	Symbol	Description
7 to 0	WaterLevel	Defines the FIFO warning threshold. In 512-byte mode, bit 8 is provided by FIFOControl.WaterLevel. HiAlert and LoAlert are calculated as described in Section 9.4.1.

9.4.3 FIFOLength

Indicates the number of bytes currently stored in the FIFO. In 512-byte mode, the value is extended by FIFOControl.FIFOLength.

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Table 56. FIFOLength register (address 04h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOLength							
Access rights	dy							

Table 57. FIFOLength bits

Bit	Symbol	Description
7 to 0	FIFOLength	Number of bytes in the FIFO. In 512-byte mode, bits 9 and 8 are provided by FIFOControl. Writing FIFOData increments the value; reading FIFOData decrements it.

9.4.4 FIFOData

FIFOData is the data port for the FIFO. Unlike ordinary register access, the register address does not advance after reading or writing FIFOData, allowing efficient multi-byte transfers. Writes increment FIFOLength and reads decrement it.

Table 58. FIFOData register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData							
Access rights	dy							

Table 59. FIFOData bits

Bit	Symbol	Description
7 to 0	FIFOData	Data input and output port for the internal FIFO buffer. Refer to Section 8.5, Buffer.

9.5 Interrupt configuration registers

IRQ0 and IRQ1 use a protected set/clear mechanism. Bit 7 selects whether writing logic 1 to a lower status bit sets or clears that status bit. For example, writing FFh sets all lower status bits, while writing 7Fh clears them.

9.5.1 IRQ0 register

Table 60. IRQ0 register (address 06h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Set	HiAlertIrq	LoAlertIrq	IdleIrq	TxIrq	RxIrq	ErrIrq	RxSOFIrq
Access rights	w	dy	dy	dy	dy	dy	dy	dy

Table 61. IRQ0 bits

Bit	Symbol	Description
7	Set	1: writing 1 to bits 6 to 0 sets the selected interrupt requests. 0: writing 1 to bits 6 to 0 clears the selected interrupt requests.
6	HiAlertIrq	Latched when HiAlert becomes set. Cleared only through the Set mechanism.
5	LoAlertIrq	Latched when LoAlert becomes set. Cleared only through the Set mechanism.
4	IdleIrq	Set when a command terminates automatically and Command returns to Idle. Starting Idle directly does not set this flag.
3	TxIrq	Set immediately after the last transmitted bit.
2	RxIrq	Set when the receiver detects the end of a data stream. This flag does not indicate whether the frame is error-free.
1	ErrIrq	Set when FIFO write error, FIFO overflow, protocol error, no-data error, or integrity error occurs.
0	RxSOFIrq	Set when a start-of-frame condition or subcarrier is detected.

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9.5.2 IRQ1 register

Table 62. IRQ1 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	Set	GlobalIrq	LPCD_Irq	Timer4Irq	Timer3Irq	Timer2Irq	Timer1Irq	Timer0Irq
Access rights	w	dy	dy	dy	dy	dy	dy	dy

Table 63. IRQ1 bits

Bit	Symbol	Description
7	Set	1: writing 1 to bits 5 to 0 sets the selected interrupt request. 0: writing 1 to bits 5 to 0 clears the selected interrupt request.
6	GlobalIrq	Set when an enabled interrupt request occurs.
5	LPCD_Irq	Set when a card is detected during an LPCD sequence.
4	Timer4Irq	Set when Timer4 underflows.
3	Timer3Irq	Set when Timer3 underflows.
2	Timer2Irq	Set when Timer2 underflows.
1	Timer1Irq	Set when Timer1 underflows.
0	Timer0Irq	Set when Timer0 underflows.

9.5.3 IRQ0En register

IRQ0En controls which IRQ0 sources propagate to GlobalIrq and controls IRQ output polarity.

Table 64. IRQ0En register (address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	Irq_Inv	HiAlertIrqEn	LoAlertIrqEn	IdleIrqEn	TxIrqEn	RxIrqEn	ErrIrqEn	RxSOFIrqEn
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 65. IRQ0En bits

Bit	Symbol	Description
7	Irq_Inv	Inverts the signal level on the IRQ pin when set.
6	HiAlertIrqEn	Enables propagation of HiAlertIrq to GlobalIrq.
5	LoAlertIrqEn	Enables propagation of LoAlertIrq to GlobalIrq.
4	IdleIrqEn	Enables propagation of IdleIrq to GlobalIrq.
3	TxIrqEn	Enables propagation of TxIrq to GlobalIrq.
2	RxIrqEn	Enables propagation of RxIrq to GlobalIrq.
1	ErrIrqEn	Enables propagation of ErrIrq to GlobalIrq.
0	RxSOFIrqEn	Enables propagation of RxSOFIrq to GlobalIrq.

9.5.4 IRQ1En

IRQ1En controls timer, LPCD, and global interrupt propagation and configures the IRQ output driver.

Table 66. IRQ1En register (address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	IrqPushPull	IrqPinEn	LPCD_IrqEn	Timer4IrqEn	Timer3IrqEn	Timer2IrqEn	Timer1IrqEn	Timer0IrqEn
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 67. IRQ1En bits

Bit	Symbol	Description
7	IrqPushPull	1: IRQ pin operates as push-pull output. 0: IRQ pin operates as open-drain output.

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Bit	Symbol	Description
6	IrqPinEn	Enables propagation of GlobalIrq to the IRQ pin.
5	LPCD_IrqEn	Enables propagation of LPCD_Irq to GlobalIrq.
4	Timer4IrqEn	Enables propagation of Timer4Irq to GlobalIrq.
3	Timer3IrqEn	Enables propagation of Timer3Irq to GlobalIrq.
2	Timer2IrqEn	Enables propagation of Timer2Irq to GlobalIrq.
1	Timer1IrqEn	Enables propagation of Timer1Irq to GlobalIrq.
0	Timer0IrqEn	Enables propagation of Timer0Irq to GlobalIrq.

9.6 Contactless interface configuration registers

9.6.1 Error

Table 68. Error register (address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	EE_Err	FIFOWrErr	FIFOOvl	MinFrameErr	NoDataErr	CollDet	ProtErr	IntegErr
Access rights	dy	dy	dy	dy	dy	dy	dy	dy

Table 69. Error bits

Bit	Symbol	Description
7	EE_Err	An error occurred during the most recent EEPROM command.
6	FIFOWrErr	Data was written to the FIFO during a state in which FIFO writes are not permitted, including certain transmit, receive-wait, or authentication phases. The flag is cleared when a new contactless command starts.
5	FIFOOvl	Data was written while the FIFO was full. Existing FIFO data remains unchanged; additional writes are ignored while this flag is set.
4	MinFrameErr	A valid SOF was received but fewer than four data bits followed. Such short frames are discarded. The flag is cleared at the beginning of receive processing.
3	NoDataErr	A transmission was requested while no data was available in the FIFO.
2	CollDet	A collision was detected. The first collision position is reported by RxColl. The flag is cleared at the beginning of receive processing.
1	ProtErr	A protocol error occurred, such as an invalid stop bit, an invalid ISO/IEC 14443B SOF/EOF, or an unexpected frame length. Reception stops and the last received byte is not stored.
0	IntegErr	A parity or CRC error was detected. Reception continues. When NoColl is set, a collision also sets IntegErr.

9.6.2 Status

Table 70. Status register (address 0Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	Crypto1On	-	-	ComState		
Access rights	RFU	RFU	dy	RFU	RFU	r		

Table 71. Status bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5	Crypto1On	Indicates whether MIFARE Crypto1 is active. Clearing this bit switches Crypto1 off; it can only be set by MFAuthent.
4 to 3	-	Reserved for future use.

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Bit	Symbol	Description
2 to 0	ComState	Contactless state-machine status: 000b: Idle 001b: TxWait 011b: Transmitting 101b: RxWait 110b: Wait for data 111b: Receiving 100b: not used

9.6.3 RxBitCtrl

Table 72. RxBitCtrl register (address 0Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	ValuesAfterColl	RxAlign			NoColl	RxLastBits		
Access rights	r/w	r/w			r/w	w		

Table 73. RxBitCtrl bits

Bit	Symbol	Description
7	ValuesAfterColl	When cleared, received bits after a collision are replaced with zero. This behavior is used for ISO/IEC 14443 anticollision.
6 to 4	RxAlign	Defines the bit position at which the first received bit is stored. RxAlign = 0h gives byte-oriented reception; non-zero values give bit-oriented reception.
3	NoColl	When set, a collision causes IntegErr to be set.
2 to 0	RxLastBits	Number of valid bits in the last received byte for bit-oriented communication. A value of zero means all eight bits are valid. The receiver updates these bits at the end of reception.

9.6.4 RxColl

Table 74. RxColl register (address 0Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	CollPosValid	CollPos						
Access rights	r	r						

Table 75. RxColl bits

Bit	Symbol	Description
7	CollPosValid	When set, CollPos contains a valid collision position. When cleared, no collision was detected or the position is outside the representable range.
6 to 0	CollPos	Bit position of the first collision in the first eight bytes of the received frame. 00h indicates the first bit, 01h the second bit, 08h the ninth bit, and 3Fh the 64th bit. RxAlign is included in the reported position. Interpret this field only for supported anticollision and ISO/IEC 15693/ICODE modes when CollPosValid is set.

9.7 Timer configuration registers

9.7.1 TControl

TControl provides protected start/stop control for Timer0 through Timer3. Bits 3 to 0 act as write strobes for the corresponding Running bits in positions 7 to 4. Writing FFh sets all Running bits; writing F0h leaves them unchanged.

Table 76. TControl register (address 0Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	T3Running	T2Running	T1Running	T0Running	T3StartStopNow	T2StartStopNow	T1StartStopNow	T0StartStopNow

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Access rights	dy	dy	dy	dy	w	w	w	w

Table 77. TControl bits

Bit	Symbol	Description
7	T3Running	Indicates whether Timer3 is running. Modified when T3StartStopNow is written.
6	T2Running	Indicates whether Timer2 is running. Modified when T2StartStopNow is written.
5	T1Running	Indicates whether Timer1 is running. Modified when T1StartStopNow is written.
4	T0Running	Indicates whether Timer0 is running. Modified when T0StartStopNow is written.
3	T3StartStopNow	Write strobe for T3Running.
2	T2StartStopNow	Write strobe for T2Running.
1	T1StartStopNow	Write strobe for T1Running.
0	T0StartStopNow	Write strobe for T0Running.

9.7.2 T0Control

Control register for Timer0.

Table 78. T0Control register (address 0Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	T0StopRx	-	T0Start		T0AutoRestart	-	T0Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 79. T0Control bits

Bit	Symbol	Description
7	T0StopRx	When set, Timer0 stops after the first four received bits. When cleared, reception does not stop Timer0 automatically. This bit has no effect during LFO trimming.
6	-	Reserved for future use.
5 to 4	T0Start	00b: no automatic start 01b: start at end of transmission 10b: LFO trimming without underflow 11b: LFO trimming with underflow
3	T0AutoRestart	1: automatically reload and restart after underflow. 0: stop at zero. Timer0Irq is set on underflow.
2	-	Reserved for future use.
1 to 0	T0Clk	00b: 13.56 MHz 01b: 211.875 kHz 10b: Timer2 underflow 11b: Timer1 underflow

9.7.2.1 T0ReloadHi

High byte of the Timer0 reload value.

Table 80. T0ReloadHi register (address 10h)

Bit	7	6	5	4	3	2	1	0
Symbol	T0ReloadHi							
Access rights	r/w							

Table 81. T0ReloadHi bits

Bit	Symbol	Description
7 to 0	T0ReloadHi	Defines the high byte of the Timer0 reload value. At the next start event, Timer0 loads T0ReloadHi and T0ReloadLo. Changes do not affect the current count until the next start event.

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9.7.2.2 T0ReloadLo

Low byte of the Timer0 reload value.

Table 82. T0ReloadLo register (address 11h)

Bit	7	6	5	4	3	2	1	0
Symbol	T0ReloadLo							
Access rights	r/w							

Table 83. T0ReloadLo bits

Bit	Symbol	Description
7 to 0	T0ReloadLo	Defines the low byte of the Timer0 reload value. At the next start event, the timer loads T0ReloadValHi and T0ReloadValLo. Changing this register affects the timer only at the next start event.

9.7.2.3 T0CounterValHi

High byte of the counter value of Timer0.

Table 84. T0CounterValHi register (address 12h)

Bit	7	6	5	4	3	2	1	0
Symbol	T0CounterValHi							
Access rights	dy							

Table 85. T0CounterValHi bits

Bit	Symbol	Description
7 to 0	T0CounterValHi	High byte of the current Timer0 counter value. This value shall not be read during reception.

9.7.2.4 T0CounterValLo

Low byte of the counter value of Timer0.

Table 86. T0CounterValLo register (address 13h)

Bit	7	6	5	4	3	2	1	0
Symbol	T0CounterValLo							
Access rights	dy							

Table 87. T0CounterValLo bits

Bit	Symbol	Description
7 to 0	T0CounterValLo	Low byte of the current Timer0 counter value. This value shall not be read during reception.

9.7.2.5 T1Control

Control register of Timer1.

Table 88. T1Control register (address 14h)

Bit	7	6	5	4	3	2	1	0
Symbol	T1STOPRx	-	T1Start		T1AutoRestart	-	T1Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 89. T1Control bits

Bit	Symbol	Description
7	T1STOPRx	If set, Timer1 stops after receiving the first four bits. If cleared, Timer1 is not stopped automatically. **Note**: This bit has no effect when LFO trimming is selected by T1Start.

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Bit	Symbol	Description
6	-	Reserved for future use.
5 to 4	T1Start	00b: Timer is not started automatically. 01b: Timer starts automatically at the end of transmission. 10b: LFO trimming without underflow (start/stop on positive edge). 11b: LFO trimming with underflow (start/stop on positive edge).
3	T1AutoRestart	1: Timer automatically reloads T1ReloadValue after reaching zero. 0: Timer decrements to zero and stops. Timer1Irq is set when the timer underflows.
2	-	Reserved for future use.
1 to 0	T1Clk	00b: 13.56 MHz. 01b: 211.875 kHz. 10b: Timer0 underflow. 11b: Timer2 underflow.

9.7.2.6 T1ReloadHi

High byte (MSB) of the Timer1 reload value.

Table 90. T1ReloadHi register (address 15h)

Bit	7	6	5	4	3	2	1	0
Symbol	T1ReloadHi							
Access rights	r/w							

Table 91. T1ReloadHi bits

Bit	Symbol	Description
7 to 0	T1ReloadHi	Defines the high byte of the Timer1 reload value. At the next start event, Timer1 loads T1ReloadValHi and T1ReloadValLo. Changing this register affects the timer only at the next start event.

9.7.2.7 T1ReloadLo

Low byte (LSB) of the Timer1 reload value.

Table 92. T1ReloadLo register (address 16h)

Bit	7	6	5	4	3	2	1	0
Symbol	T1ReloadLo							
Access rights	r/w							

Table 93. T1ReloadLo bits

Bit	Symbol	Description
7 to 0	T1ReloadLo	Defines the low byte of the Timer1 reload value. Changing this register affects the timer only at the next start event.

9.7.2.8 T1CounterValHi

High byte (MSB) of the Timer1 counter value.

Table 94. T1CounterValHi register (address 17h)

Bit	7	6	5	4	3	2	1	0
Symbol	T1CounterValHi							
Access rights	dy							

Table 95. T1CounterValHi bits

Bit	Symbol	Description
7 to 0	T1CounterValHi	High byte of the current Timer1 counter value. This value shall not be read during reception.

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9.7.2.9 T1CounterValLo

Low byte (LSB) of the Timer1 counter value.

Table 96. T1CounterValLo register (address 18h)

Bit	7	6	5	4	3	2	1	0
Symbol	T1CounterValLo							
Access rights	dy							

Table 97. T1CounterValLo bits

Bit	Symbol	Description
7 to 0	T1CounterValLo	Low byte of the current Timer1 counter value. This value shall not be read during reception.

9.7.2.10 T2Control

Control register of Timer2.

Table 98. T2Control register (address 19h)

Bit	7	6	5	4	3	2	1	0
Symbol	T2STOPRx	-	T2Start		T2AutoRestart	-	T2Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 99. T2Control bits

Bit	Symbol	Description
7	T2STOPRx	If set, Timer2 stops immediately after receiving the first four bits. If cleared, Timer2 is not stopped automatically. **Note**: This bit has no effect when LFO trimming is selected by T2Start.
6	-	Reserved for future use.
5 to 4	T2Start	00b: Timer is not started automatically. 01b: Timer starts automatically at the end of transmission. 10b: LFO trimming without underflow (start/stop on positive edge). 11b: LFO trimming with underflow (start/stop on positive edge).
3	T2AutoRestart	1: Timer automatically reloads T2ReloadValue after reaching zero. 0: Timer decrements to zero and stops. Timer2Irq is set when the timer underflows.
2	-	Reserved for future use.
1 to 0	T2Clk	00b: 13.56 MHz. 01b: 212 kHz. 10b: Timer0 underflow. 11b: Timer1 underflow.

9.7.2.11 T2ReloadHi

High byte of the Timer2 reload value.

Table 100. T2ReloadHi register (address 1Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	T2ReloadHi							
Access rights	r/w							

Table 101. T2ReloadHi bits

Bit	Symbol	Description
7 to 0	T2ReloadHi	Defines the high byte of the Timer2 reload value. At the next start event, Timer2 loads T2ReloadValHi and T2ReloadValLo. Changing this register affects the timer only at the next start event.

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9.7.2.12 T2ReloadLo

Low byte of the Timer2 reload value.

Table 102. T2ReloadLo register (address 1Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	T2ReloadLo							
Access rights	r/w							

Table 103. T2ReloadLo bits

Bit	Symbol	Description
7 to 0	T2ReloadLo	Defines the low byte of the Timer2 reload value. At the next start event, Timer2 loads T2ReloadValHi and T2ReloadValLo. Changing this register affects the timer only at the next start event.

9.7.2.13 T2CounterValHi

High byte of the Timer2 counter value.

Table 104. T2CounterValHi register (address 1Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	T2CounterValHi							
Access rights	dy							

Table 105. T2CounterValHi bits

Bit	Symbol	Description
7 to 0	T2CounterValHi	High byte of the current Timer2 counter value. This value shall not be read during reception.

9.7.2.14 T2CounterValLo

Low byte of the current Timer2 counter value.

Table 106. T2CounterValLo register (address 1Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	T2CounterValLo							
Access rights	dy							

Table 107. T2CounterValLo bits

Bit	Symbol	Description
7 to 0	T2CounterValLo	Low byte of the current Timer2 counter value. This value shall not be read during reception.

9.7.2.15 T3Control

Control register of Timer3.

Table 108. T3Control register (address 1Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	T3STOPRx	-	T3Start		T3AutoRestart	-	T3Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 109. T3Control bits

Bit	Symbol	Description
7	T3STOPRx	If set, Timer3 stops immediately after receiving the first four bits. If cleared, Timer3 is not stopped automatically. **Note**: This bit has no effect when LFO trimming is selected by T3Start.

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Bit	Symbol	Description
6	-	Reserved for future use.
5 to 4	T3Start	00b: Timer is not started automatically. 01b: Timer starts automatically at the end of transmission. 10b: LFO trimming without underflow (start/stop on positive edge). 11b: LFO trimming with underflow (start/stop on positive edge).
3	T3AutoRestart	1: Timer automatically reloads T3ReloadValue after reaching zero. 0: Timer decrements to zero and stops. Timer3Irq is set when the timer underflows.
2	-	Reserved for future use.
1 to 0	T3Clk	00b: 13.56 MHz. 01b: 211.875 kHz. 10b: Timer0 underflow. 11b: Timer1 underflow.

9.7.2.16 T3ReloadHi

High byte of the Timer3 reload value.

Table 110. T3ReloadHi register (address 1Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	T3ReloadHi							
Access rights	r/w							

Table 111. T3ReloadHi bits

Bit	Symbol	Description
7 to 0	T3ReloadHi	Defines the high byte of the Timer3 reload value. At the next start event, Timer3 loads T3ReloadValHi and T3ReloadValLo. Changing this register affects the timer only at the next start event.

9.7.2.17 T3ReloadLo

Low byte of the Timer3 reload value.

Table 112. T3ReloadLo register (address 20h)

Bit	7	6	5	4	3	2	1	0
Symbol	T3ReloadLo							
Access rights	r/w							

Table 113. T3ReloadLo bits

Bit	Symbol	Description
7 to 0	T3ReloadLo	Defines the low byte of the Timer3 reload value. At the next start event, Timer3 loads T3ReloadValHi and T3ReloadValLo. Changing this register affects the timer only at the next start event.

9.7.2.18 T3CounterValHi

High byte of the current 16-bit Timer3 counter value.

Table 114. T3CounterValHi register (address 21h)

Bit	7	6	5	4	3	2	1	0
Symbol	T3CounterValHi							
Access rights	dy							

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Table 115. T3CounterValHi bits

Bit	Symbol	Description
7 to 0	T3CounterValHi	High byte of the current Timer3 counter value. This value shall not be read during reception.

9.7.2.19 T3CounterValLo

Low byte of the current 16-bit Timer3 counter value.

Table 116. T3CounterValLo register (address 22h)

Bit	7	6	5	4	3	2	1	0
Symbol	T3CounterValLo							
Access rights	dy							

Table 117. T3CounterValLo bits

Bit	Symbol	Description
7 to 0	T3CounterValLo	Low byte of the current Timer3 counter value. This value shall not be read during reception.

9.7.2.20 T4Control

Wake-up timer T4 activates the system after a programmed interval. When enabled, it can also start the low-power card detection function.

Table 118. T4Control register (address 23h)

Bit	7	6	5	4	3	2	1	0
Symbol	T4Running	T4Start StopNow	T4Auto Trimm	T4Auto LPCD	T4Auto Restart	T4AutoWakeUp	T4Clk	
Access rights	dy	w	r/w	r/w	r/w	r/w	r/w	

Table 119. T4Control bits

Bit	Symbol	Description
7	T4Running	Shows whether Timer4 is running. If T4StartStopNow is set, this bit and Timer4 can be started or stopped.
6	T4StartStopNow	When set, T4Running can be changed.
5	T4AutoTrimm	When set, Timer4 starts an LFO trimming procedure at underflow. At least one of Timer0 to Timer3 must be configured for trimming. Timer3 shall not be used for this function when T4AutoLPCD is enabled in parallel.
4	T4AutoLPCD	When set, Timer4 starts a low-power card detection sequence. If a card is detected, an interrupt is raised and the system remains active when enabled. If no card is detected, the NF663E enters power-down mode when enabled. Timer3 defines the RF-field sampling time and therefore shall not be used for T4AutoTrimm at the same time.
3	T4AutoRestart	1: Timer4 automatically reloads T4ReloadValue after reaching zero. 0: Timer4 decrements to zero and stops. Timer4Irq is set at underflow.
2	T4AutoWakeUp	When set, the NF663E wakes automatically at Timer4 underflow. Set this bit when the device shall enter power-down after T4AutoTrimm or T4AutoLPCD and no card is detected. Clear it when the device shall remain active.
1 to 0	T4Clk	00b: LFO clock. 01b: LFO clock / 8. 10b: LFO clock / 16. 11b: LFO clock / 32.

9.7.2.21 T4ReloadHi

High byte of the 16-bit Timer4 reload value.

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Table 120. T4ReloadHi register (address 24h)

Bit	7	6	5	4	3	2	1	0
Symbol	T4ReloadHi							
Access rights	r/w							

Table 121. T4ReloadHi bits

Bit	Symbol	Description
7 to 0	T4ReloadHi	Defines the high byte of the Timer4 reload value. At the next start event, Timer4 loads T4ReloadVal. Changing this register affects the timer only at the next start event.

9.7.2.22 T4ReloadLo

Low byte of the 16-bit Timer4 reload value.

Table 122. T4ReloadLo register (address 25h)

Bit	7	6	5	4	3	2	1	0
Symbol	T4ReloadLo							
Access rights	r/w							

Table 123. T4ReloadLo bits

Bit	Symbol	Description
7 to 0	T4ReloadLo	Defines the low byte of the Timer4 reload value. At the next start event, Timer4 loads T4ReloadVal. Changing this register affects the timer only at the next start event.

9.7.2.23 T4CounterValHi

High byte of the current 16-bit Timer4 counter value.

Table 124. T4CounterValHi register (address 26h)

Bit	7	6	5	4	3	2	1	0
Symbol	T4CounterValHi							
Access rights	dy							

Table 125. T4CounterValHi bits

Bit	Symbol	Description
7 to 0	T4CounterValHi	High byte of the current Timer4 counter value.

9.7.2.24 T4CounterValLo

Low byte of the current 16-bit Timer4 counter value.

Table 126. T4CounterValLo register (address 27h)

Bit	7	6	5	4	3	2	1	0
Symbol	T4CounterValLo							
Access rights	dy							

Table 127. T4CounterValLo bits

Bit	Symbol	Description
7 to 0	T4CounterValLo	Low byte of the current Timer4 counter value.

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9.8 Transmitter configuration registers

9.8.1 TxMode

Table 128. DrvMode register (address 28h)

Bit	7	6	5	4	3	2	1	0
Symbol	Tx2Inv	Tx1Inv	-	-	TxEn	TxClkMode		
Access rights	r/w	r/w	RFU	RFU	r/w	r/w		

Table 129. DrvMode bits

Bit	Symbol	Description
7	Tx2Inv	Inverts transmitter 2 at the TX2 pin.
6	Tx1Inv	Inverts transmitter 1 at the TX1 pin.
5	-	Reserved for future use.
4	-	Reserved for future use.
3	TxEn	When set, both transmitter pins are enabled.
2 to 0	TxClkMode	Defines the transmitter clock and output stage operating mode; refer to Section 8.6.2, Table 27. Codes 011b and 110b are not supported. The output can be configured as open-drain, push-pull, high-impedance, fixed-high, or fixed-low.

9.8.2 TxAmp

The set_cw_amplitude field trades transmitter output power against power-supply rejection. More voltage headroom improves supply rejection and modulation-index accuracy. When CwMax is set, TX1 is driven to the maximum possible amplitude and the set_cw_amplitude setting is overridden.

Table 130. TxAmp register (address 29h)

Bit	7	6	5	4	3	2	1	0
Symbol	set_cw_amplitude		-	set_residual_carrier				
Access rights	r/w		RFU	r/w				

Table 131. TxAmp bits

Bit	Symbol	Description
7 to 6	set_cw_amplitude	Reduces the transmitter output amplitude by a fixed value: 0: TV_{DD} - 100 mV 1: TV_{DD} - 250 mV 2: TV_{DD} - 500 mV 3: TV_{DD} - 1000 mV
5	-	Reserved for future use.
4 to 0	set_residual_carrier	Sets the residual-carrier percentage; refer to Section 8.6.2.

9.8.3 TxCon

Table 132. TxCon register (address 2Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	OvershootT2				CwMax	TxInv	TxSel	
Access rights	r/w				r/w	r/w	r/w	

Table 133. TxCon bits

Bit	Symbol	Description
7 to 4	OvershootT2	Specifies the number of carrier clocks used for the additional modulation interval for overshoot protection. Refer to Section 8.6.2.1.

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Bit	Symbol	Description
3	CwMax	Sets the continuous-wave carrier amplitude to the maximum. When set, set_cw_amplitude in TxAmp has no effect on the continuous amplitude.
2	TxInv	Inverts the modulation signal selected by TxSel.
1 to 0	TxSel	00b: no modulation. 01b: TxEnvelope. 10b: SIGIN. 11b: reserved.

9.8.4 TxI

Table 134. TxI register (address 2Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	OvershootT1				tx_set_iLoad			
Access rights	r/w				r/w			

Table 135. TxI bits

Bit	Symbol	Description
7 to 4	OvershootT1	Overshoot interval 1 value. Refer to Section 8.6.2.1, Overshoot protection.
3 to 0	tx_set_iLoad	Factory trim value representing the expected transmitter load current. It is used to optimize the modulation index according to the expected TX load current.

9.9 CRC configuration registers

9.9.1 TxCrcPreset

Table 136. TxCrcPreset register (address 2Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	TXPresetVal			TxCRCtype		TxCRCInvert	TxCRCEn
Access rights	-	r/w			r/w		r/w	r/w

Table 137. TxCrcPreset bits

Bit	Symbol	Description
7	RFU	Reserved for future use.
6 to 4	TXPresetVal	Selects the transmitter CRC preset value; refer to Table 138.
3 to 2	TxCRCtype	00b: CRC5. 01b: CRC8. 10b: CRC16. 11b: reserved.
1	TxCRCInvert	When set, the calculated CRC is inverted before being appended to the data frame (ISO/IEC 3309).
0	TxCRCEn	When set, a CRC is appended to the transmitted data stream.

Table 138. Transmitter CRC preset value configuration

TXPresetVal[6...4]	CRC16	CRC8	CRC5
0h	0000h	00h	00h
1h	6363h	12h	12h
2h	A671h	BFh	-
3h	FFFEh	FDh	-
4h	-	-	-
5h	-	-	-

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TXPresetVal[6...4]	CRC16	CRC8	CRC5
6h	User defined	User defined	User defined
7h	FFFFh	FFh	1Fh

Remark: User-defined CRC preset values can be configured in EEPROM.

9.9.2 RxCrcCon

Table 139. RxCrcCon register (address 2Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	RxForceCRCWrite	RXPresetVal			RXCRCtype		RxCRCInvert	RxCRCEn
Access rights	r/w	r/w			r/w		r/w	r/w

Table 140. RxCrcCon bits

Bit	Symbol	Description
7	RxForceCRCWrite	When set, received CRC byte(s) are copied to the FIFO. When cleared, CRC bytes are checked but not copied. This bit shall be set for non-byte-aligned CRC formats, such as ISO/IEC 18000-3 mode 3 / EPC Class-1 HF.
6 to 4	RXPresetVal	Selects the receiver CRC preset value; refer to Table 141.
3 to 2	RxCRCtype	00b: CRC5. 01b: CRC8. 10b: CRC16. 11b: reserved.
1	RxCRCInvert	When set, the received CRC is checked in inverted form.
0	RxCRCEn	When set, the CRC is checked and an error flag is set for an invalid CRC. When cleared, the CRC is calculated but the error flag is not modified.

Table 141. Receiver CRC preset value configuration

RXPresetVal[6...4]	CRC16	CRC8	CRC5
0h	0000h	00h	00h
1h	6363h	12h	12h
2h	A671h	BFh	-
3h	FFFEh	FDh	-
4h	-	-	-
5h	-	-	-
6h	User defined	User defined	User defined
7h	FFFFh	FFh	1Fh

9.10 Transmitter configuration registers

9.10.1 TxDataNum

Table 142. TxDataNum register (address 2Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU			KeepBitGrid	DataEn	TxLastBits		
Access rights	-			r/w	r/w	r/w		

Table 143. TxDataNum bits

Bit	Symbol	Description
7 to 5	RFU	Reserved for future use.

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Bit	Symbol	Description
4	KeepBitGrid	When set, the interval between consecutive transmission starts is an integer multiple of one ETU. When cleared, a following transmission may begin within an ETU.
3	DataEn	0: a single symbol pattern can be sent without data. 1: FIFO data is transmitted.
2 to 0	TxLastBits	Defines the number of valid bits in the final data byte. 000b sends all eight bits. Bits are omitted from the end of the byte. Example for B2h sent LSB first: TxLastBits = 011b sends 010b; TxLastBits = 110b sends 010011b.

9.10.2 TxDataModWidth

Transmitter data modulation width register.

Table 144. TxDataModWidth register (address 2Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	DModWidth							
Access rights	r/w							

Table 145. TxDataModWidth bits

Bit	Symbol	Description
7 to 0	DModWidth	Specifies the pulse length for pulse-modulated data as the number of carrier clocks plus one. A pulse cannot extend beyond the end of the bit. The pulse start position is selected by TxDataMod.DPulseType. **Note**: This register is used for Miller modulation in ISO/IEC 14443A PCD mode and also controls the modulation width of start and stop symbols.

9.10.3 TxSym10BurstLen

For protocols that require an unmodulated subcarrier burst, this register defines the burst length. The high or low burst level is selected by TxSym10BurstCtrl.

Table 146. TxSym10BurstLen register (address 30h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	Sym1BurstLen			RFU	Sym0BurstLen		
Access rights	-	r/w			-	r/w		

Table 147. TxSym10BurstLen bits

Bit	Symbol	Description
7	RFU	Reserved for future use.
6 to 4	Sym1BurstLen	Specifies the number of bits in the Symbol1 burst: 00b: 8 bits. 001b: 16 bits. 010b: 32 bits. 011b: 48 bits. 100b: 64 bits. 101b: 96 bits. 110b: 128 bits. 111b: 256 bits.
3	RFU	Reserved for future use.

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Bit	Symbol	Description
2 to 0	Sym0BurstLen	Specifies the number of bits in the Symbol0 burst: 000b: 8 bits. 001b: 16 bits. 010b: 32 bits. 011b: 48 bits. 100b: 64 bits. 101b: 96 bits. 110b: 128 bits. 111b: 256 bits.

9.10.4 TxWaitCtrl

Table 148. TxWaitCtrl register (address 31h); reset value: C0h

Bit	7	6	5	4	3	2	1	0
Symbol	TxWaitStart	TxWaitEtu	TxWaitHigh			TxSTOPBitLength		
Access rights	r/w	r/w	r/w			r/w		

Table 149. TxWaitCtrl bits

Bit	Symbol	Description
7	TxWaitStart	0: TxWait starts at the end of transmitted data (TX). 1: TxWait starts at the end of received data (RX).
6	TxWaitEtu	0: TxWait time = TxWait x 16 / 13.56 MHz. 1: TxWait time = TxWait x 0.5 / DBFreq, where DBFreq is the bit-stream frequency selected by TxDataCon.
5 to 3	TxWaitHigh	High three bits of the 11-bit TxWait value; bit 5 is the most significant bit.
2 to 0	TxSTOPBitLength	Defines stop bits and extra guard time (EGT): 0h: no stop bit, no EGT. 1h: 1 stop bit, no EGT. 2h: 1 stop bit + 1 EGT. 3h: 1 stop bit + 2 EGT. 4h: 1 stop bit + 3 EGT. 5h: 1 stop bit + 4 EGT. 6h: 1 stop bit + 5 EGT. 7h: 1 stop bit + 6 EGT. **Note:** Valid only for ISO/IEC 14443 Type B.

9.10.5 TxWaitLo

Table 150. TxWaitLo register (address 32h)

Bit	7	6	5	4	3	2	1	0
Symbol	TxWaitLo							
Access rights	r/w							

Table 151. TxWaitLo bits

Bit	Symbol	Description
7 to 0	TxWaitLo	Defines the minimum interval between receiving and transmitting, or between two transmitted data streams. TxWait is an 11-bit value; its upper three bits are in TxWaitCtrl. Refer also to TxWaitEtu and TxWaitStart.

9.11 FrameCon

Table 152. FrameCon register (address 33h)

Bit	7	6	5	4	3	2	1	0
Symbol	TxParityEn	RxParityEn	-	-	STOPSym		StartSym	
Access rights	r/w	r/w	RFU	RFU	r/w		r/w	

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Table 153. FrameCon bits

Bit	Symbol	Description
7	TxParityEn	When set, a parity bit is calculated and appended to every transmitted byte.
6	RxParityEn	When set, parity checking is enabled. The received parity bit is not transferred to the FIFO.
5 to 4	-	Reserved for future use.
3 to 2	STOPSym	Selects the symbol sent as the stop symbol: 0h: no symbol. 1h: Symbol0. 2h: Symbol1. 3h: Symbol2.
1 to 0	StartSym	Selects the symbol sent as the start symbol: 0h: no symbol. 1h: Symbol0. 2h: Symbol1. 3h: Symbol2.

9.12 Receiver configuration registers

9.12.1 RxSofD

Table 154. RxSofD register (address 34h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU		SOF_En	SOFDetected	RFU	SubC_En	SubC_Detected	SubC_Present
Access rights	-		r/w	dy	-	r/w	dy	r

Table 155. RxSofD bits

Bit	Symbol	Description
7 to 6	RFU	Reserved for future use.
5	SOF_En	When set, detection of a start-of-frame condition raises RxSOFIrq.
4	SOF_Detected	Indicates that a start-of-frame condition is or was detected. Can be cleared by software.
3	RFU	Reserved for future use.
2	SubC_En	When set, detection of a subcarrier raises RxSOFIrq.
1	SubC_Detected	Indicates that a subcarrier is or was detected. Can be cleared by software.
0	SubC_Present	Indicates that a subcarrier is currently present.

9.12.2 RxCtrl

Table 156. RxCtrl register (address 35h)

Bit	7	6	5	4	3	2	1	0
Symbol	RxAllowBits	RxMultiple	RxEOFType	EGT_Check	EMD_Sup	Baudrate		
Access rights	r/w	r/w	r/w	r/w	r/w	r/w		

Table 157. RxCtrl bits

Bit	Symbol	Description
7	RxAllowBits	When set, received data is written to the FIFO even if CRC checking is enabled and the final byte is incomplete.
6	RxMultiple	When set, the receiver does not terminate automatically; refer to Section 8.10.3.6. At the end of each received data stream, an error byte containing a copy of the Error register is added to the FIFO.

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Bit	Symbol	Description
5	RxEOFType	0: EOF defined by RxEOFSymbolReg is expected. 1: ISO/IEC 14443B EOF is expected. **Note**: Clearing this bit and clearing bits 1 and 0 of RxEOFSymbolReg disables EOF checking.
4	EGT_Check	When set, extra guard time is checked. An excessive EGT sets a protocol error. Valid only for ISO/IEC 14443 Type B.
3	EMD_Sup	Enables EMD suppression according to ISO/IEC 14443. An error in the first three bytes causes those bytes to be treated as EMD, ignored, and the FIFO reset. A collision is also treated as an error. If a valid SOF was received and fewer than three bytes follow, RxIrq is not set. When RxForceCRCWrite is enabled, the FIFO shall not be read before three bytes have been written.
2 to 0	Baudrate	2h: 26 kBd. 3h: 52 kBd. 4h: 106 kBd. 5h: 212 kBd. 6h: 424 kBd. 7h: 847 kBd. All remaining values are reserved.

9.12.3 RxWait

Selects the receive blanking interval after transmission.

Table 158. RxWait register (address 36h)

Bit	7	6	5	4	3	2	1	0
Symbol	RxWaitEtu	RxWait						
Access rights	r/w	r/w						

Table 159. RxWait bits

Bit	Symbol	Description
7	RxWaitEtu	0: RxWait time = RxWait x 16 / 13.56 MHz. 1: RxWait time = RxWait x 0.5 / DBFreq.
6 to 0	RxWait	Defines the time after transmission during which all receiver inputs are ignored.

9.12.4 RxThreshold

Selects the minimum threshold level for the bit decoder.

Table 160. RxThreshold register (address 37h)

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel				MinLevelP			
Access rights	r/w				r/w			

Table 161. RxThreshold bits

Bit	Symbol	Description
7 to 4	MinLevel	Defines the minimum receiver level. The value should be higher than the system noise level.
3 to 0	MinLevelP	Defines the minimum level of the phase-shift detector.

9.12.5 Rcv

Table 162. Rcv register (address 38h)

Bit	7	6	5	4	3	2	1	0
Symbol	Rcv_Rx_single	Rx_ADCmode	SigInSel		RFU		CollLevel	
Access rights	r/w	r/w	r/w		-		r/w	

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Table 163. Rcv bits

Bit	Symbol	Description
7	Rcv_Rx_single	Selects the RXP/RXN input mode: 0: fully differential. 1: quasi-differential.
6	Rx_ADCmode	Selects the ADC operating mode: 0: normal reception. 1: LPCD mode.
5 to 4	SigInSel	Selects the signal-processing input: 0h: idle. 1h: internal analog receiver block. 2h: external envelope signal for ISO/IEC 14443A. 3h: external generic signal.
3 to 2	RFU	Reserved for future use.
1 to 0	CollLevel	Sets the signal level interpreted as a collision: 0h: at least 1/8 of signal strength. 1h: at least 1/4. 2h: at least 1/2. 3h: collision detection disabled.

9.12.6 RxAna

Controls receiver gain (rcv_gain) and high-pass corner frequency (rcv_hpcf).

Table 164. RxAna register (address 39h)

Bit	7	6	5	4	3	2	1	0
Symbol	VMid_r_sel		RFU		rcv_hpcf		rcv_gain	
Access rights	r/w		-		r/w		r/w	

Table 165. RxAna bits

Bit	Symbol	Description
7 to 6	VMid_r_sel	Factory trim value; keep at 0.
5 to 4	RFU	Reserved for future use.
3 to 2	rcv_hpcf	Selects one of four baseband-amplifier lower cut-off frequencies, approximately 40 kHz to 300 kHz.
1 to 0	rcv_gain	Selects one of four receiver gain settings, approximately 30 dB to 60 dB in differential mode.

Table 166. Effect of gain and high-pass corner register settings

rcv_gain (Hex.)	rcv_hpcf (Hex.)	f_L (kHz)	f_U (MHz)	Gain (dB20)	Bandwidth (MHz)
03	00	38	2.3	60	2.3
03	01	79	2.4	59	2.3
03	02	150	2.6	58	2.5
03	03	264	2.9	55	2.6
02	00	41	2.3	51	2.3
02	01	83	2.4	50	2.3
02	02	157	2.6	49	2.4
02	03	272	3.0	41	2.7
01	00	42	2.6	43	2.6
01	01	84	2.7	42	2.6
01	02	157	2.9	41	2.7
01	03	273	3.3	39	3.0

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rcv_gain (Hex.)	rcv_hpcf (Hex.)	f_L (kHz)	f_U (MHz)	Gain (dB20)	Bandwidth (MHz)
00	00	43	2.6	35	2.6
00	01	85	2.7	34	2.6
00	02	159	2.9	33	2.7
00	03	276	3.4	30	3.1

9.13 Clock configuration

9.13.1 SerialSpeed

This register sets the RS232 interface speed. The serial frame uses one start bit, eight data bits and one stop bit, without parity. Transfer rates above 1228.8 kbit/s are not supported.

BR_T0 = 0: transfer speed = 27.12 MHz / (BR_T1 + 1)
BR_T0 > 0: transfer speed = 27.12 MHz / [(BR_T1 + 33) × $2^{(BR\_T0 - 1)}$]

Table 167. SerialSpeed register (address 3Bh); reset value: 7Ah

Bit	7	6	5	4	3	2	1	0
Symbol	BR_T0			BR_T1				
Access rights	r/w			r/w				

Table 168. SerialSpeed bits

Bit	Symbol	Description
7 to 5	BR_T0	Selects the formula and divider exponent shown above.
4 to 0	BR_T1	Divider term used by the transfer-speed formulas.

Table 169. RS232 speed settings

Transfer speed (kbit/s)	SerialSpeed register content (Hex.)
7.2	FA
9.6	EB
14.4	DA
19.2	CB
38.4	AB
57.6	9A
115.2	7A
128.0	74
230.4	5A
460.8	3A
921.6	1C
1228.8	15

9.13.2 LFO_Trimm

Table 170. LFO_Trim register (address 3Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	LFO_trimm							
Access rights	r/w							

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Table 171. LFO_Trim bits

Bit	Symbol	Description
7 to 0	LFO_trimm	LFO trim value. Increasing the trim value decreases the oscillator frequency; refer to Section 8.8.3.

9.13.3 PLL_Ctrl register

The Integer-N PLL generates CLKOUT from the 27.12 MHz input in two stages. The first stage multiplies the input by PLLDiv_FB and divides by two; the second stage divides the result by PLLDiv_Out.

Table 172. PLL_Ctrl register (address 3Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	ClkOutSel				ClkOut_En	PLL_PD	PLLDiv_FB	
Access rights	r/w				r/w	r/w	r/w	

Table 173. PLL_Ctrl register bits

Bit	Symbol	Description
7 to 4	ClkOutSel	0h: CLKOUT used as I/O. 1h: analog PLL output. 2h: forced low. 3h: forced high. 4h: 27.12 MHz. 5h: 13.56 MHz. 6h: 6.78 MHz. 7h: 3.39 MHz. 8h to Bh: toggled by Timer0 to Timer3 overflow. Ch to Fh: RFU.
3	ClkOut_En	Enables the clock output on CLKOUT.
2	PLL_PD	Powers down the PLL when set.
1 to 0	PLLDiv_FB	PLL feedback divider selection; see Table 174.

Table 174. Setting of feedback divider PLLDiv_FB[1:0]

Bit 1	Bit 0	Division
0	0	23 (VCO frequency 312 MHz)
0	1	27 (VCO frequency 366 MHz)
1	0	28 (VCO frequency 380 MHz)
1	1	23 (VCO frequency 312 MHz)

9.13.4 PLLDiv_Out

Table 175. PLLDiv_Out register (address 3Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	PLLDiv_Out							
Access rights	r/w							

Table 176. PLLDiv_Out bits

Bit	Symbol	Description
7 to 0	PLLDiv_Out	PLL output divider factor; refer to Section 8.8.2.

Table 177. Setting for the output divider ratio PLLDiv_Out[7:0]

Value	Division
0	RFU

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Value	Division
1	RFU
2	RFU
3	RFU
4	RFU
5	RFU
6	RFU
7	RFU
8	8
9	9
10	10
...	...
253	253
254	254

9.14 Low-power card detection configuration registers

The six-bit LPCD_IMax value is distributed across bits 7 and 6 of LPCD_QMin, LPCD_QMax and LPCD_IMin.

9.14.1 LPCD_QMin

Table 178. LPCD_QMin register (address 3Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	LPCD_IMax.5	LPCD_IMax.4	LPCD_QMin					
Access rights	r/w	r/w	r/w					

Table 179. LPCD_QMin bits

Bit	Symbol	Description
7 to 6	LPCD_IMax	Highest two bits of the I-channel upper threshold.
5 to 0	LPCD_QMin	Q-channel lower threshold. Crossing the threshold raises an LPCD interrupt.

9.14.2 LPCD_QMax

Table 180. LPCD_QMax register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	LPCD_IMax.3	LPCD_IMax.2	LPCD_QMax					
Access rights	r/w	r/w	r/w					

Table 181. LPCD_QMax bits

Bit	Symbol	Description
7	LPCD_IMax.3	Bit 3 of the I-channel upper threshold.
6	LPCD_IMax.2	Bit 2 of the I-channel upper threshold.
5 to 0	LPCD_QMax	Q-channel upper threshold. Exceeding the threshold raises an LPCD interrupt.

9.14.3 LPCD_IMin

Table 182. LPCD_IMin register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	LPCD_IMax.1	LPCD_IMax.0	LPCD_IMin					
Access rights	r/w	r/w	r/w					

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Table 183. LPCD_IMin bits

Bit	Symbol	Description
7 to 6	LPCD_IMax	Lowest two bits of the I-channel upper threshold.
5 to 0	LPCD_IMin	I-channel lower threshold. Falling below the threshold raises an LPCD interrupt.

9.14.4 LPCD_Result_I

Table 184. LPCD_Result_I register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	RFU	LPCD_Result_I					
Access rights	-	-	r					

Table 185. LPCD_I_Result bits

Bit	Symbol	Description
7 to 6	RFU	Reserved for future use.
5 to 0	LPCD_Result_I	Result of the most recent LPCD measurement on the I channel.

9.14.5 LPCD_Result_Q

Table 186. LPCD_Result_Q register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	LPCD_Irq_Clr	LPCD_Result_Q					
Access rights	-	r/w	r					

Table 187. LPCD_Q_Result bits

Bit	Symbol	Description
7	RFU	Reserved for future use.
6	LPCD_Irq_Clr	Suppresses further LPCD IRQ assertion until the next LPCD procedure and may be used to clear the interrupt source.
5 to 0	LPCD_Result_Q	Result of the most recent LPCD measurement on the Q channel.

9.15 Pin configuration

9.15.1 PinEn

Table 188. PinEn register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	SIGIN_EN	CLKOUT_EN	IFSEL1_EN	IFSEL0_EN	TCK_EN	TMS_EN	TDI_EN	TDO_EN
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 189. PinEn bits

Bit	Symbol	Description
7	SIGIN_EN	Enables output functionality on SIGIN.
6	CLKOUT_EN	Enables output functionality on CLKOUT and disables the normal clock-output function.
5	IFSEL1_EN	Enables output functionality on IFSEL1.
4	IFSEL0_EN	Enables output functionality on IFSEL0.
3	TCK_EN	Enables output functionality on TCK; ignored when boundary scan is enabled in EEPROM.
2	TMS_EN	Enables output functionality on TMS; ignored when boundary scan is enabled in EEPROM.

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Bit	Symbol	Description
1	TDI_EN	Enables output functionality on TDI; ignored when boundary scan is enabled in EEPROM.
0	TDO_EN	Enables output functionality on TDO; ignored when boundary scan is enabled in EEPROM.

9.15.2 PinOut

Table 190. PinOut register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	SIGIN_OUT	CLKOUT_OUT	IFSEL1_OUT	IFSEL0_OUT	TCK_OUT	TMS_OUT	TDI_OUT	TDO_OUT
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 191. PinOut bits

Bit	Symbol	Description
7	SIGIN_OUT	Output buffer value for the SIGIN pin.
6	CLKOUT_OUT	Output buffer value for the CLKOUT pin.
5	IFSEL1_OUT	Output buffer value for the IFSEL1 pin.
4	IFSEL0_OUT	Output buffer value for the IFSEL0 pin.
3	TCK_OUT	Output buffer value for the TCK pin.
2	TMS_OUT	Output buffer value for the TMS pin.
1	TDI_OUT	Output buffer value for the TDI pin.
0	TDO_OUT	Output buffer value for the TDO pin.

9.15.3 PinIn

Table 192. PinIn register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	SIGIN_IN	CLKOUT_IN	IFSEL1_IN	IFSEL0_IN	TCK_IN	TMS_IN	TDI_IN	TDO_IN
Access rights	r	r	r	r	r	r	r	r

Table 193. PinIn bits

Bit	Symbol	Description
7	SIGIN_IN	Input buffer value for the SIGIN pin.
6	CLKOUT_IN	Input buffer value for the CLKOUT pin.
5	IFSEL1_IN	Input buffer value for the IFSEL1 pin.
4	IFSEL0_IN	Input buffer value for the IFSEL0 pin.
3	TCK_IN	Input buffer value for the TCK pin.
2	TMS_IN	Input buffer value for the TMS pin.
1	TDI_IN	Input buffer value for the TDI pin.
0	TDO_IN	Input buffer value for the TDO pin.

9.15.4 SigOut

Table 194. SigOut register (address 47h)

Bit	7	6	5	4	3	2	1	0
Symbol	PadSpeed	RFU			SigOutSel			
Access rights	r/w	-			r/w			

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Table 195. SigOut bits

Bit	Symbol	Description
7	PadSpeed	Enables fast I/O switching. This increases peak current and the supply must support simultaneous switching currents.
6 to 4	RFU	Reserved for future use.
3 to 0	SigOutSel	0h, 1h: high impedance. 2h: logic 0. 3h: logic 1. 4h: TX envelope. 5h: TX active. 6h: S3C/generic signal. 7h: RX envelope (ISO/IEC 14443A, 106 kBd only). 8h: RX active. 9h: RX bit signal.

9.16 Protocol configuration registers

9.16.1 TxBitMod

Table 196. TxBitMod register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	TxMSBFirst	RFU	TxParityType	RFU	TxStopBitType	RFU	TxStartBitType	TxStartBitEn
Access rights	r/w	-	r/w	-	r/w	-	r/w	r/w

Table 197. TxBitMod bits

Bit	Symbol	Description
7	TxMSBFirst	1: transmit bytes MSB first. 0: transmit bytes LSB first.
6	RFU	Reserved for future use.
5	TxParityType	1: odd parity. 0: even parity.
4	RFU	Reserved for future use.
3	TxStopBitType	Defines the stop-bit level: 0 for logic low, 1 for logic high.
2	RFU	Reserved for future use.
1	TxStartBitType	Defines the start-bit level: 0 for logic low, 1 for logic high.
0	TxStartBitEn	When set, a start bit is transmitted.

9.16.2 TxDataCon

Table 198. TxDataCon register (address 4Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	DCodeType				DSCFreq	DBFreq		
Access rights	r/w				r/w	r/w		

Table 199. TxDataCon bits

Bit	Symbol	Description
7 to 4	DCodeType	0h: no special coding. 1h: collider data stream decoded. 2h, 3h: RFU. 4h to 7h: return-to-zero pulse at positions 1 to 4. 8h: 1-out-of-4 coding. 9h: 1-out-of-256, range 0 to 255 (ICODE SLI). Ah: 1-out-of-256; 00h has no modulation and value 256 is unused. Bh: 1-out-of-256; 00h uses a pulse in the last position. Ch: pulse-interval encoding for ISO/IEC 18000-3 mode 3 / EPC Class-1 HF. Dh to Fh: RFU.

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Bit	Symbol	Description
3	DSCFreq	Subcarrier frequency: 0 = 424 kHz, 1 = 848 kHz. Relevant only when the selected envelope uses a subcarrier.
2 to 0	DBFreq	0h, 1h: RFU. 2h: 26 kHz. 3h: 53 kHz. 4h: 106 kHz. 5h: 212 kHz. 6h: 424 kHz. 7h: 848 kHz.

9.16.3 TxDataMod

Table 200. TxDataMod register (address 4Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	FrameStep	DMillerEn	DPulseType		DInvert	DEnvType		
Access rights	r/w	r/w	r/w		r/w	r/w		

Table 201. TxDataMod bits

Bit	Symbol	Description
7	FrameStep	1: each byte is transmitted as a separate framed unit. 0: the complete FIFO data stream is framed once.
6	DMillerEn	Enables modified Miller pulse modulation; use with DPulseType = 1h.
5 to 4	DPulseType	0h: no pulse modulation. 1h: pulse at start of bit. 2h: pulse at start of second half. 3h: pulse at start of third quarter.
3	DInvert	Inverts the data envelope when set.
2 to 0	DEnvType	0h: direct. 1h: Manchester. 2h: Manchester with subcarrier. 3h: BPSK. 4h: RZ pulse at beginning of second half. 5h: RZ pulse at beginning of bit. 6h, 7h: RFU.

9.16.4 TxSymFreq

Table 202. TxSymFreq register (address 4Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	S32SCFreq	S32BFreq			S10SCFreq	S10BFreq		
Access rights	r/w	r/w			r/w	r/w		

Table 203. TxSymFreq bits

Bit	Symbol	Description
7	S32SCFreq	Symbol2/3 subcarrier: 0 = 424 kHz, 1 = 848 kHz.
6 to 4	S32BFreq	Symbol2/3 bit rate: 000b,001b RFU; 010b 26 kHz; 011b 53 kHz; 100b 106 kHz; 101b 212 kHz; 110b 424 kHz; 111b 848 kHz.
3	S10SCFreq	Symbol0/1 subcarrier: 0 = 424 kHz, 1 = 848 kHz.
2 to 0	S10BFreq	Symbol0/1 bit rate: 000b,001b RFU; 010b 26 kHz; 011b 53 kHz; 100b 106 kHz; 101b 212 kHz; 110b 424 kHz; 111b 848 kHz.

9.16.5 TxSym0

TxSym0H and TxSym0L form the 16-bit Symbol0 pattern.

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9.16.5.1 TxSym0H

Table 204. TxSym0H register (address 4Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	TxSym0H							
Access rights	r/w							

Table 205. TxSym0H bits

Bit	Symbol	Description
7 to 0	Symbol0_H	Higher eight bits of the Symbol0 definition.

9.16.5.2 TxSym0L

Table 206. TxSym0L register (address 4Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	TxSym0L							
Access rights	r/w							

Table 207. TxSym0L bits

Bit	Symbol	Description
7 to 0	Symbol0_L	Lower eight bits of the Symbol0 definition.

9.16.6 TxSym1

TxSym1H and TxSym1L form the 16-bit Symbol1 pattern.

9.16.6.1 TxSym1H

Table 208. TxSym1H register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	TxSym1H							
Access rights	r/w							

Table 209. TxSym1H bits

Bit	Symbol	Description
7 to 0	Symbol1_H	Higher eight bits of the Symbol1 definition.

9.16.6.2 TxSym1L

Table 210. TxSym1L register (address 50h)

Bit	7	6	5	4	3	2	1	0
Symbol	TxSym1L							
Access rights	r/w							

Table 211. TxSym1L bits

Bit	Symbol	Description
7 to 0	Symbol1_L	Lower eight bits of the Symbol1 definition.

9.16.7 TxSym2

Table 212. TxSym2 register (address 51h)

Bit	7	6	5	4	3	2	1	0
Symbol	TxSym2							

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Access rights	r/w

Table 213. TxSym2 bits

Bit	Symbol	Description
7 to 0	Symbol2	Symbol2 definition.

9.16.8 TxSym3

Table 214. TxSym3 register (address 52h)

Bit	7	6	5	4	3	2	1	0
Symbol	TxSym3							
Access rights	r/w							

Table 215. TxSym3 bits

Bit	Symbol	Description
7 to 0	Symbol3	Symbol3 definition.

9.16.9 TxSym10Len

Table 216. TxSym10Len register (address 53h)

Bit	7	6	5	4	3	2	1	0
Symbol	Sym1Len				Sym0Len			
Access rights	r/w				r/w			

Table 217. TxSym10Len bits

Bit	Symbol	Description
7 to 4	Sym1Len	Valid length of Symbol1: 1 bit (0h) to 16 bits (Fh).
3 to 0	Sym0Len	Valid length of Symbol0: 1 bit (0h) to 16 bits (Fh).

9.16.10 TxSym32Len

Table 218. TxSym32Len register (address 54h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	Sym3Len			RFU	Sym2Len		
Access rights	-	r/w			-	r/w		

Table 219. TxSym32Len bits

Bit	Symbol	Description
7	RFU	Reserved for future use.
6 to 4	Sym3Len	Valid length of Symbol3: 1 bit (0h) to 8 bits (7h).
3	RFU	Reserved for future use.
2 to 0	Sym2Len	Valid length of Symbol2: 1 bit (0h) to 8 bits (7h).

9.16.11 TxSym10BurstCtrl

Table 220. TxSym10BurstCtrl register (address 55h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	Sym1BurstType	Sym1BurstOnly	Sym1BurstEn	RFU	Sym0BurstType	Sym0BurstOnly	Sym0BurstEn
Access rights	-	r/w	r/w	r/w	-	r/w	r/w	r/w

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Table 221. TxSym10BurstCtrl bits

Bit	Symbol	Description
7	RFU	Reserved for future use.
6	Sym1BurstType	Logic level used by the Symbol1 burst.
5	Sym1BurstOnly	When set, Symbol1 contains only a burst and no symbol pattern.
4	Sym1BurstEn	Enables the Symbol1 burst with the length defined by TxSym10BurstLen.
3	RFU	Reserved for future use.
2	Sym0BurstType	Logic level used by the Symbol0 burst.
1	Sym0BurstOnly	When set, Symbol0 contains only a burst and no symbol pattern.
0	Sym0BurstEn	Enables the Symbol0 burst with the length defined by TxSym10BurstLen.

9.16.12 TxSym10Mod

Table 222. TxSym10Mod register (address 56h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	S10MillerEn	S10PulseType		S10Inv	S10EnvType		
Access rights	-	r/w	r/w		r/w	r/w		

Table 223. TxSym10Mod bits

Bit	Symbol	Description
7	RFU	Reserved for future use.
6	S10MillerEn	Enables modified Miller pulse modulation; use with S10PulseType = 1h.
5 to 4	S10PulseType	0h: no pulse modulation. 1h: pulse at start of bit. 2h: pulse at start of second half. 3h: pulse at start of third quarter.
3	S10Inv	Inverts Symbol0 and Symbol1.
2 to 0	S10EnvType	0h: direct. 1h: Manchester. 2h: Manchester with subcarrier. 3h: BPSK. 4h: RZ pulse at beginning of second half. 5h: RZ pulse at beginning of bit. 6h,7h: RFU.

9.16.13 TxSym32Mod

Table 224. TxSym32Mod register (address 57h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU	S32MillerEn	S32PulseType		S32Inv	S32EnvType		
Access rights	-	r/w	r/w		r/w	r/w		

Table 225. TxSym32Mod bits

Bit	Symbol	Description
7	RFU	Reserved for future use.
6	S32MillerEn	Enables modified Miller pulse modulation; use with S32PulseType = 1h.
5 to 4	S32PulseType	0h: no pulse modulation. 1h: pulse at start of bit. 2h: pulse at start of second half. 3h: pulse at start of third quarter.
3	S32Inv	Inverts Symbol2 and Symbol3.

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Bit	Symbol	Description
2 to 0	S32EnvType	0h: direct. 1h: Manchester. 2h: Manchester with subcarrier. 3h: BPSK. 4h: RZ pulse at beginning of second half. 5h: RZ pulse at beginning of bit. 6h,7h: RFU.

9.17 Receiver configuration

9.17.1 RxBitMod

Table 226. RxBitMod register (address 58h)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU		RxStopOnInvPar	RxStopOnLength	RxMSBFirst	RxStopBitEn	RxParityType	RFU
Access rights	-		r/w	r/w	r/w	r/w	r/w	-

Table 227. RxBitMod bits

Bit	Symbol	Description
7 to 6	RFU	Reserved for future use.
5	RxStopOnInvPar	Inverse parity is treated as a stop condition when set.
4	RxStopOnLength	Stops reception when the received byte count reaches the frame length given by the first data byte.
3	RxMSBFirst	1: receive bytes MSB first. 0: receive bytes LSB first.
2	RxStopBitEn	Enables stop-bit checking and extraction. An incorrect stop bit sets a frame error and aborts reception. The expected stop bit is logic 1.
1	RxParityType	0: even parity. 1: odd parity.
0	RFU	Reserved for future use.

9.17.2 RxEofSym

Table 228. RxEofSym register (address 59h)

Bit	7	6	5	4	3	2	1	0
Symbol	RxEOFSymbol							
Access rights	r/w							

Table 229. RxEofSym bits

Bit	Symbol	Description
7 to 0	RxEOFSymbol	Defines an EOF pattern of up to four bits. Each two-bit tuple represents one symbol bit: 0h = no bit/end, 1h = zero, 2h = one, 3h = collision. The least-significant tuple is evaluated first. If bits 1:0 are 00, EOF detection is disabled. Example: 1Dh = zero-collision-zero; E8h = disabled because bits 1:0 are zero.

9.17.3 RxSyncValH

Table 230. RxSyncValH register (address 5Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	RxSyncValH							
Access rights	r/w							

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Table 231. RxSyncValH bits

Bit	Symbol	Description
7 to 0	RxSyncValH	High byte of the start-of-frame synchronization pattern.

9.17.4 RxSyncValL

Table 232. RxSyncValL register (address 5Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	RxSyncValL							
Access rights	r/w							

Table 233. RxSyncValL bits

Bit	Symbol	Description
7 to 0	RxSyncValL	Low byte of the start-of-frame synchronization pattern.

9.17.5 RxSyncMod

Table 234. RxSyncMod register (address 5Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	SyncLen				SyncNegEdge	LastSyncHalf	SyncType	
Access rights	r/w				r/w	r/w	r/w	

Table 235. RxSyncMod bits

Bit	Symbol	Description
7 to 4	SyncLen	Number of valid bits in RxSyncValH/L. Set to 0 for ISO/IEC 14443B.
3	SyncNegEdge	For SOF without a correlation peak, the first negative correlation edge defines the bit grid.
2	LastSyncHalf	The last synchronization bit has half the normal length; used by ISO/IEC 18000-3 mode 3 / EPC Class-1 HF.
1 to 0	SyncType	0: all 16 SyncVal bits form a burst. 1: each nibble encodes one data/collision bit. 2: synchronize at every byte start bit (Type B). 3: RFU.

9.17.6 RxMod

Table 236. RxMod register (address 5Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	RFU		PreFilter	RectFilter	SyncHigh	CorrInv	FSK	BPSK
Access rights	-		r/w	r/w	r/w	r/w	r/w	r/w

Table 237. RxMod bits

Bit	Symbol	Description
7 to 6	RFU	Reserved for future use.
5	PreFilter	Averages four samples into one value when set.
4	RectFilter	Shapes ADC values toward a rectangular waveform when set.
3	SyncHigh	Selects correlation maximum (1) or minimum (0) as the bit-grid reference.
2	CorrInv	Manchester correlation polarity control.
1	FSK	Enables FSK demodulation.
0	BPSK	Enables BPSK demodulation.

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9.17.7 RxCorr

Table 238. RxCorr register (address 5Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	CorrFreq		CorrSpeed		CorrLen	RFU		
Access rights	r/w		r/w		r/w	-		

Table 239. RxCorr bits

Bit	Symbol	Description
7 to 6	CorrFreq	0h: 212 kHz. 1h: 424 kHz. 2h: 848 kHz. 3h: 848 kHz.
5 to 4	CorrSpeed	0h: ISO/IEC 14443. 1h: ICODE 53 kBd / FeliCa 424 kBd. 2h: ICODE 26 kBd / FeliCa 212 kBd. 3h: RFU.
3	CorrLen	0: 64 correlation values. 1: 32 values, used by ISO/IEC 18000-3 mode 3 / EPC Class-1 HF and two-pulse Manchester at 848 kHz subcarrier.
2 to 0	RFU	Reserved for future use.

9.17.8 FabCali

Table 240. FabCali register (address 5Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	FabCali							
Access rights	r/w							

Table 241. FabCali bits

Bit	Symbol	Description
7 to 0	FabCali	Receiver fabrication calibration. Do not change the boot value.

9.18 Version register

9.18.1 Version

Table 242. Version register (address 7Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	Version					SubVersion		
Access rights	r					r		

10 Limiting values

Table 244. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		-0.5	+5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage		-0.5	+5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage		-0.5	+5.5	V
$V_{i(RXP)}$	Input voltage on RXP		-0.5	+2.0	V

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Symbol	Parameter	Conditions	Min	Max	Unit
$V_{i(RXN)}$	Input voltage on RXN		-0.5	+2.0	V
P_{tot}	Total power dissipation	Per package	-	1125	mW
$V_{ESD(HBM)}$	Electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage	CDM	-	500	V
$T_{j(max)}$	Maximum junction temperature		-	150	° C

11 Recommended operating conditions

Table 245. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3	5	5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage	[1]	3	5	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage		3	5	5.5	V
T_{amb}	Ambient temperature		-25	-	+85	° C

12 Thermal characteristics

Table 246. Thermal characteristics

Symbol	Parameter	Conditions	Package	Typ	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	Still air; exposed pad soldered to a four-layer JEDEC PCB	HVQFN32	40	K/W

13 Characteristics

Table 247. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics - I/O pin characteristics, IF3-SDA in I²C configuration						
I_{LI}	Input leakage current	Output disabled	-	2	100	nA
V_{IL}	LOW-level input voltage		-0.5	-	$0.3V_{DD(PVDD)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$ + 0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.3	V

Table 247. Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; Standard/Fast mode	4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.6 V; Standard/Fast mode	6	-	-	mA
$t_{f(o)}$	Output fall time	Standard/Fast mode; C_L < 400 pF	-	-	250	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{f(o)}$	Output fall time	Fast-mode Plus; C_L < 550 pF	-	-	120	ns
t_{SP}	Input-filter spike suppression pulse width	-	0	-	50	ns
C_i	Input capacitance	-	-	3.5	5	pF
C_L	Load capacitance	Standard mode	-	-	400	pF
C_L	Load capacitance	Fast mode	-	-	550	pF
t_{EER}	EEPROM data-retention time	T_{amb} = +55 ° C	10	-	-	year
N_{EEC}	EEPROM endurance	All operating conditions	5×10^5	-	-	cycle
Analog and digital supply AVDD, DVDD						
V_{DDA}	Analog supply voltage	-	-	1.8	-	V
V_{DDD}	Digital supply voltage	-	-	1.8	-	V
C_L	Load capacitance	AVDD	220	470	-	nF
C_L	Load capacitance	DVDD	220	470	-	nF
Current consumption						
I_{stb}	Standby current	Standby bit = 1	-	3	6	μA
I_{DD}	Supply current	Modem on	-	17	20	mA
I_{DD}	Supply current	Modem off	-	0.45	0.5	mA
$I_{DD(TVDD)}$	TVDD supply current	-	-	100	200	mA
I/O pins SIGIN, SIGOUT, CLKOUT, IFSEL0/1, TCK, TMS, TDI, TDO, IRQ, IF0/1/2, SCL2 and SDA2						
I_{LI}	Input leakage current	Output disabled	-	50	500	nA
V_{IL}	LOW-level input voltage	-	-0.5	-	$0.3V_{DD(PVDD)}$	V
V_{IH}	HIGH-level input voltage	-	$0.7V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$ + 0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; $V_{DD(PVDD)}$ = 5.0 V	-	-	0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; $V_{DD(PVDD)}$ = 3.3 V	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OL} = 4 mA; $V_{DD(PVDD)}$ = 5.0 V	4.6	-	-	V
V_{OH}	HIGH-level output voltage	I_{OL} = 4 mA; $V_{DD(PVDD)}$ = 3.3 V	2.9	-	-	V
C_i	Input capacitance	-	-	2.5	4.5	pF
Pull-up resistance for TCK, TMS, TDI and IF2						
R_{pu}	Pull-up resistance	-	50	72	120	kΩ
Pin characteristics AUX1 and AUX2						
V_o	Output voltage	-	0	-	1.8	V
C_L	Load capacitance	-	-	-	400	pF
Pin characteristics RXP and RXN						
V_i	Input voltage	-	0	-	1.8	V
C_i	Input capacitance	-	2	3.5	5	pF
$V_{mod(pp)}$	Modulation voltage	$V_{i(pp)(max)} - V_{i(pp)(min)}$	-	2.5	-	mV
V_{pp}	Signal on RXP/RXN	-	-	-	1.65	V
Pins TX1 and TX2						
V_o	Output voltage	-	$V_{SS(TVSS)}$	-	$V_{DD(TVDD)}$	V
R_o	Output resistance	-	-	1.5	-	Ω
Current consumption						
I_{pd}	Power-down current	T_{amb} = 25 ° C	-	8	40	nA
I_{pd}	Power-down current	T_{amb} = 85 ° C	-	200	400	nA
I_{stby}	Standby current	T_{amb} = 25 ° C [1]	-	3	6	μA
I_{LPCD}	LPCD sleep current	[1]	-	3	6	μA
I_{DD}	Supply current	-	-	17	20	mA
I_{DD}	Supply current	Modem off; transceiver off	-	0.45	0.5	mA
$I_{DD(PVDD)}$	PVDD supply current	No load on digital pins [2]	-	-	10	μA
$I_{DD(TVDD)}$	TVDD supply current	[3][4][5]	-	100	200	mA
Clock frequency at CLKOUT						
f_{clk}	Clock frequency	Configured to 27.12 MHz	-	27.12	-	MHz
δ_{clk}	Clock duty cycle	-	-	50	-	%
Crystal oscillator						
$V_{o(p-p)}$	Peak-to-peak output voltage	XTAL1	-	1	-	V
V_i	Input voltage	XTAL1	0	-	1.8	V
C_i	Input capacitance	XTAL1	-	3	-	pF
Typical crystal requirements						
f_{xtal}	Crystal frequency	-	-	27.12	-	MHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent series resistance	-	-	50	100	Ω
C_L	Load capacitance	-	-	10	-	pF
P_{xtal}	Crystal power dissipation	-	-	50	100	μW

[1] I_{pd} is the total current for all supplies. [2] $I_{DD(PVDD)}$ depends on the total load at the digital pins. [3] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external TX1/TX2 circuit. [4] Typical total current is below 100 mA. [5] Typical value uses a complementary driver and a 40 Ω matched antenna at 13.56 MHz.

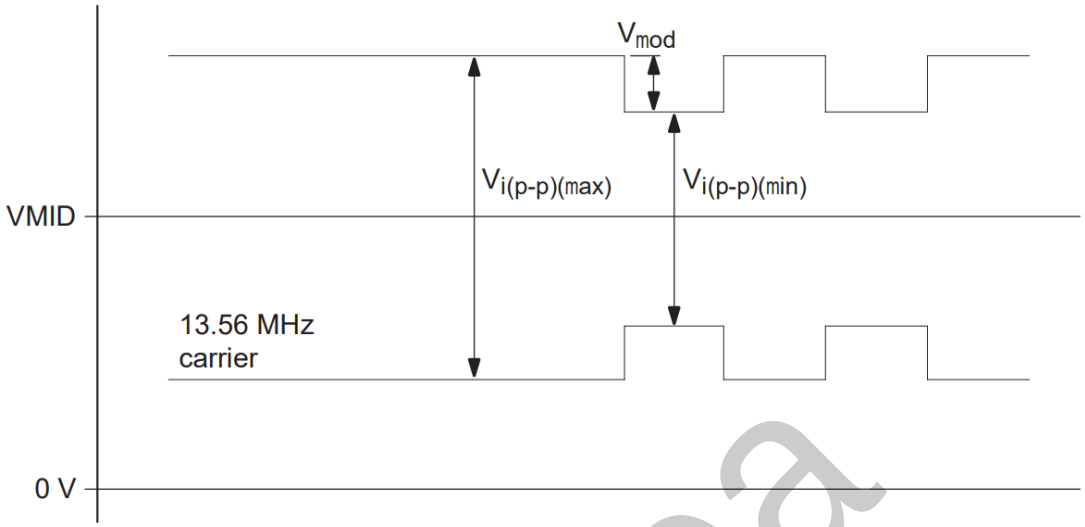


Figure 34. Pin RX input voltage

13.1 Timing characteristics

Table 248. SPI timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	-	50	-	-	ns
t_{SCKH}	SCK HIGH time	-	50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data-input hold time	SCK to changing MOSI	25	-	-	ns
$t_{su(D-SCKH)}$	Data-input to SCK HIGH set-up time	Changing MOSI to SCK	25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data-output hold time	SCK to changing MISO	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time	-	0	-	-	ns
t_{NSSH}	NSS HIGH time	Before communication	50	-	-	ns

Remark: Keep NSS LOW while sending multiple bytes in one data stream. Raise NSS between separate data streams.

Table 249. I²C-bus timing in Fast mode and Fast-mode Plus

Symbol	Parameter	Conditions	Fast mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	-	0	400	0	1000	kHz
$t_{HD;STA}$	Hold time for a repeated START condition	Before first clock pulse	600	-	260	-	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	-	600	-	260	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	-	600	-	260	-	ns
t_{LOW}	LOW period of SCL	-	1300	-	500	-	ns
t_{HIGH}	HIGH period of SCL	-	600	-	260	-	ns
$t_{HD;DAT}$	Data hold time	-	0	900	-	450	ns

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Symbol	Parameter	Conditions	Fast mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	
$t_{SU;DAT}$	Data set-up time	-	100	-	-	-	ns
t_r	Rise time	SCL signal	20	300	-	120	ns
t_f	Fall time	SCL signal	20	300	-	120	ns
t_r	Rise time	SDA and SCL signals	20	300	-	120	ns
t_f	Fall time	SDA and SCL signals	20	300	-	120	ns
t_{BUF}	Bus free time between STOP and START	-	1.3	-	0.5	-	μs

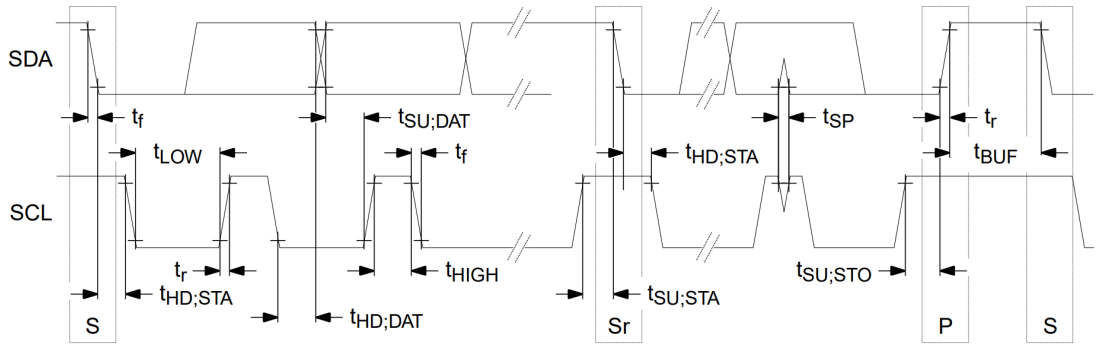


Figure 35. Timing for fast and standard mode devices on the I²C-bus

14 Application information

Figure 36 shows a typical complementary antenna connection for the NF663E. Antenna tuning and RF matching are described in the referenced application notes.

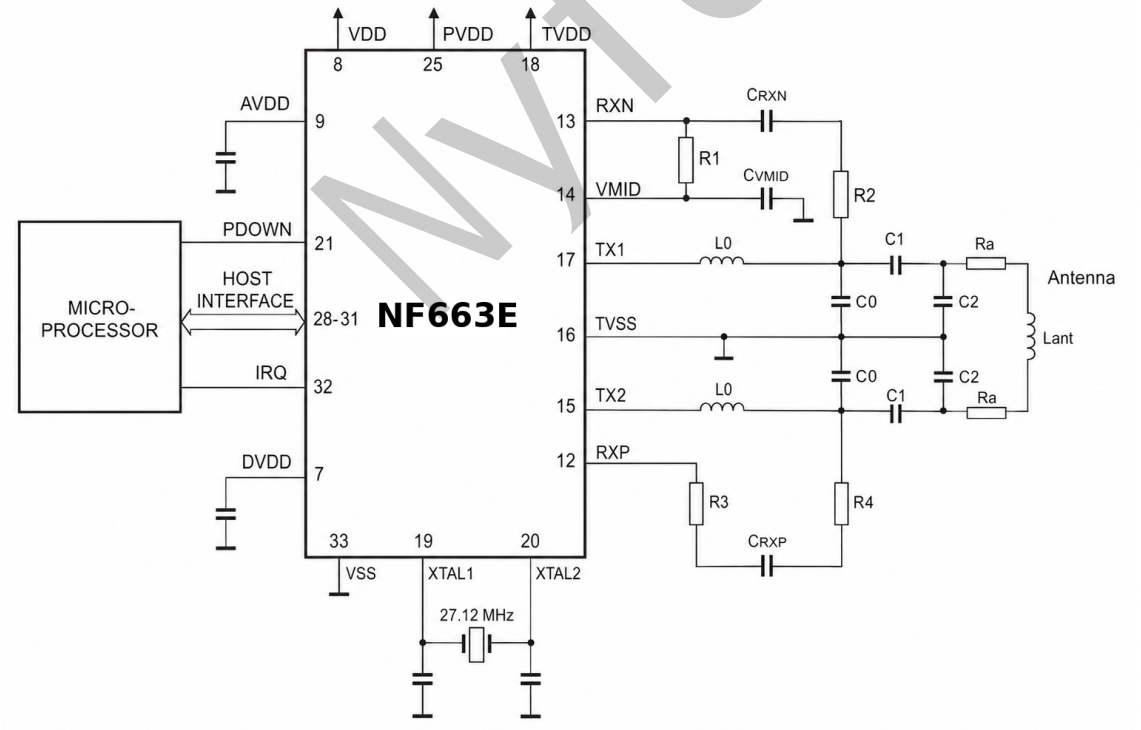


Figure 36. Typical application antenna circuit diagram

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14.1 Antenna design description

The antenna interface contains an EMI suppression stage (L0/C0), an impedance-transformation network (C1/C2), balanced receive-path components and the antenna element. Receiver component values must be selected for the NF663E; reusing values intended for a different reader IC without adjustment can reduce performance.

14.1.1 EMC low-pass filter

The 13.56 MHz transmit carrier also generates harmonic components. The output filter must attenuate these components sufficiently to meet EMC emission limits. PCB layout has a major influence on filter performance.

14.1.2 Antenna matching

The antenna coil is tuned to a defined impedance through the output filter and matching network. Initial values can be calculated and then optimized experimentally for the actual coil geometry. The loaded Q factor, EMC behavior and installation environment must be considered together.

14.1.3 Receiving circuit

The differential RXP/RXN receiver extracts information from both sidebands of the load-modulated subcarrier. The internally generated VMID voltage should bias the receiver inputs through R2 and R4; C4 and C6 provide a stable AC ground reference. The R/C divider in each receive branch must keep the input swing within the specified RXP/RXN limits.

14.1.4 Antenna coil

A circular or rectangular antenna can be estimated with the formula shown below. Because the original formula is complex, it is retained as a cropped vector-like source image rather than reconstructed with unreliable HTML glyph positioning.

$$L_1 = 2 \cdot I_1 \cdot \left(\ln\left\langle \frac{I_1}{D_1} \right\rangle + -K \right) N_1^{1,8}$$

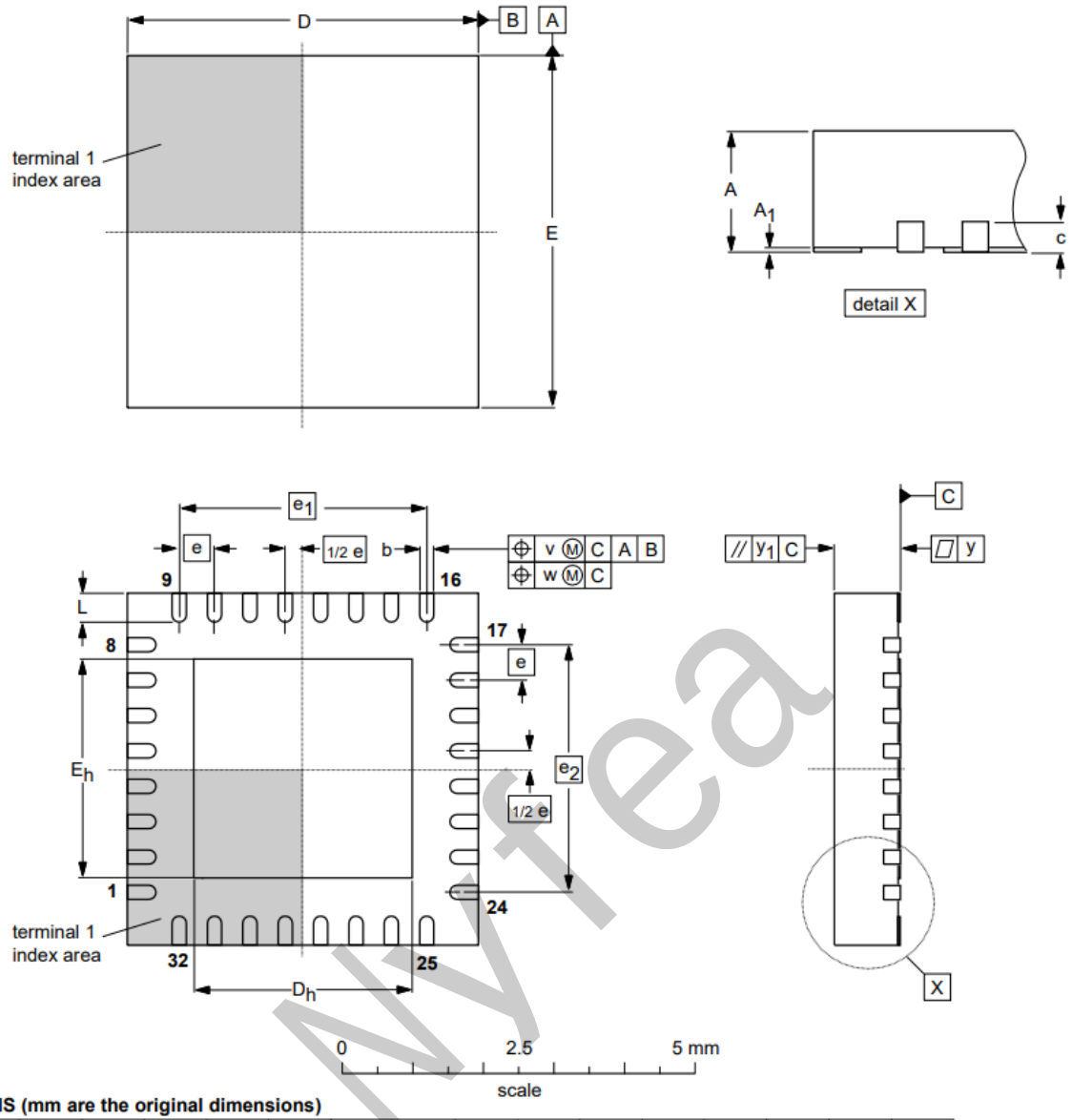
- I_1: length of one conductor-loop turn in cm
- D_1: conductor diameter or PCB trace width
- K: antenna shape factor, approximately 1.07 for circular antennas and 1.47 for square antennas
- L_1: inductance in nH
- N_1: number of turns
- ln: natural logarithm

The actual inductance, resistance and capacitance at 13.56 MHz also depend on PCB construction, conductor thickness, winding spacing, shielding and nearby metal or ferrite. Measurements should therefore be verified in the intended operating environment.

15 Package outline

HVQFN32: plastic thermal-enhanced very-thin quad-flat package; no leads; 32 terminals; 5 mm × 5 mm × 0.85 mm body; SOT617-1.

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DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	---	MO-220	---			

Figure 37. Package outline SOT617-1 (HVQFN32)

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16 Handling information

Moisture Sensitivity Level evaluation is performed in accordance with JEDEC J-STD-020. The HVQFN32 package is specified as MSL 2 with a 260 ° C convection-reflow temperature.

- MSL 2: dry pack required; one-year out-of-pack floor life at up to 30 ° C and 85% RH.
- MSL 1: no dry pack and no floor-life limitation.

17 Packing information

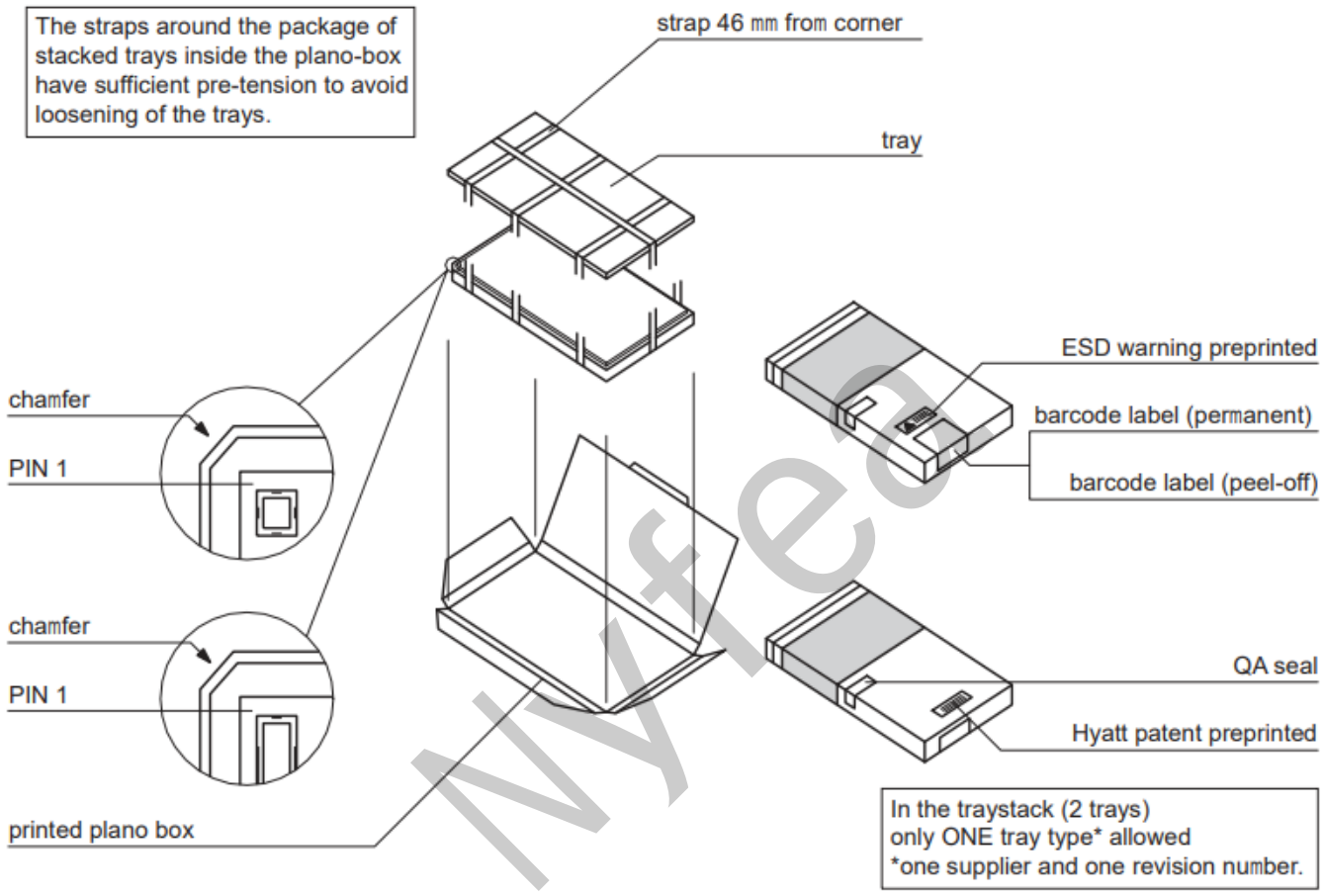


Figure 38. Packing information – 1 tray

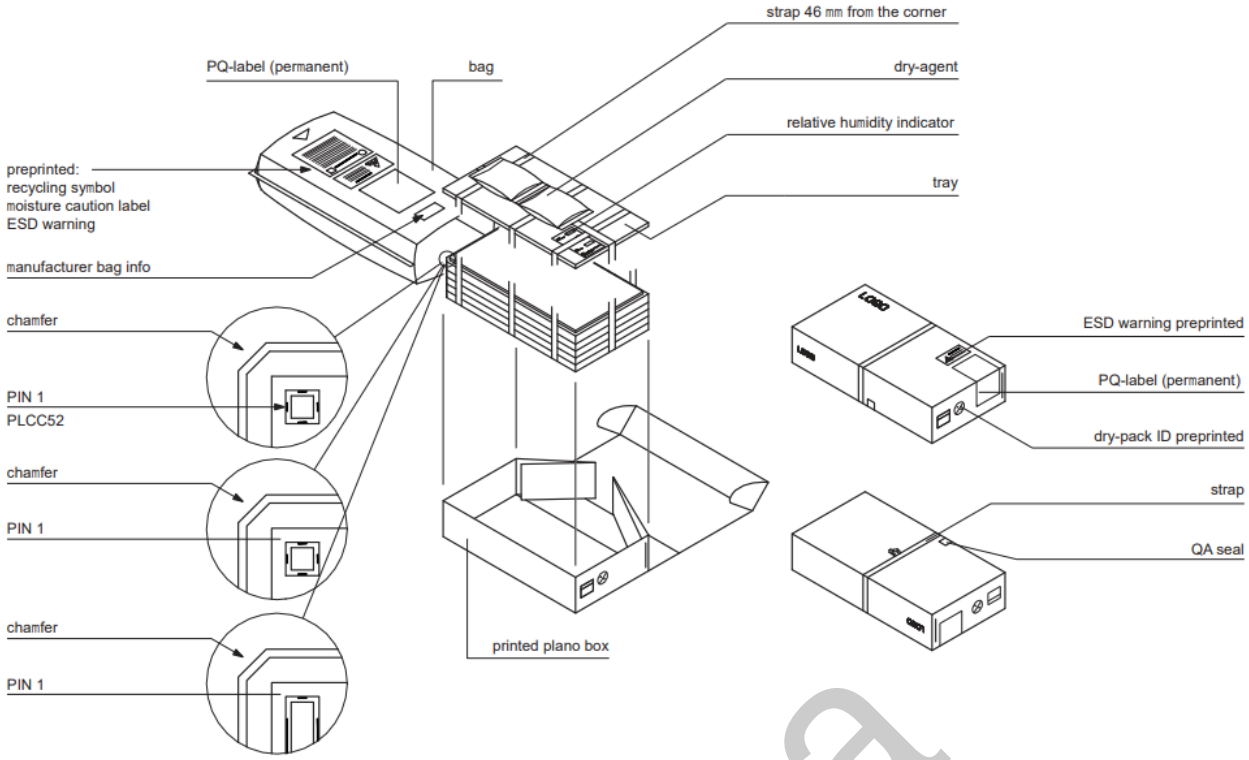


Figure 39. Packing information – 5 trays

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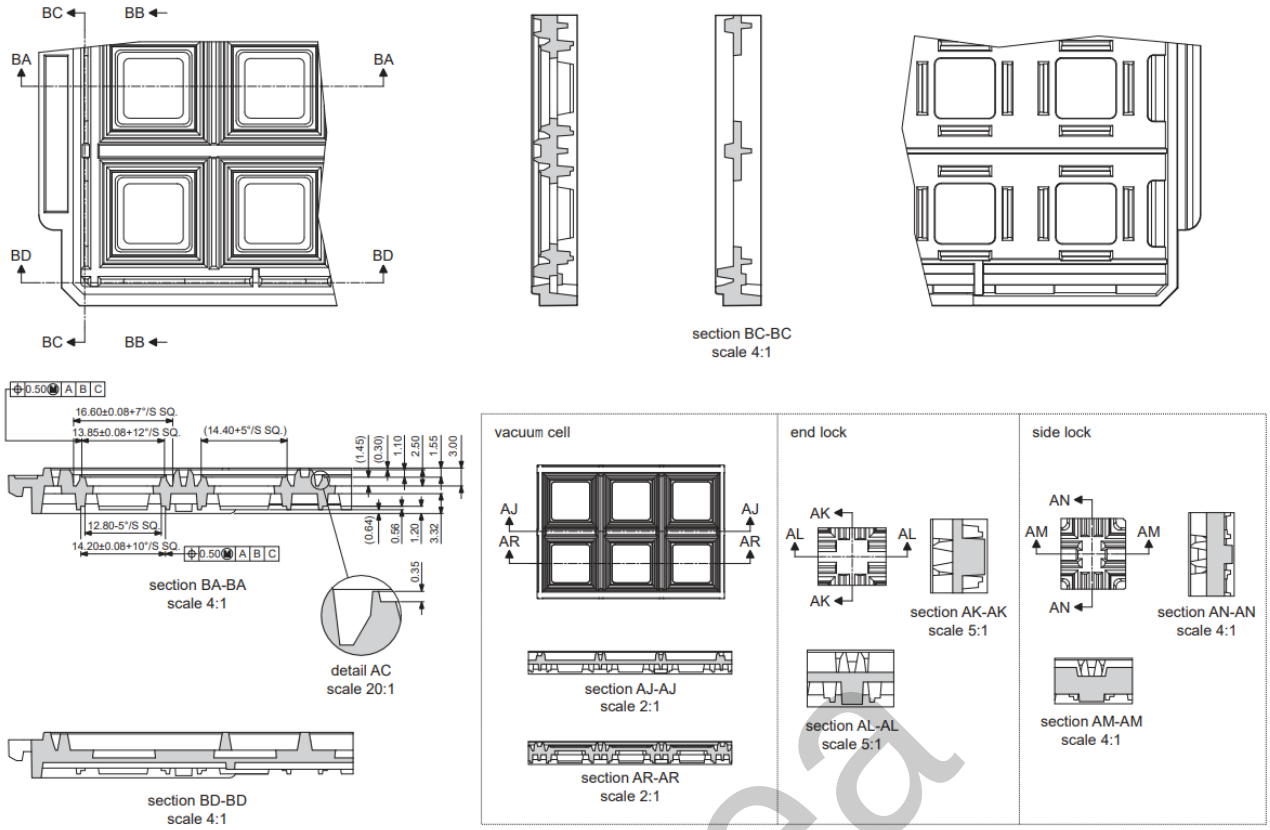


Figure 40. Tray details

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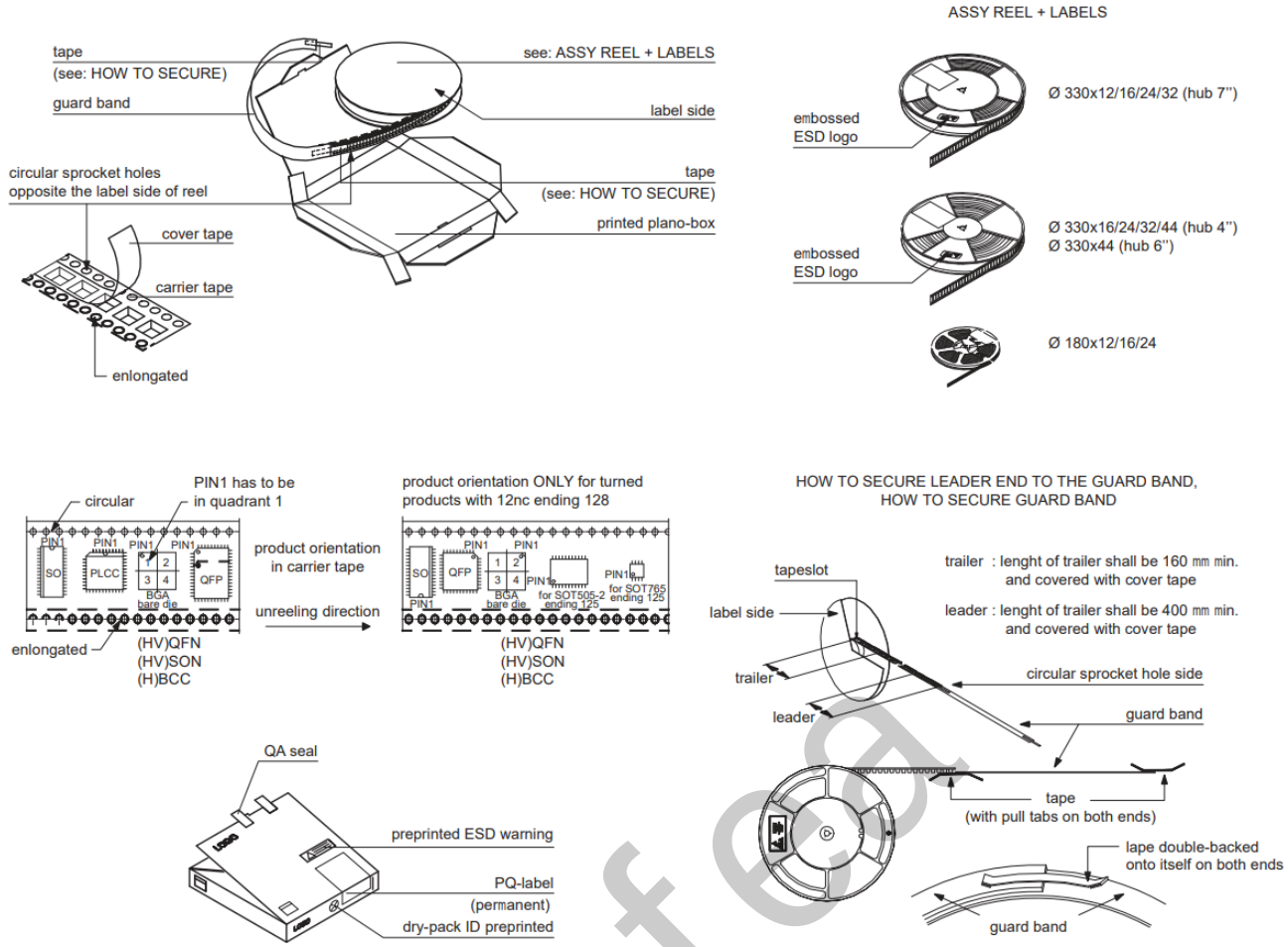


Figure 41. Reel, carrier-tape and guard-band packing information

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