

## Small Size, 12-bit 3 MSPS SAR ADC

### Features

- 12-Bit ADCs, no Missing Code
- Throughput: 3 MSPS
- INL:  $\pm 0.7$  LSB
- DNL:  $\pm 0.6$  LSB
- SNR: 72.5 dB
- SINAD: 72 dB
- Single-ended Input Range: 0 V  $\sim$   $V_{DD}$
- No Pipeline Delay
- Single Supply: 2.7 V to 3.6 V
- Packages: TSOT23-6
- Operating Temperature Range: -40 °C to +125 °C

### Applications

- Data Acquisition
- Automated Testing
- Precision Instrument
- Medical Instrument

### General Description

ZJC2039 is high speed, low power consumption, 12-bit single-ended input SAR ADC with throughput up to 3 MSPS. The part is available in small package and easy to use. It can reduce the power consumption and complexity of the system, thus achieve high density designs.

ZJC2039 requires single power supply to sample the analog input voltage IN up to  $V_{DD}$ , which is also used as the reference voltage. Depending on  $V_{DD}$ , the ZJC2039 can be compatible with logic interface at  $V_{DD}$  level. The part provides one SPI-compatible serial port.

ZJC2039 is available in 6-lead TSOT23. The operating temperature is -40 °C to +125 °C.

### Typical Application

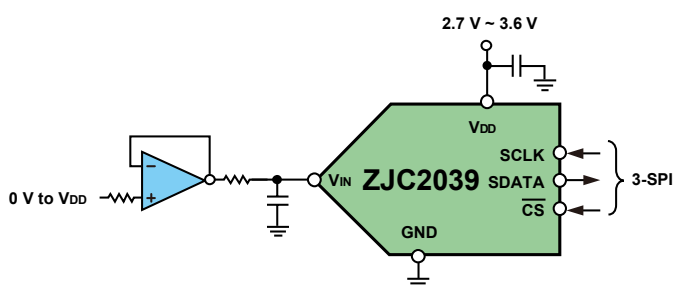


Figure 1. Application Examples

### Typical Characteristics

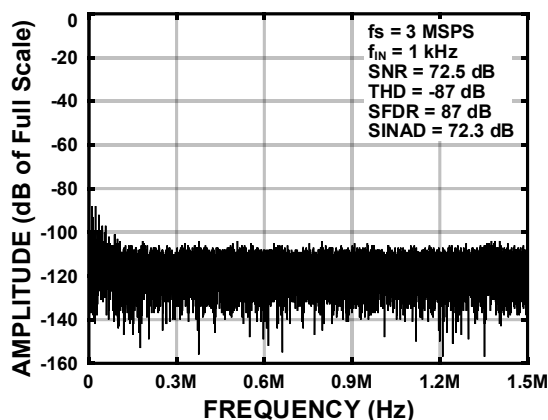


Figure 2. FFT vs. Frequency\_  $V_{DD}$  (3.3 V)

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**Version (Release A)<sup>1</sup>**

**Jun. 2026 — Release A**

Jan. 2026 — Preliminary

Changes to Single Supply, Typical Performance Characteristics and  $V_{DD}$  to GND.

Apr. 2025 — Initial

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Pin Configurations and Function Descriptions

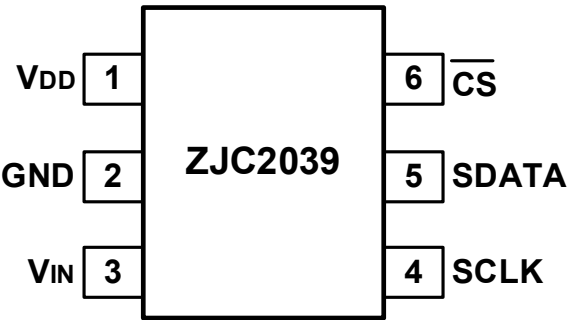


Figure 3. 6-lead TSOT23 Pin Configuration

| Mnemonic               | Pin No.  | I/O <sup>1</sup> | Description                                                                                                                                                                                                                                                                                                      |
|------------------------|----------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                        | TSOT23-6 |                  |                                                                                                                                                                                                                                                                                                                  |
| V <sub>DD</sub>        | 1        | P                | Power Supply pin. V <sub>DD</sub> ranges from 2.7 V to 3.6 V functionally. It is recommended that V <sub>DD</sub> be bypassed through at least a 100 nF ceramic capacitors to GND. It is also used for ADC internal reference voltage, so it should be made clean and accurate for low noise performance.        |
| GND                    | 2        | G                | Power Ground.                                                                                                                                                                                                                                                                                                    |
| V <sub>IN</sub>        | 3        | AI               | Single-ended analog input channel. The input range is 0 V to V <sub>DD</sub> .                                                                                                                                                                                                                                   |
| SCLK                   | 4        | DI               | Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process of ZJC2039.                                                                                                                             |
| SDATA                  | 5        | DO               | Data Out. Logic output. The conversion result from the ZJC2039 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the ZJC2039 consists of two leading zeros followed by 12 bits of conversion data and two trailing zeros. |
| $\overline{\text{CS}}$ | 6        | DI               | Chip Select. Active low logic input. This input provides the dual function of initiating conversion and framing the serial data transfer.                                                                                                                                                                        |

<sup>1</sup> DI/O: Digital Input/Output.; G: Ground; P: Power; AI: Analog Input.

Absolute Maximum Ratings <sup>1</sup>

| Parameter                                  | Rating                           |
|--------------------------------------------|----------------------------------|
| V <sub>DD</sub> to GND                     | -0.3 V ~ 3.8 V                   |
| Analog Input Range                         | -0.3 V ~ V <sub>DD</sub> + 0.3 V |
| Digital Input to GND                       | -0.3 V ~ 3.8 V                   |
| Digital Output to GND                      | -0.3 V ~ V <sub>DD</sub> + 0.3 V |
| Storage Temperature Range                  | -65 °C to +150 °C                |
| Input Current to Any Pin Except Supplies   | ±10 mA                           |
| Junction Temperature Range                 | 150 °C                           |
| Lead Temperature (Soldering, 10 seconds)   | 300 °C                           |
| Maximum Reflow Temperature <sup>2</sup>    | 260 °C                           |
| Electrostatic Discharge (ESD) <sup>3</sup> |                                  |
| Human Body Model (HBM) <sup>4</sup>        | 3 kV                             |
| CDM                                        | 2 kV                             |

Thermal Resistance <sup>6</sup>

| Package Type  | θ <sub>JA</sub> | θ <sub>JC</sub> | Unit |
|---------------|-----------------|-----------------|------|
| 6-lead TSOT23 | 230             | 92              | °C/W |

<sup>1</sup> These ratings apply at 25 °C, unless otherwise noted.  
Stresses above these ratings may cause permanent damage.  
Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

<sup>2</sup> IPC/JEDECJ-STD-020 Compliant.

<sup>3</sup> Charged devices and circuit boards can discharge without detection.

Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

<sup>4</sup> ANSI/ESDA/JEDEC JS-001 Compliant.

<sup>6</sup> θ<sub>JA</sub> addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

## Specifications

The ● denotes the full temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) for specified performance. Unless otherwise noted,  $V_{\text{DD}} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$ ,  $f_{\text{SCLK}} = 48\text{ MHz}$ ,  $f_{\text{SAMPLE}} = 3\text{ MSPS}$ .

| Parameter                       | Symbol          | Conditions                                            |   | Min                   | Typ. | Max                   | Unit             |
|---------------------------------|-----------------|-------------------------------------------------------|---|-----------------------|------|-----------------------|------------------|
| Dynamic Performance             |                 | f <sub>IN</sub> = 1 kHz Sine Wave                     |   |                       |      |                       |                  |
| Signal-to-Noise                 | SNR             |                                                       | ● | 71                    | 72.5 |                       | dB               |
| Signal-to-(Noise + Distortion)  | SINAD           |                                                       | ● | 70.5                  | 72   |                       | dB               |
| Total Harmonic Distortion       | THD             |                                                       |   |                       | -83  |                       | dB               |
| Spurious-free Dynamic Range     | SFDR            |                                                       |   |                       | 85   |                       | dB               |
| Full Power Bandwidth            |                 | @ -3 dB                                               |   |                       | 45   |                       | MHz              |
| DC Accuracy                     |                 |                                                       |   |                       |      |                       |                  |
| Resolution                      |                 |                                                       | ● | 12                    |      |                       | bits             |
| Integral Nonlinear Error        | INL             |                                                       | ● | -1.5                  | ±0.7 | 1.5                   | LSB <sup>1</sup> |
| Differential Nonlinear Error    | DNL             | Guaranteed no missed codes to 12 bits                 | ● | -0.99                 | ±0.6 | 0.99                  | LSB              |
| Offset Error                    | ZE              |                                                       | ● | -1.5                  |      | 1.5                   | LSB              |
| Gain Error Temperature Drift    |                 |                                                       | ● | -1.5                  |      | 1.5                   | LSB              |
| Analog Input                    |                 |                                                       |   |                       |      |                       |                  |
| Input Voltage Ranges            |                 |                                                       |   | 0                     |      | V <sub>DD</sub>       | V                |
| DC Leakage Current              |                 | -40 °C to +85 °C                                      | ● |                       |      | 1                     | μA               |
|                                 |                 | 85 °C to +125 °C                                      | ● |                       |      | 5                     | μA               |
| Input Capacitance               |                 | Sampling                                              |   |                       | 32   |                       | pF               |
|                                 |                 | Holding                                               |   |                       | 10   |                       | pF               |
| Logic Inputs                    |                 |                                                       |   |                       |      |                       |                  |
| Logic Level                     | V <sub>IH</sub> | 2.7 V < V <sub>DD</sub> ≤ 3.6 V                       | ● | 0.7 × V <sub>DD</sub> |      |                       | V                |
|                                 | V <sub>IL</sub> | 2.7 V < V <sub>DD</sub> ≤ 3.6 V                       | ● |                       |      | 0.3 × V <sub>DD</sub> | V                |
| Input Current                   | I <sub>IN</sub> | V <sub>IN</sub> = 0 V or V <sub>DD</sub>              | ● | -1                    |      | 1                     | μA               |
| Input Capacitance               | C <sub>IN</sub> |                                                       |   |                       | 3    |                       | pF               |
| Logic Outputs                   |                 |                                                       |   |                       |      |                       |                  |
| Output High Voltage             | V <sub>OH</sub> | I <sub>SOURCE</sub> = 200 μA                          | ● | V <sub>DD</sub> - 0.2 |      |                       | V                |
| Output Low Voltage              | V <sub>OL</sub> | I <sub>SINK</sub> = 200 μA                            | ● |                       |      | 0.2                   | V                |
| Output Coding                   |                 | Straight (natural) Binary                             |   |                       |      |                       |                  |
| Conversion Rate                 |                 |                                                       |   |                       |      |                       |                  |
| Conversion Time                 |                 |                                                       | ● |                       |      | 290                   | ns               |
| Track-and-hold Acquisition Time |                 |                                                       | ● | 60                    |      |                       | ns               |
| Throughput Rate                 |                 |                                                       | ● |                       |      | 3                     | MSPS             |
| Power Requirements              |                 |                                                       |   |                       |      |                       |                  |
| V <sub>DD</sub>                 |                 |                                                       | ● | 2.7                   |      | 3.6                   | V                |
| I <sub>DD</sub>                 |                 |                                                       |   |                       |      |                       |                  |
| Normal Mode (Static)            |                 | V <sub>DD</sub> = 3.3 V, SCLK On or Off               |   |                       | 1.7  |                       | mA               |
| Full Power-Down Mode (Static)   |                 | 85 °C to 125 °C                                       | ● |                       |      | 2                     | μA               |
| Power Dissipation               |                 |                                                       |   |                       |      |                       |                  |
| Normal Mode (Operational)       |                 | V <sub>DD</sub> = 3.3 V, f <sub>SAMPLE</sub> = 3 MSPS |   |                       | 12.6 |                       | mW               |
| Full Power-Down                 |                 | V <sub>DD</sub> = 3.3 V;                              | ● |                       |      | 3.3                   | μW               |
| Temperature Range               |                 |                                                       |   |                       |      |                       |                  |
| Specified Performance           |                 | T <sub>MIN</sub> to T <sub>MAX</sub>                  |   | -40                   |      | +125                  | °C               |

<sup>1</sup> LSB means least significant bit. 1 LSB = 0.81 mV for 3.3 V input range.

## Timing Specifications

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise specified,  $T_A = 25\text{ °C}$ ,  $V_{DD} = 2.7\text{ V}$  to  $3.6\text{ V}$ .

| Parameter                                                                                                | Symbol        |   | Min                   | Typ.                 | Max | Unit |
|----------------------------------------------------------------------------------------------------------|---------------|---|-----------------------|----------------------|-----|------|
| SCLK Frequency                                                                                           | $f_{SCLK}$    | ● | 0.5                   |                      | 48  | MHz  |
| Convert Time                                                                                             | $t_{CONVERT}$ |   |                       | $14 \times t_{SCLK}$ |     | ns   |
| Quiet Time (Minimum quiet time required between the bus relinquish and the start of the next conversion) | $t_{QUIET}$   | ● | 5                     |                      |     | ns   |
| Minimum $\overline{CS}$ pulse width                                                                      | $t_1$         | ● | 5                     |                      |     | ns   |
| $\overline{CS}$ to SCLK setup time                                                                       | $t_2$         | ● | 6                     |                      |     | ns   |
| Delay from $\overline{CS}$ until SDATA three-state disabled                                              | $t_3$         | ● |                       |                      | 10  | ns   |
| Data access time after SCLK falling edge                                                                 | $t_4$         | ● |                       |                      | 15  | ns   |
| SCLK Low Pulse Width                                                                                     | $t_5$         | ● | $0.4 \times t_{SCLK}$ |                      |     | ns   |
| SCLK High Pulse Width                                                                                    | $t_6$         | ● | $0.4 \times t_{SCLK}$ |                      |     | ns   |
| SCLK to data valid hold time                                                                             | $t_7$         | ● | 3                     |                      |     | ns   |
| SCLK falling edge to SDATA three-state                                                                   | $t_8$         | ● | 5                     |                      | 15  | ns   |
| $\overline{CS}$ rising edge to SDATA three-state                                                         | $t_9$         | ● |                       |                      | 10  | ns   |

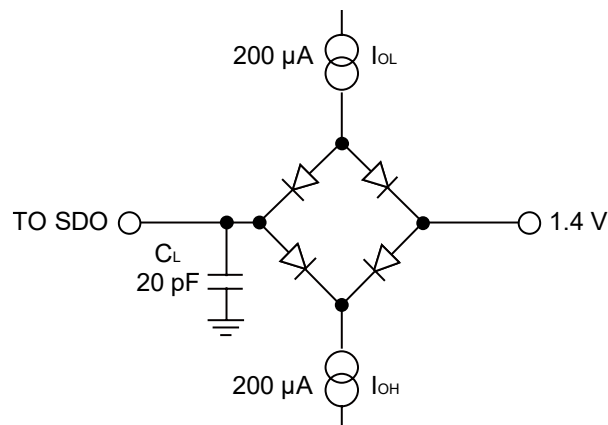


Figure 4. Load Circuit for Digital Interface Timing

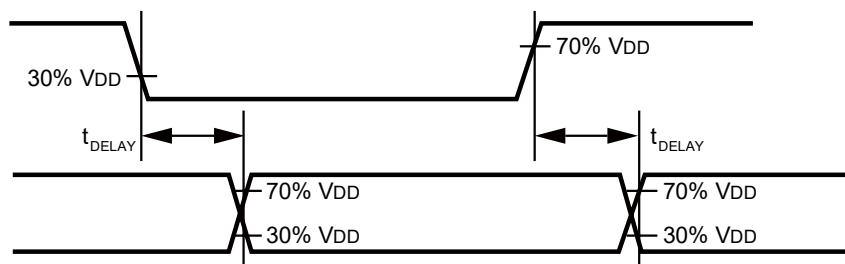
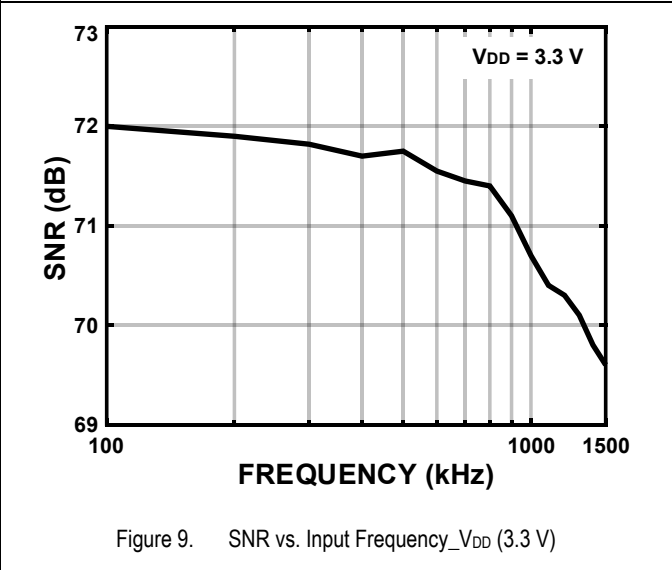
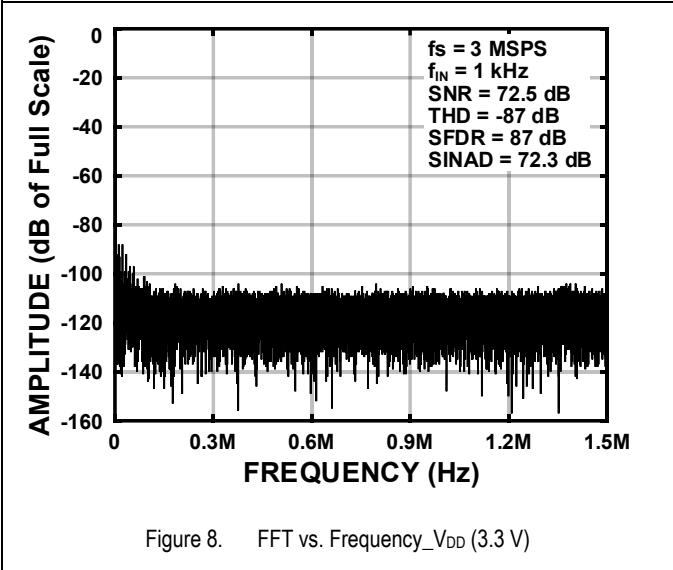
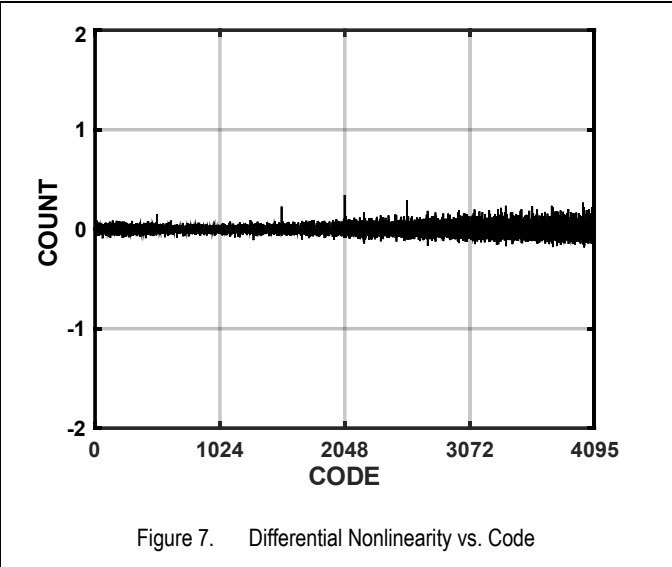
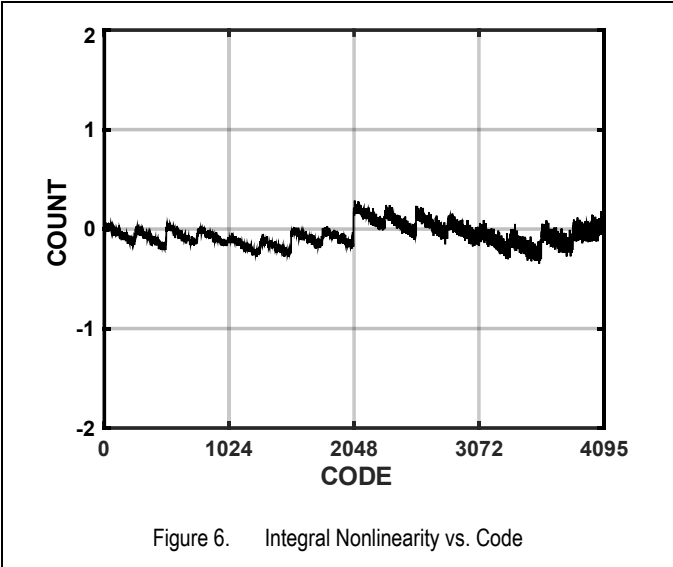


Figure 5. Voltage Levels for Digital Interface Timing

Typical Performance Characteristics

Unless otherwise noted,  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ .



Transfer Function

The ideal transfer function of ZJC2039 is shown in Figure 10.

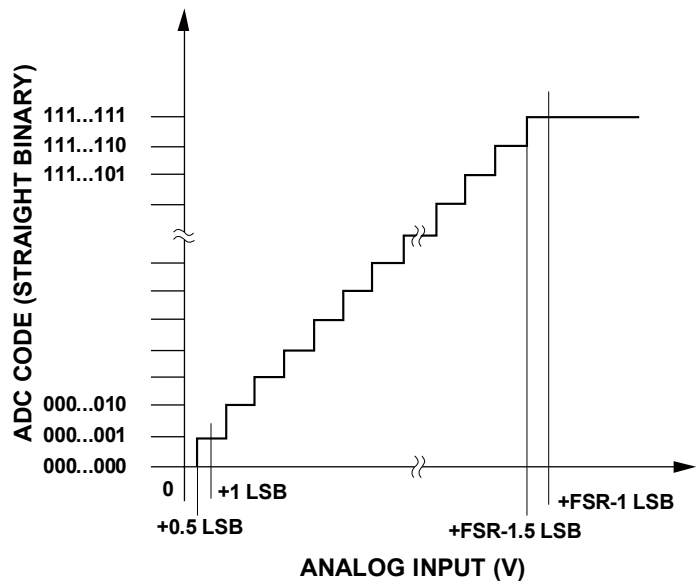


Figure 10. ADC ideal transfer function

Output Code and Ideal Input Voltage:

| Description      | Analog Input $V_{DD} = 3.3\text{ V}$ | Digital Output (Hex) |
|------------------|--------------------------------------|----------------------|
| FSR – 1 LSB      | 3.29919 V                            | 0xFFF <sup>1</sup>   |
| Midscale + 1 LSB | 1.65081 V                            | 0x801                |
| Midscale         | 1.65 V                               | 0x800                |
| ZSR + 1 LSB      | 0.81 mV                              | 0x001                |
| ZSR              | 0 V                                  | 0x000 <sup>2</sup>   |

<sup>1</sup> This is also the code for an over-range analog input ( $V_{IN}$  above  $V_{DD} - V_{GND}$ ).

<sup>2</sup> This is also the code for an under-ranged analog input ( $V_{IN}$  below  $V_{GND}$ ).

## Modes of Operation

The mode of operation of the ZJC2039 is selected by controlling the logic state of the  $\overline{CS}$  signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. The point at which  $\overline{CS}$  is pulled high after the conversion has been initiated determines which power-down mode, if any, the device enters. Similarly, if the device is already in power-down mode,  $\overline{CS}$  can control whether the device returns to normal operation or remains in power-down mode. These modes of operation are designed to provide flexible power management options, which can be chosen to optimize the power dissipation/ throughput rate ratio for different application requirements.

### Normal Mode

This mode is intended for fastest throughput rate performance because the device remains fully powered at all times, eliminating worry about power-up times.

The conversion is initiated on the falling edge of  $\overline{CS}$  as described in the Serial Interface section. To ensure that the part remains fully powered up at all times,  $\overline{CS}$  must remain low until at least 10 SCLK falling edges elapse after the falling edge of  $\overline{CS}$ . If  $\overline{CS}$  is brought high after the 10<sup>th</sup> SCLK falling edge but before the 16<sup>th</sup> SCLK falling edge, the part remains powered up, but the conversion is terminated and SDATA goes back into three-state.

$\overline{CS}$  can idle high until the next conversion or low until  $\overline{CS}$  returns high before the next conversion (effectively idling  $\overline{CS}$  low). Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time,  $t_{\text{QUIET}}$ , has elapsed by bringing  $\overline{CS}$  low again.

### Partial Power-Down Mode

To enter partial power-down mode, interrupt the conversion process by bringing  $\overline{CS}$  high between the second and 10<sup>th</sup> falling edges of SCLK.

Once  $\overline{CS}$  is brought high in this window of SCLKs, the part enters partial power-down mode, the conversion that was initiated by the falling edge of  $\overline{CS}$  is terminated, and SDATA goes back into three-state. If  $\overline{CS}$  is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This prevents accidental power-down due to glitches on the  $\overline{CS}$  line.

To exit this mode of operation and power up the ZJC2039, users should perform a dummy conversion. On the falling edge of  $\overline{CS}$ , the device begins to power up and continues to power up as long as  $\overline{CS}$  is held low until after the falling edge of the 10<sup>th</sup> SCLK. The device is fully powered up once 16 SCLKs elapse; valid data results from the next conversion. If  $\overline{CS}$  is brought high before the 10<sup>th</sup> falling edge of SCLK, the ZJC2039 goes into full power-down mode. Therefore, although the device can begin to power up on the falling edge of  $\overline{CS}$ , it powers down on the rising edge of  $\overline{CS}$  as long as this occurs before the 10<sup>th</sup> SCLK falling edge.

If the ZJC2039 is already in partial power-down mode and  $\overline{CS}$  is brought high before the 10<sup>th</sup> falling edge of SCLK, the device enters full power-down mode. For more information on the power-up times associated with partial power-down mode in various configurations, see the Power-up Times section.

### Full Power-Down Mode

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required because power-up from a full power-down takes substantially longer than that from a partial power-down. This mode is suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus, power down.

When the ZJC2039 is in full power-down mode, all analog circuitry is powered down. To enter full power-down mode, put the device into partial power-down mode by bringing  $\overline{CS}$  high between the second and 10<sup>th</sup> falling edges of SCLK. In the next conversion cycle,

interrupt the conversion process in the same way by bringing  $\overline{\text{CS}}$  high before the 10<sup>th</sup> SCLK falling edge. Once  $\overline{\text{CS}}$  is brought high in this window of SCLKs, the part powers down completely. Note that it is not necessary to complete the 16 SCLKs once  $\overline{\text{CS}}$  is brought high to enter either of the power-down modes.

Glitch protection is not available when entering full power-down mode. To exit full power-down mode and to power up the ZJC2039, users should perform a dummy conversion, similar to when powering up from partial power-down mode. On the falling edge of  $\overline{\text{CS}}$ , the device begins to power up and continues to power up as long as  $\overline{\text{CS}}$  is held low until after the falling edge of the 10<sup>th</sup> SCLK. The required power-up time must elapse before a conversion can be initiated. See the Power-Up Times section for the power-up times associated with the ZJC2039.

### Power-Up Times

The ZJC2039 has two power-down modes, partial power-down and full power-down, which are described in detail in the Modes of Operation section. This section deals with the power-up time required when coming out of either of these modes. To power up from partial power-down mode, one cycle is required. Therefore, with an SCLK frequency of up to 48 MHz, one dummy cycle is sufficient to allow the device to power up from partial power-down mode. Once the dummy cycle is complete, the ADC is fully powered up and the input signal is acquired properly. The quiet time,  $t_{\text{QUIET}}$ , must still be allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of  $\overline{\text{CS}}$ .

To power up from full power-down, approximately 30  $\mu\text{s}$  should be allowed from the falling edge of  $\overline{\text{CS}}$ , as  $t_{\text{POWER-UP}}$ . Note that during power-up from partial power-down mode, the track-and-hold, which is in hold mode while the part is powered down, returns to track mode after the first SCLK edge, following the falling edge of  $\overline{\text{CS}}$ .

When power supplies are first applied to the ZJC2039, the ADC can power up in normal mode. One dummy cycle is needed, in which  $\overline{\text{CS}}$  must be brought high between the second and 10<sup>th</sup> SCLK falling edges.

Alternatively, if the part is to be placed into full power-down mode, two dummy cycles must be initiated. Two dummy cycles place the part into full power-down mode. See the Modes of Operation section.

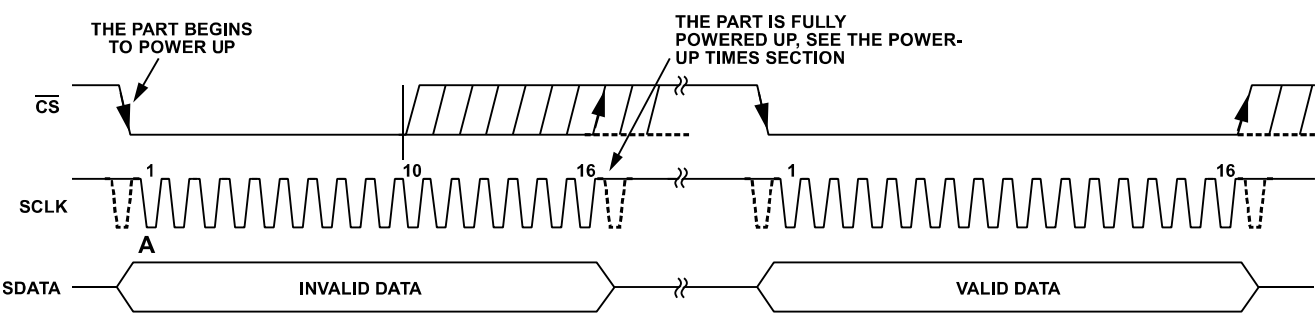


Figure 11. Exiting Partial Power-Down Mode

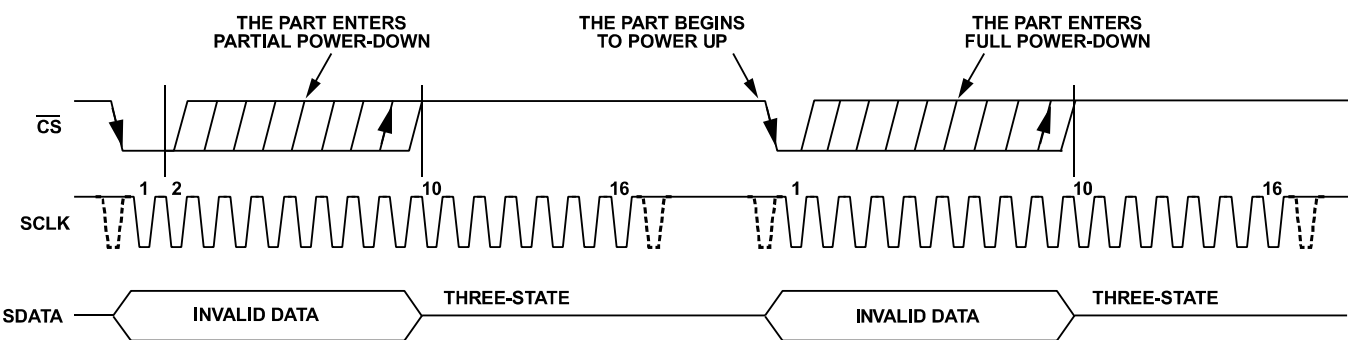


Figure 12. Entering Full Power-Down Mode

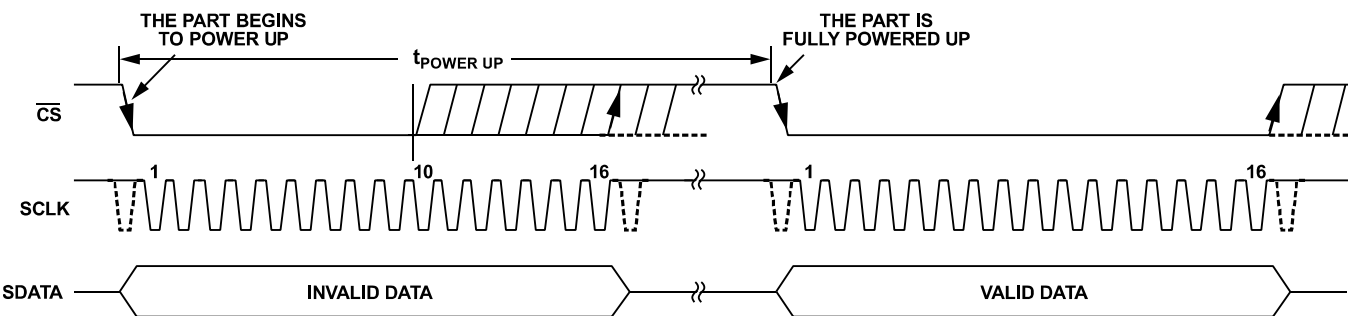


Figure 13. Exiting Full Power-Down Mode

## Digital Interface

The  $\overline{CS}$  signal initiates the data transfer and conversion process. The falling edge of  $\overline{CS}$  rising edge puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion is initiated at this point. The conversion requires completing 14 SCLK cycles. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track mode on the next SCLK rising edge. If the rising edge of CS occurs before 14 SCLKs have elapsed, the conversion is terminated and the SDATA line goes back into three-state. If 16 SCLKs are considered in the cycle, the last two bits are zeros and SDATA returns to three-state on the 16<sup>th</sup> SCLK falling edge.

$\overline{CS}$  going low clocks out the first leading zero to be read by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero. Therefore, the first falling clock edge on the serial clock provides the first leading zero and clocks out the second leading zero. The final bit in the data transfer is valid on the 16<sup>th</sup> falling edge, because it is clocked out on the previous (15<sup>th</sup>) falling edge.

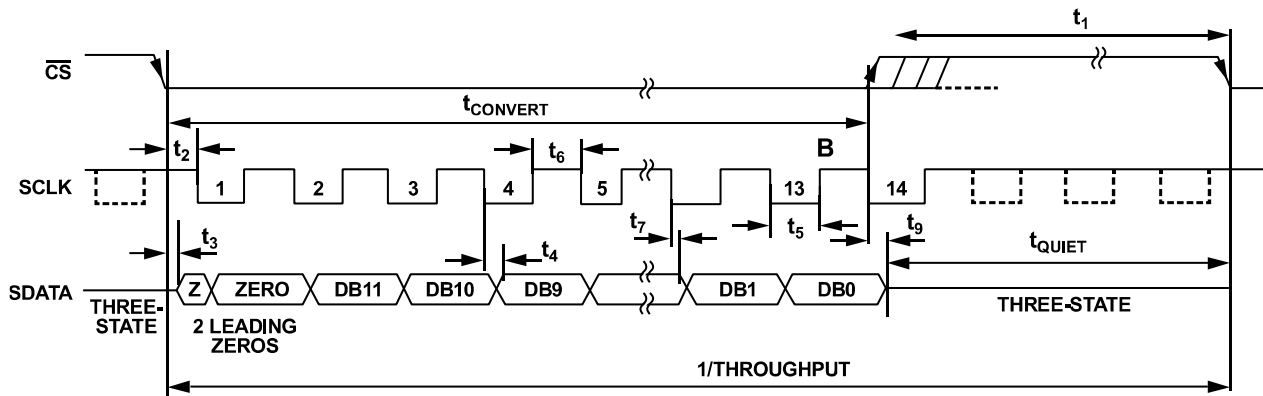


Figure 14. Serial Interface without Busy Indication Connection Diagram

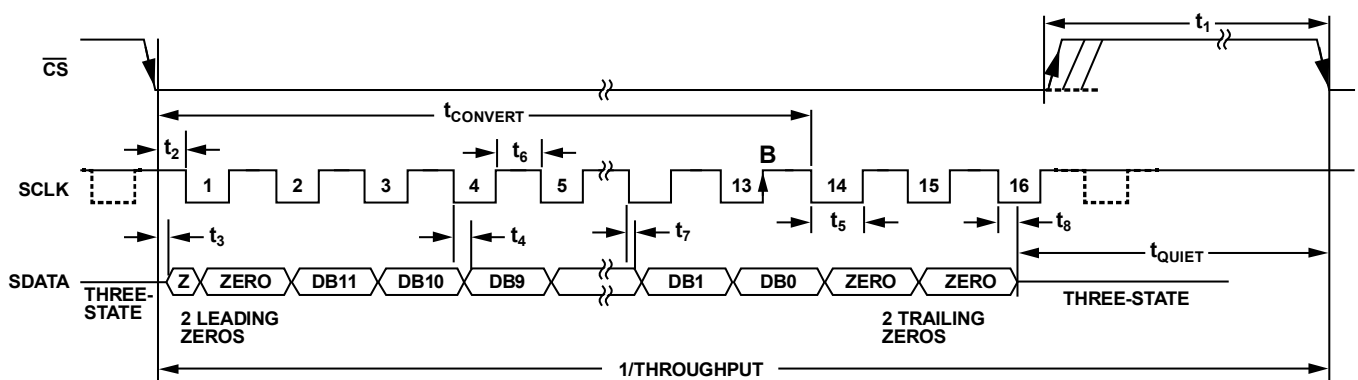


Figure 15. Serial Interface without Busy Indication Timing

Outline Dimensions

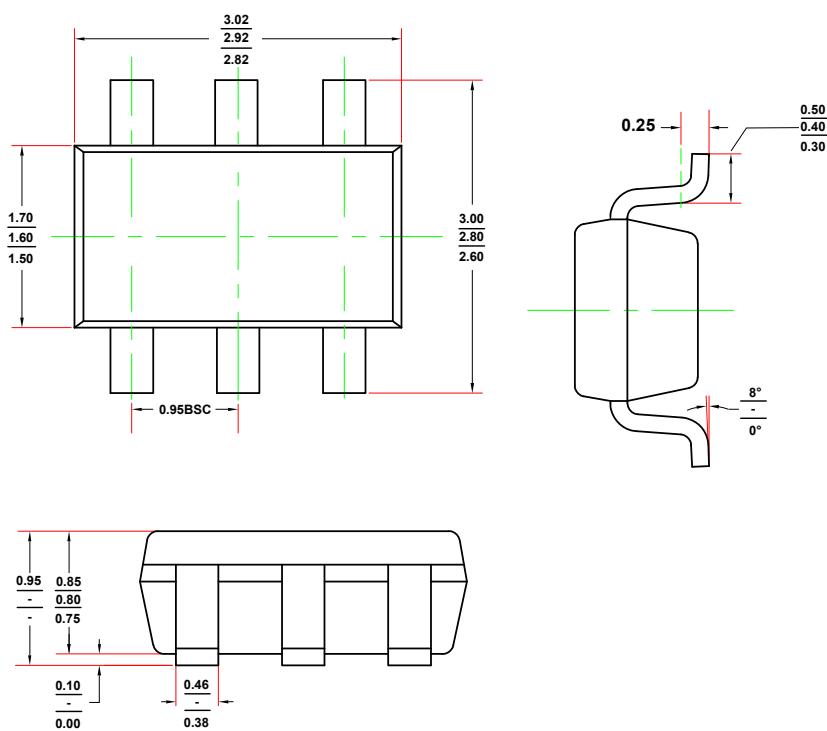
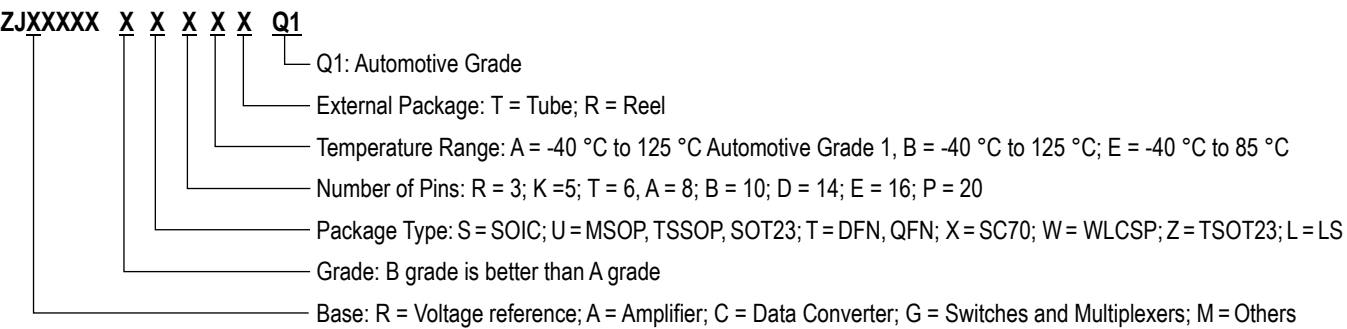


Figure 16. 6-Lead TSOT23 Package Dimensions Shown in Millimeter

Ordering Guide

| Model   | Orderable Device | Package  | Temperature Range (°C) | External Package |
|---------|------------------|----------|------------------------|------------------|
| ZJC2039 | ZJC2039AZTBR     | TSOT23-6 | -40 to +125            | 7" Reel          |

Product Order Model



## Related Parts

| Part Number               | Description                                                                           | Comments                                                                                                                                                         |
|---------------------------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC                       |                                                                                       |                                                                                                                                                                  |
| ZJC2020                   | 20-bit 350 kSPS SAR ADC                                                               | Fully differential input, SINAD 101.4 dB, THD -118 dB                                                                                                            |
| ZJC2000/2010              | 18-bit 400 kSPS/200 kSPS SAR ADC                                                      | Fully differential input, SINAD 99.3 dB, THD -113 dB                                                                                                             |
| ZJC2001/2011              | 16-bit 500 kSPS/250 kSPS SAR ADC                                                      | Fully differential input, SINAD 95.3 dB, THD -113 dB                                                                                                             |
| ZJC2002/2012              | 16-bit 500 kSPS/250 kSPS SAR ADC                                                      | Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB                                                                                                   |
| ZJC2003/2013              |                                                                                       | Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB                                                                                                    |
| ZJC2004/2014              | 18-bit 400 kSPS/200 kSPS SAR ADC                                                      | Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB                                                                                                   |
| ZJC2005/2015              |                                                                                       | Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB                                                                                                    |
| ZJC2007/2017              | 14-bit 600 kSPS/300 kSPS SAR ADC                                                      | Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB                                                                                                     |
| ZJC2008/2018              |                                                                                       | Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB                                                                                                      |
| ZJC2100/1-18              | 18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB        |                                                                                                                                                                  |
| ZJC2100/1-16              | 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB        |                                                                                                                                                                  |
| ZJC2102/3-18              | 18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB |                                                                                                                                                                  |
| ZJC2102/3-16              | 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB |                                                                                                                                                                  |
| ZJC2102/3-14              | 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB   |                                                                                                                                                                  |
| ZJC2104/5-18              | 18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB |                                                                                                                                                                  |
| ZJC2104/5-16              | 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB |                                                                                                                                                                  |
| DAC                       |                                                                                       |                                                                                                                                                                  |
| ZJC2541-18/16/14          | 18/16/14-bit 1 MSPS single channel DAC with unipolar output                           | Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages                                                      |
| ZJC2543-18/16/14          |                                                                                       |                                                                                                                                                                  |
| ZJC2542-18/16/14          | 18/16/14-bit 1 MSPS single channel DAC with bipolar output                            | Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages                                                      |
| ZJC2544-18/16/14          |                                                                                       |                                                                                                                                                                  |
| Amplifier                 |                                                                                       |                                                                                                                                                                  |
| ZJA3000-1/2/4             | Single/Dual/Quad 36 V low bias current precision Op Amps                              | 3 MHz, 35 $\mu$ V max Vos, 0.5 $\mu$ V/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V                                    |
| ZJA3001-1/2/4             |                                                                                       |                                                                                                                                                                  |
| ZJA3018-2                 | OVP $\pm$ 75 V, 36 V, Low Power, High Precision Op Amp                                | 1.3 MHz, 10 $\mu$ V max Vos, 0.5 $\mu$ V/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP $\pm$ 75 V (ZJA3018 only), RRO, 4.5 V to 36 V                             |
| ZJA3008-2                 |                                                                                       |                                                                                                                                                                  |
| ZJA3512-2                 | Dual 36 V 7 MHz precision JFET Op Amps                                                | 7 MHz, 35 V/ $\mu$ S, 50 $\mu$ V max Vos, 1 $\mu$ V/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V                                                                      |
| ZJA3216/06/02-1/2         | Precision 20/10/5 MHz CMOS RRIO Op Amps                                               | 20/10/5 MHz, RRIO, 30 $\mu$ V max Vos, 1 $\mu$ V/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V                                                                         |
| ZJA3600/1                 | 36 V ultra-high precision in-amp                                                      | CMRR 105 dB min (G = 1), 25 pA max Ib, 25 $\mu$ V max Vosi, $\pm$ 2.4 V to $\pm$ 18 V, -40 °C to 125 °C                                                          |
| ZJA3611, ZJA3609          | 36 V precision wider bandwidth precision in-amp (G $\geq$ 10)                         | CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 $\mu$ V max Vosi, 1.2 MHz BW (G = 10)                                                                              |
| ZJA3676/7                 | Low power, G = 1 Single/Dual 36 V difference amplifier                                | Input protection to $\pm$ 65 V, CMRR 104 dB min (G = 1), Vos 100 $\mu$ V max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 $\mu$ A/channel, 2.7 V to 36 V      |
| ZJA3678/9                 | Low power, G = 0.5/2 Single/Dual 36 V difference amplifier                            |                                                                                                                                                                  |
| ZJA3669                   | High Common-Mode Voltage Difference Amplifier                                         | $\pm$ 270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8                                                                                     |
| ZJA3100                   | 15 V precision fully differential amplifier                                           | 145 MHz, 447 V/ $\mu$ S, 50 nS to 16-bit, 50 $\mu$ V max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16                                                                     |
| ZJA3236/26/22-2           | Low-cost 20/10/5 MHz CMOS RRIO Op Amps                                                | 20/10/5 MHz, RRIO, 2 mV max Vos, 6 $\mu$ V/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V                                                                               |
| ZJA3622/8                 | 36 V low-cost precision in-amp                                                        | 0.5 nA max Ibias, 125 $\mu$ V max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, $\pm$ 2.4 V to $\pm$ 18 V                                                                |
| Voltage Reference         |                                                                                       |                                                                                                                                                                  |
| ZJR1004                   | 40 V supply precision voltage reference                                               | $V_{OUT}$ = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C                                                                                    |
| ZJR1001/2                 | 5.5 V low power voltage reference (ZJR1001 with noise filter option)                  | $V_{OUT}$ = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, $\pm$ 0.05% initial error, 130 $\mu$ A, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8 |
| ZJR1003                   |                                                                                       |                                                                                                                                                                  |
| ZJR1302                   | 5.5 V low power compact precision voltage reference                                   | $V_{OUT}$ = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 $\mu$ A, SOT23-3                                                                  |
| Switches and Multiplexers |                                                                                       |                                                                                                                                                                  |
| ZJG4438/4439              | 36 V fault protection 8:1/dual 4:1 multiplexer                                        | Protection to $\pm$ 50 V power on & off, latch-up immune, Ron 270 $\Omega$ , 14.8 pC, tON 166 nS                                                                 |
| ZJG4428/4429              | 36 V 8:1/dual 4:1 multiplexer                                                         | Latch-up immune, Ron 270 $\Omega$ , 14.8 pC charge injection, tON 166 nS                                                                                         |
| Quad Matching Resistor    |                                                                                       |                                                                                                                                                                  |
| ZJM5400                   | $\pm$ 75 V precision match resistors                                                  | Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV  |