

128 Taps Digital Potentiometer with I²C Interface

Features

- Single-channel, 128-position Resolution
- ZJC2701/2-10: 10 kΩ Normal Resistance
- ZJC2701/2-100: 100 kΩ Normal Resistance
- INL: ± 0.1 LSB
- DNL: ± 0.1 LSB
- Low Temperature Coefficient: 20 ppm/°C (10 kΩ)
- I²C Serial Interface
- A and B Versions Have Different I²C Addresses
A: 0101110; B: 0111110
- 2.7 V to 5.5 V Single Supply Operation
- Resistance Tolerance: $\pm 20\%$
- Available in Industry Standard SC70-6 Packages
- Temperature Range: -40 °C to +125 °C

Applications

- Laser Gas Detector
- Mechanical Potentiometer Replacement
- Adjustable Power Supplies
- Adjustable Gain Amplifiers and Offset Trimming
- Precision Calibration of Set Point Thresholds
- Sensor Trimming and Calibration

Block Diagram

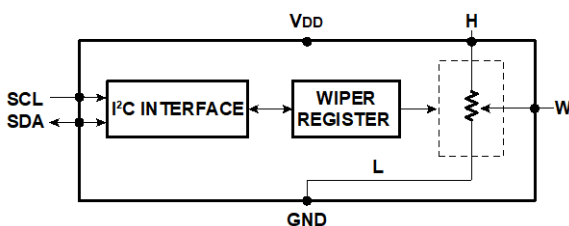


Figure 1. ZJC2701 Block Diagram

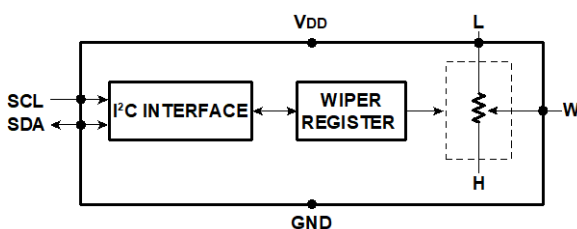


Figure 2. ZJC2702 Block Diagram

General Description

The ZJC2701/2-10 or ZJC2701/2-100 device is a single-channel, linear-taper digital potentiometer with 128 wiper positions. The low terminal(L) of ZJC2701 is internal and connected to GND, while the high terminal(H) of ZJC2702 is internal and floating.

The position of the wiper can be adjusted using an I²C interface.

The ZJC2701/2 is available in a 6-pin SC70 package with a specified temperature range of -40 °C to +125 °C. The part has a 10 kΩ or 100 kΩ end-to-end resistance and can operate with a supply voltage range of 2.7 V to 5.5 V.

Typical Characteristics

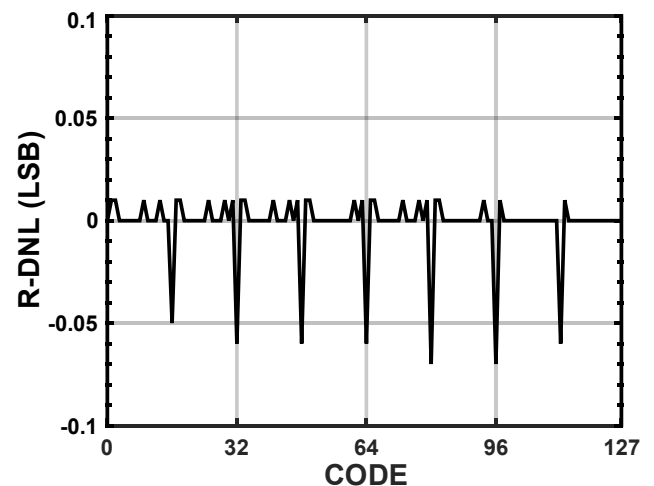


Figure 3. R-DNL vs. Code (10 kΩ)

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Version (Release B)¹

Aug. 2026 — Release B

Update Specifications with production data

Jul. 2026 — Release A

Update Specifications with production data

May. 2026 — Preliminary

Update digital interface, chars

Feb. 2026 — Initial

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Pin Configurations and Function Descriptions

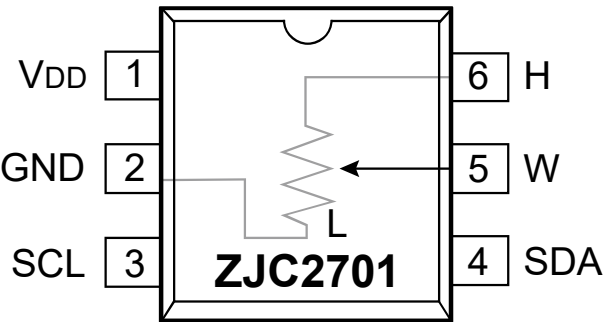


Figure 4. ZJC2701 Pin Configuration (SC70-6)

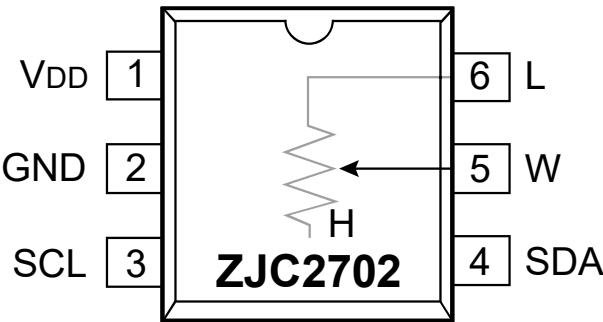


Figure 5. ZJC2702 Pin Configuration (SC70-6)

Mnemonic	Pin No. (ZJC2701)	Pin No. (ZJC2702)	I/O ¹	Description
V _{DD}	1	1	P	Positive Supply Voltage
GND	2	2	G	Ground
SCL	3	3	DI	I ² C Clock
SDA	4	4	DI/O	I ² C Data
W	5	5	AI/O	Wiper Terminal
H	6	--	AI/O	High Terminal (Internally floating in ZJC2702)
L	--	6	AI/O	Low Terminal (Internally connected to GND in ZJC2701)

¹ AI: Analog Input; AO: Analog Output; P: Power; G: Ground; DI: Digital Input; DO: Digital Output.

Absolute Maximum Ratings¹

Parameter	Rating
Supply Voltage, V_{DD} to GND	-0.3 V to +7 V
Continuous Current, I_A , I_B , I_W	± 3 mA (10k version) ± 1 mA (100k version)
Digital Input Pins (SDA, SCL)	-0.3 V to ($V_{DD} + 0.3$ V)
Analog Pins (H, W, L)	-0.3 V to ($V_{DD} + 0.3$ V)
Operating Temperature Range	-40 °C to +125 °C
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature Range	150 °C
Electrostatic Discharge (ESD) ²	
Human Body Model (HBM) ³	± 5 kV
Charged Device Model (CDM) ⁴	± 2 kV

Thermal Resistance⁵

Package Type	θ_{JA}	θ_{JC}	Unit
SC70-6	235	112	°C/W

¹ These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

² Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection

circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

³ ANSI/ESDA/JEDEC JS-001 Compliant.

⁴ ANSI/ESDA/JEDEC JS-002 Compliant

⁵ θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications (10k version)

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, $T_A = 25\text{ °C}$ and $V_{DD} = 5.0\text{ V}$.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
End-to-end Resistance	R_{TOTAL}		● 8	10	12	k Ω
Terminal Resistance	R_H/R_L		●	50	100	Ω
Wiper Resistance	R_W		●	50	100	Ω
Terminal Capacitance	C_H/C_L			6		pF
Wiper Capacitance	C_W			8		pF
Resistance Temperature Coefficient	TC_R			20		ppm/°C
V_{DD} Standby Current	$I_{DD}(STBY)$		●		5	μA
Digital Pins Leakage Current (SCL, SDA Inputs)	I_{IN-DIG}		● -1		1	μA

Serial Interface Specs (SDA, SCL)

Input High Voltage	V_{IH}		● $0.7 \times V_{DD}$		V_{DD}	V
Input Low Voltage	V_{IL}		● 0		$0.3 \times V_{DD}$	V
Output Low Voltage	V_{OL}	SDA Pin, $I_{OL} = 4\text{ mA}$	●		0.4	V
Pin Capacitance	C_{IN}	SCL, SDA Inputs		6		pF

Voltage Divider Mode ($V_H = V_{DD}$, $V_W = \text{Not Loaded}$), only for ZJC2701-10A/B

Integral Non-linearity	INL ^{1,2}		● -0.3	± 0.1	0.3	LSB
Differential Non-linearity	DNL ^{2,3}		● -0.2	± 0.1	0.2	LSB
Zero-scale Error	ZS_{ERROR} ^{4,5}		●	0.6	1.5	LSB
Full-scale Error	FS_{ERROR} ^{5,6}		● -1.5	-0.6		LSB
Ratiometric Temperature Coefficient	T_{CV}	Wiper set at mid-scale		5		ppm/°C
Bandwidth	BW	Wiper set at mid-scale, $C_{LOAD} = 10\text{ pF}$		3500		kHz
Wiper Settling Time	T_{SW}			0.2		μs
Total Harmonic Distortion	THD	$V_H = 1\text{ V}_{RMS}$ at 1 kHz, measurement at W		0.015		%

Rheostat Mode ($V_H = V_{DD}$, $V_W = \text{Not Loaded}$)

Rheostat-mode Integral Non-linearity	RINL ^{7,8}	-40 °C to +125 °C, $V_{DD} = 5\text{ V}$	● -0.3	± 0.1	0.3	LSB
		-40 °C to +85 °C, $V_{DD} = 5\text{ V}$		± 0.1	0.2	LSB
		-40 °C to +125 °C, $V_{DD} = 3\text{ V}$	● -0.5		0.5	LSB
Rheostat-mode Differential Non-linearity	RDNL ^{8,9}		● -0.25	± 0.1	0.25	LSB
Rheostat-mode Zero Scale Error	R_{OFFSET} ^{10,11}		●	0.9	2.0	LSB

¹ $INL = (V_{MEAS}[\text{code } x] - V_{MEAS}[\text{code } 0]) / LSB - [\text{code } x]$

² $LSB = (V_{MEAS}[\text{code } 127] - V_{MEAS}[\text{code } 0]) / 127$

³ $DNL = (V_{MEAS}[\text{code } x] - V_{MEAS}[\text{code } x-1]) / LSB - 1$

⁴ $ZS_{ERROR} = V_{MEAS}[\text{code } 0] / IDEAL_LSB$

⁵ $IDEAL_LSB = V_H / 127$

⁶ $FS_{ERROR} = (V_{MEAS}[\text{code } 127] - V_H) / IDEAL_LSB$

⁷ $RINL = (R_{MEAS}[\text{code } x] - R_{MEAS}[\text{code } 0]) / RLSB - [\text{code } x]$

⁸ $RLSB = (R_{MEAS}[\text{code } 127] - R_{MEAS}[\text{code } 0]) / 127$

⁹ $RDNL = (R_{MEAS}[\text{code } x] - R_{MEAS}[\text{code } x-1]) / RLSB - 1$

¹⁰ $R_{OFFSET} = R_{MEAS}[\text{code } 0] / IDEAL_RLSB$

¹¹ $IDEAL_RLSB = R_{TOT} / 127$

Specifications (100k version)

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, $T_A = 25\text{ °C}$ and $V_{DD} = 5.0\text{ V}$.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
End-to-end Resistance	R_{TOTAL}		● 80	100	120	k Ω
Terminal Resistance	R_H/R_L		●	50	100	Ω
Wiper Resistance	R_W		●	50	100	Ω
Terminal Capacitance	C_H/C_L			6		pF
Wiper Capacitance	C_W			8		pF
Resistance Temperature Coefficient	TC_R			20		ppm/°C
V_{DD} Standby Current	$I_{DD}(STBY)$		●		5	μA
Digital Pins Leakage Current (SCL, SDA Inputs)	I_{IN-DIG}		● -1		1	μA

Serial Interface Specs (SDA, SCL)

Input High Voltage	V_{IH}		● $0.7 \times V_{DD}$		V_{DD}	V
Input Low Voltage	V_{IL}		● 0		$0.3 \times V_{DD}$	V
Output Low Voltage	V_{OL}	SDA Pin, $I_{OL} = 4\text{ mA}$	●		0.4	V
Pin Capacitance	C_{IN}	SCL, SDA Inputs	●	6		pF

Voltage Divider Mode ($V_H = V_{DD}$, $V_W = \text{Not Loaded}$), only for ZJC2701-100A/B

Integral Non-linearity	INL ^{1,2}		● -0.3	± 0.1	0.3	LSB
Differential Non-linearity	DNL ^{2,3}		● -0.15	± 0.1	0.15	LSB
Zero-scale Error	ZS _{ERROR} ^{4,5}		●	0.6	1.5	LSB
Full-scale Error	FS _{ERROR} ^{5,6}		● -1.5	-0.6		LSB
Ratiometric Temperature Coefficient	T_{CV}	Wiper set at mid-scale		5		ppm/°C
Bandwidth	BW	Wiper set at mid-scale, $C_{LOAD} = 10\text{ pF}$		350		kHz
Wiper Settling Time	T_{SW}			2		μs
Total Harmonic Distortion	THD	$V_H = 1\text{ V}_{RMS}$ at 1 kHz, measurement at W		0.01		%

Rheostat Mode ($V_H = V_{DD}$, $V_W = \text{Not Loaded}$)

Rheostat-mode Integral Non-linearity	RINL ^{7,8}	-40 °C to +125 °C, $V_{DD} = 3\text{ to }5\text{ V}$	● -0.6	± 0.1	0.6	LSB
		-40 °C to +85 °C, $V_{DD} = 3\text{ to }5\text{ V}$	-0.25	± 0.1	0.25	LSB
Rheostat-mode Differential Non-linearity	RDNL ^{8,9}		● -0.2	± 0.1	0.2	LSB
Rheostat-mode Zero Scale Error	ROFFSET ^{10,11}		●	0.12	0.25	LSB

¹ $INL = (V_{MEAS}[\text{code } x] - V_{MEAS}[\text{code } 0]) / LSB - [\text{code } x]$

² $LSB = (V_{MEAS}[\text{code } 127] - V_{MEAS}[\text{code } 0]) / 127$

³ $DNL = (V_{MEAS}[\text{code } x] - V_{MEAS}[\text{code } x-1]) / LSB - 1$

⁴ $ZS_{ERROR} = V_{MEAS}[\text{code } 0] / IDEAL_LSB$

⁵ $IDEAL_LSB = V_H / 127$

⁶ $FS_{ERROR} = (V_{MEAS}[\text{code } 127] - V_H) / IDEAL_LSB$

⁷ $RINL = (R_{MEAS}[\text{code } x] - R_{MEAS}[\text{code } 0]) / RLSB - [\text{code } x]$

⁸ $RLSB = (R_{MEAS}[\text{code } 127] - R_{MEAS}[\text{code } 0]) / 127$

⁹ $RDNL = (R_{MEAS}[\text{code } x] - R_{MEAS}[\text{code } x-1]) / RLSB - 1$

¹⁰ $ROFFSET = R_{MEAS}[\text{code } 0] / IDEAL_RLSB$

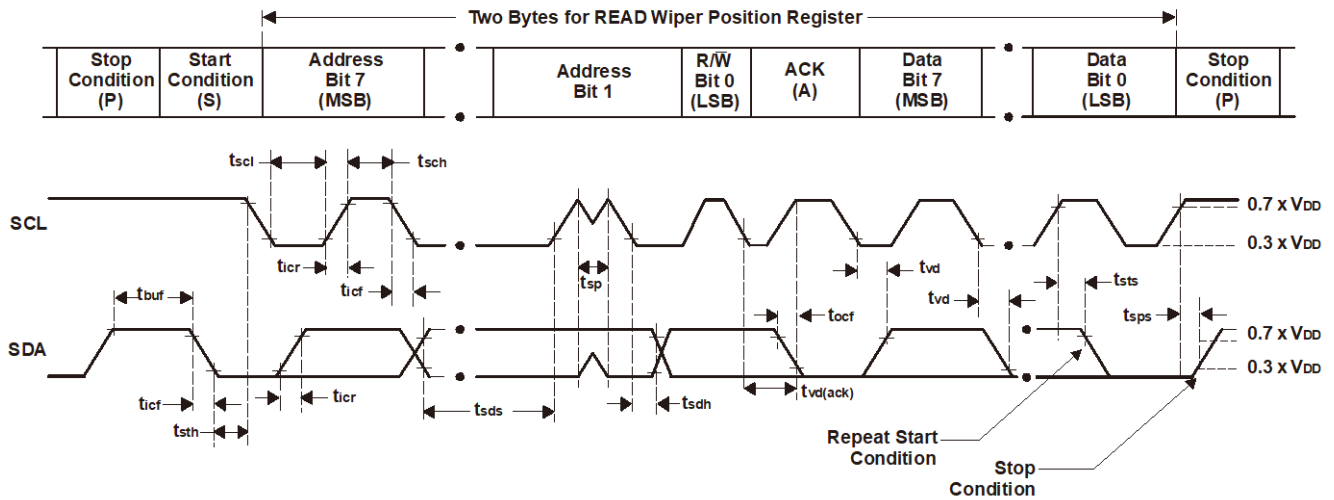
¹¹ $IDEAL_RLSB = R_{TOT} / 127$

Timing Requirements

		Min	Max	Unit
Standard Mode				
I ² C Clock Frequency	F _{scl}	0	100	kHz
I ² C Clock High Time	T _{sch}	4		μs
I ² C Clock Low Time	T _{scl}	4.7		μs
I ² C Spike Time	T _{sp}	0	50	ns
I ² C Serial Data Setup Time	T _{sds}	250		ns
I ² C Serial Data Hold Time	T _{sdh}	10		ns
I ² C Input Rise Time	T _{icr}		1000	ns
I ² C Input Fall Time	T _{icf}		300	ns
I ² C Output Fall Time, 10 pF to 400 pF Bus	T _{ocf}		300	ns
I ² C Bus Free Time between Stop and Start	T _{buf}	4.7		μs
I ² C Start or Repeater Start Condition Setup Time	T _{sts}	4.7		μs
I ² C Start or Repeater Start Condition Hold Time	T _{sth}	4		μs
I ² C Stop Condition Setup Time	T _{sps}	4		μs
Valid Data Time, SCL Low to SDA Output Valid	T _{vd}		1	μs
Valid Data Time of ACK Condition, ACK Signal from SCL Low to SDA (out) Low	T _{vd(ack)}		1	μs
Fast Mode				
I ² C Clock Frequency	F _{scl}	0	400	kHz
I ² C Clock High Time	T _{sch}	0.6		μs
I ² C Clock Low Time	T _{scl}	1.3		μs
I ² C Spike Time	T _{sp}	0	50	ns
I ² C Serial Data Setup Time	T _{sds}	100		ns
I ² C Serial Data Hold Time	T _{sdh}	10		ns
I ² C Input Rise Time	T _{icr}	20	300	ns
I ² C Input Fall Time	T _{icf}	20 x (V _{DD} / 5.5)	300	ns
I ² C Output Fall Time, 10 pF to 400 pF Bus	T _{ocf}	(V _{DD} / 5.5) x 20	300	ns
I ² C Bus Free Time between Stop and Start	T _{buf}	1.3		μs
I ² C Start or Repeater Start Condition Setup Time	T _{sts}	1.3		μs
I ² C Start or Repeater Start Condition Hold Time	T _{sth}	0.6		μs
I ² C Stop Condition Setup Time	T _{sps}	0.6		μs
Valid Data Time, SCL Low to SDA Output Valid	T _{vd}		1	μs
Valid Data Time of ACK Condition, ACK Signal from SCL Low to SDA (out) Low	T _{vd(ack)}		1	μs

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	Data	ACK	Stop
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Figure 6. I²C Interface 3-Byte Write

Figure 7. I²C Interface Read Timing

Start	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop
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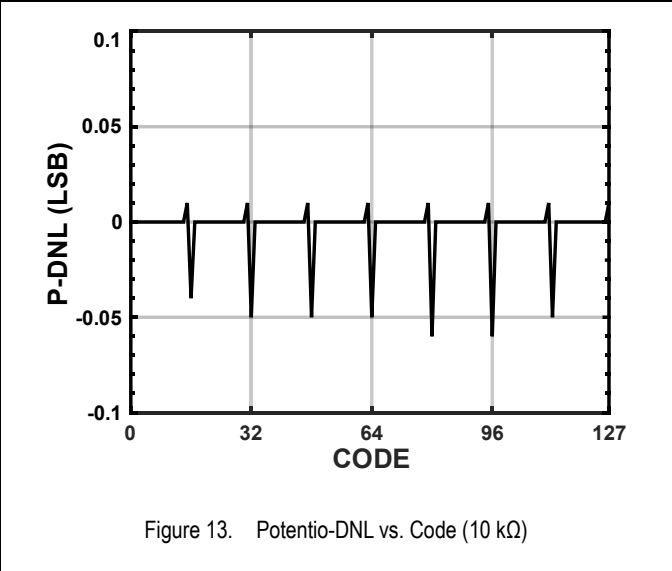
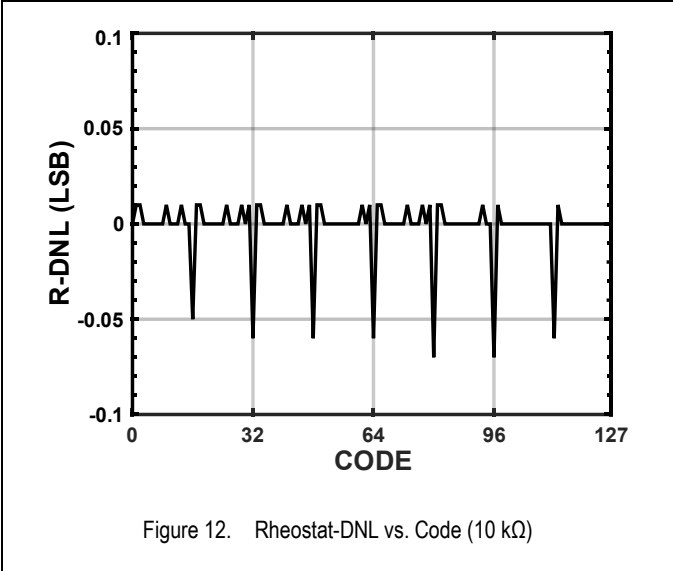
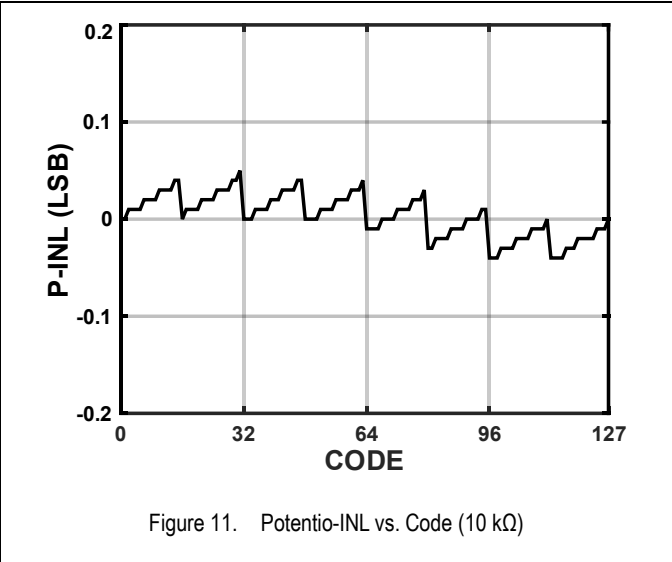
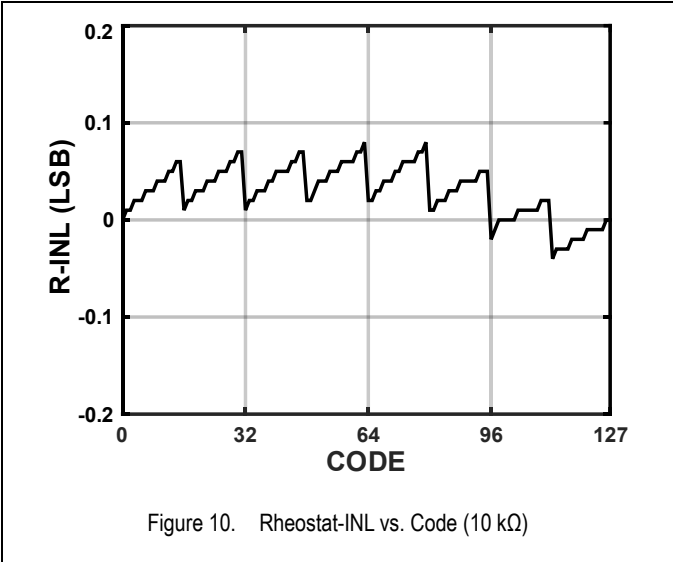
Figure 8. I²C Interface 2-Byte Read (Short Mode)

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	reStart	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop
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Figure 9. I²C Interface Read

Typical Performance Characteristics

Unless otherwise stated, $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$.



Serial Interface

Communications from the controller to the ZJC2701/2 digital potentiometers is by using the I²C serial interface.

Write Operation

To write on the I²C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. After the slave responds with an acknowledge, the master then sends the register address byte which is 0x00. The slave acknowledges again, letting the master know that it is ready. After this, the master starts sending the register data (LSB 7 bits are used) to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	Data	ACK	Stop
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Figure 14. I²C Interface 3-Byte Write

Read Operation

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave with the register address it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START (or repeat START) condition again, followed by the slave address with the R/W bit set to 1 (Signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. The master continues to send out the clock pulses, for each byte of data that it wishes to receive. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data.

When the master has received the number of bytes it was expecting (or needs to stop communication), it should send a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	reStart	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop
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Figure 15. I²C Interface Read

It is also possible to read the register data back with 2 bytes, as shown below.

Start	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop
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Figure 16. I²C Interface 2-Byte Read (Short Mode)

Programming the Variable Resistor

Rheostat Operation—±20% Resistor Tolerance

When the ZJC2701/2 operates in rheostat mode, only two terminals are used as a variable resistor.

The nominal resistance between Terminal H (internally) and Terminal L, R_{HL} , is 10 kΩ or 100 kΩ, and has 128 tap points accessed by the wiper terminal. The 7-bit data in the RDAC latch is decoded to select one of the 128 possible wiper settings. The general equation for determining the digitally programmed output resistance between Terminal W and Terminal L is

$$R_{WL}(D) = \frac{D}{128} \times R_{HL} + R_W \text{ From } 0x00 \text{ to } 0x7F$$

where:

- D is the decimal equivalent of the binary code in the 7-bit RDAC register.
- R_{HL} is the end to end resistance.
- R_W is the wiper resistance.

Outline Dimensions

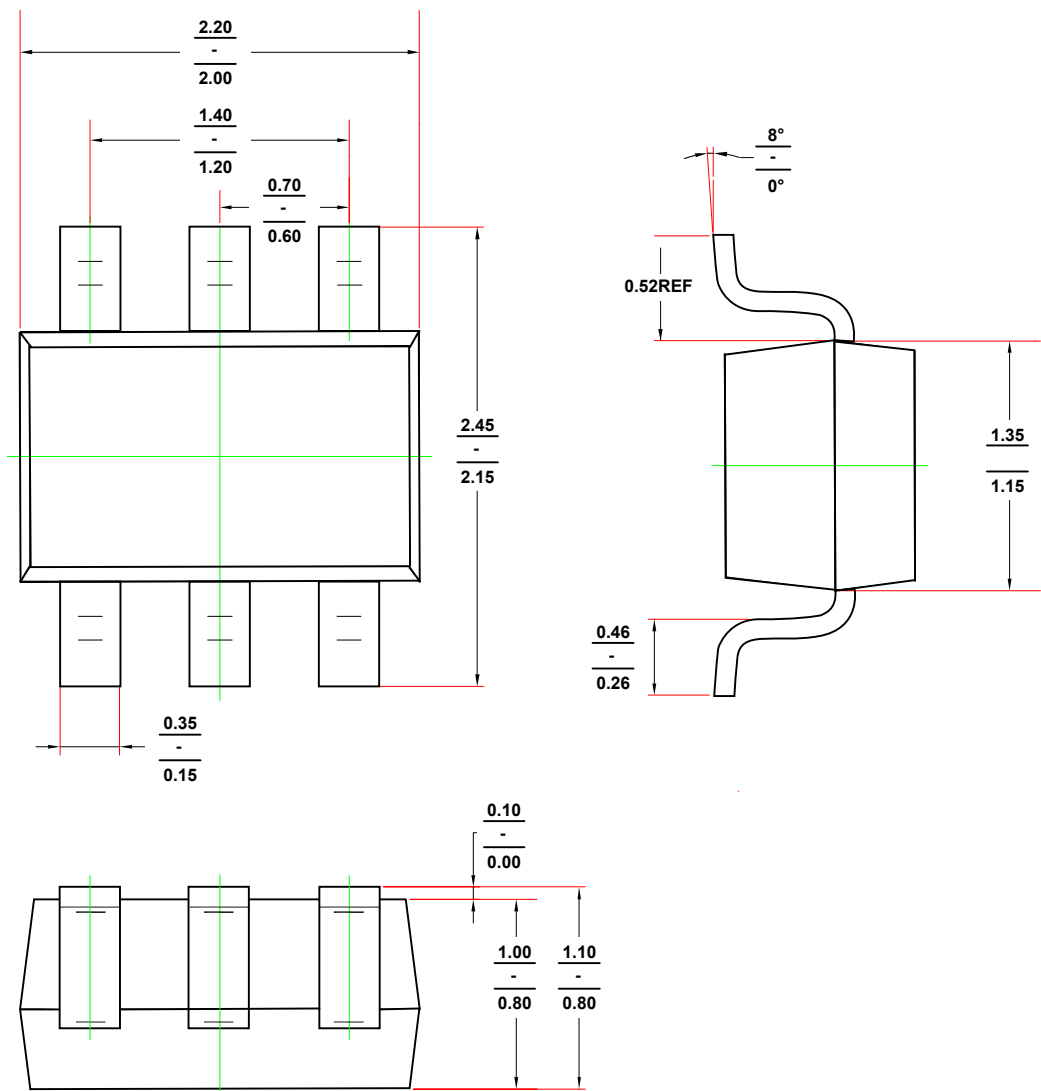


Figure 17. 6-lead SC70 Package Dimensions Shown in Millimeters

Ordering Guide

Model	Orderable Device	Marking (NN: Date Code)	End-to-End Resistance (Ω)	I ² C Address	Package	External Package
ZJC2701	ZJC2701-10AXTBR	01NN	10k	0101110	SC70-6	7" Reel
	ZJC2701-10BXTBR	02NN	10k	0111110		
	ZJC2701-100AXTBR	05NN	100k	0101110		
	ZJC2701-100BXTBR	06NN	100k	0111110		
ZJC2702	ZJC2702-10AXTBR	03NN	10k	0101110		
	ZJC2702-10BXTBR	04NN	10k	0111110		
	ZJC2702-100AXTBR	07NN	100k	0101110		
	ZJC2702-100BXTBR	08NN	100k	0111110		

Product Order Model

ZJXXXXX-X X X X X Q1

Q1: Automotive Grade

External Package: T = Tube; R = Reel

Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C

Number of Pins: R = 3; K = 5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20

Package Type: S = SOIC; U = MSOP, TSSOP, SOT23; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23; L = LS

I²C Address: A (0101110), B (0111110)

End-to-End Resistance: 10 = 10k; 100 = 100k;

Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2003/2013		Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2005/2015		Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB
ZJC2008/2018		Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB	
ZJC2100/1-16	16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2102/3-16	16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
ZJC2102/3-14	14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2104/5-16	16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V _{REF} /2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2543-18/16/14		
ZJC2542-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V _{REF} /2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
ZJC2544-18/16/14		
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 μV max Vos, 0.5 μV/°C max TC _{Vos} , 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3001-1/2/4		
ZJA3018-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 μV max Vos, 0.5 μV/°C max TC _{Vos} , 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3008-2		
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/μS, 50 μV max Vos, 1 μV/°C max TC _{Vos} , 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 μV max Vos, 1 μV/°C max TC _{Vos} , 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 μV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 μV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7	Low power, G = 1 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 μV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 μA/channel, 2.7 V to 36 V
ZJA3678/9	Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/μS, 50 nS to 16-bit, 50 μV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 μV/°C max TC _{Vos} , 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 μV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V _{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V _{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 μA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1003		
ZJR1302	5.5 V low power compact precision voltage reference	V _{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 μA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t _{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t _{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV