VIEWE P4 MODULE SPECIFICATION

ESP32-P4-Core-VIEWE	
Model:	PCBA-ESP32-P4-Core-A
Version:	V1.1
Date:	2025-12-1

Customer Confirmation

Approved by	Notes

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REVISION HISTORY

Revision	Date	Contents of Revision Change	Remark
V1.0	20251120	Preliminary release	
V1.1	20231201	Add reference design cases and 3D drawings, etc	

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1 Introduction











ESP32-P4-Core is a high-performance dual-core RISC-V module designed by Viewe, based on the ESP32-P4 chip. It uses ESP32-C6FH4 to expand WIFI6 functionality. It supports a variety of human-machine interaction interfaces, including MIPI-CSI (integrated with Image Signal Processor ISP) and MIPI-DSI interfaces. In addition, it supports common peripherals such as SPI, I2S, I2C, LED PWM, MCPWM, RMT, ADC, UART, and TWAI™. It also supports USB OTG 2.0 HS, Ethernet, and SDIO Host 3.0 for high-speed connections, with its peripherals optimized for low-power applications. The chip integrates a digital signature peripheral and a dedicated key management unit to ensure its security. ESP32-P4-Core is specially designed for high-performance and high-security applications, supporting ultra-large on-chip memory and featuring powerful image and voice processing capabilities. It fully meets the higher requirements of embedded applications in terms of human-machine interface support, edge computing capabilities, and IO connection characteristics.

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2 Functional Features

2.1 CPU

- 32-bit RISC-V dual-core processor up to 360 MHz(The default is 360MHZ. If 400MHZ is needed, please contact us) for HP system
- 32-bit RISC-V single-core processor up to 40 MHz for LP system
- Equipped with an ESP32-C6 WIFI/BT coprocessor, it expands functions such as WIFI 6 and Bluetooth 5 through SDIO

2.2 Memory

- 128 KB HP ROM
- 16 KB LP ROM
- 768 KB HP L2MEM
- 32 KB LP SRAM
- 8 KB system SPM (Scratchpad Memory)
- 32 MB PSRAM is stacked and encapsulated inside, and a 16MB Nor Flash is connected via the QSPI interface.

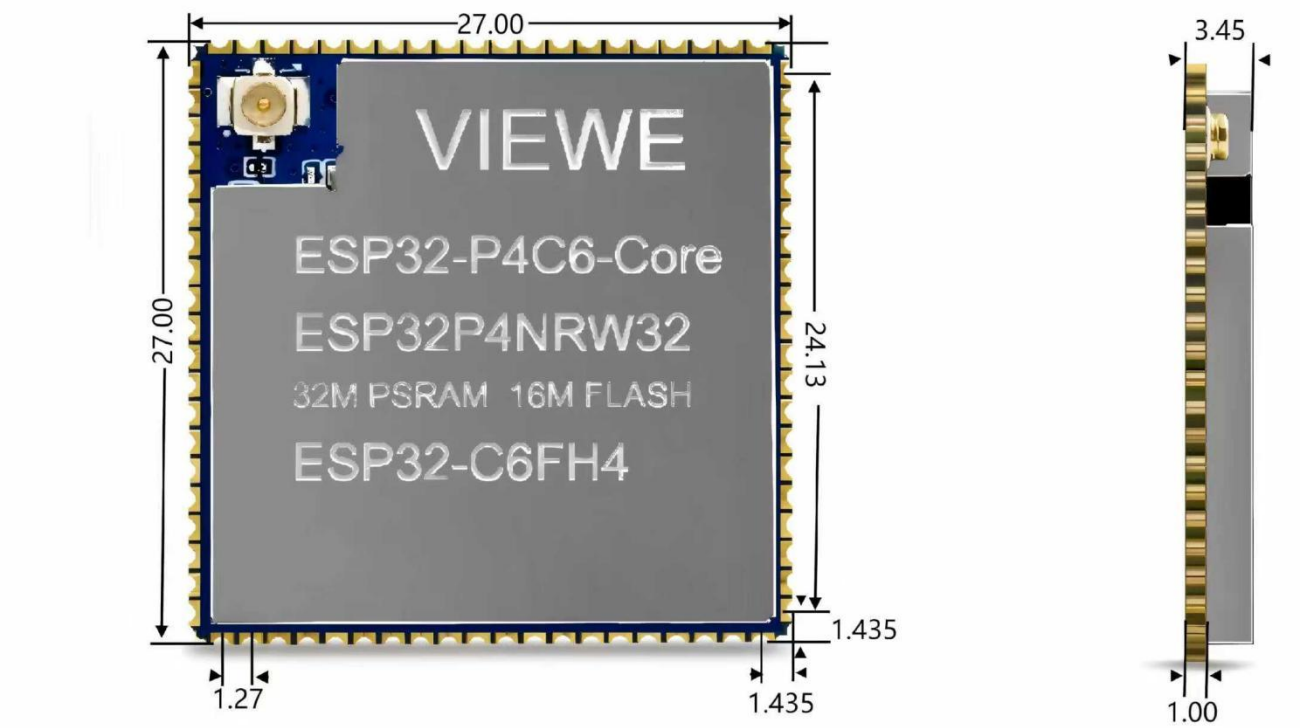
2.3 Applications

With low power consumption, ESP32-P4 is an ideal choice for IoT devices in the following areas:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- Retail Self-Service Terminals (POS, Vending Machines)
- Service Robot
- Multimedia Player
- Cameras for Video Streaming
- High-Speed USB Host and Device
- Smart Voice Interaction Terminal
- Edge Vision AI Processor
- HMI Control Pane

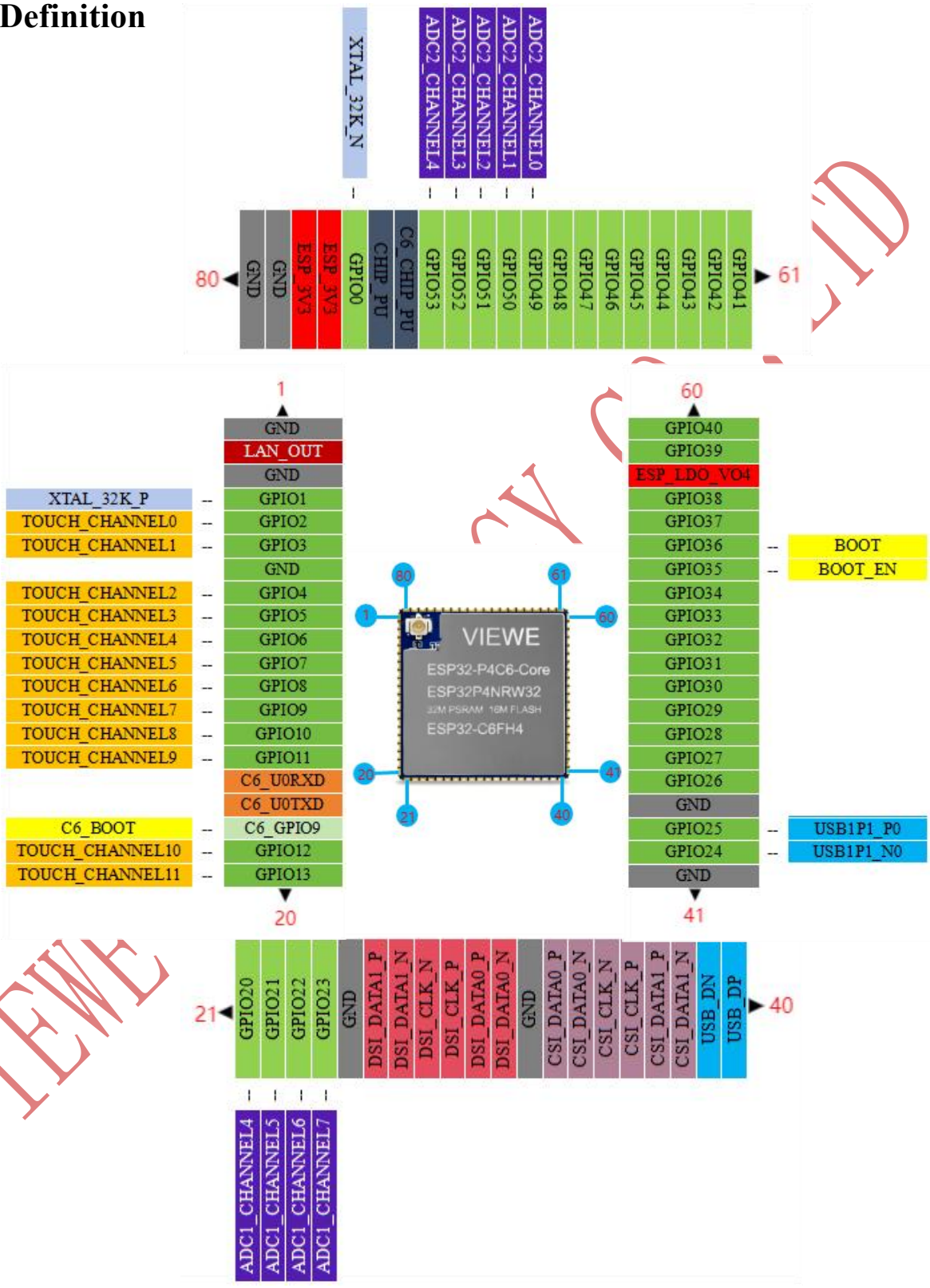
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3 Product Size



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4 PIN Definition



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5 GPIO Description

Table 2-7. Analog Functions

Pin No.	Analog IO Name	Description	Analog Function
1	GND	GND	
2	LAN_OUT	The antenna pin of ESP32-C6 is, by default, led out to the pin pad, and can be switched to the IPEX Generation 1 antenna socket through the reserved 0R resistor	
3	GND	GND	
4	GPIO1	GPIO1 can be connected to a 32.768KHz crystal oscillator together with GPIO0, serving as the crystal oscillator source for the LP system	XTAL_32K_P
5	GPIO2	GPIO2	TOUCH_CHANNEL0
6	GPIO3	GPIO3	TOUCH_CHANNEL1
7	GND	GND	
8	GPIO4	GPIO4	TOUCH_CHANNEL2
9	GPIO5	GPIO5	TOUCH_CHANNEL3
10	GPIO6	GPIO6	TOUCH_CHANNEL4
11	GPIO7	GPIO7	TOUCH_CHANNEL5
12	GPIO8	GPIO8	TOUCH_CHANNEL6
13	GPIO9	GPIO9	TOUCH_CHANNEL7
14	GPIO10	GPIO10	TOUCH_CHANNEL8
15	GPIO11	GPIO11	TOUCH_CHANNEL9
16	C6_U0RXD	The UART RXD of ESP32-C6 can be used for burning firmware into ESP32-C6	
17	C6_U0TXD	The UART TXD of ESP32-C6 can be used for burning firmware into ESP32-C6	

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TabIe 3-1 - cont,d from previous page

Pin No.	Analog IO Name	Description	Analog Function
18	C6_GPIO9	When pulled low before power-up, it can enter the download mode.	C6_BOOT
19	GPIO12	GPIO12	TOUCH_CHANNEL10
20	GPIO13	GPIO13	TOUCH_CHANNEL11
21	GPIO20	GPIO20	ADC1_CHANNEL4
22	GPIO21	GPIO21	ADC1_CHANNEL5
23	GPIO22	GPIO22	ADC1_CHANNEL6
24	GPIO23	GPIO23	ADC1_CHANNEL7
25	GND	GND	
26	DSI_DATA1_P	MIPI-DSI data signal line	
27	DSI_DATA1_N	MIPI-DSI data signal line	
28	DSI_CLK_N	MIPI-DSI clock signal line	
29	DSI_CLK_P	MIPI-DSI clock signal line	
30	DSI_DATA0_P	MIPI-DSI data signal line	
31	DSI_DATA0_N	MIPI-DSI data signal line	
32	GND	GND	
33	CSI_DATA0_P	MIPI-DSIdata signal line	
34	CSI_DATA0_N	MIPI-DSIdata signal line	
35	CSI_CLK_N	MIPI-CSIclock signal line	
36	CSI_CLK_P	MIPI-CSIclock signal line	
37	CSI_DATA1_P	MIPI-DSIdata signal line	
38	CSI_DATA1_N	MIPI-DSIdata signal line	
39	USB_DN	USB 2.0 full-speed pin	
40	USB_DP	USB 2.0 full-speed pin	
41	GND	GND	
42	GPIO24	GPIO24,USB 2.0 full-speed pin	USB1P1_N0
43	GPIO25	GPIO25,USB 2.0 full-speed pin	USB1P1_P0
44	GND	GND	
45	GPIO26	GPIO26	
46	GPIO27	GPIO27	

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Pin No.	Analog IO Name	Description	Analog Function
47	GPIO28	GPIO28	
48	GPIO29	GPIO29	
49	GPIO30	GPIO30	
50	GPIO31	GPIO31	
51	GPIO32	GPIO32	
52	GPIO33	GPIO33	
53	GPIO34	GPIO34	
54	GPIO35	GPIO35,If GPIO36 is in pull-up mode and is pulled low before power-on, the download mode can be entered	BOOT
55	GPIO36	GPIO36,It is recommended to pull up a 10k resistor to 3.3V	BOOT_EN
56	GPIO37	GPIO37	
57	GPIO38	GPIO38	
58	ESP_LDO_VO4	The internal LDO output pin of ESP32-P4 outputs 1.8V by default; the output voltage can be controlled through programming to control the voltage domain of GPIO39 to GPIO48	
59	GPIO39	GPIO39	
60	GPIO40	GPIO40	
61	GPIO41	GPIO41	
62	GPIO42	GPIO42	
63	GPIO43	GPIO43	
64	GPIO44	GPIO44	
65	GPIO45	GPIO45	
66	GPIO46	GPIO46	
67	GPIO47	GPIO47	
68	GPIO48	GPIO48	
69	GPIO49	GPIO49	ADC2_CHANNEL0
70	GPIO50	GPIO50	ADC2_CHANNEL1

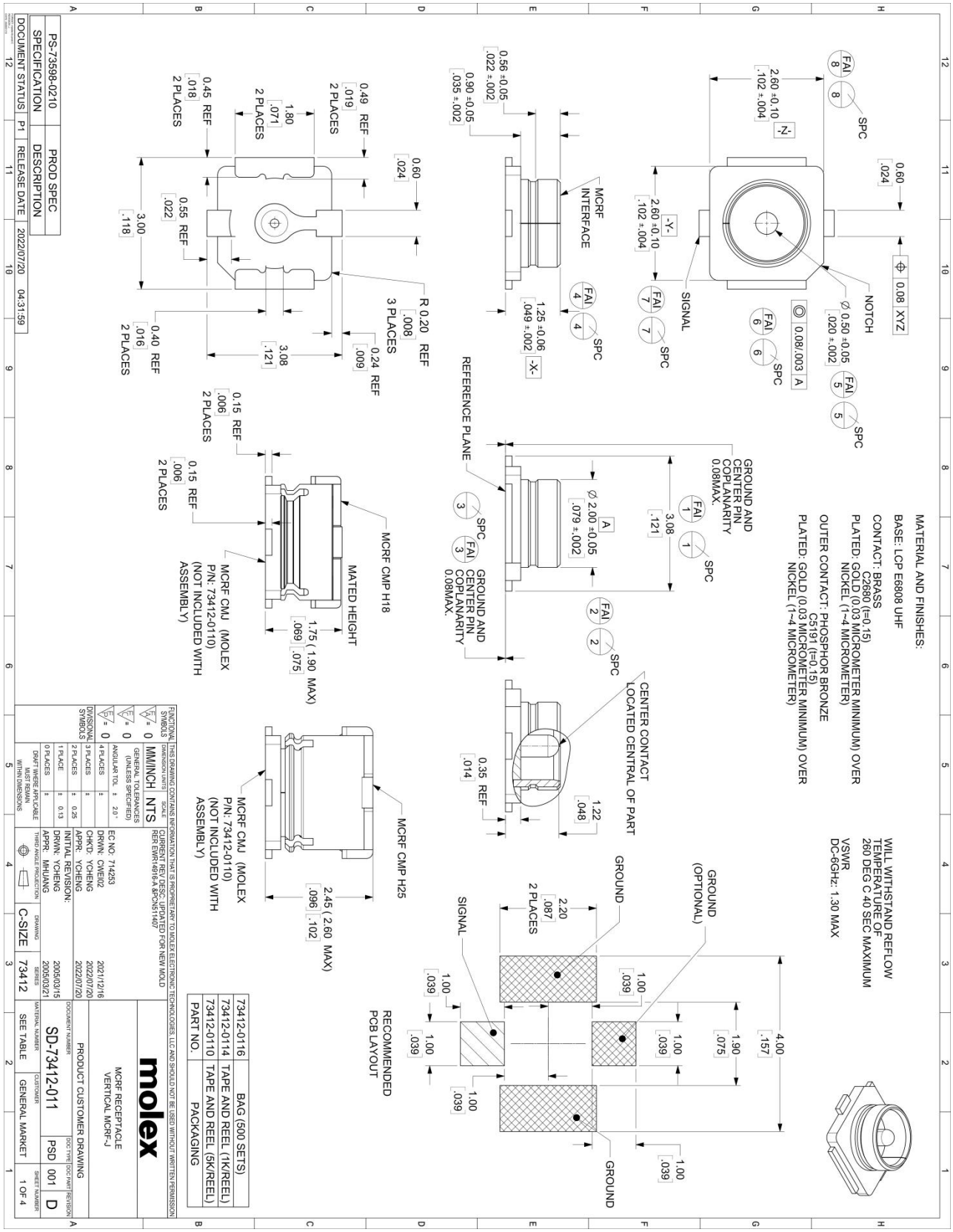
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Pin No.	Analog IO Name	Description	Analog Function
71	GPIO51	GPIO51	ADC2_CHANNEL2
72	GPIO52	GPIO52	ADC2_CHANNEL3
73	GPIO53	GPIO53	ADC2_CHANNEL4
74	C6_CHIP_PU	ESP32-C6 enable pin, pulled high by default to enable	
75	CHIP_PU	ESP32-P4 enable pin, pulled high by default to enable	
76	GPIO0	GPIO0 can be connected to a 32.768KHz crystal oscillator together with GPIO1, serving as the crystal oscillator source for the LP system	XTAL_32K_N
77	ESP_3V3	Power supply pin, it is recommended to connect to 3.3V by default.	
78	ESP_3V3	Power supply pin, it is recommended to connect to 3.3V by default.	
79	GND	GND	
80	GND	GND	

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6 Antenna mount drawings



7 Related Documents

7.1 Schematic Diagram

- ESP32-P4-Core Schematic Diagram

7.2 3D Drawing

- ESP32-P4-Core 3D Drawing

7.3 PCB Footprint Drawing

- ESP32-P4-Core Footprint Drawing

7.4 Data Sheet

- ESP32-P4 Datasheet (Chinese)
- ESP32-P4 Datasheet (English)
- ESP32-P4 Technical Reference Manual (Chinese)
- ESP32-P4 Technical Reference Manual (English)
- FR Antenna Datasheet
- ESP32-C6 Datasheet(Chinese)
- ESP32-C6 Datasheet(English)

7.5 Design Reference

- ESP32-P4-PI-VIEWE Schematic Diagram

7.6 Git

GitHub：VIEWESMART/ESP32-P4-Core: ESP32-P4-Core is a high-performance dual-core RISC-V module designed by Viewe, based on the ESP32-P4 chip. It uses ESP32-C6FH4 to expand WIFI6 functionality.

Gitee:ESP32-P4-Core: ESP32-P4-Core 是由优奕视界基于 ESP32-P4 芯片设计的高性能双核 RISC-V 模块。它采用 ESP32-C6FH4 来扩展 WIFI6 功能。

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